Microphone Preamplifier with Variable Compression and Noise Gating

Data Sheet

SSM2166

FEATURES

Complete microphone conditioner in a 14-lead SOIC package
Single 5 V operation
Adjustable noise gate threshold
Compression ratio set by external resistor
Automatic limiting feature—prevents ADC overload
Adjustable release time
Low noise and distortion
Power-down feature
20 kHz bandwidth (±1 dB)

APPLICATIONS

Microphone preamplifiers/processors
Computer sound cards
Public address/paging systems
Communication headsets
Telephone conferencing
Guitar sustain effects generators
Computerized voice recognition
Surveillance systems
Karaoke and DJ mixers

GENERAL DESCRIPTION

The SSM2166 integrates a complete and flexible solution for conditioning microphone inputs in computer audio systems. It is also excellent for improving vocal clarity in communications and public address systems. A low noise, voltage-controlled amplifier (VCA) provides a gain that is dynamically adjusted by a control loop to maintain a set compression characteristic. The compression ratio is set by a single resistor and can be varied from 1:1 to over 15:1 relative to a user-defined rotation point; signals above the rotation point are limited to prevent overload and to eliminate popping. In the 1:1 compression setting, the SSM2166 can be programmed with a fixed gain of up to 20 dB; this gain is in addition to the variable gain in other compression settings. The input buffer can also be configured for front-end gains of 0 dB to 20 dB. A downward expander (noise gate) prevents amplification of noise or hum. This results in optimized signal levels prior to digitization, thereby eliminating the need for additional gain or attenuation in the digital domain that may add noise or impair accuracy of speech recognition algorithms. The compression ratio and time constants are set externally. A high degree of flexibility is provided by the VCA gain, rotation point, and noise gate adjustment pins.

The SSM2166 is an ideal companion product for audio codecs used in computer systems. The SSM2166 is available in a 14-lead SOIC package and is guaranteed for operation over the extended industrial temperature range of −40°C to +85°C.

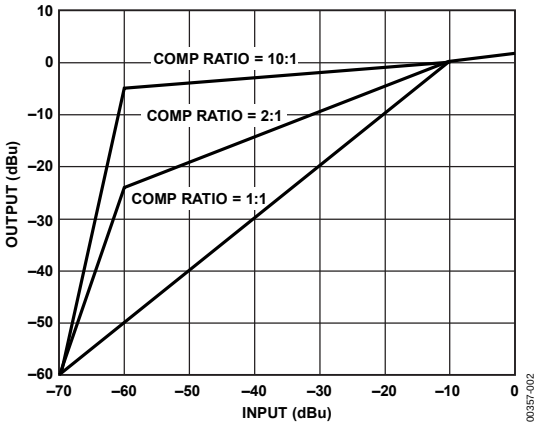

Figure 1. Compression and Gating Characteristics with 10 dB of Fixed Gain (The Gain Adjust Pin Can Be Used to Vary This Fixed Gain Amount)

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL SPEECH APPLICATION

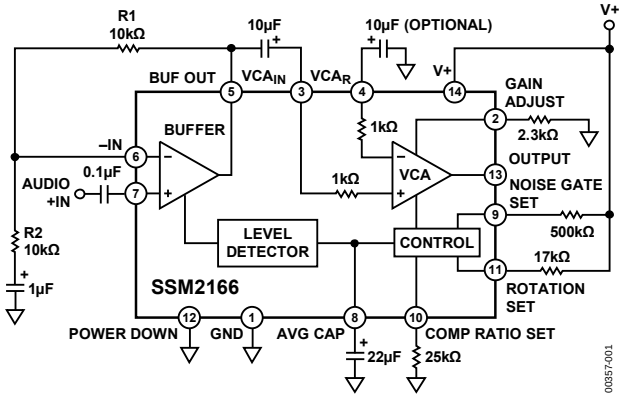

Figure 2.

Rev. E **Document Feedback**

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7/08—Rev. C to Rev. D

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5/08—Rev. B to Rev. C

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SPECIFICATIONS

V+ = 5 V, f = 1 kHz, R_L = 100 kΩ, R_{GATE} = 600 kΩ, $R_{ROT\ PT}$ = 3 kΩ, R_{COMP} = 0 Ω, R1 = 0 Ω, R2 = ∞ Ω, T_A = 25°C, unless otherwise noted; V_{IN} = 300 mV rms.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AUDIO SIGNAL PATH						
Voltage Noise Density	e_n	15:1 Compression		17		nV/√Hz
Noise		20 kHz bandwidth, V_{IN} = GND		−109		dBu[1]
Total Harmonic Distortion and Noise	THD + N	Second and third harmonics, V_{IN} = −20 dBu, 22 kHz low-pass filter		0.25	0.5	%
Input Impedance	Z_{IN}			180		kΩ
Output Impedance	Z_{OUT}			75		Ω
Load Drive		Resistive	5			kΩ
		Capacitive			2	nF
Buffer						
Input Voltage Range		1% THD		1		V rms
Output Voltage Range		1% THD		1		V rms
VCA						
Input Voltage Range		1% THD		1		V rms
Output Voltage Range		1% THD		1.4		V rms
Gain Bandwidth Product		1:1 compression, VCA gain = 60 dB		30		MHz
CONTROL SECTION						
VCA Dynamic Gain Range				60		dB
VCA Fixed Gain Range				−60 to +19		dB
Compression Ratio, Minimum				1:1		
Compression Ratio, Maximum		See Figure 19 for $R_{COMP}/R_{ROT\ PT}$, rotation point = 100 mV rms		15:1		
Control Feedthrough		15:1 compression, rotation point = −10 dBu, R2 = 1.5 kΩ		±5		mV
POWER SUPPLY						
Supply Voltage Range	V+		4.5		5.5	V
Supply Current	I_{SY}			7.5	10	mA
Quiescent Output Voltage Level				2.2		V
Power Supply Rejection Ratio	PSRR			50		dB
POWER DOWN						
Supply Current		Pin 12 = V+[2]		10	100	µA

[1] 0 dBu = 0.775 V rms.
[2] Normal operation for Pin 12 is 0 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	10 V
Audio Input Voltage	Supply voltage
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead SOIC	120	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

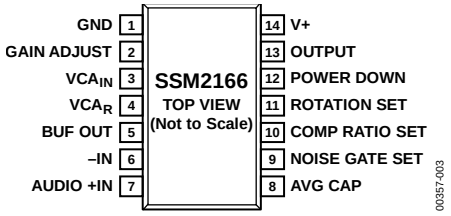


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground.
2	GAIN ADJUST	VCA Gain Adjust Pin. A resistor from this pin to ground sets the fixed gain of the VCA. To check the setting of this pin, make sure the compression ratio set pin (Pin 10) is grounded for no compression. The gain can be varied from 0 dB to 20 dB. For 20 dB, leave the pin open. For 0 dB of fixed gain, a typical resistor value is approximately 1 kΩ. For 10 dB of fixed gain, the resistor value is approximately 2 kΩ to 3 kΩ. For resistor values <1 kΩ, the VCA can attenuate or mute (see Figure 6).
3	VCA_{IN}	VCA Input Pin. A typical connection is a 10 µF capacitor from the buffer output pin (Pin 5) to this pin.
4	VCA_R	Inverting Input to the VCA. This input can be used as a nonground reference for the audio input signal (see the Applications Information section).
5	BUF OUT	Input Buffer Amplifier Output Pin. This pin must not be loaded by capacitance to ground.
6	−IN	Inverting Input to the Buffer. A 10 kΩ feedback resistor, R1, from the buffer output (Pin 5) to this input pin and a resistor, R2, from this pin through a 1 µF capacitor to ground give gains of 6 dB to 20 dB for R2 = 10 kΩ to 1.1 kΩ.
7	AUDIO +IN	Input Audio Signal. The input signal should be ac-coupled (0.1 µF typical) into this pin.
8	AVG CAP	Detector Averaging Capacitor. A capacitor, 1 µF to 22 µF, to ground from this pin is the averaging capacitor for the detector circuit.
9	NOISE GATE SET	Noise Gate Threshold Set Point. A resistor to V+ sets the level below which input signals are downward expanded. For a 0.7 mV threshold, the resistor value is approximately 380 kΩ. Increasing the resistor value reduces the threshold (see Figure 5).
10	COMP RATIO SET	Compression Ratio Set Pin. A resistor to ground from this pin sets the compression ratio, as shown in Figure 2. Figure 19 gives resistor values for various rotation points.
11	ROTATION SET	Rotation Point Set Pin. This pin is set by adding a resistor to the positive supply. This resistor together with the gain adjust pin determines the onset of limiting. A typical value for this resistor is 17 kΩ for a 100 mV rotation point. Increasing the resistor value reduces the level at which limiting occurs (see Figure 9).
12	POWER DOWN	Power-Down Pin. Connect this pin to ground for normal operation. Connect this pin to the positive supply for power-down mode.
13	OUTPUT	Output Signal.
14	V+	Positive Supply, 5 V Nominal.

TYPICAL PERFORMANCE CHARACTERISTICS

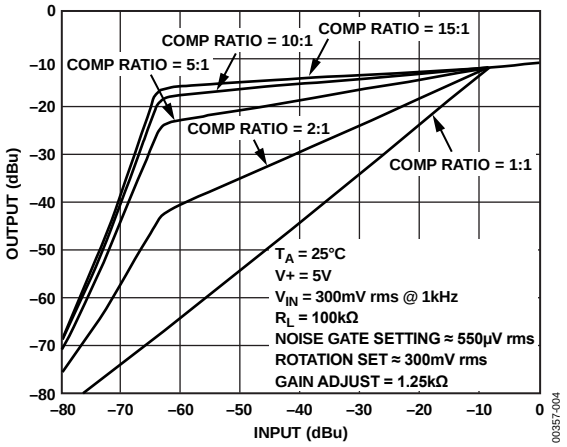


Figure 4. Output vs. Input Characteristics

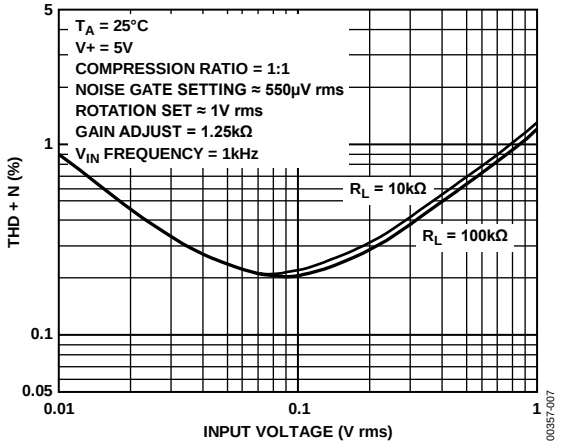


Figure 7. THD + N (%) vs. Input (V rms)

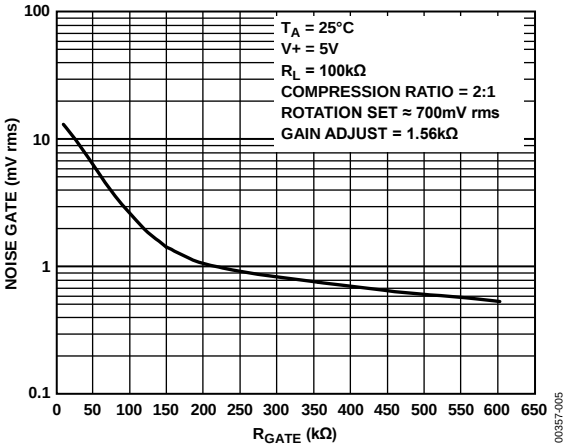


Figure 5. Noise Gate vs. R_{GATE} (Pin 9 to V+)

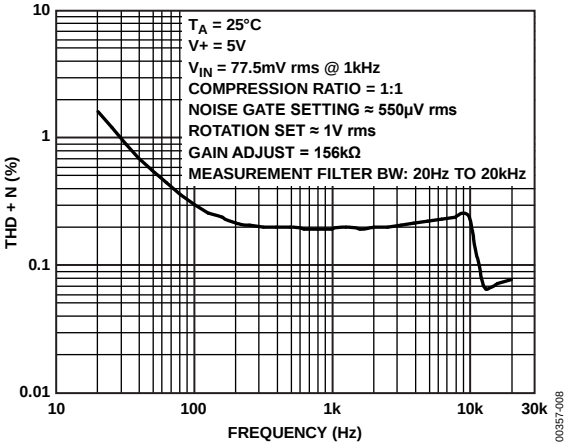


Figure 8. THD + N (%) vs. Frequency (Hz)

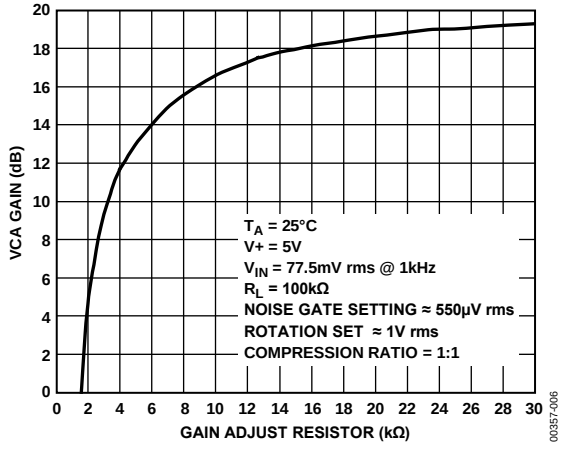


Figure 6. VCA Gain vs. R_{GAIN} (Pin 2 to GND)

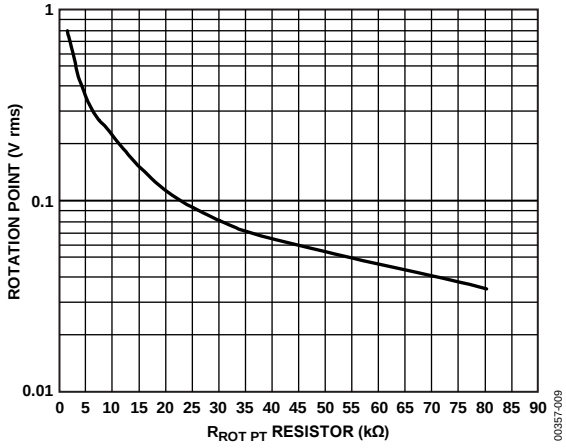


Figure 9. Rotation Point vs. $R_{ROT\ PT}$ (Pin 11 to V+)

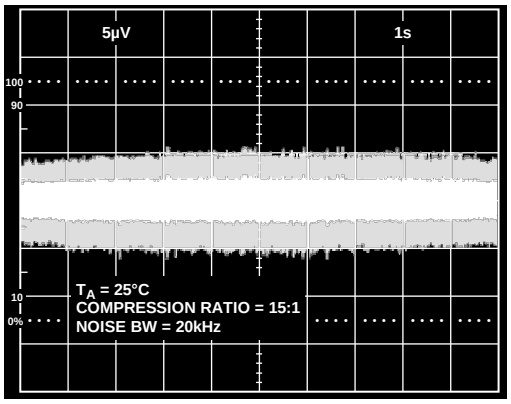


Figure 10. Wideband Peak-to-Peak Output Noise

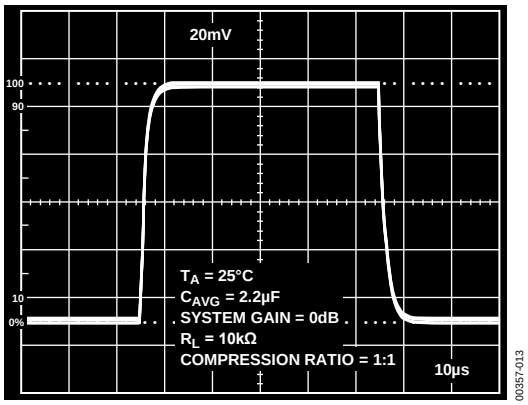


Figure 13. Small Signal Transient Response

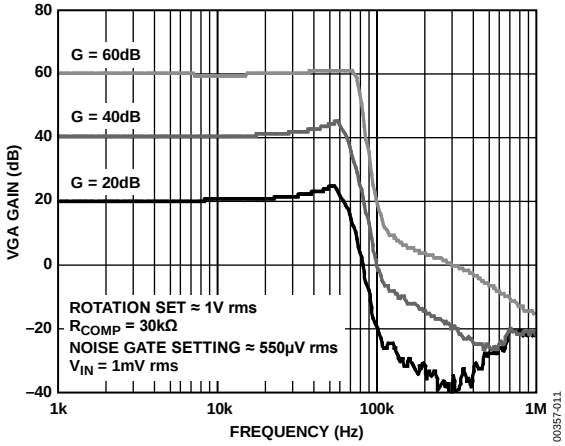


Figure 11. VCA Gain Bandwidth Curves vs. Frequency

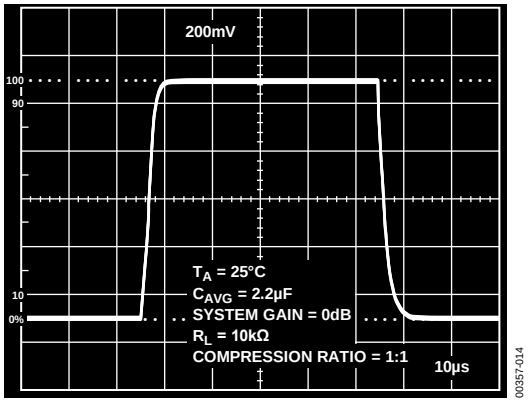


Figure 14. Large Signal Transient Response

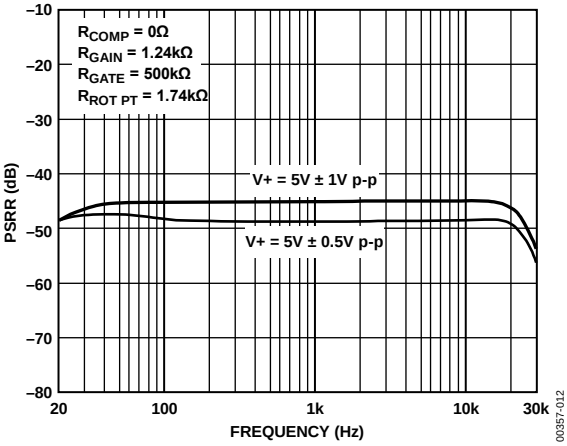


Figure 12. PSRR vs. Frequency

THEORY OF OPERATION

Figure 15 illustrates a typical transfer characteristic for the SSM2166 where the output level in decibels is plotted as a function of the input level in decibels. The dotted line indicates the transfer characteristic for a unity-gain amplifier. For input signals in the range of V_{DE} (downward expansion) to V_{RP} (rotation point), an r dB change in the input level causes a 1 dB change in the output level. Here, r is defined as the compression ratio. The compression ratio can be varied from 1:1 (no compression) to over 15:1 via a single resistor, R_{COMP}. Input signals above V_{RP} are compressed with a fixed compression ratio of approximately 15:1. This region of operation is the limiting region. Varying the compression ratio has no effect on the limiting region. The break-point between the compression region and the limiting region is referred to as the limiting threshold or the rotation point and is user specified in the SSM2166. The term "rotation point" derives from the observation that the straight line in the compression region rotates about this point on the input/output characteristic as the compression ratio is changed.

The gain of the system with an input signal level of V_{RP} is fixed by R_{GAIN}, regardless of the compression ratio, and is the nominal gain of the system. The nominal gain of the system can be increased by the user via the on-board VCA by up to 20 dB. Additionally, the input buffer of the SSM2166 can be configured to provide fixed gains of 0 dB to 20 dB with R1 and R2.

Input signals below V_{DE} are downward expanded; that is, a −1 dB change in the input signal level causes approximately a −3 dB change in the output level. As a result, the gain of the system is small for very small input signal levels, even though it may be quite large for small input signals above V_{DE}. The downward expansion threshold, V_{DE}, is set externally by the user via R_{GATE} at Pin 9 (NOISE GATE SET). The SSM2166 provides an active high, CMOS-compatible digital input whereby a power-down feature reduces the device supply current to less than 100 µA.

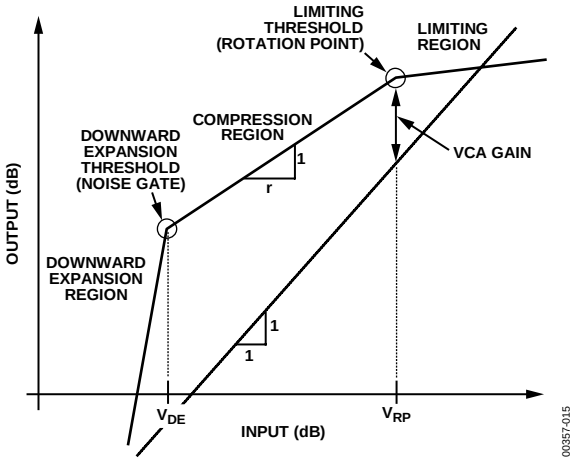


Figure 15. General Input/Output Characteristics

APPLICATIONS INFORMATION

The SSM2166 is a complete microphone signal conditioning system on a single integrated circuit. Designed primarily for voice-band applications, this integrated circuit provides amplification, rms detection, limiting, variable compression, and downward expansion. An integral voltage-controlled amplifier (VCA) provides up to 60 dB of gain in the signal path with approximately 30 kHz bandwidth. Additional gain is provided by an input buffer, op amp circuit that can be set anywhere from 0 dB to 20 dB for a total signal path gain of up to 80 dB. The device operates on a single 5 V supply, accepts input signals up to 1 V rms, and produces output signal levels >1 V rms (3 V p-p) into loads >5 kΩ. The internal rms detector has a time constant set by an external capacitor.

The SSM2166 contains an input buffer and automatic gain control (AGC) circuit for audio-band and voice-band signals. Circuit operation is optimized by providing a user-adjustable time constant and compression ratio. A downward expansion (noise gating) feature eliminates circuit noise in the absence of an input signal. The SSM2166 allows the user to set the downward expansion threshold, the limiting threshold (rotation point), the input buffer fixed gain, and the internal VCA nominal gain at the rotation point. The SSM2166 also features a power-down mode and muting capability.

SIGNAL PATH

Figure 16 illustrates the block diagram of the SSM2166. The audio input signal is processed by the input buffer and then by the VCA. The input buffer presents an input impedance of approximately 180 kΩ to the source. A dc voltage of approximately 1.5 V is present at AUDIO +IN (Pin 7), requiring the use of a blocking capacitor (C1) for ground referenced sources. A 0.1 µF capacitor is a good choice for most audio applications. The input buffer is a unity-gain stable amplifier that can drive the low impedance input of the VCA.

The VCA is a low distortion, variable-gain amplifier (VGA) whose gain is set by the side-chain control circuitry. The input to the VCA is a virtual ground in series with approximately 1 kΩ. An external blocking capacitor (C6) must be used between the buffer output and the VCA input. The 1 kΩ impedance between amplifiers determines the value of this capacitor, which is typically between 1 µF and 10 µF. An aluminum electrolytic capacitor is an economical choice. The VCA amplifies the input signal current flowing through C6 and converts this current to a voltage at the OUTPUT pin (Pin 13). The net gain from input to output can be as high as 60 dB (without additional buffer gain), depending on the gain set by the control circuitry.

The gain of the VCA at the rotation point is set by the value of a resistor, R_{GAIN}, connected between Pin 2 and GND. The relationship between the VCA gain and R_{GAIN} is shown in Figure 6. The AGC range can be as high as 60 dB. The VCA_{IN} pin (Pin 3) is the non-inverting input terminal to the VCA. The inverting input of the VCA is available at the VCA_R pin (Pin 4) and exhibits an input impedance of 1 kΩ, as well. As a result, this pin can be used for differential inputs or for the elimination of grounding problems by connecting a capacitor whose value equals that used in series with the VCA_{IN} pin to ground (see Figure 26 for more details).

The output impedance of the SSM2166 is typically less than 75 Ω, and the external load on Pin 13 should be >5 kΩ. The nominal output dc voltage of the device is approximately 2.2 V. Use a blocking capacitor for grounded loads.

The bandwidth of the SSM2166 is quite wide at all gain settings. The upper 3 dB point is approximately 30 kHz at gains as high as 60 dB (using the input buffer for additional gain, circuit bandwidth is unaffected). The gain bandwidth (GBW) plots are shown in Figure 11. The lower 3 dB cutoff frequency of the SSM2166 is set by the input impedance of the VCA (1 kΩ) and C6. While the noise of the input buffer is fixed, the input referred noise of the VCA is a function of gain. The VCA input noise is designed to be a minimum when the gain is at a maximum, thereby optimizing the usable dynamic range of the part. A plot of wideband peak-to-peak output noise is shown in Figure 10.

LEVEL DETECTOR

The SSM2166 incorporates a full-wave rectifier and true rms level detector circuit whose averaging time constant is set by an external capacitor connected to the AVG CAP pin (Pin 8). For optimal low frequency operation of the level detector down to 10 Hz, the value of the capacitor should be 2.2 µF. Some experimentation with larger values for the AVG CAP may be necessary to reduce the effects of excessive low frequency ambient background noise. The value of the averaging capacitor affects sound quality: too small a value for this capacitor may cause a pumping effect for some signals, while too large a value may result in slow response times to signal dynamics. Electrolytic capacitors are recommended for lowest cost and should be in the range of 2 µF to 47 µF. Capacitor values from 18 µF to 22 µF have been found to be more appropriate in voice-band applications where capacitors on the low end of the range seem more appropriate for music program material.

The rms detector filter time constant is approximately given by 10 × C_{AVG} milliseconds, where C_{AVG} is in µF. This time constant controls both the steady-state averaging in the rms detector as well as the release time for compression; that is, the time it takes for the system gain to react when a large input is followed by a small signal. The attack time, the time it takes for the gain to be reduced when a small signal is followed by a large signal, is controlled partly by the AVG CAP value but is mainly controlled by internal circuitry that speeds up the attack for large level changes. This limits overload time to less than 1 ms in most cases.

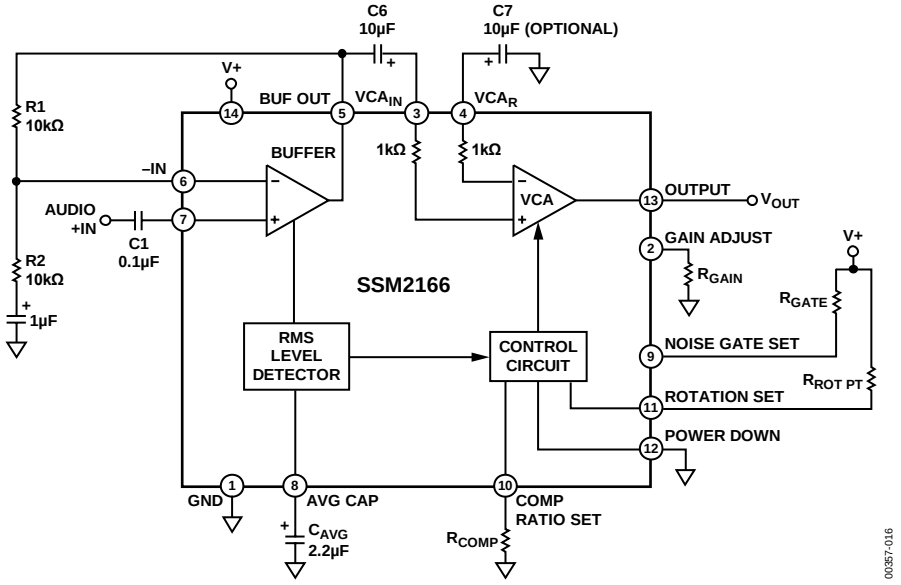


Figure 16. Functional Block Diagram and Typical Application

The performance of the rms level detector is illustrated for a C_{AVG} of 2.2 µF in Figure 17 and for a C_{AVG} of 22 µF in Figure 18. In each of these images, the input signal to the SSM2166 (not shown) is a series of tone bursts in six successive 10 dB steps. The tone bursts range from −66 dBV (0.5 mV rms) to −6 dBV (0.5 V rms). As shown in Figure 17 and Figure 18, the attack time of the rms level detector is dependent only on C_{AVG}, but the release times are linear ramps whose decay times are dependent on both C_{AVG} and the input signal step size. The rate of release is approximately 240 dB/s for a C_{AVG} of 2.2 µF and 12 dB/s for a C_{AVG} of 22 µF.

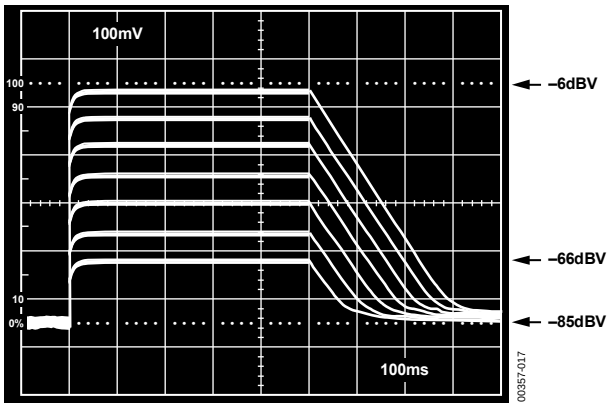


Figure 17. RMS Level Detector Performance with C_{AVG} = 2.2 µF

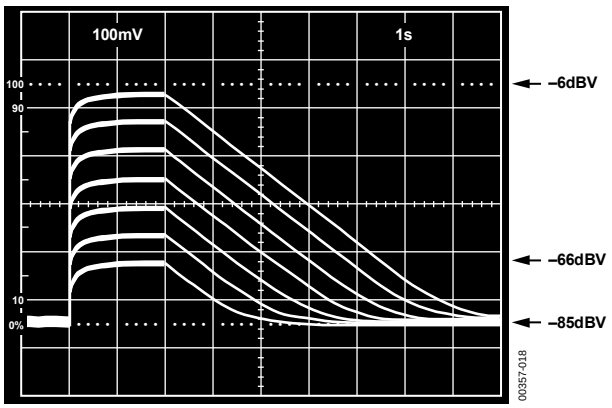


Figure 18. RMS Level Detector Performance with C_{AVG} = 22 µF

CONTROL CIRCUITRY

The output of the rms level detector is a signal proportional to the log of the true rms value of the buffer output with an added dc offset. The control circuitry subtracts a dc voltage from this signal, scales it, and sends the result to the VCA to control the gain. The gain control of the VCA is logarithmic—a linear change in the control signal causes a decibel change in gain. It is this control law that allows linear processing of the log rms signal to provide the flat compression characteristic on the input/output characteristic shown in Figure 15.

Compression Ratio

Changing the scaling of the control signal fed to the VCA causes a change in the circuit compression ratio, r. This effect is shown in Figure 20. The compression ratio can be set by connecting a resistor between the COMP RATIO SET pin (Pin 10) and GND. Lowering R_{COMP} gives smaller compression ratios as shown in Figure 19, with values of approximately 0.17 kΩ or less resulting in a compression ratio of 1:1. AGC performance is achieved with compression ratios between 2:1 and 15:1 and is dependent on the application. A 100 kΩ potentiometer can be used to allow this parameter to be adjusted. On the evaluation board (see Figure 26), an optional resistor can be used to set the compression equal to 1:1 when the wiper of the potentiometer is at its full counterclockwise (CCW) position.

COMPRESSION RATIO / ROTATION POINT	1:1	2:1	5:1	10:1	15:1
100mV rms	0.1	8.7	19.4	45	395
300mV rms	0.1	8.7	19.4	45	N/A
1V rms	0.1	8.7	19.4	45	N/A

TYPICAL R_{COMP} VALUES IN kΩ.

00357-031

Figure 19. Compression Ratio vs. R_{COMP} (Pin 10 to GND)

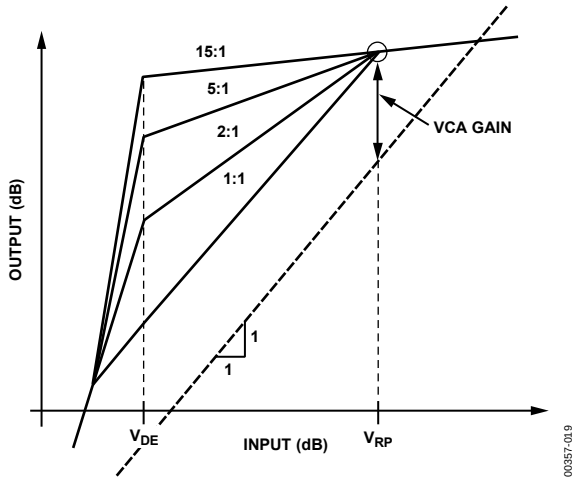


Figure 20. Effect of Varying the Compression Ratio

Rotation Point

An internal dc reference voltage in the control circuitry, used to set the rotation point, is user specified, as illustrated in Figure 9. The effect on rotation point is shown in Figure 21. By varying a resistor, $R_{ROT\ PT}$, connected between the positive supply and the ROTATION SET pin (Pin 11), the rotation point may be varied by approximately 20 mV rms to 1 V rms. From Figure 21, the rotation point is inversely proportional to $R_{ROT\ PT}$. For example, a 1 kΩ resistor would typically set the rotation point at 1 V rms, whereas a 55 kΩ resistor would typically set the rotation point at approximately 30 mV rms.

Because limiting occurs for signals larger than the rotation point ($V_{IN} > V_{RP}$), the rotation point effectively sets the maximum output signal level. It is recommended that the rotation point be set at the upper extreme of the range of typical input signals so that the compression region covers the entire desired input signal range. Occasional larger signal transients are then attenuated by the action of the limiter.

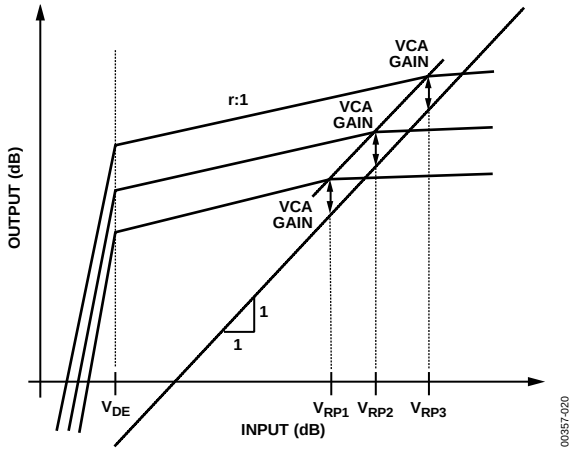


Figure 21. Effect of Varying the Rotation Point

VCA Gain Setting and Muting

The maximum gain of the SSM2166 is set by the GAIN ADJUST pin (Pin 2) via R_{GAIN}. This resistor, with a range of 1 kΩ to 20 kΩ, causes the nominal VCA gain to vary from 0 dB to approximately 20 dB, respectively. Setting the VCA gain to its maximum can also be achieved by leaving the GAIN ADJUST pin in an open condition (no connect). Figure 22 illustrates the effect on the transfer characteristic by varying this parameter. For low level signal sources, the VCA should be set to maximum gain using a 20 kΩ resistor.

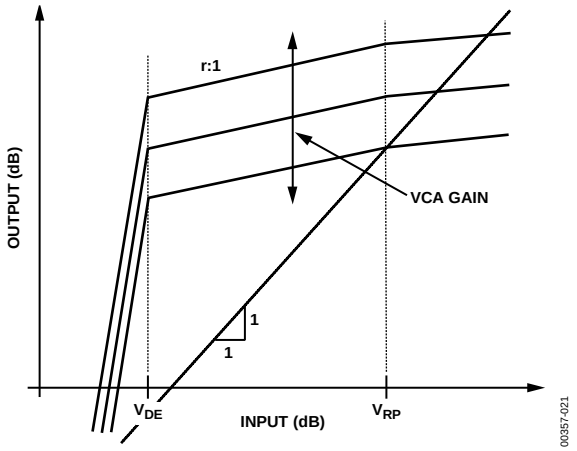


Figure 22. Effect of Varying the VCA Gain Setting

The gain of the VCA can be reduced below 0 dB by making R_{GAIN} smaller than 1 kΩ. Switching Pin 2 through 330 Ω or less to GND mutes the output. Either a switch connected to ground or a transistor can be used, as shown in Figure 23. To avoid audible clicks when using the mute feature, a capacitor (C5) can be connected from Pin 2 to GND. The value of the capacitor is arbitrary and should be determined empirically, but a 0.01 µF capacitor is a good starting value.

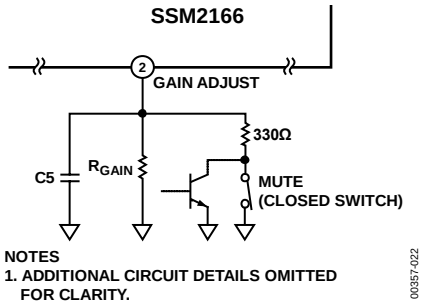


Figure 23. Details of Mute Option

Downward Expansion Threshold

The downward expansion threshold, or noise gate, is determined via a second reference voltage internal to the control circuitry. This second reference can be varied in the SSM2166 using a resistor, R_{GATE}, connected between the positive supply and the NOISE GATE SET pin (Pin 9). The effect of varying this threshold is shown in Figure 24. The downward expansion threshold can be set between 300 µV rms and 20 mV rms by varying the resistance value between Pin 9 and the supply voltage. Like the ROTATION SET pin, the downward expansion threshold is inversely proportional to the value of this resistance: setting this resistance to 1 MΩ sets the threshold at approximately 250 µV rms, whereas a 10 kΩ resistance sets the threshold at approximately 20 mV rms. This relationship is illustrated in Figure 5. A potentiometer network is provided on the evaluation board for this adjustment. In general, the downward expansion threshold should be set at the lower extreme of the desired range of the input signals so that signals below this level are attenuated.

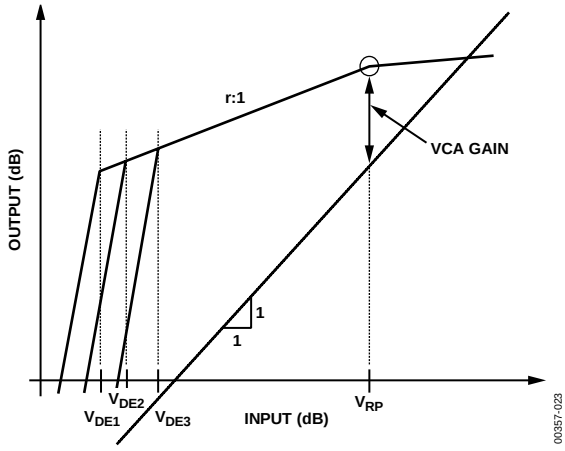


Figure 24. Effect of Varying the Downward Expansion (Noise Gate) Threshold

POWER-DOWN FEATURE

The supply current of the SSM2166 can be reduced to less than 100 µA by applying an active high, 5 V CMOS-compatible input to the POWER DOWN pin (Pin 12). In this state, the input and output circuitry of the SSM2166 assumes a high impedance state; as such, the potentials at the input pin and the output pin are determined by the external circuitry connected to the SSM2166. The SSM2166 takes approximately 200 ms to settle from a power-down to power-on command. For power-on to power-down, the SSM2166 requires more time, typically less than 1 second. Cycling the power supply to the SSM2166 can result in quicker settling times: the off-to-on settling time of the SSM2166 is less than 200 ms, while the on-to-off settling time is less than 1 ms. In either implementation, transients may appear at the output of the device. To avoid these output transients, use mute control of the VCA gain as previously mentioned.

PCB LAYOUT CONSIDERATIONS

Because the SSM2166 is capable of wide bandwidth operation and can be configured for as much as 80 dB of gain, special care must be exercised in the layout of the PCB that contains the IC and its associated components. The following recommendations should be considered and/or followed:

- In some high system gain applications, the shielding of input wires to minimize possible feedback from the output of the SSM2166 back to the input circuit may be necessary.
- A single-point (star) ground implementation is recommended in addition to maintaining short lead lengths and PCB runs. The evaluation board layout shown in Figure 27, Figure 28, and Figure 29 demonstrates the single-point grounding scheme. In applications where an analog ground and a digital ground are available, the SSM2166 and its surrounding circuitry should be connected to the analog ground of the system. Because of these recommendations, wire-wrap board connections and grounding implementations should be avoided.
- The internal buffer of the SSM2166 was designed to drive only the input of the internal VCA and its own feedback network. Stray capacitive loading to ground from the BUF OUT pin in excess of 5 pF to 10 pF can cause excessive phase shift and can lead to circuit instability.
- When using high impedance sources (≥5 kΩ), system gains in excess of 60 dB are not recommended. This configuration is rarely appropriate because virtually all high impedance inputs provide larger amplitude signals that do not require as much amplification. When using high impedance sources, however, it can be advantageous to shunt the source with a capacitor to ground at the input pin of the IC (Pin 7) to lower the source impedance at high frequencies, as shown in Figure 25. A capacitor with a value of 1000 pF is a good starting value and sets a low-pass corner at 31 kHz for 5 kΩ sources. In applications where the source ground is not as clean as would be desirable, a capacitor (illustrated as C7 on the evaluation board) from the VCA_R input to the source ground may prove beneficial. This capacitor is used in addition to the grounded capacitor (illustrated as C2 on the evaluation board) used in the feedback around the buffer, assuming that the buffer is configured for gain.

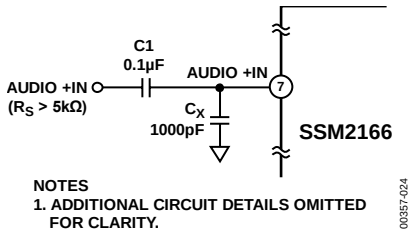


Figure 25. Circuit Configuration for Use with High Impedance Signal Sources

The value of C7 should be the same as C6, which is the capacitor value used between BUF OUT and VCA_{IN}. This connection makes the source ground noise appear as a common-mode signal to the VCA, allowing the common-mode noise to be rejected by the VCA differential input circuitry. C7 can also be useful in reducing ground loop problems and in reducing noise coupling from the power supply by balancing the impedances connected to the inputs of the internal VCA.

EVALUATION BOARD

A schematic diagram of the SSM2166 evaluation board is illustrated in Figure 26. As a design aid, the layouts for the topside silkscreen and the topside and backside metallization layers are shown in Figure 27, Figure 28, and Figure 29. Although not shown to scale, the finished dimension of the evaluation board is 3.5 inches by 3.5 inches and comes complete with pin sockets and a sample of the SSM2166.

Signal sources are connected to the SSM2166 through a 1/8-inch phone jack where a 0.1 µF capacitor couples the input signal to the AUDIO +IN pin (Pin 7). As shown in Figure 26 and in microphone applications, the phone jack shield can be optionally connected to the ground plane of the board (Jumper J1 inserted into the board socket for Pin 1 and Pin 2) or to the VCA_R input at Pin 4 (J1 inserted into the board socket for Pin 1 and Pin 3). If the signal source is a waveform or function generator, the phone jack shield should be connected to ground.

For ease in making adjustments for all configuration parameters, single-turn potentiometers are used throughout. Optional Jumper J2 connects the COMP RATIO SET pin to ground and sets the SSM2166 for no compression (that is, compression ratio = 1:1). Optional Jumper J3 connects the POWER DOWN (Pin 12) input to ground for normal operation. J3 can be replaced by an open-drain logic buffer for a digitally controlled shutdown function. An output signal mute function can be implemented on the SSM2166 by connecting the GAIN ADJUST pin (Pin 2) through a 330 Ω resistance to ground. This is provided on the evaluation board via R11 and S1. Capacitor C5, connected between Pin 2 and ground and provided on the evaluation board, can be used to avoid audible clicks when using the mute function.

To configure the SSM2166 input buffer for gain, provisions for R1, R2, and C2 have been included. To configure the input buffer for unity-gain operation, R1 and R2 are removed and a direct connection is made between the –IN pin (Pin 6) and the BUF OUT pin (Pin 5).

The output stage of the SSM2166 is capable of driving >1 V rms (3 V p-p) into >5 kΩ loads and is externally available through an RCA phono jack provided on the board. If the output of the SSM2166 is required to drive a lower load resistance or an audio cable, the on-board OP113 can be used. To use the OP113 buffer, insert Jumper J4 into the board socket for Pin 4 and Pin 5 and insert Jumper J5 into the board socket for Pin 6 and Pin 7. If the output buffer is not required, remove Jumper J5 and insert Jumper J4 into board socket Pin 5 and Pin 7.

There are no blocking capacitors either on the input or at the output of the buffer. As a result, the output dc level of the buffer matches the output dc level of the SSM2166, which is approximately 2.3 V. A dc blocking capacitor can be inserted at Pin 6 and Pin 7. An evaluation board and setup procedure is available from an Analog Devices, Inc., sales representative.

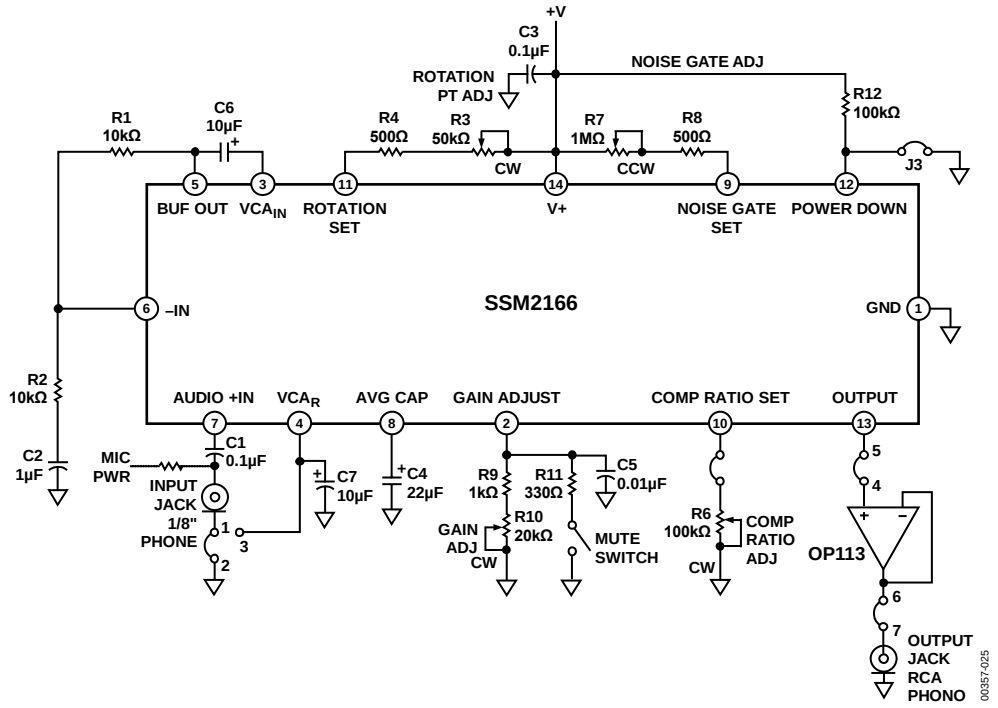


Figure 26. Evaluation Board Schematic

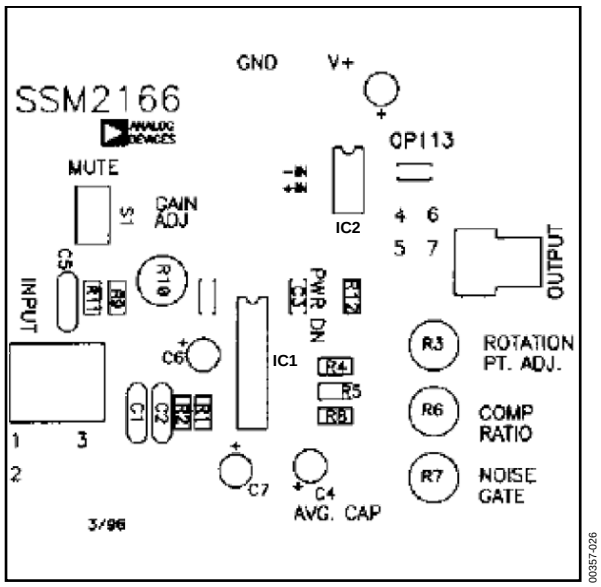


Figure 27. Evaluation Board Topside Silkscreen (Not to Scale)

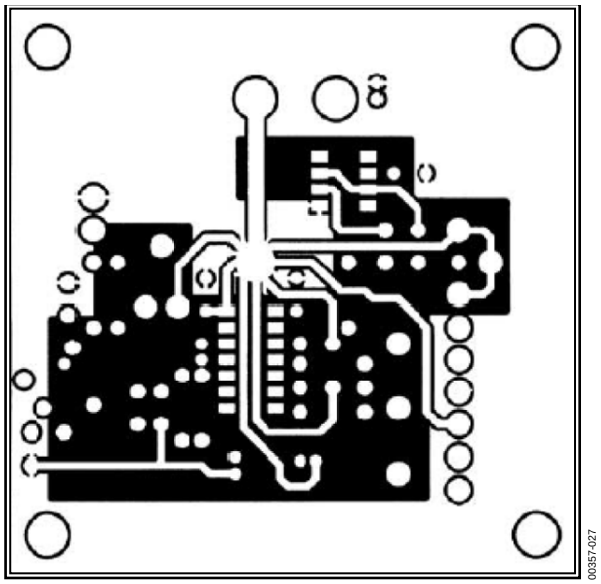


Figure 28. Evaluation Board Topside Metallization (Not to Scale)

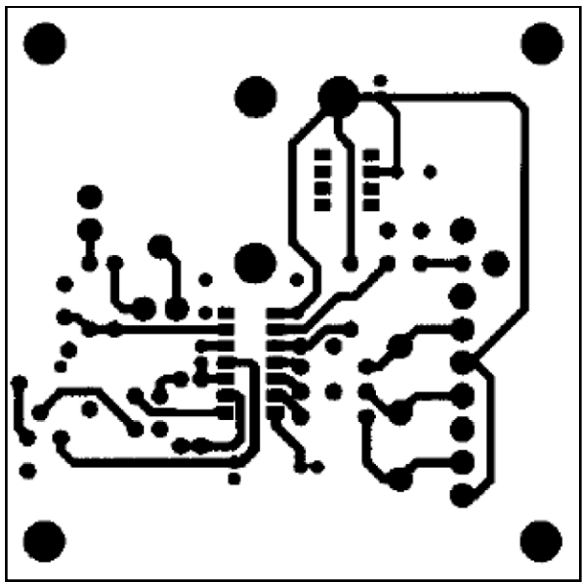


Figure 29. Evaluation Board Backside Metallization (Not to Scale)

EVALUATION BOARD EXAMPLES

To illustrate how easy it is to program the SSM2166, a practical example is provided. The SSM2166 was used to interface an electret-type microphone to a postamplifier. The evaluation board or the circuit configuration shown in Figure 26 can be used. The signal from the microphone was measured under actual conditions to vary from 1 mV to 15 mV. The postamplifier requires no more than 500 mV at its input. The required gain from the SSM2166 is, therefore

$$G_{TOTAL} = 20 \times \log(500/15) = 30 \text{ dB}$$

The input buffer gain is set to 20 dB, and the VCA gain is adjusted to 10 dB. The limiting or rotation point is set at 500 mV output. A 2:1 compression ratio and a noise gate threshold that operates below 100 µV is also used. These objectives are summarized in Table 5. The transfer characteristic implemented is illustrated in Figure 30.

Table 5. Objective Specifications

Parameter	Value
Input Range	1 mV to 15 mV
Output Range	To 500 mV
Limiting Level	500 mV
Compression	2:1
Buffer Gain	20 dB
VCA Gain	10 dB
Noise Gate	100 µV

Note that the SSM2166 processes the output of the buffer, which in the previous example is 20 dB or 10 times the input level. Use the oscilloscope to verify that the buffer is not being driven into clipping with excessive input signals. In the application, take the minimum gain in the buffer consistent with the average source level as well as the crest factor (ratio of peak to rms).

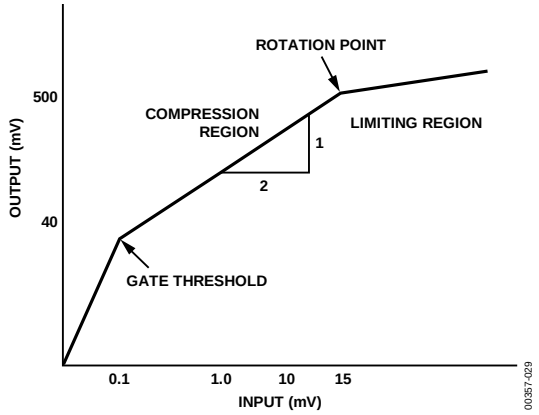


Figure 30. Transfer Characteristic

EVALUATION BOARD SETUP PROCEDURE

When building a breadboard, keep the leads to Pin 3, Pin 4, and Pin 5 short. An evaluation board is available from an Analog Devices sales representative. The R and C designations refer to the demonstration board schematic of Figure 26 and the parts list in Table 7.

TEST EQUIPMENT SETUP

The recommended equipment and configuration are shown in Figure 31. A low noise audio generator with a smooth output adjustment range of 50 µV to 50 mV is a suitable signal source. A 40 dB pad is useful to reduce the level of most generators by 100× to simulate the microphone levels. The input voltmeter can be connected before the pad and need only go down to 10 mV. The output voltmeter should go up to 2 V. The oscilloscope is used to verify that the output is sinusoidal and that no clipping occurs in the buffer, and to set the limiting and noise gating knees.

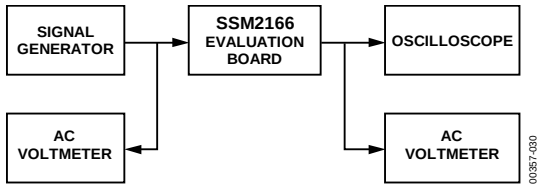


Figure 31. Test Equipment Setup

Step 1: Configure the Buffer

The SSM2166 has an input buffer that can be used when the overall gain required exceeds 20 dB, the maximum user-selectable gain of the VCA. In the example, the desired output is 500 mV for an input of ~15 mV, requiring a total gain of 30 dB. Set the buffer gain at 20 dB and adjust the VCA for 10 dB. In the socket pins provided on the evaluation board, insert R1 = 100 kΩ and R2 = 11 kΩ. The buffer gain is set to 20 dB (×10).

Step 2: Initializing Potentiometers

With the power off, preset the potentiometers per Table 6.

Step 3: Testing Setup

With the power on, adjust the generator for an input level of 15 mV, 1 kHz. The output meter should indicate approximately 100 mV; if not, check the setup.

Step 4: Adjusting the Rotation Point

Set the input level to 15 mV and observe the output on the oscilloscope. Adjust R3, ROTATION PT ADJ, until the output level just begins to drop, then reverse so that the output is 500 mV. The limiting has been set to 500 mV.

Step 5: Adjusting the VCA Gain

Set the input level to 15 mV. Adjust R10, GAIN ADJ, clockwise (CW) for an output level of 500 mV. The VCA gain has been set to 10 dB.

Step 6: Adjusting the Compression Ratio

Set the input signal for an output of 500 mV but not in limiting. Note the value (around 15 mV). Next, reduce the input to 1/10 of the value noted (around 1.5 mV) for a change of −20 dB. Next, adjust R6, COMP RATIO ADJ, CW until the output is 160 mV for an output change of −10 dB. The compression, which is the ratio of the output change to the input change, in decibels (dB), has been set to 2:1.

Step 7: Setting the Noise Gate

With the input set at 100 µV, observe the output on the oscilloscope and adjust R7, NOISE GATE ADJ, CCW until the output drops rapidly. Rock the control back and forth to find the knee. The noise gate has been set to 100 µV. The range of the noise gate is from 0.3 mV to over 0.5 mV relative to the output of the buffer. To fit this range to the application, it may be necessary to attenuate the input or apportion the buffer gain and VCA gain differently.

Step 8: Listening

At this time, it may be desirable to connect an electret microphone to the SSM2166 and listen to the results. Be sure to include the proper power for the internal FET of the microphone (usually 2 V dc to 5 V dc through a 2.2 kΩ resistor). Experiment with the settings to hear how the results change. Varying the averaging capacitor, C4, changes the attack and decay times, which are best determined empirically. The compression ratio keeps the output steady over a range of microphone to speaker distances, and the noise gate keeps the background sounds subdued.

Step 9: Recording Values

With the power removed from the test fixture, measure and record the values of all potentiometers, including any fixed resistance in series with them. If the averaging capacitor, C4, changes, also note its value.

SETUP SUMMARY

The transfer condition of Figure 2 has been implemented. For inputs below the 100 µV noise gate threshold, circuit and background noise is minimized. Above it, the output increases at a rate of 1 dB for each 2 dB input increase until the 500 mV rotation point is reached at an input of approximately 15 mV. For higher inputs that drive the output beyond 500 mV, limiting occurs and there is little further increase. The SSM2166 processes the output of the buffer, which in the previous example is 20 dB, or 10× the input level. Use the oscilloscope to ensure that the buffer is not being driven into clipping with the highest expected input peaks. Always take the minimum gain in the buffer consistent with the average source level and crest factor (ratio of peak to rms). The wide program range of the SSM2166 makes it useful in many applications other than microphone signal conditioning.

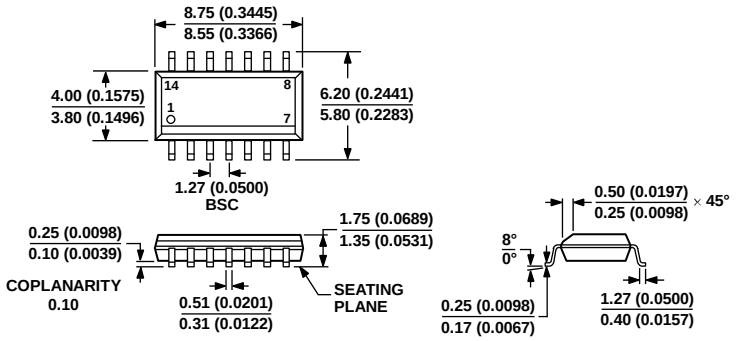
Table 6. Initial Potentiometer Settings

Function	Potentiometer	Range	Initial Position	Initial Resistance	Effect of Change
Gain Adjust (VCA)	R10	0 kΩ to 20 kΩ	CCW	0 Ω	0 dB; CW to increase VCA gain
Rotation Point	R3	0 kΩ to 50 kΩ	CCW	0 Ω	1 V; CW to reduce rotation point
Compression Point	R6	0 kΩ to 100 kΩ	CCW	0 Ω	1:1; CW to increase compression
Noise Gate	R7	0 kΩ to 1 MΩ	CW	1 MΩ	300 µV; CCW to increase threshold

Table 7. Demonstration Board Parts List

Component	Value	Description
R1	10 kΩ resistor	Feedback
R2	10 kΩ resistor	Input
R3	50 kΩ potentiometer	Rotation point, adjust
R4	500 Ω resistor	Rotation point, fixed
R5	0 Ω resistor	Compression ratio, fixed
R6	100 kΩ potentiometer	Compression ratio, adjust
R7	1 MΩ potentiometer	Noise gate, adjust
R8	500 Ω resistor	Noise gate, fixed
R9	1 kΩ resistor	Gain adjust, fixed
R10	20 kΩ potentiometer	Gain adjust
R11	330 Ω resistor	Mute
R12	100 kΩ resistor	Power-down, pull-up
C1	0.1 µF capacitor	Input dc block
C2	1 µF capacitor	Buffer low F, G = 1
C3	0.1 µF capacitor	+V bypass
C4	2.2 µF to 22 µF capacitor	Average capacitor
C5	0.01 µF capacitor	Mute click suppress
C6	10 µF capacitor	Coupling
C7	10 µF capacitor	VCA noise/dc balance
IC1	SSM2166	MIC preamp
IC2	OP113, IC	Operational amplifier, output buffer
S1	SPST, Switch	Mute
J1	1/8-inch mini phone plug jumper	MIC input
J2	RCA female jumper	Output jack

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 32. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2166SZ	−40°C to +85°C	14-Lead SOIC_N	R-14
SSM2166SZ-REEL	−40°C to +85°C	14-Lead SOIC_N	R-14
SSM2166SZ-REEL7	−40°C to +85°C	14-Lead SOIC_N	R-14

[1] Z = RoHS Compliant Part.

Top Branding Revision Reflecting Die Replacement

Version	Original Die Revision (Prior to Rev. C of Data Sheet)	New Die Revision (Rev. C to Current Revision of Data Sheet)
Pb-Free (RoHS) Version	Top Line 1: SSM Top Line 2: 2166 Top Line 3: # XXXX[2]	Top Line 1: SSM Top Line 2: 2166A[1] Top Line 3: # XXXX[2]

[1] Letter A designates new die revision; refer to revised external component values in Figure 5, Figure 6, Figure 9, and Figure 19.
[2] # designates RoHS version.

NOTES

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