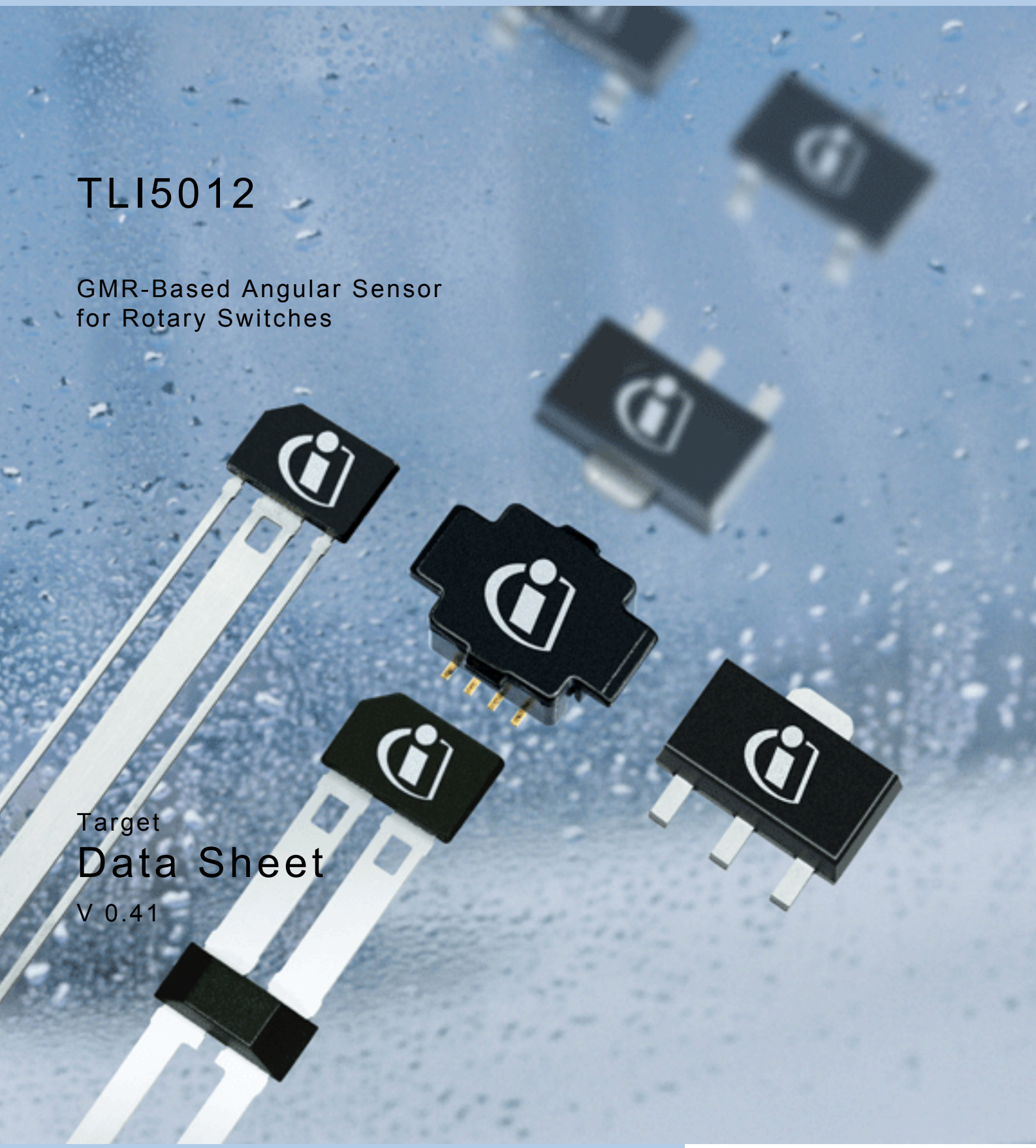
March 2009

TLI5012

GMR-Based Angular Sensor
for Rotary Switches



Target

Data Sheet

V 0.41

Sensors

Never stop thinking

Edition 2009-03

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TLI5012 GMR-Based Angular Sensor

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Page	Subjects (major changes since last revision)
general	Correction of typing errors
gerneral	Name of product type changed
7	Marking and Ordering Code added
12	Figure 4 updated
14	Figure 5 and figure 6 updated
15	Magnetic Induction reduced in Table 3; Storage Temperature reduced in Table 2; Note added
16	Calculation of the Junction Temperature added
18	Figure 7 updated
19	Angle Delay Time with Prediction in Table 7 added; Figure 8 updated
20	Figure 9 and Figure 10 updated
42	Table 14, Thermal resistance added

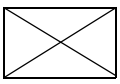
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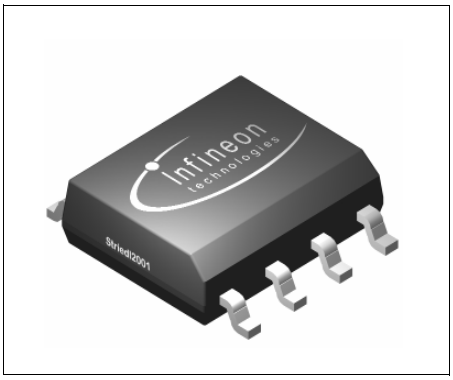
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1 Product Description



1.1 Overview

The TLI5012 is a 360° angle sensor that detects the orientation of a magnetic field. This is achieved by measuring sine and cosine angle components with monolithic **i**ntegrated **G**iant **M**agneto **R**esistance (**iGMR**) elements.

An angle error smaller than 5° will be achieved over temperature.

Data communications are accomplished with a bi-directional SSC Interface that is SPI compatible.

The absolute angle value and other values are transmitted via SSC or via a Pulse-Width-Modulation (PWM) Protocol. Also the sine and cosine raw values can be read out. These raw signals are digitally processed internally to calculate the angle orientation of the magnetic field (magnet).

The TLI5012 is a precalibrated sensor. The calibration parameters are stored in laser fuses. At start-up the values of the fuses are written into Flip-Flops, where these values can be changed by the application specific parameters.

Product Type	Marking	Ordering Code	Package
TLI5012	I5012	SP000634318	PG-DSO-8

1.2 Features

- **G**iant **M**agneto **R**esistance (GMR)-based principle
- Integrated magnetic field sensing for angle measurement
- Full calibrated 0 - 360° angle measurement with revolution counter and angle speed measurement
- Two separate highly accurate single bit SD-ADC
- 15 bit representation of absolute angle value on the output (resolution of 0.01°)
- Bi-directional SSC Interface up to 8Mbit/s
- Interfaces: SSC, PWM
- 0.25 µm CMOS technology
- Temperature range: -40°C to 125°C (Junction Temperature)
- ESD > 2kV (HBM)
- Green package with lead-free (Pb-free) plating

1.3 Application Example

The TLI5012 GMR-Based Angular Sensor is designed for angular position sensing in industrial applications, such as:

- Rotary Switch
- General Angular Sensing

2 Functional Description

2.1 General

The GMR sensor is implemented using vertical integration. This means that the GMR sensitive areas are integrated above the logic portion of the TLI5012 device. These GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone Sensor Bridge. These GMR elements sense one of two components of the applied magnetic field:

- X component, V_x (cosine) or the
- Y component, V_y (sine)

The advantage of a full-bridge structure is that the amplitude of the GMR signal is doubled and temperature effects cancel out each other.

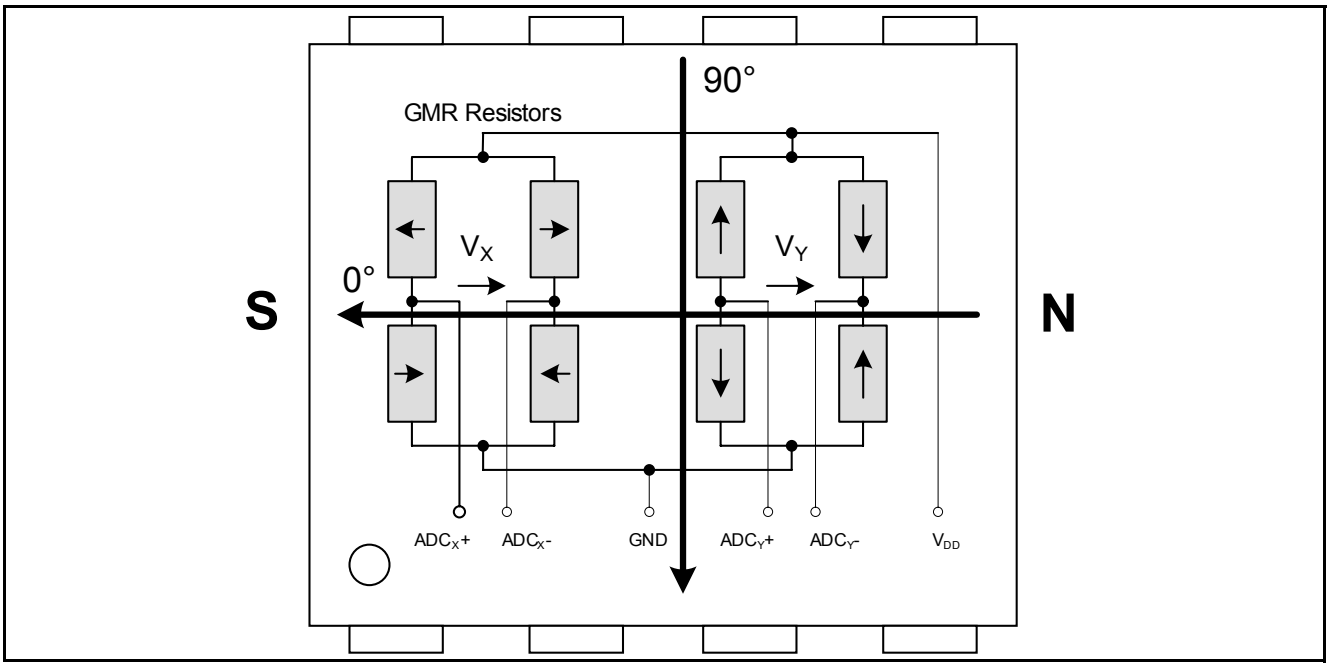


Figure 1 Sensitive Bridges of the GMR Sensor

*Note: In **Figure 1**, the arrows in the resistors symbolize the direction of the Reference Layer, which is used for the further explanation.*

The output signal of each bridge is only unambiguous over 180° between two maxima. Therefore two bridges are orientated orthogonally to each other to measure 360°.

With the trigonometric function ARCTAN, the true 360° angle value can be calulated which is represented by the relation of X and Y signals.

Because only the relative values influence the result, the absolute size of the two signals is of minor importance. Therefore, most influences to the amplitudes are compensated.

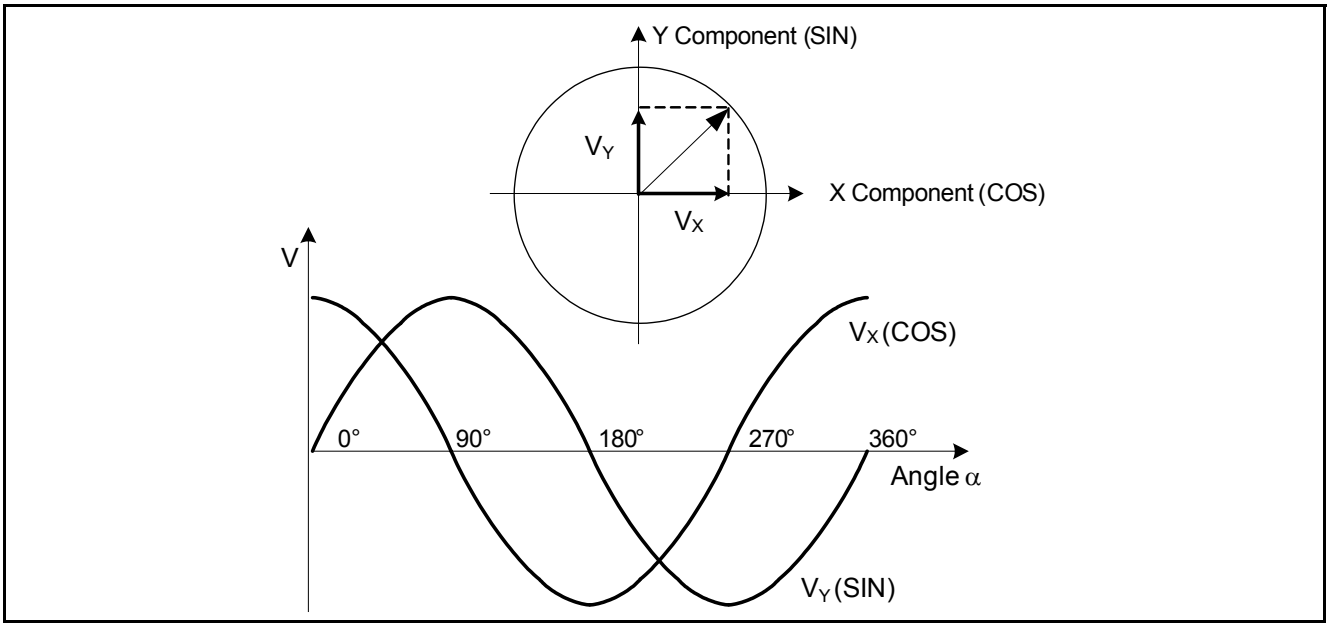


Figure 2 Ideal Output of the GMR Sensor Bridges

2.2 Pin Configuration

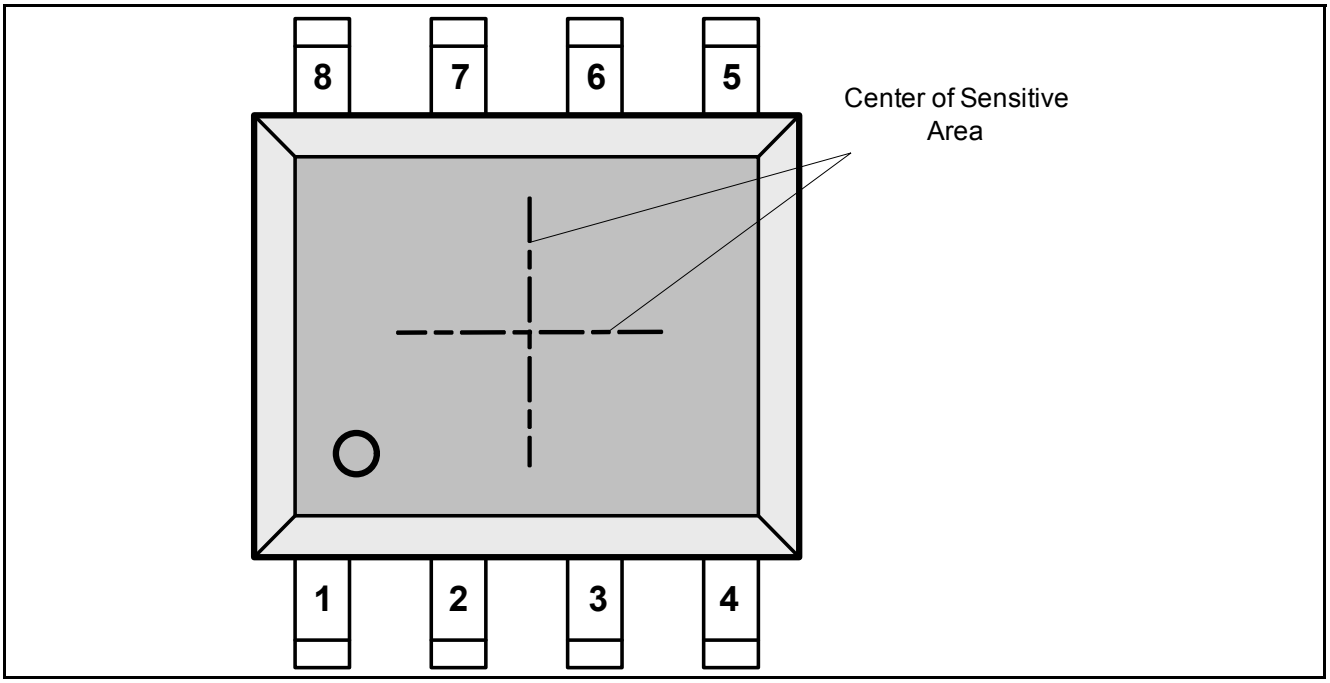


Figure 3 Pin Configuration (Top View)

2.3 Pin Description

Table 1 Pin Description

Pin No.	Symbol	In/Out	Function
1	CLK	I	External Clock (must be connected to GND for PWM output)
2	SCK	I	SSC Clock
3	CSQ	I	SSC Chip Select
4	DATA	I/O	SSC Data
5	IFA PWM	O	Interface A: PWM
6	V_{DD}	-	Supply Voltage
7	GND	-	Ground
8	IFB	O	Interface B: could be remain open or connected via resistor to GND

2.4 Block Diagram

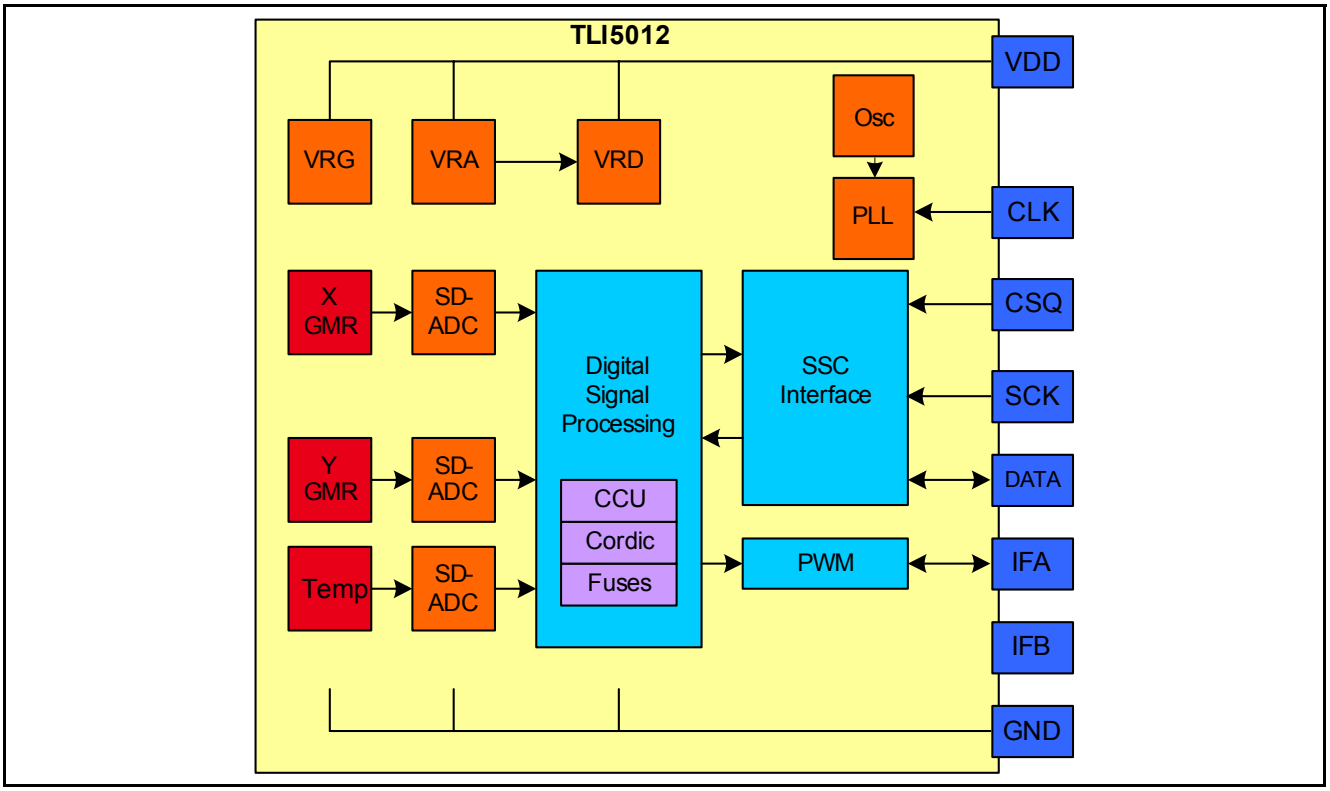


Figure 4 TLI5012 Block Diagram

2.5 Functional Block Description

2.5.1 Internal Power Supply

The internal stages of the TLI5012 are supplied with different voltage regulators.

- GMR Voltage Regulator VRG
- Analog Voltage Regulator VRA
- Digital Voltage Regulator VRD (derived from VRA)

These regulators are directly connected to the supply voltage V_{DD}.

2.5.2 Oscillator and PLL

The internal frequency oscillator feeds the **P**hase **L**ocked **L**oop (**PLL**). Also the external clock (CLK) can be used therefore.

2.5.3 SD-ADC

The SD-ADCs transform the analog GMR-voltages and temperature-voltage into the digital domain.

2.5.4 Digital Signal Processing Unit

The Digital Signal Processing Unit (DSPU) contains the:

- **C**apture **C**ompare **U**nit (**CCU**), which is used to generate the PWM signal
- **CO**ordinate **R**otation **DI**gital **C**omputer (**CORDIC**), which contains the trigonometric function for angle calculation
- Fuses, which contain the calibration parameters

2.5.5 Interfaces

Different Interfaces can be selected:

- SSC Interface
- PWM

3 Specification

3.1 Application Circuit

The application circuit in **Figure 5** and **Figure 6** show the different communication possibilities of TLI5012.

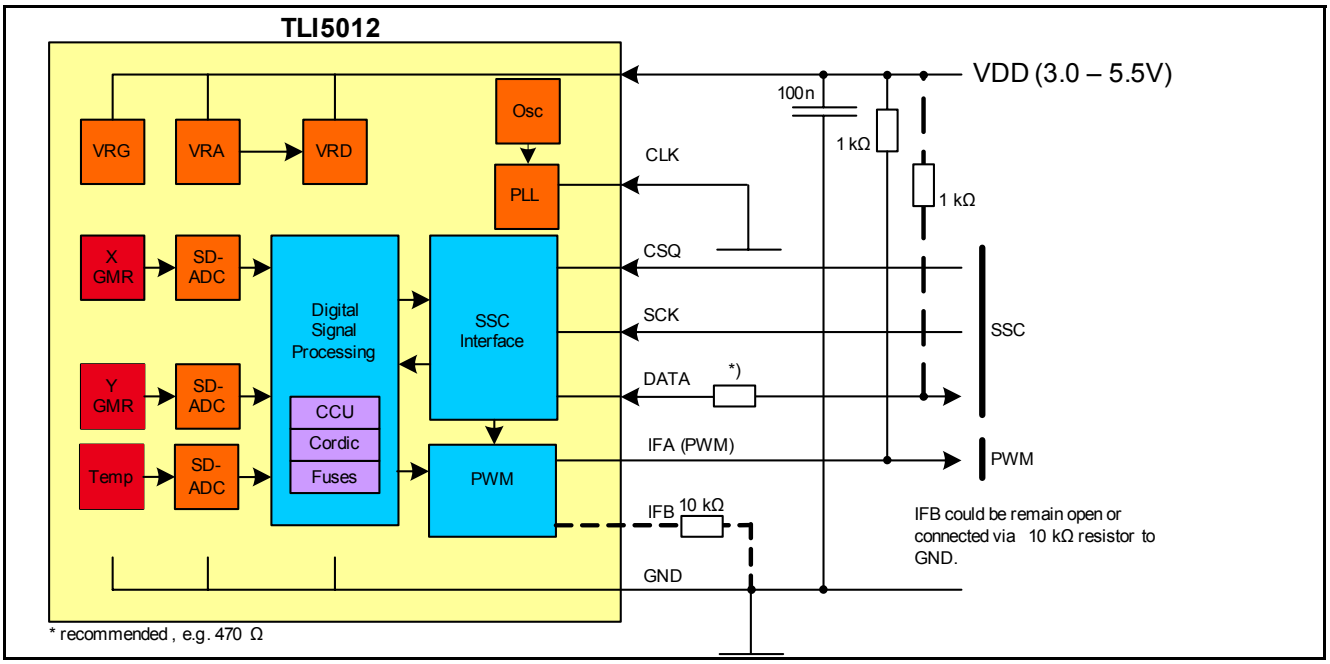


Figure 5 Application Circuit for TLI5012 with SSC and PWM Interface (using internal CLK)

Figure 5 shows a basic block-diagram of the TLI5012 with PWM- Interface. This interface is selectable by connecting CLK to GND. Additionally to the PWM the SSC Interface could be used. Within the SSC- Interface the PWM mode is selectable between Push-Pull and Open Drain.

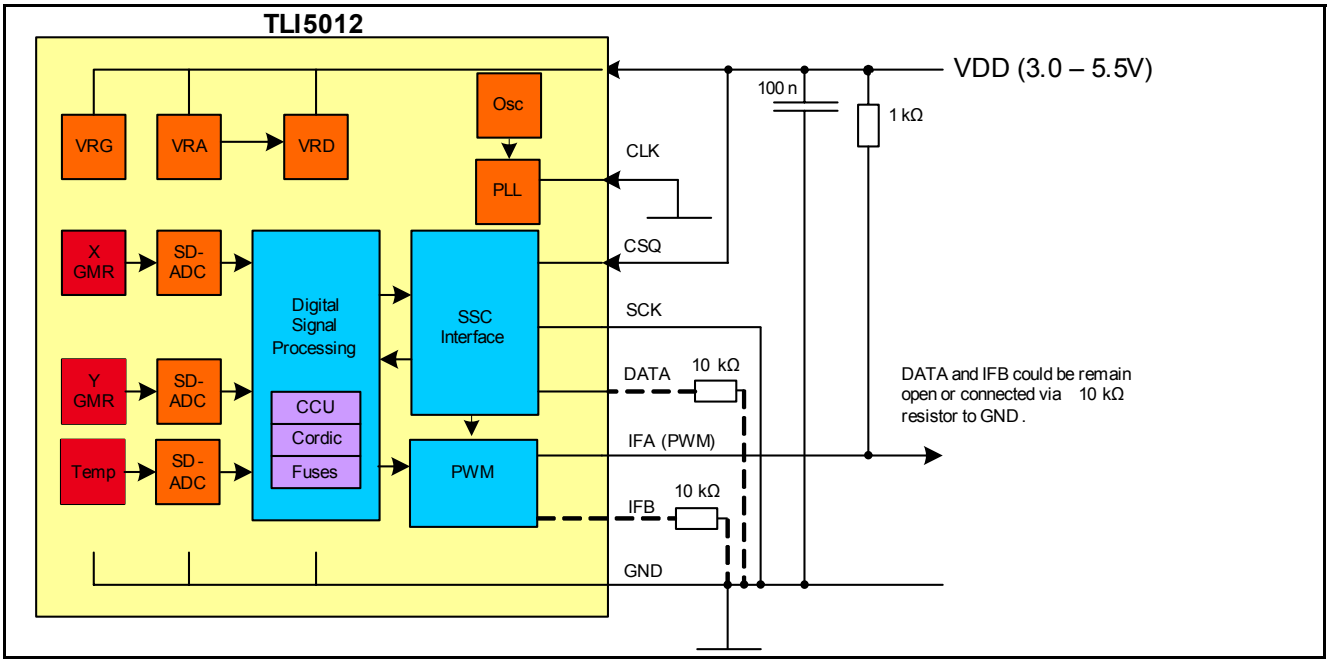


Figure 6 Application Circuit for TLI5012 with only PWM Interface (using internal CLK)

3.2 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage on V_{DD} pin respect to ground (V_{SS})	V_{DD}	-0.5	-	6.5	V	max 40 h/Lifetime
Voltage on any pin respect to ground (V_{SS})	V_{IN}	-0.5	-	6.5	V	additionally V_{DD} + 0.5 V may not be exceeded
Junction Temperature	T_J	-40	-	125	°C	
		-	-	125	°C	for 3000h not additive
Magnetic Field Induction	B	-	-	|125|	mT	max. 5 min @ t_A = 25°C
		-	-	|100|		max. 5 h @ t_A = 25°C
Storage Temperature	T_{ST}	-40	-	125	°C	

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE5012.

All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 3 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	3.0	5.0	5.5	V	1)
Output Current (DATA-Pad)	I_Q	-	-	-25	mA	PAD_DRV ='0x', sink current2)
		-	-	-5		PAD_DRV ='10', sink current2)
		-	-	-0.4		PAD_DRV ='11', sink current2)
Output Current (IFA / IFB-Pad)	I_Q	-	-	-15	mA	PAD_DRV ='0x', sink current2)
		-	-	-5		PAD_DRV ='1x', sink current2)
Input Voltage	V_{IN}	-0.3	-	5.5	V	V_{DD} + 0.3 V may not be exceeded
Magnetic Induction	B_{XY}	30	-	50	mT	in X/Y direction3)
Angle Range	Ang	0	-	360	°	

1) Directly blocked with 100nF ceramic capacitor

2) Max. current to GND over Open Drain Output

3) Values refer to an homogenous magnetic field (B_{XY}) without vertical magnetic induction (B_Z = 0mT).

*Note: The thermal resistances listed in **Table 14 "Package Parameters" on Page 42** must be used to calculate the corresponding ambient temperature. **Table 3** is valid for -40°C < T_J < 125°C.*

Calculation of the Junction Temperature

The total power dissipation P_{TOT} of the chip increases its temperature above the ambient temperature.

The power multiplied by the total thermal resistance R_{thJA} (Junction to Ambient) leads to the final junction temperature. R_{thJA} is the sum of the addition of the values of the two components *Junction to Case* and *Case to Ambient*.

$$R_{thJA} = R_{thJC} + R_{thCA} \quad (1)$$

$$T_J = T_A + \Delta T$$

$$\Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + V_{OUT} \times I_{OUT}$$ (I_{DD}, I_{OUT} > 0, if direction is into IC)

Example (assuming no load on V_{out}):

$$V_{DD} = 5V \quad (2)$$

$$I_{DD} = 12mA$$

$$\Delta T = 150\left[\frac{K}{W}\right] \times 5[V] \times 0.012[A] + 0[VA] = 9K$$

For moulded sensors, the calculation with R_{thJC} is more adequate.

3.4 Characteristics

3.4.1 Electrical Parameters

The indicated electrical parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage V_{DD} = 5.0 V and 25 °C, unless individually specified. All other values correspond to -40 °C < T_J < 125°C.

Table 4 Electrical Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Current	I_{DD}	-	12	13	mA	
POR Level	V_{POR}	2.0	-	2.9	V	Power On Reset
POR Hysteresis	V_{PORhy}	-	30	-	mV	
Power On Time	t_{Pon}	-	4	5	ms	$V_{DD} > V_{DDmin}$ 1)
Input Signal Low Level	V_L	-	-	0.3 V_{DD}	V	
Input Signal High Level	V_H	0.7 V_{DD}	-	-	V	
Pull-Up Current	I_{PU}	-10	-	-225	µA	CSQ
		-10	-	-150		DATA
Pull-Down Current	I_{PD}	10	-	225	µA	SCK
		10	-	150	µA	CLK, IFA, IFB
Output Signal Low Level	V_{OL}	-	-	1	V	DATA; I_Q = - 25 mA (PAD_DRV='0x'), I_Q = - 5 mA (PAD_DRV='10'), I_Q = - 0.4 mA (PAD_DRV='11')
		-	-	1		IFA,IFB; I_Q = - 15 mA (PAD_DRV='0x'), I_Q = - 5 mA (PAD_DRV='1x')

1) Within "Power On Time" write access is not permitted

3.4.2 ESD Protection

Table 5 ESD Protection

Parameter	Symbol	Values		Unit	Notes
		min.	max.		
ESD Voltage	V_{HBM}	-	±2.0	kV	Human Body Model 1)
	V_{SDM}	-	±0.5	kV	Socketed Device Model 2)

1) Human Body Model (HBM) according to: JEDEC EIA/JESD22-A114-B

2) Socketed Device Model (SDM) according to: ESD ASS.STD.DS5.3-93

3.4.3 Angle Performance

After internal calculation the sensor has a remaining error, as shown in **Table 6**. The error value refers to B_Z = 0mT and the operating conditions given in **Table 3 "Operating Range" on Page 15**.

The overall angle error represents the relative angle error. This error describes the deviation to the reference line after zero angle definition.

Table 6 Angle Performance

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overall Angle Error	α_{Err}	-	0.7[1)]	5.0	°	including temperature drift[2)3)]

1) At 25°C, B =30 mT

2) Including hysteresis error, caused by revolution direction change.

3) With magnetic setup in chip production (Fused Calibration Parameters); Relative error after zero angle definition.

3.4.4 Signal Processing

The signal path of the TLI5012 is depicted in **Figure 7**. It consists of the GMR-bridge, ADC, filter and angle calculation. Depending on the filter configuration a different total delay time is achieved. Additional to this delay time, the delay time of the interface has to be considered. The delay time leads to an additional angle error at higher speeds. With enabling the prediction, the signal delay time will be reduced (**Figure 8**).

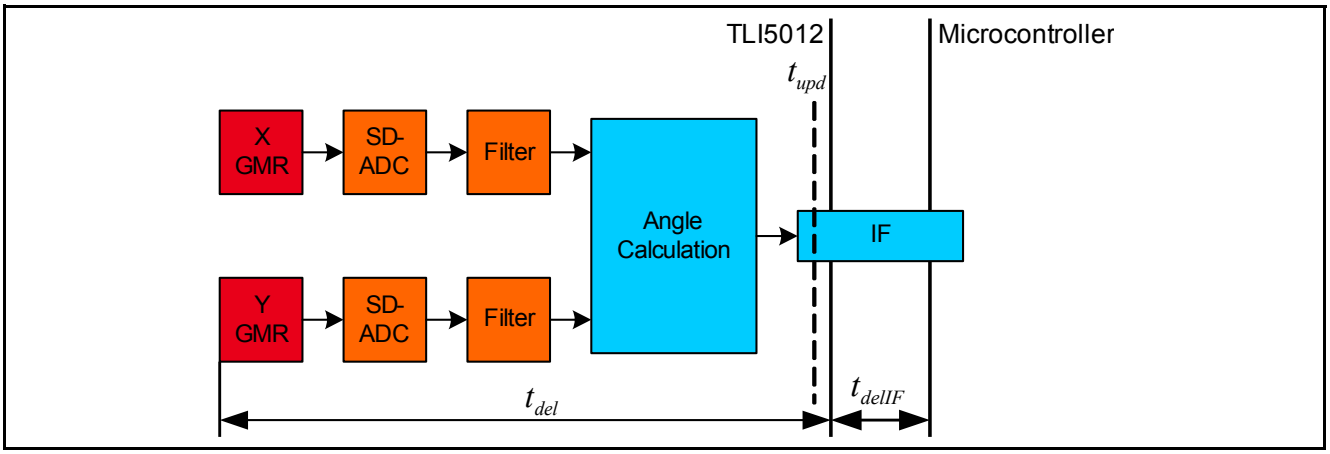


Figure 7 TLI5012 Signal path

At FIR_MD = 0 only raw values can be read out, due to the more time consuming angle calculation.

Table 7 Signal Processing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Update Rate at Interface	t_{upd}	-	21.3	-	µs	FIR_MD = 0 (only raw values)[1)2)]
		-	42.7	-		FIR_MD = 1[1)2)]
		-	85.3	-		FIR_MD = 2 (default)[1)2)]
		-	170.6	-		FIR_MD = 3[1)2)]

Table 7 Signal Processing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Angle Delay Time[3)]	t_{del}	-	60	70	µs	FIR_MD = 1[1)2)]
		-	80	95		FIR_MD = 2[1)2)]
		-	120	140		FIR_MD = 3[1)2)]
Angle Delay Time with Prediction[3)]	t_{del}	-	20	30	µs	FIR_MD = 1; PREDICT = 1 [1)2)]
		-	5	20		FIR_MD = 2; PREDICT = 1 [1)2)]
		-	-40	-20		FIR_MD = 3; PREDICT = 1 [1)2)]
Angle Noise	N_{Angle}	-	0.11	-	°	FIR_MD = 0, (1 Sigma)[2)]
		-	0.08	-		FIR_MD = 1, (1 Sigma)[2)]
		-	0.05	-		FIR_MD = 2, (1 Sigma)[2)] (default)
		-	0.04	-		FIR_MD = 3, (1 Sigma)[2)]

1) depends on internal oscillator frequency variation
2) guaranteed by laboratory characterization
3) valid at constant rotation speed

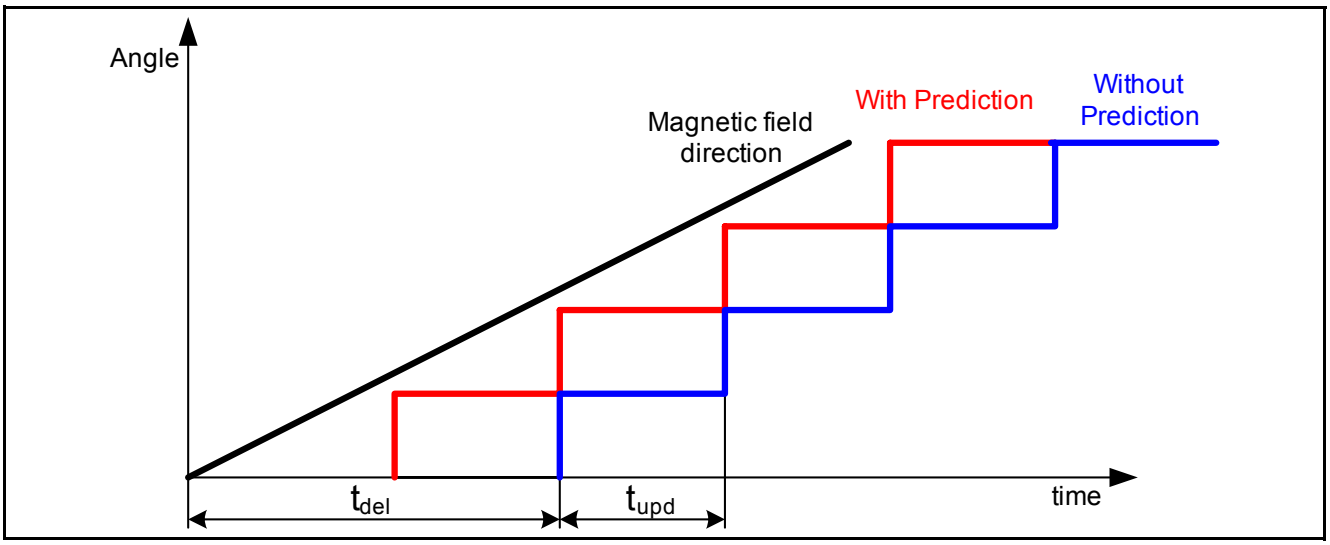


Figure 8 Delay of Sensor Output

3.5 Interfaces

3.5.1 Synchronous Serial Communication (SSC) Interface

The 3-pin SSC Interface has a bi-directional push-pull data line, serial clock signal and chip select. The SSC Interface is designed to communicate with a microcontroller pear to pear for fast applications.

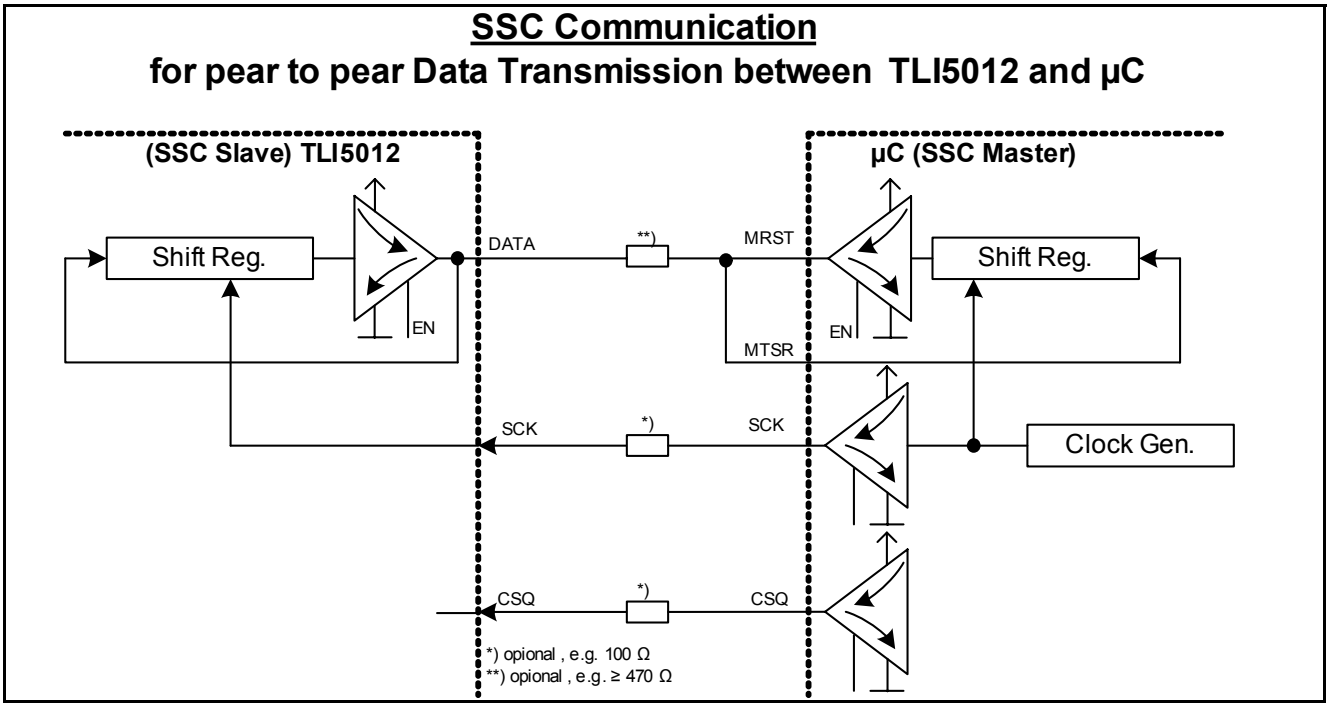


Figure 9 SSC Configuration in Sensor-Slave Mode with Push-Pull Outputs (High Speed Application)

Another possibility is a 3-pin SSC Interface with bidirectional open-drain data line, serial clock signal and chip select. This setup is designed to communicate with a microcontroller in a bus system, together with other SSC slaves (e.g. two TLI5012 for redundancy reasons). This mode can be activated using bit SSC_OD.

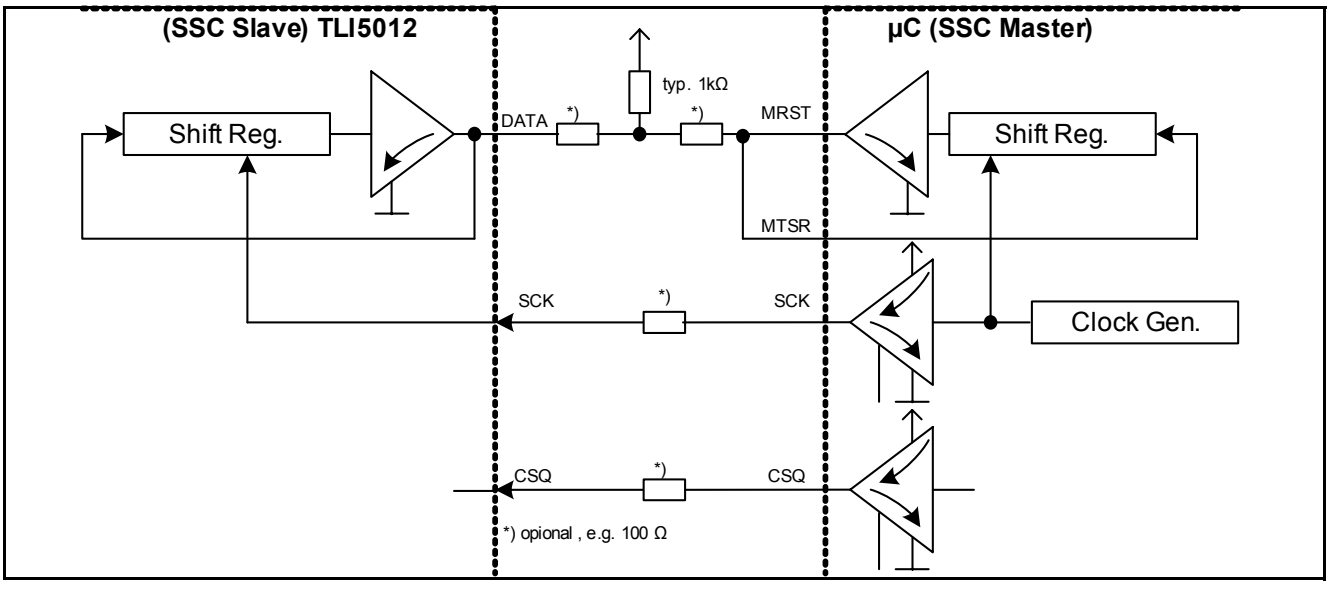


Figure 10 SSC Configuration in Sensor-Slave Mode and Open Drain (Safe Bus Systems)

3.5.1.1 SSC Timing Definition

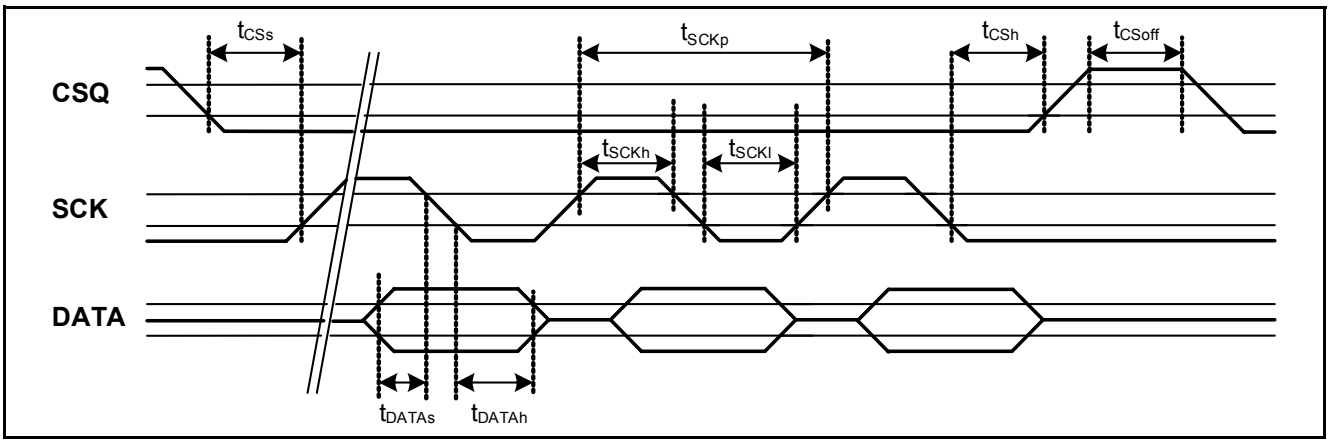


Figure 11 SSC Timing

SSC Inactive Time (CS_{off})

The SSC inactive time defines the delay time after a transfer before the TLE5012 can be selected again.

Table 8 SSC Push-Pull Timing Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC Baud Rate	f_{SSC}	-	8.0	-	Mbit/s	
CSQ Setup Time	t_{CSs}	105	-	-	ns	
CSQ Hold Time	t_{CSh}	105	-	-	ns	
CSQ off	t_{CSoff}	600	-	-	ns	SSC inactive time
SCK Period	t_{SCKp}	120	125	-	ns	
SCK High	t_{SCKh}	40	-	-	ns	
SCK Low	t_{SCKl}	30	-	-	ns	
DATA Setup Time	t_{DATAs}	25	-	-	ns	
DATA Hold Time	t_{DATAh}	40	-	-	ns	
Write Read Delay	t_{wr_delay}	130	-	-	ns	

Table 9 SSC Open Drain Timing Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC Baud Rate	f_{SSC}	-	2.0	-	Mbit/s	Pull-up Resistor = 1kΩ
CSQ Setup Time	t_{CSs}	300	-	-	ns	
CSQ Hold Time	t_{CSh}	400	-	-	ns	
CSQ off	t_{CSoff}	600	-	-	ns	SSC inactive time
SCK Period	t_{SCKp}	500	-	-	ns	
SCK High	t_{SCKh}	-	190	-	ns	

Table 9 SSC Open Drain Timing Specification (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCK Low	t_{SCKl}	-	190	-	ns	
DATA Setup Time	t_{DATAs}	25	-	-	ns	
DATA Hold Time	t_{DATAh}	40	-	-	ns	
Write Read Delay	t_{wr_delay}	130	-	-	ns	

3.5.1.2 SSC Data Transfer

The SSC data transfer is word aligned. The following transfer words are possible:

- Command word (to access and change operating modes of the TLI5012)
- Data words (any data transferred in any direction)
- Safety word (confirms the data transfer and provide status information)

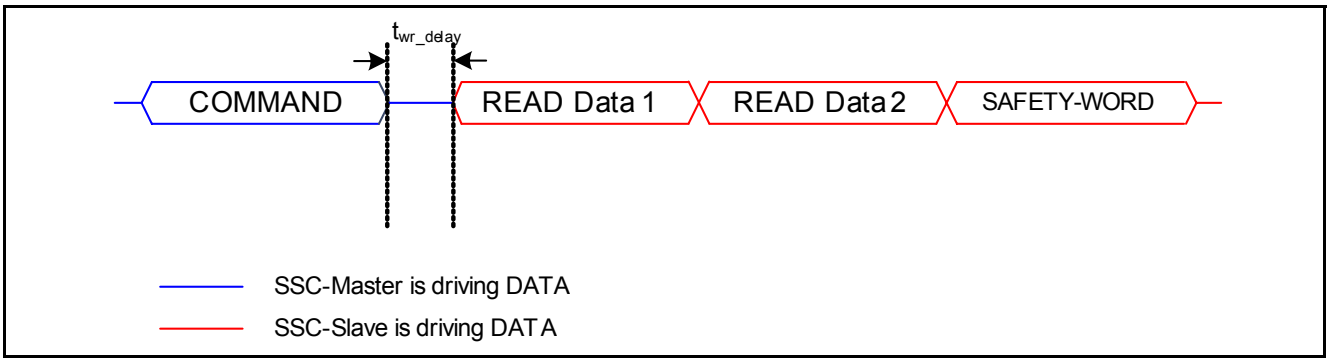


Figure 12 SSC Data Transfer (Data Read Example)

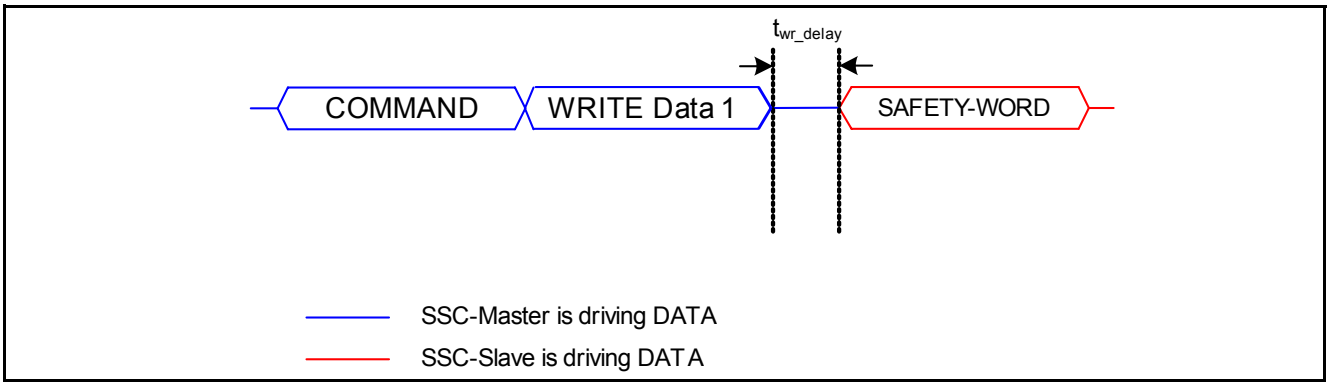


Figure 13 SSC Data Transfer (Data Write Example)

Command Word

TheTLI5012 is controlled by a command word. It is sent first at every data transmission.

Table 10 Structure of the Command Word

Name	Bits	Description
RW	[15]	Read - Write 0:Write 1:Read
Lock	[14..11]	4 bit Lock Value 0x00: Default Operating Access 0x02: Config- Access
UPD	[10]	Update-Register Access 0: Access to current values 1: Access to updated values
ADDR	[9..4]	6 bit Address
ND	[3..0]	4 bit Number of Data-Words

Safety Word

The safety word contains following bits:

Table 11 Structure of the Safety Word

Name	Bits	Description
STAT	Chip and Interface Status	
	[15]	Indication of Chip-Reset (resets after readout) via SSC 0: No reset 1: Reset occurred Reset: 0_B
	[14]	System Error (e.g. Overvoltage; Undervoltage; V_{DD}-, GND- off; ROM;...) 0: No error 1: Error occurred (S_VR; S_DSPU; S_OV; S_XYOL: S_MAGOL; S_ADCM)
	[13]	Interface Access Error (access to wrong address; wrong lock) 0: No error 1: Error occurred
	[12]	Valid Angle Value (no system error; no interface error; NO_GMR_A = ’0’; NO_GMR_XY=’0’) 0: Angle value valid 1: Angle value invalid
RESP	[11..8]	Sensor Number Response Indicator The sensor no. bit is pulled low and the other bits are high.
CRC	[7..0]	Cyclic Redundancy Check (CRC)

Data Communication via SSC

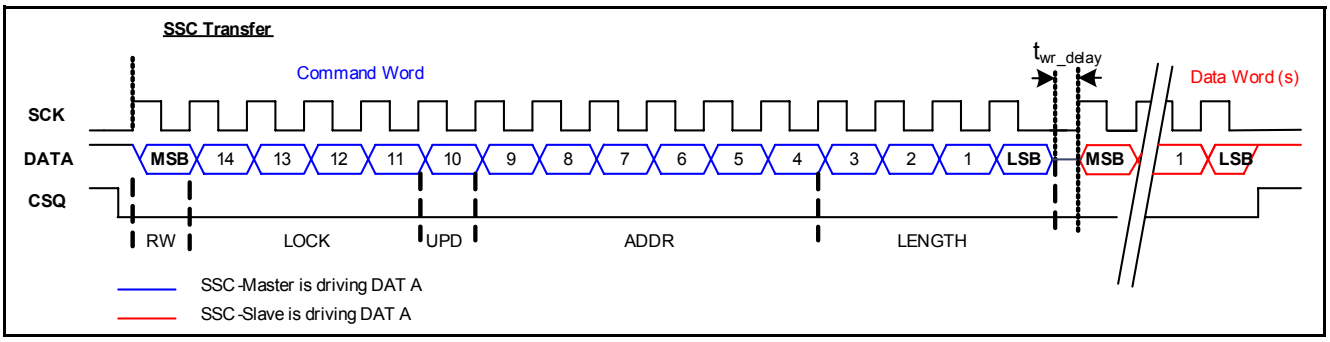


Figure 14 SSC Bit Ordering (Read Example)

The data communication via SSC interface has the following characteristic:

- The data transmission order is “Most Significant Bit (MSB) first”.
- Data is put on the data line with the rising edge on SCK and read with the falling edge on SCK.
- The SSC Interface is word-aligned. All functions are activated after each transmitted word.
- A “high” condition on the negated Chip Select pin (CSQ) of the selected TLE5012 interrupts the transfer immediately. The CRC calculator is automatically reset.
- After changing the data direction, a delay (t_{wr_delay}) has to be considered before continuing the data transfer. This is necessary for internal register access.
- Every access to the TLI5012 with the number of data (ND) ≥ 1 is performed with address auto-increment.
- At an overflow at address $3F_H$ the transfer continuous at address 00_H.
- With ND = 0 no auto-increment is done and a continuously readout of the same address can be realized. Afterwards no Safety Word is send and the transfer ends with high condition on CSQ.
- After every data transfer with ND ≥ 1 the 16 bit Safety Word will be appended by the selected TLI5012.
- At a rising edge of CSQ without data transfer before (no SCK-pulse), the update-registers are updated with according values.
- After sending the Safety Word the transfer ends. To start another data transfer, the CSQ has to be deselected once for t_{CSoff}.
- The SSC is default Push-Pull. The Push-Pull driver is only active, if the TLI5012 has to send data, otherwise the Push-Pull is disabled for receiving data from the microcontroller.

Cyclic Redundancy Check (CRC)

- This CRC is according to the J1850 Bus-Specification.
- Every new transfer resets the CRC generation.
- Every Byte of a transfer will be taken into account to generate the CRC (also the sent command(s)).
- Generator-Polynomial: X8+X4+X3+X2+1, but for the CRC generation the fast-CRC generation circuit is used (see **Figure 15**)
- The remainder of the fast CRC circuit is initial set to ’11111111_B’.
- Remainder is inverted before transmission.

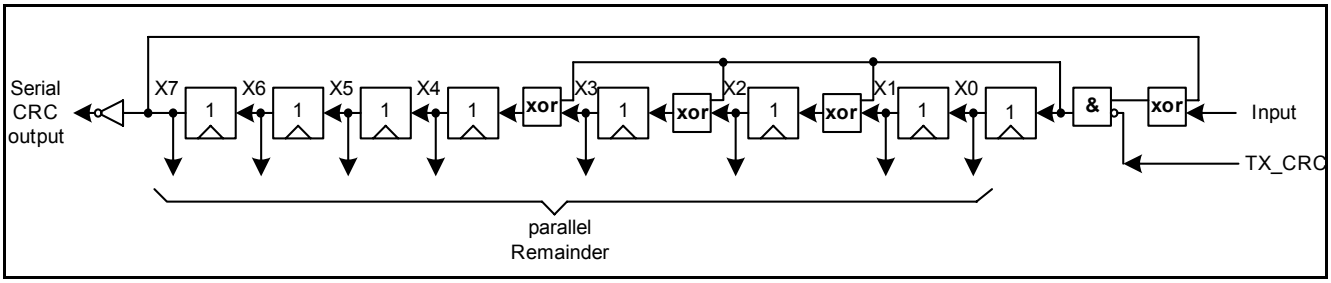


Figure 15 Fast CRC Polynomial Division Circuit

3.5.1.3 Registers Chapter

This chapter defines the registers of the TLI5012 . It also defines the read/write access rights of the specific registers. **Table 12** identifies the values with symbols. Access to the registers is accomplished via the SSC Interface.

Table 12 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Registers Chapter, TLI5012 Register			
STAT	Status Register	00_H	**26**
ACSTAT	Activation Status Register	01_H	**28**
AVAL	Angle Value Register	02_H	**29**
ASPD	Angle Speed Register	03_H	**30**
AREV	Angle Revolution Register	04_H	**30**
FSYNC	Frame Synchronization Register	05_H	**31**
MOD_1	Interface Mode1 Register	06_H	**32**
SIL	SIL Register	07_H	**33**
MOD_2	Interface Mode2 Register	08_H	**34**
MOD_3	Interface Mode3 Register	09_H	**35**
OFFX	Offset X	$0A_H$	**36**
OFFY	Offset Y	$0B_H$	**36**
SYNCH	Synchronicity	$0C_H$	**37**
IFAB	IFAB Register	$0D_H$	**37**
MOD_4	Interface Mode4 Register	$0E_H$	**38**
TCO_Y	Temperature Coeffizient Register	$0F_H$	**39**
ADC_X	X-raw value	10_H	**39**
ADC_Y	Y-raw value	11_H	**40**

The register is addressed wordwise.

3.5.1.3.1 TLI5012 Register

Status Register

STAT	Offset	Reset Value
Status Register	**00_H**	**8001_H**

15	14	13	12	11	10	9	8
RD_ST	**S_NR**		**NO_GMR_A**	**NO_GMR_XY**	**S_ROM**	**S_ADCT**	Res
r	r		r	r	r	r	

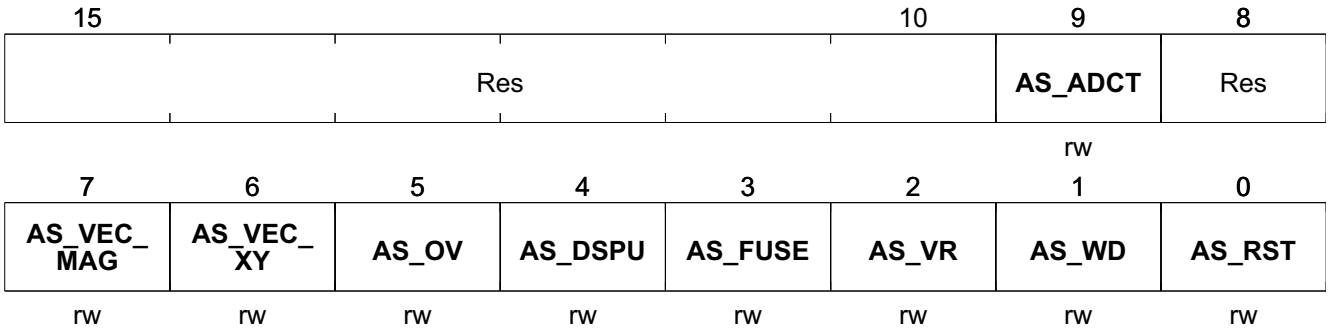
7	6	5	4	3	2	1	0
S_MAGOL	**S_XYOL**	**S_OV**	**S_DSPU**	**S_FUSE**	**S_VR**	**S_WD**	**S_RST**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RD_ST	15	r	**Read Status** 0_B after readout 1_B status values changed Reset: 1_B
S_NR	14:13	r	**Slave Number** Reset: 00_B
NO_GMR_A	12	r	**No GMR Angle Value** 0_B valid GMR angle value on the interface 1_B no valid GMR angle value on the interface Reset: 0_B
NO_GMR_XY	11	r	**No GMR XY Values** 0_B valid GMR_XY values on the interface 1_B no valid GMR_XY values on the interface Reset: 0_B
S_ROM	10	r	**Status ROM** 0_B after readout, CRC ok 1_B CRC fail or running Reset: 0_B
S_ADCT	9	r	**Status ADC-Test** 0_B after readout 1_B Test vectors out of limit Reset: 0_B
S_MAGOL	7	r	**Status Magnitude Out of Limit** 0_B after readout 1_B GMR-magnitude out of limit (>23230 digits) Reset: 0_B

Field	Bits	Type	Description
S_XYOL	6	r	**Status X,Y Data Out of Limit** 0_B after readout 1_B X,Y data out of limit (>23230 digits) Reset: 0_B
S_OV	5	r	**Status Overflow** 0_B after readout 1_B DSPU overflow occurred Reset: 0_B
S_DSPU	4	r	**Status Digital Signal Processing Unit** 0_B after readout 1_B DSPU self test not ok, or selftest is running Reset: 0_B
S_FUSE	3	r	**Status Fuse CRC** 0_B after readout, Fuse CRC ok 1_B Fuse CRC fail Reset: 0_B
S_VR	2	r	**Status Voltage Regulator** 0_B after readout 1_B V_{DD} overvoltage; V_{DD} undervoltage; V_{DD}-off; GND-off; or V_{OVG}; V_{OVA}; V_{OVD} too high Reset: 0_B
S_WD	1	r	**Status Watchdog** 0_B after chip reset 1_B watchdog counter expired Reset: 0_B
S_RST	0	r	**Status Reset** 0_B after readout 1_B indication of power-up, short power-break or active reset Reset: 1_B

Activation Status Register

ACSTAT	Offset	Reset Value
Activation Status Register	01_H	$5CEE_H$

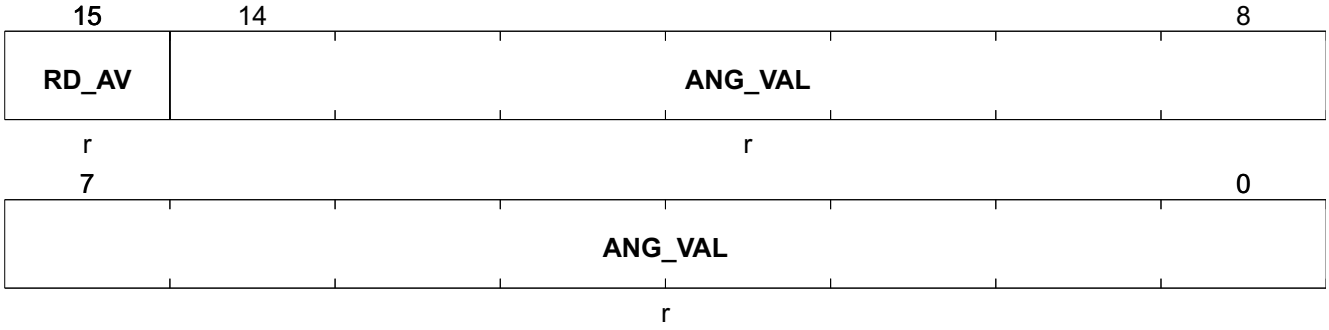


Field	Bits	Type	Description
Res	15:10		**Reserved** Reset: 010111_B
AS_ADCT	9	rw	**Enable GMR Vector check** Reset: 0_B
AS_VEC_MAG	7	rw	**Activation of ADC-Redundancy-BIST** 0_B after execution 1_B activation of redundancy BIST Reset: 1_B
AS_VEC_XY	6	rw	**Activation of ADC-BIST** 0_B after execution 1_B activation of BIST Reset: 1_B
AS_OV	5	rw	**Enable of DSPU Overflow Check** Reset: 1_B
AS_DSPU	4	rw	**Activation DSPU BIST** 0_B after execution 1_B activation of DSPU BIST Reset: 0_B
AS_FUSE	3	rw	**Activation Fuse CRC** 0_B after execution 1_B activation of Fuse CRC Reset: 1_B
AS_VR	2	rw	**Enable Voltage Regulator Check** Reset: 1_B
AS_WD	1	rw	**Enable DSPU Watchdog-HW-Reset** Reset: 1_B

Field	Bits	Type	Description
AS_RST	0	rw	**Activation of Hardware Reset** Activation occurs after CSQ switches from ’0’ to ’1’ after SSC transfer. 0_B after execution 1_B activation of HW Reset Reset: 0_B

Angle Value Register

AVAL	Offset	Reset Value
Angle Value Register	**02_H**	**8000_H**

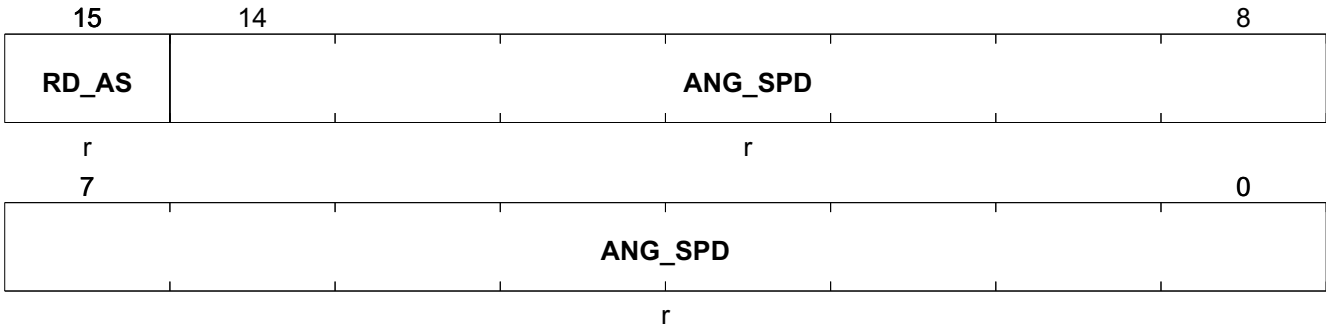


Field	Bits	Type	Description
RD_AV	15	r	**Read Status, Angle Value** 0_B after readout 1_B new angle value (ANG_VAL) present Reset: 1_B
ANG_VAL	14:0	r	**Calculated Angle Value** (ANG_RANGE = 0x080) 4000_H -180° 0000_H 0° $3FFF_H$ +179.99° Reset: 0_H

Angle Speed Register

ASPD **Offset** **Reset Value**

Angle Speed Register **03_H** **8000_H**

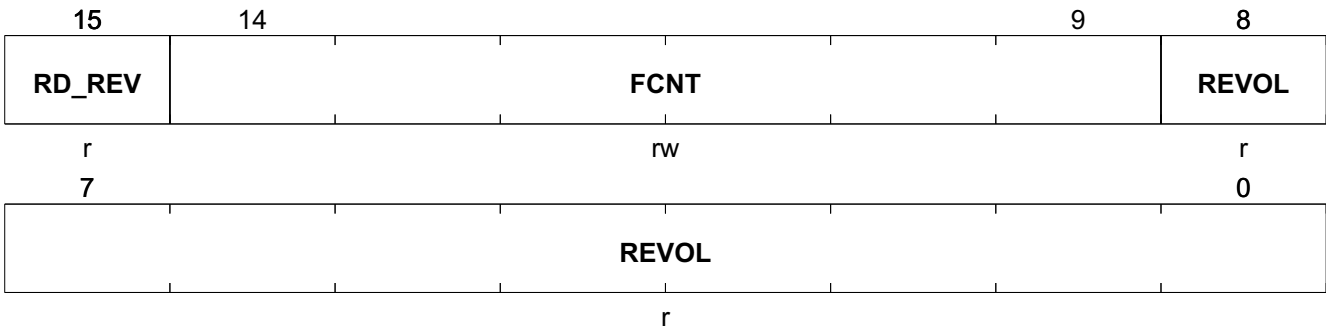


Field	Bits	Type	Description
RD_AS	15	r	**Read Status, Angle Speed** 0_B after readout 1_B new angle speed value (ANG_SPD) present Reset: 1_B
ANG_SPD	14:0	r	**Calculated Angle Speed** Difference between two consecutive angle values. Reset: 0_H

Angle Revolution Register

AREV **Offset** **Reset Value**

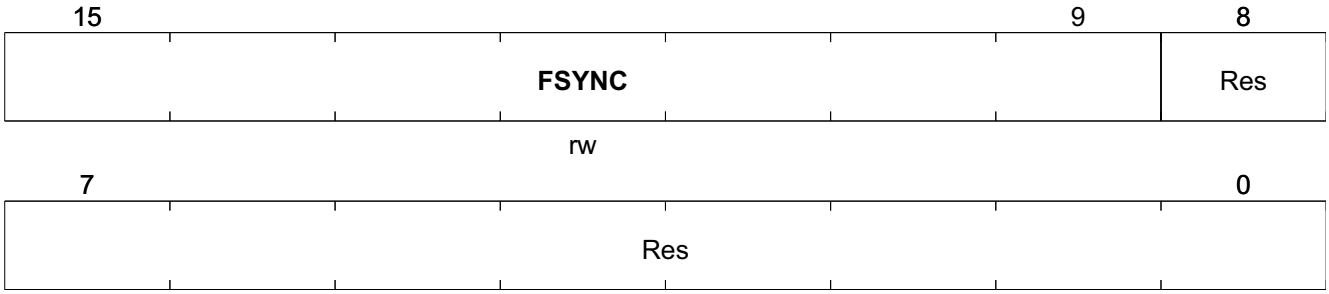
Angle Revolution Register **04_H** **8000_H**



Field	Bits	Type	Description
RD_REV	15	r	**Read Status, Revolution** 0_B after readout 1_B new value (REVOL) present Reset: 1_B
FCNT	14:9	rw	**Frame Counter (unsigned 6 bit value)** Counts every new angle value Reset: 0_H
REVOL	8:0	r	**Number of Revolutions (signed 9 bit value)** Reset: 0_H

Frame Synchronization Register

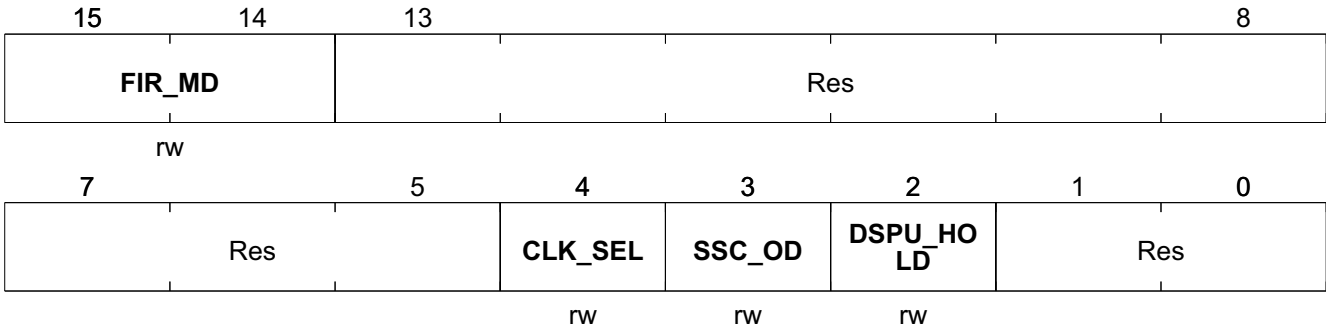
FSYNC	Offset	Reset Value
Frame Synchronization Register	**05_H**	**0000_H**



Field	Bits	Type	Description
FSYNC	15:9	rw	**Frame Synchronization Counter Value** Sub counter within one frame. Reset: 0_H

Interface Mode1 Register

MOD_1	Offset	Reset Value
Interface Mode1 Register	**06_H**	**8001_H**



Field	Bits	Type	Description
FIR_MD	15:14	rw	**Filter Decimation Setting** 00_B 21.3µs 01_B 42.7µs 10_B 85.3µs 11_B 170.6µs Reset: 10_B
CLK_SEL	4	rw	**Clock Source Select** 0_B internal oscillator 1_B external 4MHz clock Reset: 0_B
SSC_OD	3	rw	**SSC-Interface** 0_B Push-Pull 1_B Open Drain Reset: 0_B
DSPU_HOLD	2	rw	**Hold DSPU Operation** 0_B DSPU in normal schedule operation 1_B DSPU is on hold Reset: 0_B
Res	1:0		**Reserved** Reset: 01_B

SIL Register

SIL	Offset	Reset Value
SIL Register	07_H	0000_H

15	14	13	11	10	9	8
FILT_PAR	**FILT_INV**	Res		**FUSE_REL**	Res	
rw	rw			rw		

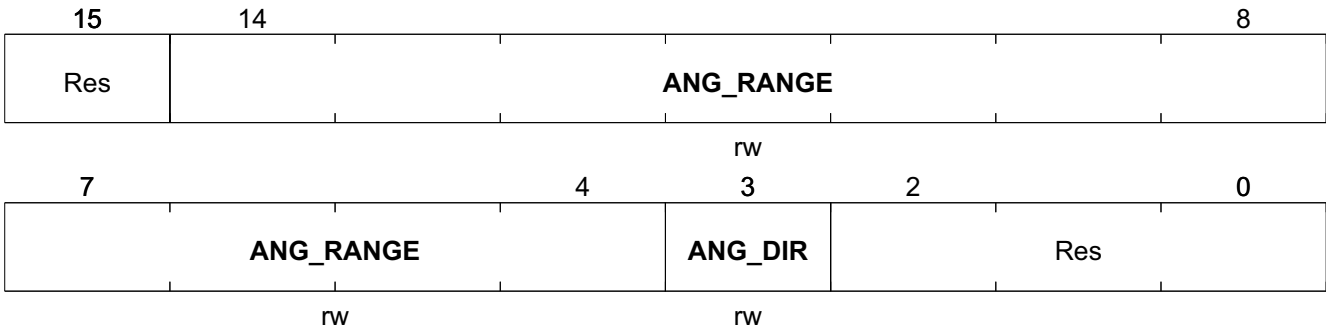
7	6	5	3	2	0
Res	**ADCTV_EN**	**ADCTV_Y**		**ADCTV_X**	
	rw	rw		rw	

Field	Bits	Type	Description
FILT_PAR	15	rw	**Filter Parallel** 0_B filter parallel disabled 1_B filter parallel enabled (source: X-value) Reset: 0_B
FILT_INV	14	rw	**Filter Inverted** 0_B filter inverted disabled 1_B filter inverted enabled Reset: 0_B
FUSE_REL	10	rw	**Fuse Reload** 0_B fuse reload disabled 1_B fuse parameters reloaded to DSPU at next cycle start Reset: 0_B
ADCTV_EN	6	rw	**ADC-Test vectors** 0_B ADC-Test vectors disabled 1_B ADC-Test vectors enabled Reset: 0_B
ADCTV_Y	5:3	rw	**Test vector Y** 000_B 0V 001_B +70% 010_B +100% 011_B +Overflow 101_B -70% 110_B -100% 111_B -Overflow Reset: 000_B

Field	Bits	Type	Description
ADCTV_X	2:0	rw	**Test vector X** 000_B 0V 001_B +70% 010_B +100% 011_B +OV 101_B -70% 110_B -100% 111_B -OV Reset: 000_B

Interface Mode2 Register

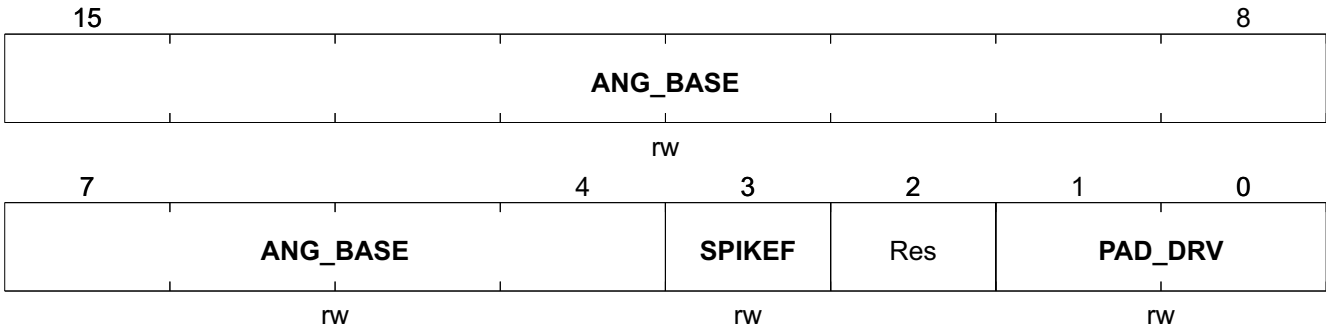
MOD_2	Offset	Reset Value
Interface Mode2 Register	**08_H**	**0800_H**



Field	Bits	Type	Description
ANG_RANGE	14:4	rw	**Angle Range** Angle Range [°] = 360° * (2^7 / ANG_RANGE) 200_H represents 90° 080_H represents 360° Reset: 080_H
ANG_DIR	3	rw	**Angle Direction** 0_B counterclockwise rotation of magnet° 1_B clockwise rotation of magnet Reset: 0_B

Interface Mode3 Register

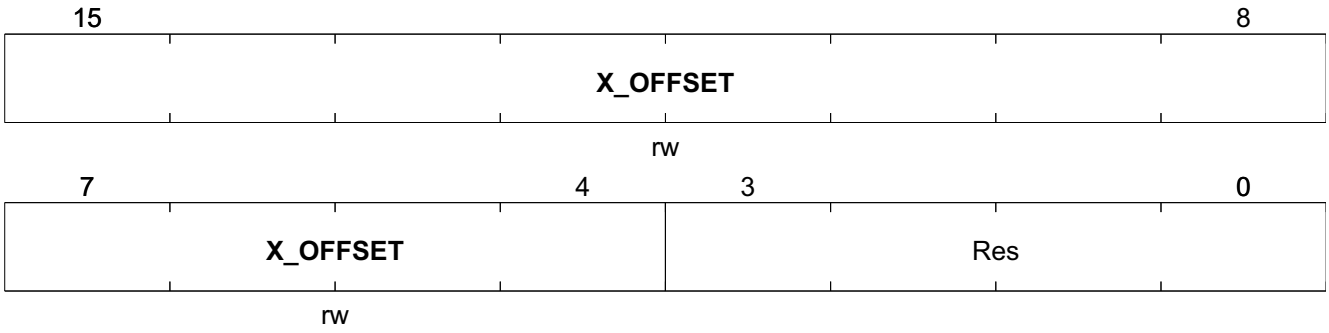
MOD_3	Offset	Reset Value
Interface Mode3 Register	09_H	0000_H



Field	Bits	Type	Description
ANG_BASE	15:4	rw	**Angle Base** 800_H -180° 000_H 0° 001_H 0.00879° $7FF_H$ +179.912° Reset: 0_H
SPIKEF	3	rw	**Analog Spike Filters of Input Pads** 0_B spike filter disabled 1_B spike filter enabled Reset: 0_B
PAD_DRV	1:0	rw	**Configuration of Pad-Driver** 00_B IFA/IFB: strong driver, DATA: strong driver, fast edge 01_B IFA/IFB: strong driver, DATA: strong driver, slow edge 10_B IFA/IFB: weak driver, DATA: medium driver, fast edge 11_B IFA/IFB: weak driver, DATA: weak driver, slow edge Reset: 00_B

Offset X Register

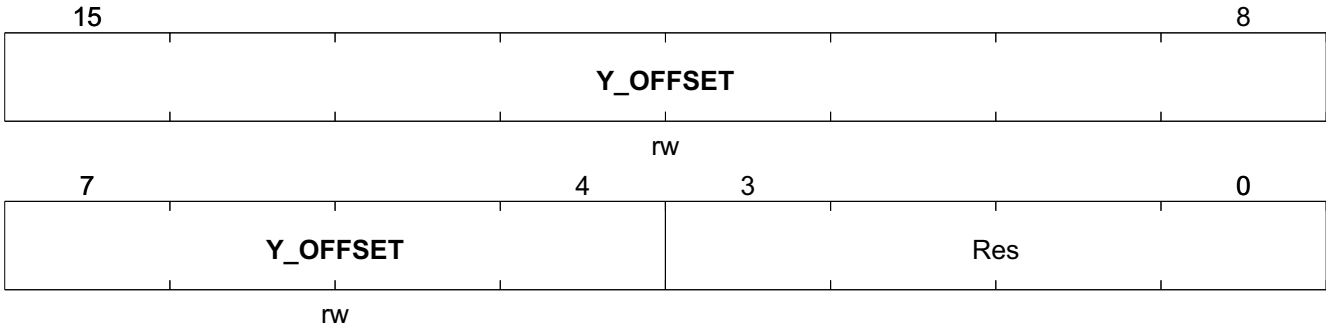
OFFX	Offset	Reset Value
Offset X	$0A_H$	0000_H



Field	Bits	Type	Description
X_OFFSET	15:4	rw	**Offset Correction of X-value** Reset: 0_H

Offset Y Register

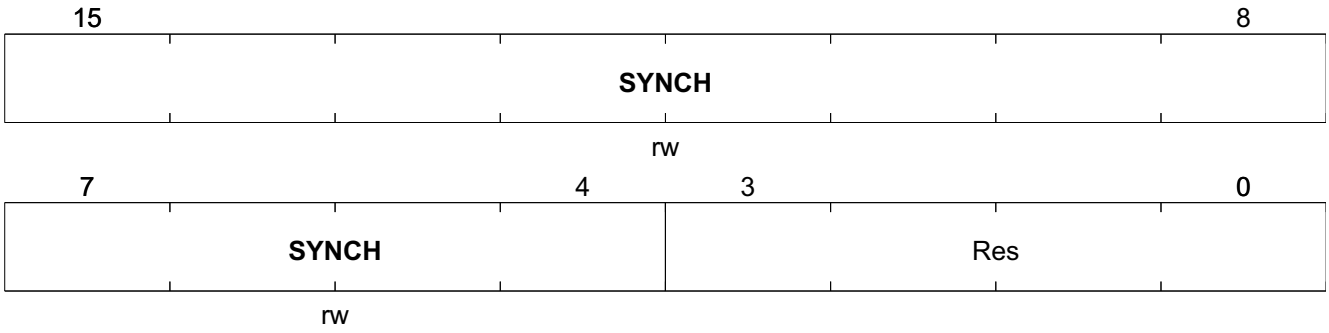
OFFY	Offset	Reset Value
Offset Y	$0B_H$	0000_H



Field	Bits	Type	Description
Y_OFFSET	15:4	rw	**Offset Correction of Y-value** Reset: 0_H

Synchronicity Register

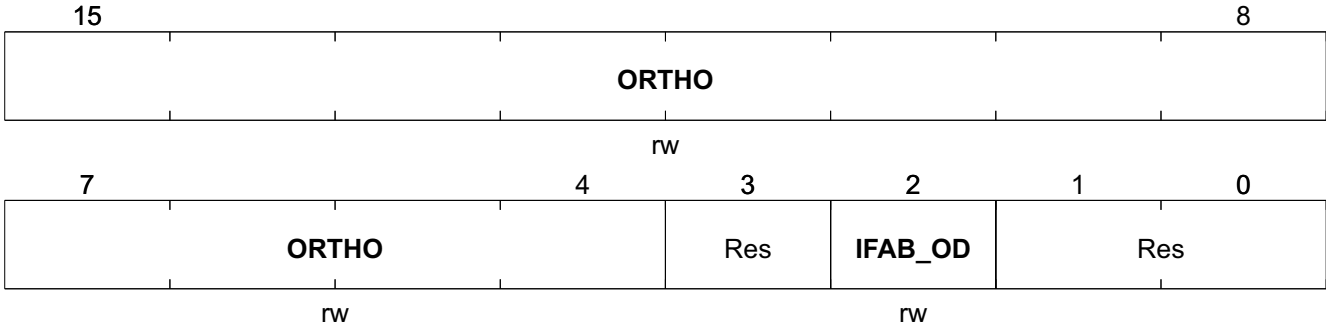
SYNCH	Offset	Reset Value
Synchronicity	$0C_H$	0000_H



Field	Bits	Type	Description
SYNCH	15:4	rw	**Amplitude Synchronicity** $+2047_D$ 112.494% 0_D 100% -2047_D 87.500% Reset: 0_H

IFAB Register

IFAB	Offset	Reset Value
IFAB Register	$0D_H$	0004_H

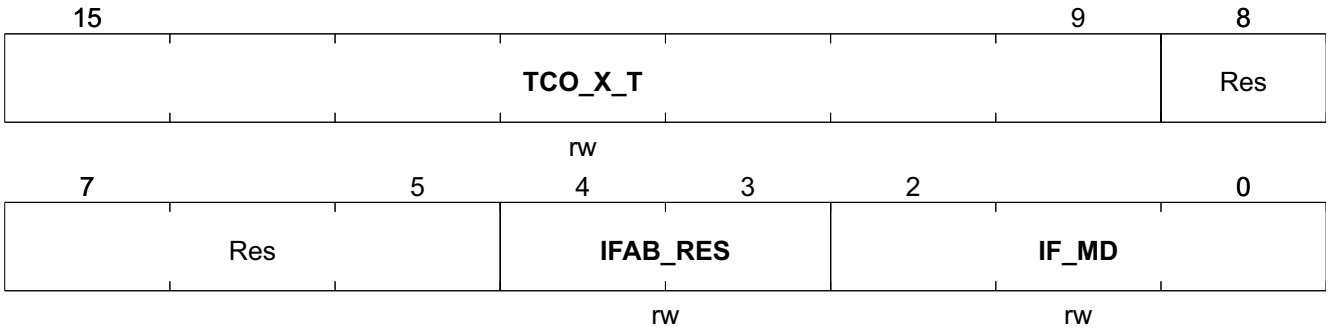


Field	Bits	Type	Description
ORTHO	15:4	rw	**Orthogonality Correction of X and Y Components** $+2047_D$ 11.2445° 0_D 0° -2047_D -11.2500° Reset: 0_H

Field	Bits	Type	Description
IFAB_OD	2	rw	**IFA & IFB Open Drain** 0_B Push-Pull 1_B Open Drain Reset: 1_B

Interface Mode4 Register

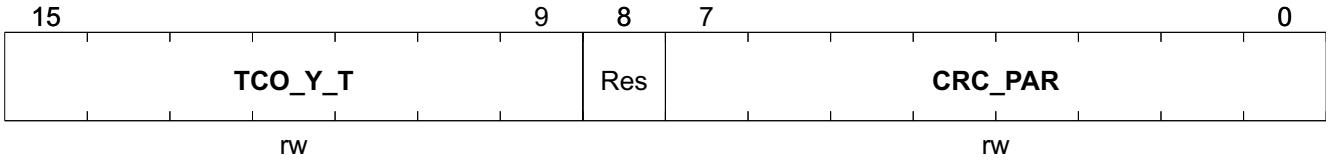
MOD_4	Offset	Reset Value
Interface Mode4 Register	**$0E_H$**	**0011_H**



Field	Bits	Type	Description
TCO_X_T	15:9	rw	**Offset Temperature Coefficient for X-Component** Reset: 0_H
IFAB_RES	4:3	rw	**IFAB Resolution** 00_B 12bit = 0.088° (244Hz) 01_B 11bit = 0.176° (488Hz) 10_B 10bit = 0.352° (977Hz) 11_B 9bit = 0.703° (1953Hz) Reset: 10_B
IF_MD	2:0	rw	**Interface Mode** PWM if CLK is connected to GND at startup. *Note: Not mentioned combinations are not allowed* 001_B SSC mode; PWM Reset: 001_B

Temperature Coeffizient Register

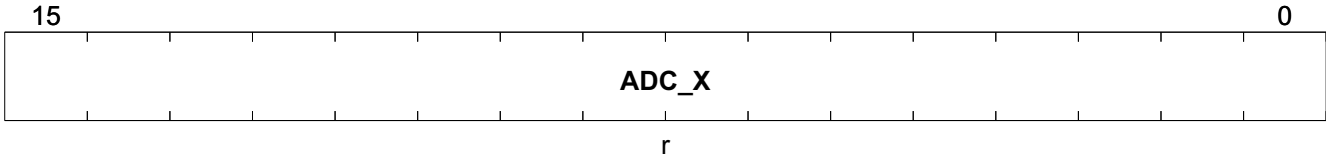
TCO_Y	Offset	Reset Value
Temperature Coeffizient Register	$0F_H$	0000_H



Field	Bits	Type	Description
TCO_Y_T	15:9	rw	**Offset Temperature Coefficient for Y-Component** Reset: 0_H
CRC_PAR	7:0	rw	**CRC of Parameters** CRC of parameters from address 08_H to $0F_H$ Reset: 0_H

X-raw Value Register

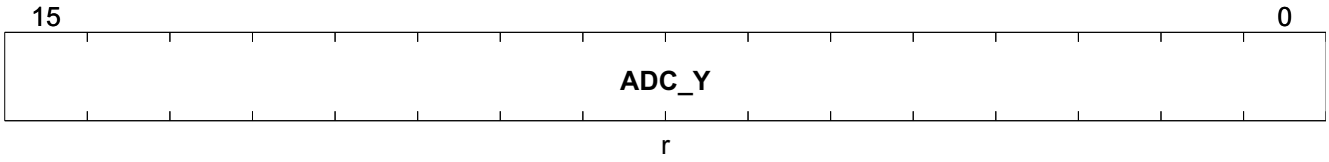
ADC_X	Offset	Reset Value
X-raw value	10_H	0000_H



Field	Bits	Type	Description
ADC_X	15:0	r	**ADC value of X-GMR** Read out of this register will update ADC_Y Reset: 0_H

Y-raw Value Register

ADC_Y	Offset	Reset Value
Y-raw value	11_H	0000_H



Field	Bits	Type	Description
ADC_Y	15:0	r	**ADC value of Y-GMR** Updated when ADC_X or ADC_y is read. Reset: 0_H

3.5.2 Pulse Width Modulation Interface

The **P**ulse **W**idth **M**odulation (**PWM**) update rate can be programmed within the register $0E_H$ (IFAB_RES) in following steps:

- 0.25 kHz with 12 bit resolution
- 0.5 kHz with 11 bit resolution
- 1.0 kHz with 10 bit resolution (default)
- 2.0 kHz with 9 bit resolution

PWM uses a square wave with constant frequency whose duty cycle is modulated resulting in an average value of the waveform.

Figure 16 shows the principle behavior of a PWM with different duty cycles and the definition of timing values. The duty cycle of a PWM is defined by following general formulas:

$$Duty\ Cycle = \frac{t_{on}}{t_{PWM}}$$

$$t_{PWM} = t_{on} + t_{off}$$

$$f_{PWM} = \frac{1}{t_{PWM}} \quad (3)$$

The range between 0 - 6.25% and 93.75 - 100% is used only for diagnostic purposes. More details are given in **Table 13**.

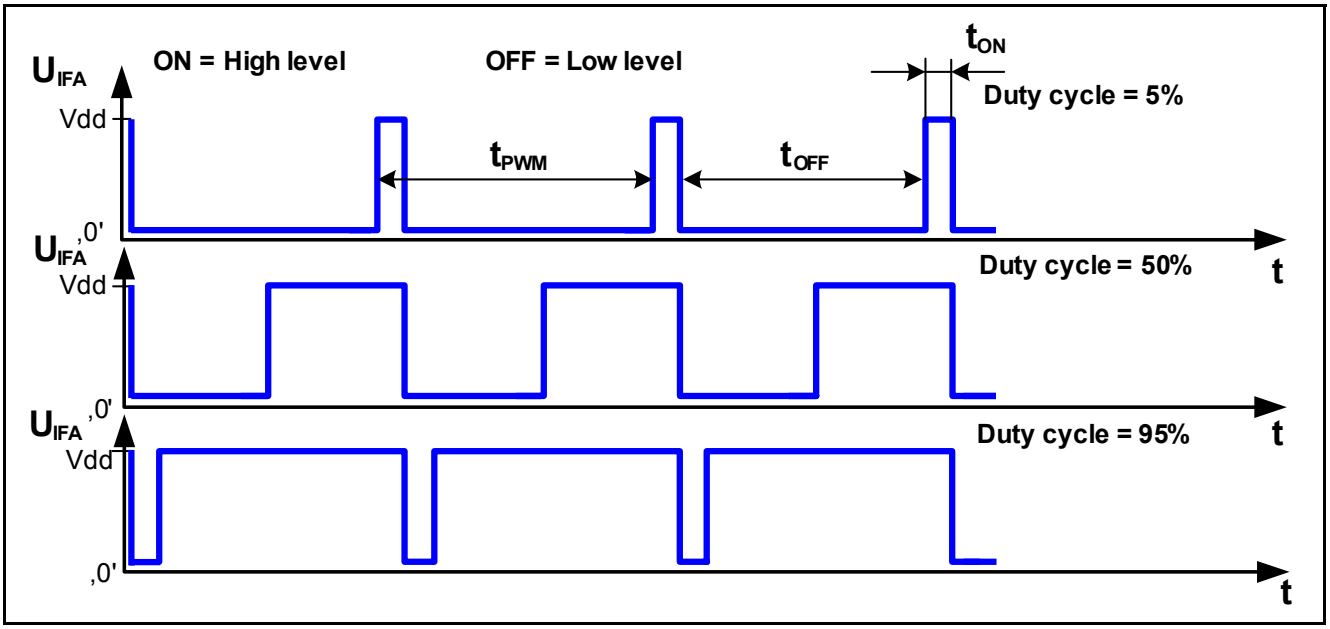


Figure 16 Typical Example for a PWM Signal

Table 13 PWM Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PWM Output Frequency	f_{PWM}	244	-	1953	Hz	selectable by IFAB_RES[1)]
Output Duty Cycle Range	DY_{PWM}	6.25	-	93.75	%	Absolute Angle
		-	2	-	%	Electrical Error (S_RST; S_VR)
		-	98	-	%	System Error (S_FUSE; S_OV; S_XYOL; S_MAGOL; S_ADCT)
		0	-	1	%	Short to GND
		99	-	100	%	Short to V_{DD}, Power-Loss
PWM Period Variation	t_{PWMvar}	-5	-	5	%	2)

1) $f_{PWM} = (f_{DIG} * 2^{IFAB_RES}) / (24 * 4096)$

2) depends on internal oscillator frequency variation

4 Package Information

4.1 Package Parameters

Table 14 Package Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal Resistance	R_{thJA}	-	150	200	K/W	Junction to Air[1)]
	R_{thJC}	-	-	75	K/W	Junction to Case
	R_{thJL}	-	-	85	K/W	Junction to Lead
Soldering Moisture Level	MSL 3					260°C
Lead Frame	Cu					
Plating	Sn 100%					> 7 µm

1) according to Jedec JESD51-7

4.2 Package Outline

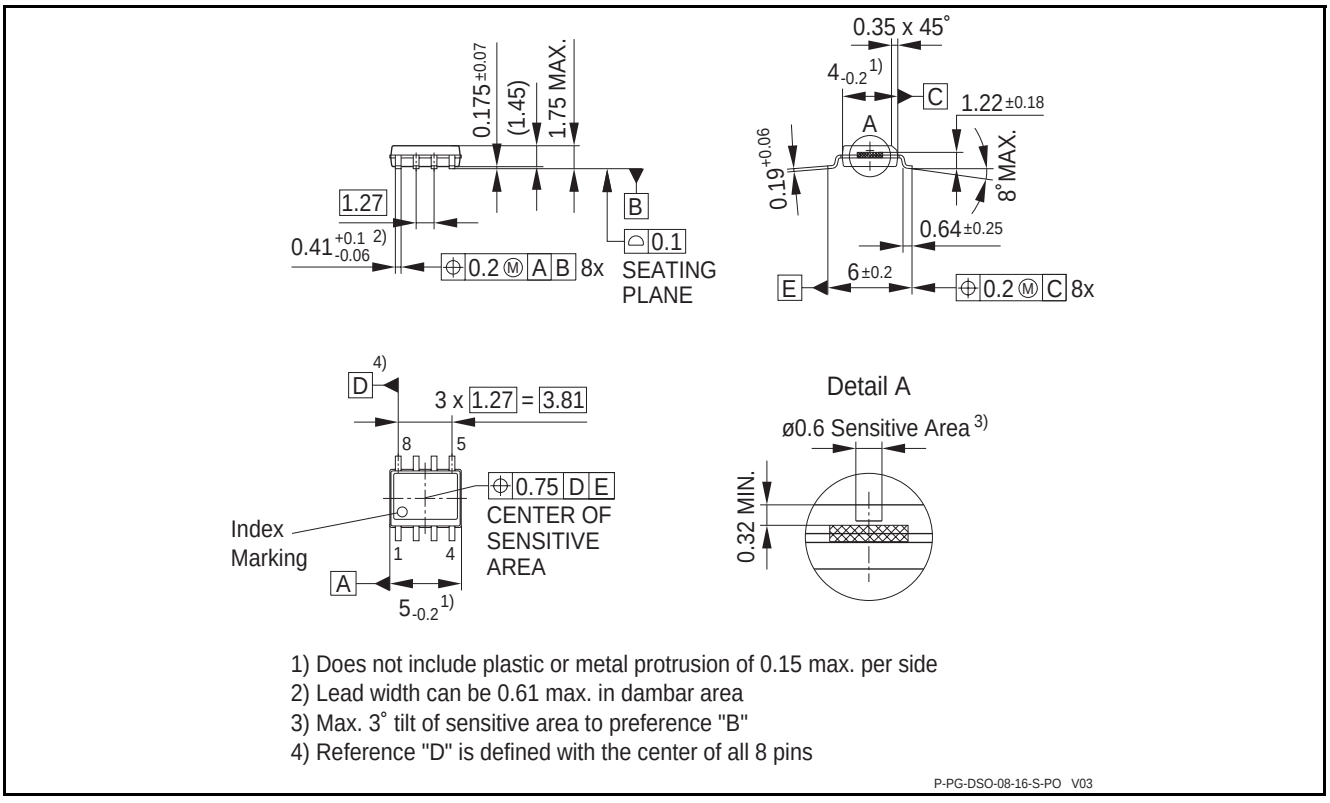


Figure 17 PG-DSO-8 Package Dimension

4.3 Footprint

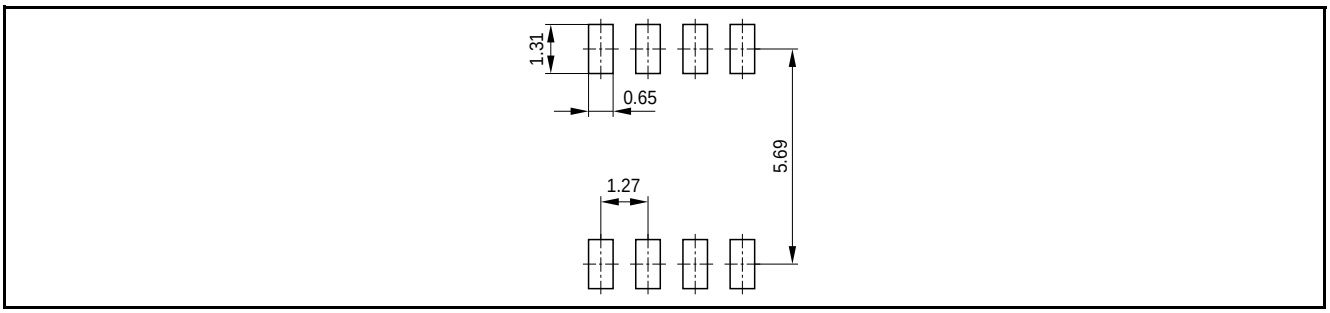


Figure 18 Footprint PG-DSO-8

4.4 Packing

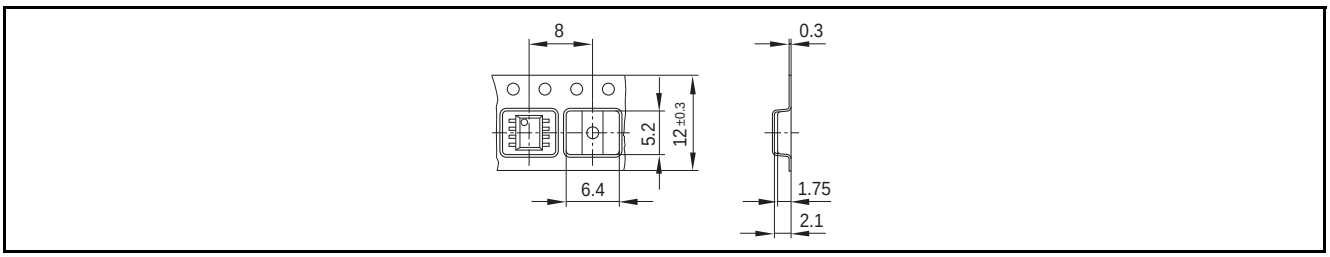


Figure 19 Tape and Reel

4.5 Marking

Position	Marking	Description
1st Line	I5012xx	See ordering table on page 7
2nd Line	xxx	Lot code
3rd Line	Gxxxx	G..green, 4-digit..date code

Processing

Note: For processing recommendations, please refer to Infineon's Notes on processing

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