bq24250C 2A Single Input I²C, Standalone Switch-Mode Li-Ion Battery Charger with Power-Path Management

1 Features

- High-efficiency Switch-mode Charger with Separate Power Path
- Start up System from Deeply Discharged or Missing Battery
- USB Charging Compliant
  - Selectable Input Current Limit of 100 mA, 500 mA, 900 mA, 1.5 A, and 2 A
- In Host Mode (After I²C Communication Starts and Before Watchdog Timer Times Out)
  - Programmable Battery Charge Voltage, V_{BATREG}
  - Programmable Charge Current (I_{CHG})
  - Programmable Input Current Limit (I_{LIM})
  - Programmable Input Voltage Based Dynamic Power Management threshold, (V_{IN_DPM})
  - Programmable Input Overvoltage Protection Threshold (V_{OVP})
  - Programmable Safety Timer
- Resistor Programmable Defaults for:
  - I_{CHG} up to 2 A with Current Monitoring Output (ISET)
  - I_{LIM} up to 2 A with Current Monitoring Output (ILIM)
  - V_{IN_DPM} (VDPM)
- Watchdog Timer Disable Bit
- Integrated 4.9 V, 50 mA LDO
- Complete System Level Protection
  - Input UVLO, Input Over-voltage Protection (OVP), Battery OVP, Sleep Mode, VIN_DPM
  - Input Current Limit
  - Charge Current Limit
  - Thermal Regulation
  - Thermal Shutdown
  - Voltage Based NTC Monitoring Input
  - Safety Timer
- 20 V Maximum Input Voltage Rating
- 10.5 V Maximum Operating Input Voltage
- Low $R_{DS(on)}$ Integrated Power FETs for up to 2 A Charging Rate
- Open Drain Status Outputs
- Synchronous Fixed-frequency PWM Controller Operating at 3MHz for Small Inductor Support
- *AnyBoot* Robust Battery Detection Algorithm
- Charge Time Optimizer for improved charge times at any given charge current
- 2.4 x 2.0 mm 30-ball WCSP Packages

2 Applications

- Smart Phones
- MP3 Players
- Portable Media Players
- Handheld Devices

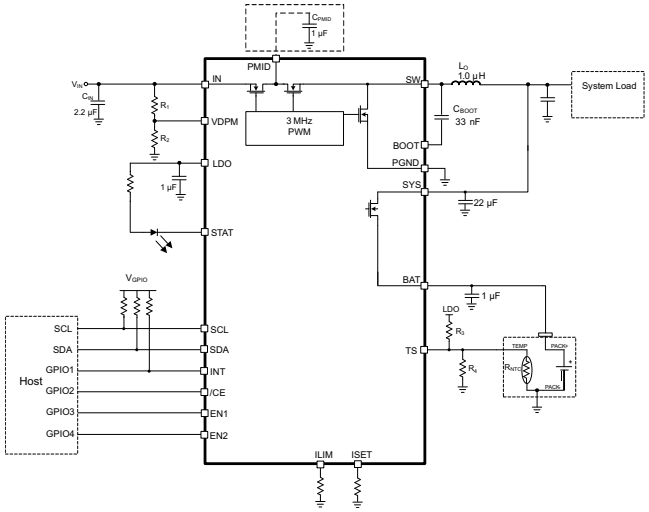
3 Description

The bq24250C is a highly integrated single-cell Li-Ion battery charger and system power-path management device targeted for space-limited, portable applications with high capacity batteries. The single cell charger has a single input that operates from either a USB port or AC wall adapter for a versatile solution.

Device Information

PART NUMBER	PACKAGE	BODY SIZE
bq24250C	DSBGA (30)	2.427 mm × 2.027 mm

Typical Application



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4 Revision History

DATE	REVISION	NOTES
July 2014	*	Initial Release

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5 Description (Continued)

The power path management feature allows the bq24250C to power the system from a high efficiency DC/DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This allows for proper charge termination and enables the system to run with a defective or absent battery pack. Additionally, this enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This enables the use of a smaller adapter.

The battery is charged in four phases: trickle charge, pre-charge, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. Additionally, a voltage-based battery pack thermistor monitoring input (TS) is included that monitors battery temperature for safe charging.

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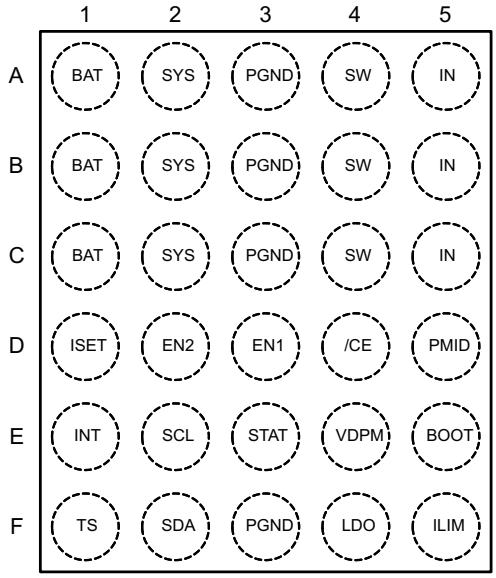
6 Pin Configuration and Functions

YFF Package
(30-Ball 2.4 mm × 2 mm DSBGA)
Top View



bq24250C

Pin Descriptions

PIN NAME	bq24250C YFF	bq24250C RGE	I/O	DESCRIPTION
AGND	–	4		Analog Ground for QFN only. Connect to the thermal pad and the ground plane of the circuit.
BAT	A1, B1, C1	11–12	I/O	Battery Connection. Connect to the positive pin of the battery. Additionally, bypass BAT with a >1µF capacitor.
BOOT	E5	21	I	High Side MOSFET Gate Driver Supply. Connect a 0.033µF ceramic capacitor (voltage rating > 15V) from BOOT to SW to supply the gate drive for the high side MOSFETs.
$\overline{CE}$	D4	1	I	Charge Enable Active-Low Input. Connect CE to a high logic level to place the battery charger in standby mode.
$\overline{CHG}$	–	–	O	Charge Status Open Drain Output. $\overline{CHG}$ is pulled low when a charge cycle starts and remains low while charging. $\overline{CHG}$ is high impedance when the charging terminates and when no supply exists. $\overline{CHG}$ does not indicate recharge cycles.
EN1	D3	2	I	Input Current Limit Configuration Inputs. Use EN1, and EN2 to control the maximum input current and enable USB compliance. See Table 1 for programming details.
EN2	D2	3	I	
ILIM	F5	22	I	Input Current Limit Programming Input. Connect a resistor from ILIM to GND to program the input current limit for IN. The current limit is programmable from 0.5A to 2A. ILIM has no effect on the USB input. If an external resistor is not desired, short to GND for a 2A default setting.
IN	A5,B5,C5	19	I	Input power supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to PGND with >2µF ceramic capacitor
INT	E1	8	O	Status Output. INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 256µs pulse is sent out as an interrupt for the host. INT will indicate recharge cycles. Connect INT to a logic rail through a 10kΩ resistor to communicate with the host processor.

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Pin Descriptions (continued)

PIN NAME	bq24250C YFF	bq24250C RGE	I/O	DESCRIPTION
ISET	D1	10	I	Charge Current Programming Input. Connect a resistor from ISET to GND to program the fast charge current. The charge current is programmable from 300mA to 2A.
LDO	F4	24	O	LDO output. LDO is regulated to 4.9V and drives up to 50mA. Bypass LDO with a 1µF ceramic Capacitor. LDO is enabled when $V_{UVLO} < V_{IN} < 18V$.
PGND	A3, B3, C3, F3	15–16		Ground pin. Connect to the ground plane of the circuit.
PMID	D5	20	I	Connection between blocking FET and high-side FET.
SCL	E2	6	I	I^2C Interface Clock. Connect SCL to the logic rail through a 10kΩ resistor.
SDA	F2	5	I/O	I^2C Interface Data. Connect SDA to the logic rail through a 10kΩ resistor.
STAT	E3	7	O	Status Output. STAT is an open-drain output that signals charging status and fault interrupts. STAT pulls low during charging. STAT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 256µs pulse is sent out as an interrupt for the host. STAT is enabled/disabled using the EN_STAT bit in the control register. STAT will indicate recharge cycles. Connect STAT to a logic rail using an LED for visual indication or through a 10kΩ resistor to communicate with the host processor.
SW	A4, B4, C4	17–18	O	Inductor Connection. Connect to the switching side of the external inductor.
SYS	A2, B2, C2	13–14	I	System Voltage Sense and SMPS output filter connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with >20µF.
TS	F1	9	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from LDO to GND. The NTC is connected from TS to GND. See the *NTC Monitor* section for more details on operation and selecting the resistor values.
VDPM	E4	23	I	Input DPM Programming Input. Connect a resistor divider between IN and GND with VDPM connected to the center tap to program the Input Voltage based Dynamic Power Management threshold (V_{IN_DPM}). The input current is reduced to maintain the supply voltage at V_{IN_DPM}. The reference for the regulator is 1.2V. Short pin to GND if external resistors are not desired—this sets a default of 4.68V for the input DPM threshold (EN1=1,EN2=0).

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin Voltage (with respect to GND)	IN	–0.3	20	V
	SW	–0.7	12	V
	BOOT	–0.3	20	V
	LDO,STAT, INT, $\overline{CHG}$, EN1, EN2, $\overline{CE}$, ILIM, ISET, VDPM, TS	–0.3	7	V
	SYS, BAT	–0.3	5	V
BOOT relative to SW		–0.3	7	V
Output Current (Continuous)	IN		2	A
	SYS, BAT		4	
Output Sink Current	STAT, $\overline{CHG}$		5	mA
Operating free-air temperature		–40	85	°C
Junction temperature, T_J		–40	125	°C
Input Power	IN		15	W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{STG}		Storage temperature range	–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)(1)	0	2000	V

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

7.3 Recommended Operating Conditions

All voltages are with respect to PGND if not specified. Currents are positive into, negative out of the specified pin. Consult Packaging Section of the data book for thermal limitations and considerations of packages

		MIN	MAX	UNIT
V_{IN}	IN voltage range	4.35	18(1)	V
	IN operating voltage range	4.35	10.5	
I_{IN}	Input current		2	A
I_{CHG}	Current in charge mode, BAT		2	A
I_{DISCHG}	Current in discharge mode, BAT		4	A
R_{ISET}	Charge current programming resistor range	75		Ω
R_{ILIM}	Input current limit programming resistor range	105		Ω
P_{IN}	Input Power		12	W
T_J	Operating junction temperature range	0	125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. Small routing loops for the power nets in layout minimize switching noise.

7.4 Thermal Information

THERMAL METRIC(1)		bq24250C		UNIT
		YFF	RGE	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.5	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	32.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	44	10.6	
ψ_{JT}	Junction-to-top characterization parameter	1.6	0.3	
ψ_{JB}	Junction-to-board characterization parameter	43.4	10.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = 0ºC-125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{IN}	Supply current from IN	$V_{DPM} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$ PWM switching, CE Enable		13		mA
		$V_{DPM} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$ PWM switching, CE Disable			5	mA
		0°C< T_J < 85°C, High-Z Mode		170	225	µA
I_{BAT}	Battery discharge current in high impedance mode, (BAT, SW, SYS)	0°C< T_J < 85°C, VBAT = 4.2 V, VIN = 0V or 5V, High-Z Mode		16	22	µA
	Battery discharge current in SYSOFF mode, (BAT, SW, SYS)	0°C< T_J < 85°C, VBAT = 4.2 V, VIN < UVLO, SYSOFF Mode			1	µA

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Electrical Characteristics (continued)

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = 0ºC-125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-PATH MANAGEMENT						
V_{SYSREG}	System Regulation Voltage	MINSYS stage (no DPM or DPPM)	–1%	3.52	1%	V
		MINSYS stage (DPM or DPPM active)	–1.50%	V_{MINSYS} –200mV	1.50%	
		BATREG stage		V_{BAT} + I_{CHG} R_{on}		
		SYSREG stage	V_{BATREG} +2.1%	V_{BATREG} +3.1%	V_{BATREG} +4.1%	
V_{SPLM}	Enter supplement mode voltage threshold	V_{BAT} = 3.6V		V_{BAT} – 40mV		V
I_{SPLM}	Exit supplement mode current threshold	V_{BAT} = 3.6V		20		mA
BATTERY CHARGER						
$R_{ON(BAT-SYS)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to SYS, V_{BAT} = 4.2V (WCSP)		20	30	mΩ
V_{BATREG}	I^2C host mode	Operating in voltage regulation, Programmable Range	3.5		4.44	V
	SA mode or I^2C default mode			4.2		
	Voltage Regulation Accuracy	T_J = 25°C	–0.5%		0.5%	
		T_J = 0°C to 125°C	–0.75%		0.75%	
I_{CHG}	Fast Charge Current Range	$V_{LOWV} \le V_{BAT} < V_{BAT(REG)}$	500		2000	mA
	Fast Charge Current Accuracy	I^2C mode	–7%		7%	
$I_{CHG-LOW}$	Low Charge Current Setting	Set via I^2C	297	330	363	mA
K_{ISET}	Programmable Fast Charge Current Factor	$I_{CHG} = \frac{K_{ISET}}{R_{ISET}}$	232.5	250	267.5	AΩ
V_{ISET}	Maximum ISET pin voltage (in regulation)		0.39	0.42	0.45	V
$R_{ISET-SHORT}$	Short circuit resistance threshold		40	55	75	Ω
V_{LOWV}	Pre-charge to fast charge threshold	Rising	2.9	3	3.1	V
	Hysteresis for V_{LOWV}	Battery voltage falling		100		mV
I_{PRECHG}	Pr-charge current ($V_{BATUVLO} < V_{BAT} < V_{LOWV}$)	Ipre-chg is a precentile of the external fast charge settings.	8%	10	12%	
V_{BAT_UVLO}	Battery Under voltage lockout threshold	V_{BAT} rising	2.39	2.52	2.65	V
	Battery UVLO hysteresis			200		mV
$V_{BATSHRT}$	Trickle charge to pre-charge threshold		1.9	2	2.1	V
	Hysteresis for VBATSHRT	Battery voltage falling		100		mV
$I_{BATSHRT}$	Trickle charge mode charge current ($V_{BAT} < V_{BATSHRT}$)		25	35	50	mA
I_{TERM}	Termination Current Threshold	Termination current on SA only		10		%ICHG
	Termination Current Threshold Tolerance		–10%		10%	
V_{RCH}	Recharge threshold voltage	Below V_{BATREG}	70	115	160	mV

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Electrical Characteristics (continued)

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = 0ºC-125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY DETECTION						
V_{BATREG_HI}	Battery Detection High Regulation Voltage	Same as V_{BATREG}		V_{BATREG}		V
V_{BATREG_LO}	Battery Detection Low Regulation Voltage	360 mV offset from V_{BATREG}		V_{BATREG} –480mV		V
$V_{BATDET\ Hi}$	Battery detection comparator	V_{BATREG} = VBATREG_HI		V_{BATREG} –120mV		V
$V_{BATDET\ LO}$	Battery detection comparator	$V_{BATREG} = V_{BATREG_LO}$		V_{BATREG} +120mV		V
I_{DETECT}	Battery Detection Current Sink	Always on during battery detection		7.5		mA
Tsafe	Safety Timer Accuracy		–10%		+10%	
INPUT PROTECTION						
I_{IN}	Input current limiting	I_{IN_LIMIT} = 100 mA	90	95	100	mA
		I_{IN_LIMIT} = 150 mA	135	142.5	150	
		I_{IN_LIMIT} = 500 mA	450	475	500	
		I_{IN_LIMIT} = 900 mA	810	860	910	
		I_{IN_LIMIT} = 1500 mA	1400	1475	1550	
		I_{IN_LIMIT} = 2000 mA	1850	1950	2050	
		I_{IN_LIMIT} = External		$I_{LIM} = \frac{K_{ILIM}}{R_{ILIM}}$		
I_{LIM}	Maximum input current limit programmable range for IN input		500		2000	mA
K_{ILIM}	Maximum input current factor for IN input	I_{LIM} = 500 mA to 2.0 A	240	270	300	AΩ
V_{ILIM}	Maximum ILIM pin voltage (in regulation)			0.42		V
$R_{ILIM\text{-}SHORT}$	Short circuit resistance threshold		55	83	105	Ω
V_{IN_DPM}	V_{IN_DPM} threshold range	SA mode	4.2		10	V
		I^2C mode	4.2		4.76	
	V_{IN_DPM} threshold for USB Input in SA mode	USB100, USB150, USB500, USB900, current limit selected. Also I^2C register default.	4.27	4.36	4.45	
	V_{IN_DPM} threshold with adaptor current limit and VDPM shorted to GND	Must set to external resistor settings via the EN1/EN2 pins or the I^2C register interface.	V_{IN_DPM} –2%	V_{IN_DPM}	V_{IN_DPM} +2%	
	V_{IN_DPM} threshold Accuracy	Both I^2C and SA mode	–2%		2%	
V_{REF_DPM}	DPM regulation voltage	External resistor setting only	1.15	1.2	1.25	V
V_{DPM_SHRT}	VIN_DPM short threshold	If VDPM is shorted to ground, V_{IN_DPM} threshold will use internal default value		0.3		V
V_{UVLO}	IC active threshold voltage	V_{IN} rising	3.15	3.35	3.5	V
	IC active hysteresis	V_{IN} falling from above V_{UVLO}		175		mV
V_{SLP}	Sleep-mode entry threshold, $V_{IN\text{-}VBAT}$	2.0 V ≤ V_{BAT} ≤ V_{BATREG}, V_{IN} falling	0	50	100	mV
	Sleep-mode exit hysteresis, $V_{IN\text{-}VBAT}$	2.0 V ≤ V_{BAT} ≤ V_{BATREG}	40	100	160	mV
V_{OVP}	Input supply OVP threshold voltage	IN rising	Input OVP –200mV	Input OVP	Input OVP +200mV	V
	VOVP hysteresis	IN falling from V_{OVP}		100		mV
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{BATREG} to turn off charger during charge	102.5	105	107.5	% V_{BATREG}
	VBOVP hysteresis	Lower limit for V_{BAT} falling from above V_{BOVP}		1		% V_{BATREG}

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Electrical Characteristics (continued)

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = 0ºC-125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM CONVERTER						
$R_{ON(BLK)}$	Internal blocking MOSFET on-resistance	Measured from IN to PMID		60	100	mΩ
$R_{ON(HS)}$	Internal high-side MOSFET on-resistance	Measured from PMID to SW		100	150	mΩ
$R_{ON(LS)}$	Internal low-side MOSFET on-resistance	Measured from SW to PGND		110	165	mΩ
I_{CbC}	Cycle-by-cycle current limit	VSYS shorted	2.6	3.2	3.8	A
f_{OSC}	Oscillator frequency		2.7	3	3.3	MHz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0%			
T_{SHTDWN}	Thermal trip			150		°C
	Thermal hysteresis			10		
T_{REG}	Thermal regulation threshold	Charge current begins to cut off		125		
LDO						
V_{LDO}	LDO Output Voltage	V_{IN} = 5.5 V, I_{LDO} = 0 to 50 mA	4.65	4.95	5.25	V
I_{LDO}	Maximum LDO Output Current		50			mA
V_{DO}	LDO Dropout Voltage ($V_{IN} – V_{LDO}$)	V_{IN} = 5.0 V, I_{LDO} = 50 mA		200	300	mV
BATTERY-PACK NTC MONITOR (1)						
V_{HOT}	High temperature threshold	V_{TS} falling	29.6	30	30.4	% V_{LDO}
$V_{HYS(HOT)}$	Hysteresis on high threshold	V_{TS} rising	0.6	0.9	1.2	
V_{WARM}	Warm temperature threshold	V_{TS} falling	37.9	38.3	38.7	
$V_{HYS(WARM)}$	Hysteresis on warm temperature threshold	V_{TS} rising	0.6	0.9	1.2	
V_{COOL}	Cool temperature threshold	V_{TS} rising	48.1	48.5	48.9	
$V_{HSY(COOL)}$	Hysteresis on cool temperature threshold	V_{TS} falling	0.6	0.9	1.2	
V_{COLD}	Low temperature threshold	V_{TS} rising	59.6	60	60.4	
$V_{HYS(COLD)}$	Hysteresis on low threshold	V_{TS} falling	0.6	0.9	1.2	
V_{FRZ}	Freeze temperature threshold	V_{TS} rising	62	62.5	63	
$V_{HYS(FRZ)}$	Hysteresis on freeze threshold	V_{TS} falling	0.6	0.9	1.2	
I_{TS}	TS current in charge mode	V_{IN} = 5.0 V, V_{TS} = 2.0 V, V_{BAT} = 3.5 V		0.005	0.1	µA
INPUTS (EN1, EN2, $\overline{CE}$, SCL, SDA)						
V_{IH}	Input high threshold		1			V
V_{IL}	Input low threshold				0.4	V
STATUS OUTPUTS ($\overline{CHG}$, STAT, INT)						
V_{OL}	Low-level output saturation voltage	I_O = 5 mA, sink current			0.4	V
I_{IH}	High-level leakage current	Hi-Z and 5V applies			1	µA

7.6 Timing Requirements

$V_{UVLO} < V_{IN} < V_{OVP}$ and $V_{IN} > V_{BAT}+V_{SLP}$, T_J = 0ºC-125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-PATH MANAGEMENT						
$t_{DGL(SC1)}$	Deglitch Time, OUT Short Circuit during Discharge or Supplement Mode	Measured from (V_{BAT} – V_{SYS}) = 300 mV		740		µs
$t_{REC(SC1)}$	Recovery Time, OUT Short Circuit during Discharge or Supplement Mode			64		ms
BATTERY CHARGER						
$t_{DGL(LOWV)}$	Deglitch time for pre-charge to fast charge transition			32		ms
$t_{DGL(BATSHRT)}$	Deglitch time for trickle charge to pre-charge transition			256		µs
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL} = 100 ns		64		ms
$t_{DGL(RCH)}$	Deglitch time	V_{BAT} falling below V_{RCH}, t_{FALL} = 100 ns		32		ms
BATTERY DETECTION						
t_{DETECT}	Battery detection time	For both V_{BATREG_HI} and V_{BATREG_LO}		32		ms
INPUT PROTECTION						
$t_{DGL(SLP)}$	Deglitch time for IN rising above VIN+VSLP_EXIT	Rising voltage, 2-mV over drive, t_{RISE} = 100 ns		32		ms
$t_{DGL(OVP)}$	Deglitch time for IN Rising above VOVP	IN rising voltage, t_{RISE} = 100 ns		32		ms
$t_{DGL(BOVP)}$	BOVP Deglitch	Battery entering/exiting BOVP		1		ms
BATTERY-PACK NTC MONITOR (1)						
$t_{DGL(TS)}$	Deglitch time on TS change			32		ms
TIMERS						
t_{SAFETY}	45 min safety timer			2700		s
	6 hr safety timer			21600		
	9 hr safety timer			32400		
$t_{WATCH-DOG}$	Watch dog timer			50		s

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7.7 Typical Characteristics

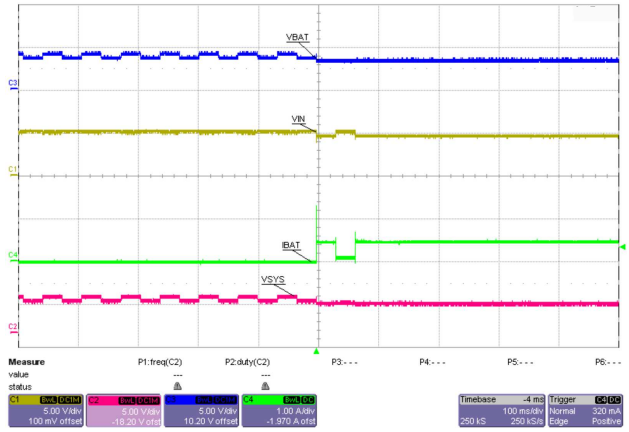

Figure 1. Battery Detection

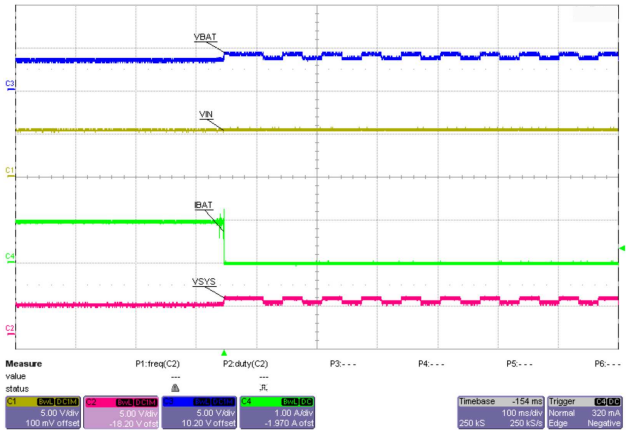

Figure 2. Battery Removal

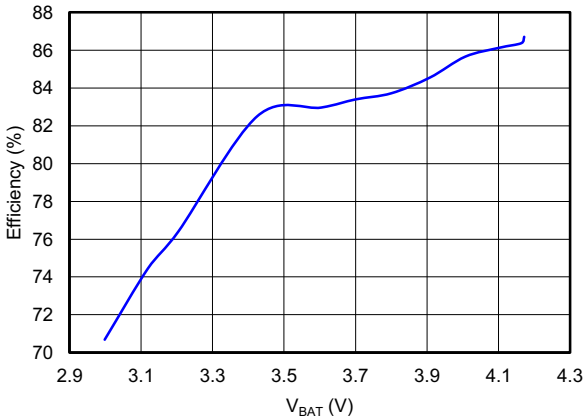

Figure 3. Efficiency vs Battery Voltage

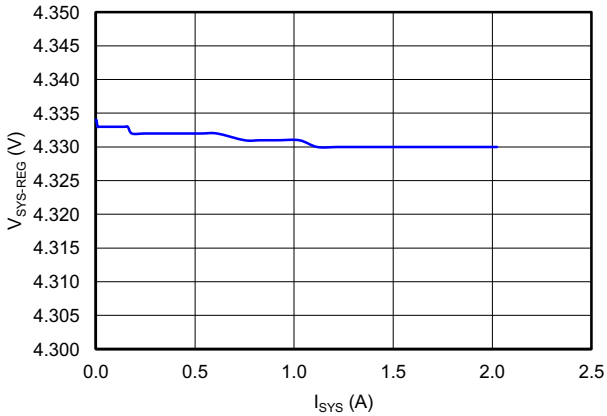

Figure 4. System Voltage Regulation vs Load Current

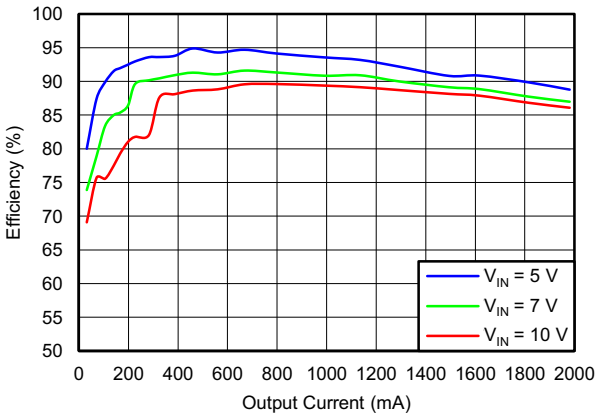

Figure 5. Efficiency vs Output Current

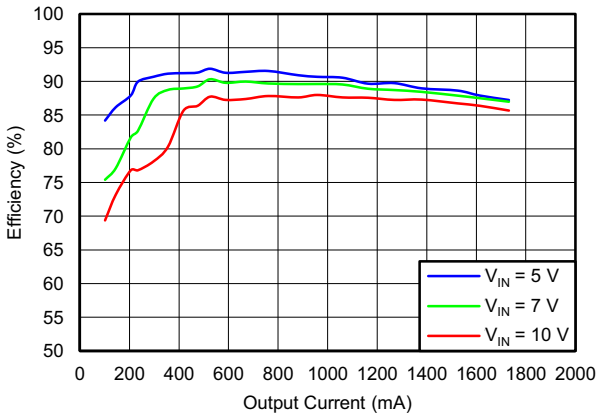

Figure 6. Efficiency vs Output Current

Typical Characteristics (continued)

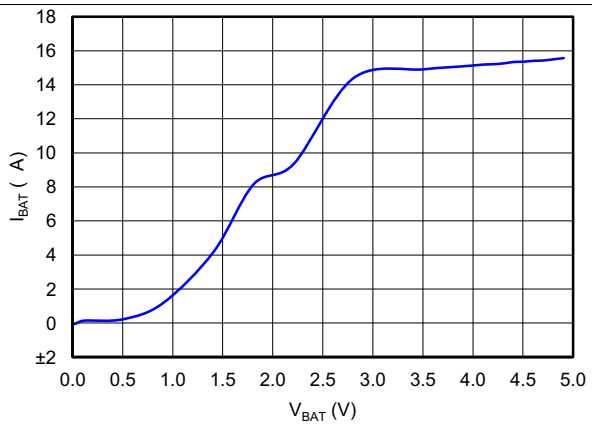

Figure 7. BAT IQ, SYSOFF = 0

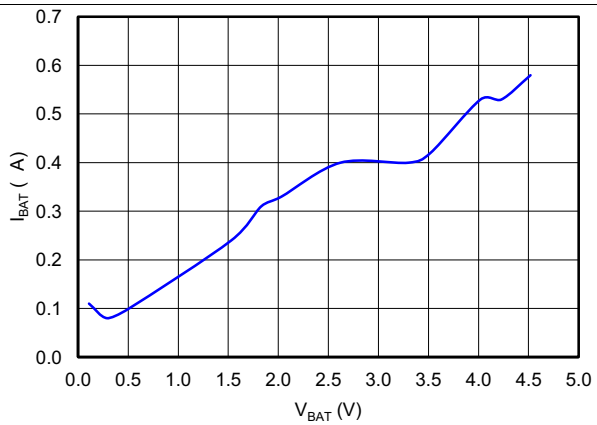

Figure 8. BAT IQ, SYSOFF = 1

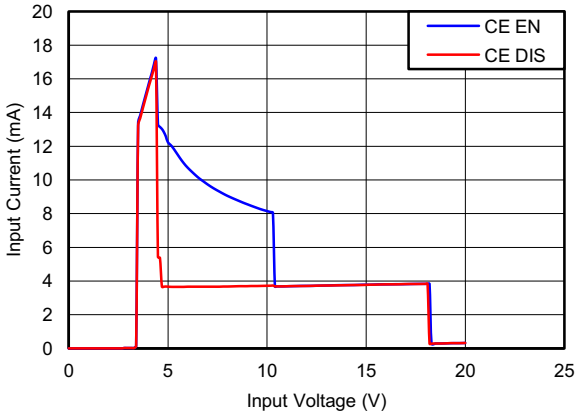

Figure 9. Input IQ With Charge DIS and EN

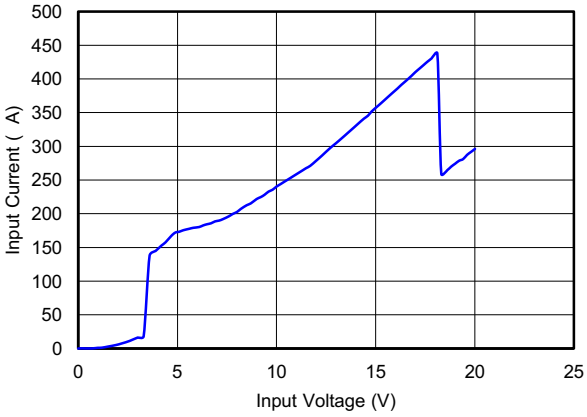

Figure 10. Input IQ with Charge Enable and Hi-Z

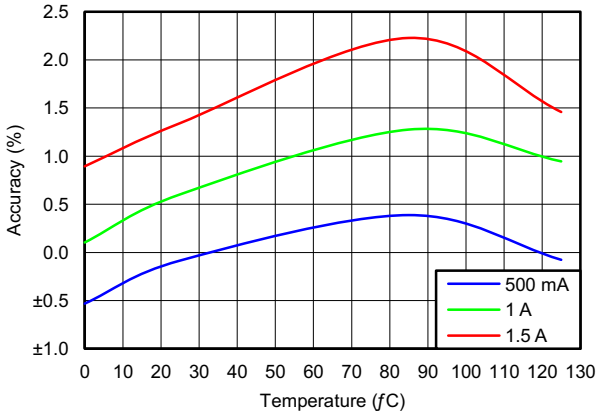

Figure 11. I_{CHG} Accuracy with Internal Settings, V_{BAT} = 3.3 V

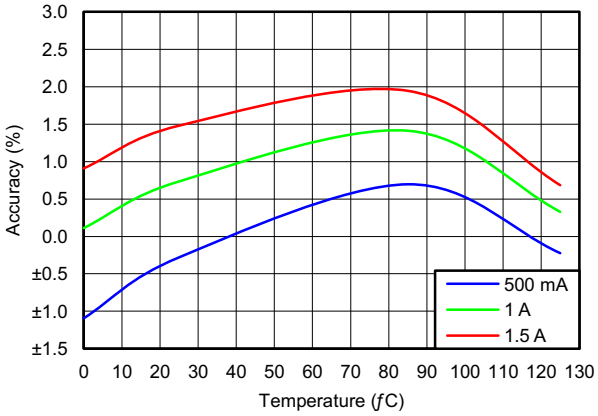

Figure 12. I_{CHG} Accuracy with Internal Settings, V_{BAT} = 3.8 V

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Typical Characteristics (continued)

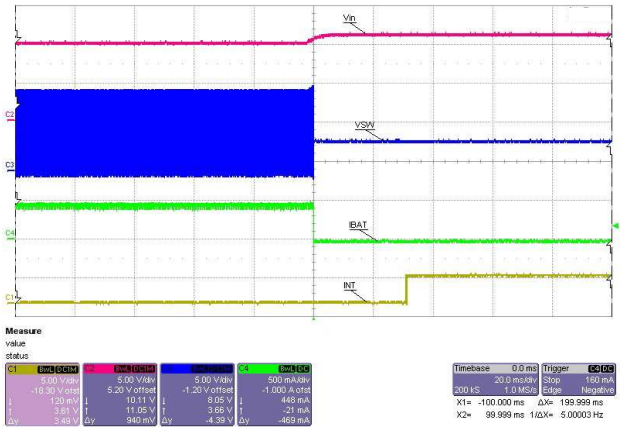

Figure 13. Input OVP Event with INT

8 Detailed Description

8.1 Overview

The bq24250C is a highly-integrated, single-cell, Li-Ion battery charger with integrated current sense resistors targeted for space-limited, portable applications with high-capacity batteries. The single-cell charger has a single input that operates from either a USB port or AC wall adapter for a versatile solution.

The bq24250C device has two modes of operation: 1) I2C mode, and 2) standalone mode. In I2C mode, the host adjusts the charge parameters and monitors the status of the charger operation. In standalone mode, the external resistor sets the input-current limit, and charge current limit. Standalone mode also serves as the default settings when a DCP adapter is present. It enters host mode while the I2C registers are accessed and the watchdog timer has not expired (if enabled). The battery is charged in four phases: trickle charge, pre-charge, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded.

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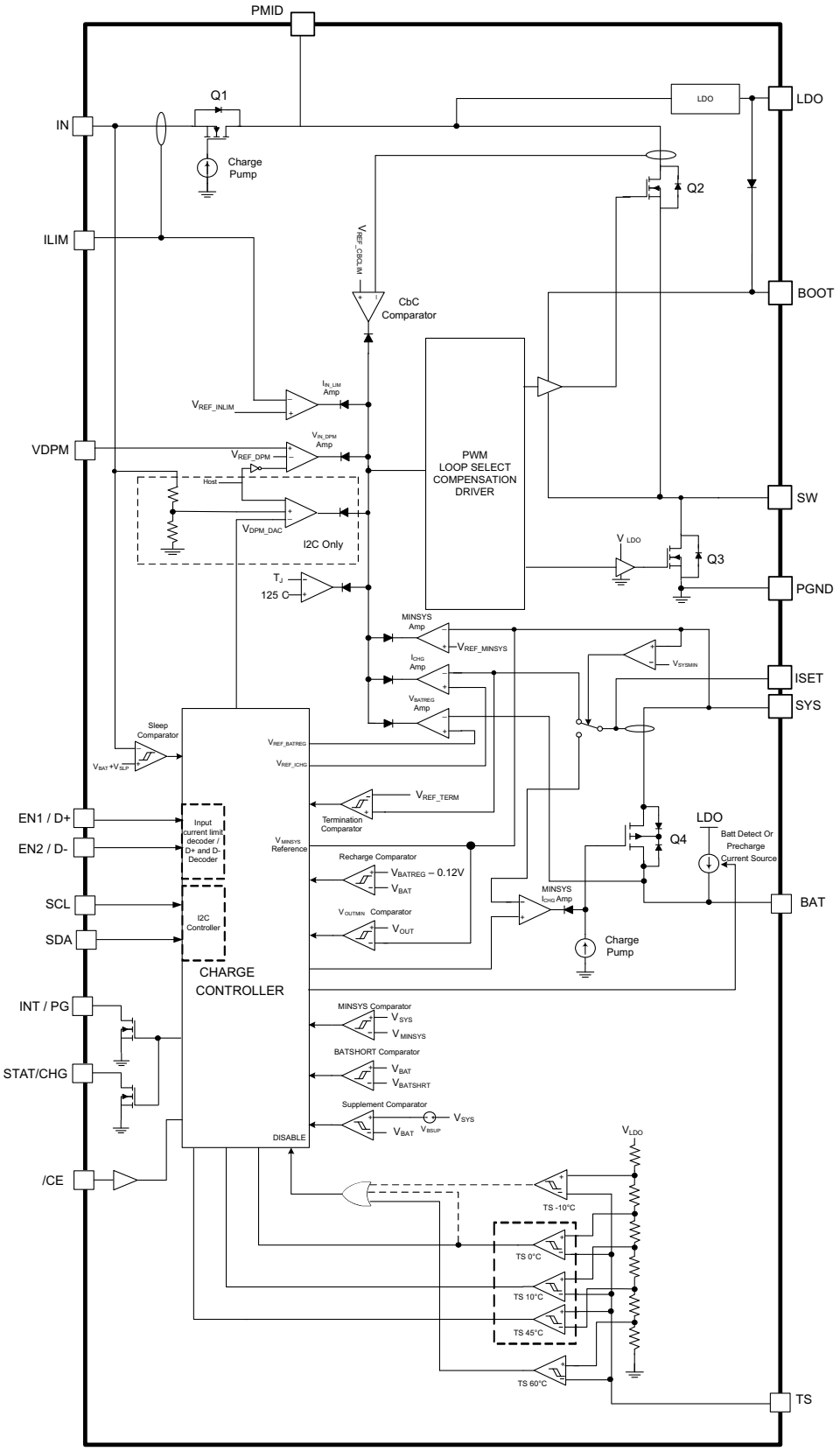
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Dynamic Power Path Management

The bq24250C features a SYS output that powers the external system load connected to the battery. This output is active whenever a valid source is connected to IN or BAT. The following discusses the behavior of SYS with a source connected to the supply or a battery source only.

When a valid input source is connected to the input and the charge is enabled, the charge cycle is initiated. In case of VBAT > ~3.5V, the SYS output is connected to VBAT. If the SYS voltage falls to VMINSYS, it is regulated to the VSYSREG threshold to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET is linearly regulated to regulate the charge current into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS.

The dynamic power path management (DPPM) circuitry of the bq24250C monitors the current limits continuously and if the SYS voltage falls to the VMINSYS voltage, it adjusts charge current to maintain the minimum system voltage and supply the load on SYS. If the charge current is reduced to zero and the load increases further, the bq24250C enters battery supplement mode. During supplement mode, the battery FET is turned on and the battery supplements the system load.

If the battery is ever 5% above the regulation threshold, the battery OVP circuit shuts the PWM converter off and the battery FET is turned on to discharge the battery to safe operating levels. Battery OVP FAULT is shown in the I2C FAULT registers.

When no input source is available at the input and the battery is connected, the battery FET is turned on similar to supplement mode. The battery must be above VBATUVLO threshold to turn on the SYS output. In this mode, the current is not regulated;

8.3.2 Production Test Mode

To aid in end mobile device product manufacturing, the bq24250C includes a Production Test Mode (PTM), where the device is essentially a DC-DC buck converter. In this mode the input current limit to the charger is disabled and the output current limit is limited only by the inductor cycle-by-cycle current (e.g. 3.5A). The PTM mode can be used to test systems with high transient loads such as GSM transmission without the need of a battery being present.

As a means of safety, the Anyboot algorithm determines if a battery is not present at the output prior to enabling the PTM mode. If a battery is present and the software attempts to enter PTM mode, the device will not enable PTM mode.

8.3.3 *AnyBoot* Battery Detection

The bq24250C includes a sophisticated battery detection algorithm used to provide the system with the proper status of the battery connection. The AnyBoot battery algorithm also ensures the detection of voltage based battery protectors that may have a long closure time (due to the hysteresis of the protection switch and the cell capacity). The AnyBoot battery detection algorithm utilizes a dual-voltage based detection methodology where the system rail switches between two primary voltage levels. The period of the voltage level shift is 64ms and therefore the power supply rejection of the down-system electronics detects this shift as essentially DC.

The AnyBoot algorithm has essentially 3 states. The 1st state is used to determine if the device has terminated with a battery attached. If it has terminated due to the battery not being present, then the algorithm moves to the 2nd and 3rd states. The 2nd and 3rd states shift the system voltage level between 4.2V and 3.72V. In each state there are comparator checks to determine if a battery has been inserted. The two states ensure the detection of a battery even if the voltage of the cell is at the same level of the comparator thresholds. The algorithm will remain in states 2 and 3 until a battery has been inserted. The flow diagram details for the Anyboot algorithm are shown in Figure 14.

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Feature Description (continued)

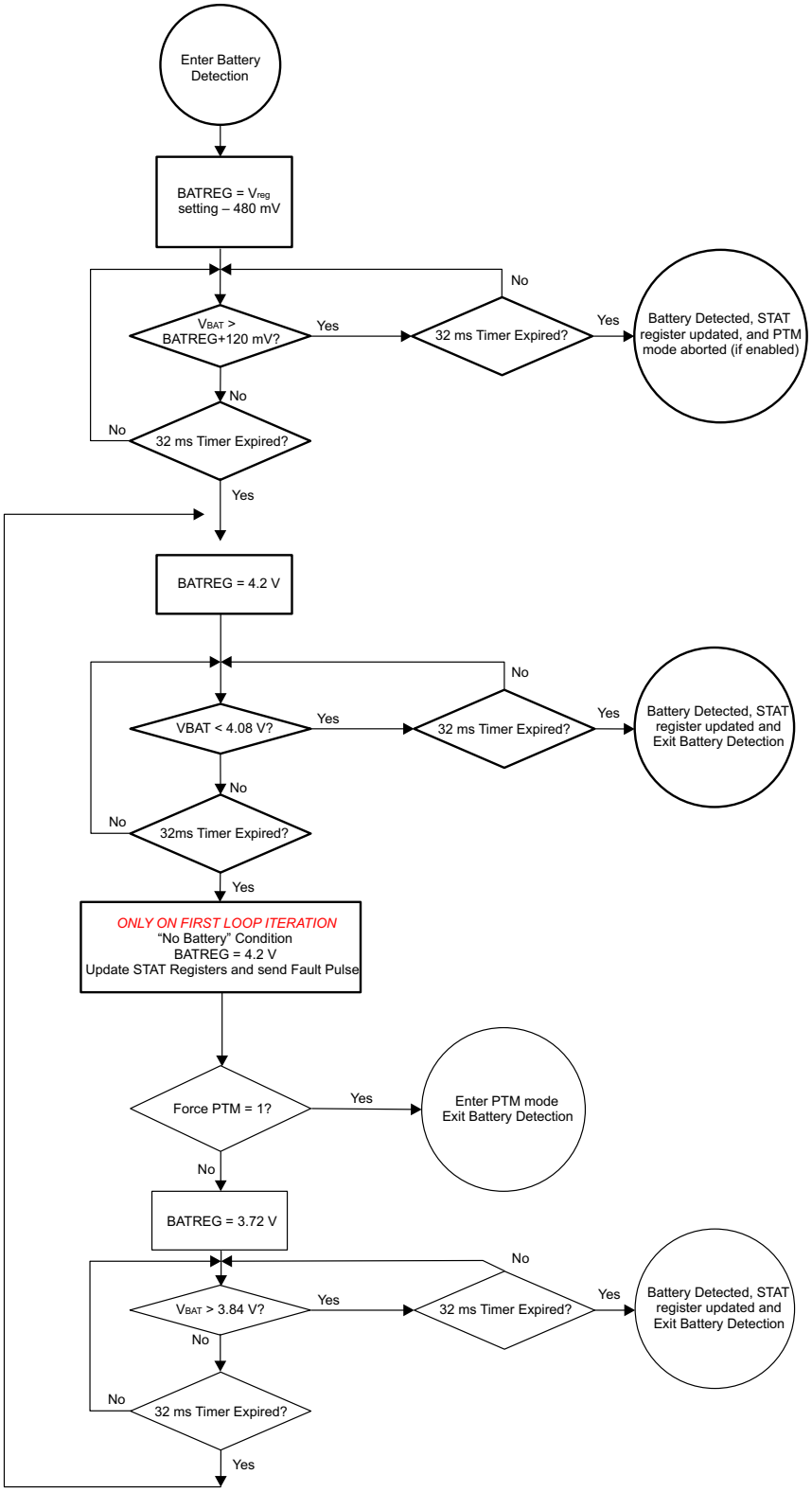

Figure 14. AnyBoot Battery Detection Flow Diagram

8.4 Device Functional Modes

8.4.1 Charge Profile

The bq24250C provides a switch-mode buck regulator with output power path and a charge controller to provide optimum performance over the full battery charge cycle. The control loop for the buck regulator has 7 primary feedback loops that can set the duty cycle:

1. Constant Current (CC)
2. Constant Voltage (CV)
3. Minimum System Voltage (MINSYS)
4. Input Current (I_{ILIM})
5. Input Voltage (V_{IN_DPM})
6. Die Temperature
7. Cycle by Cycle Current

The feedback with the minimum duty cycle will be chosen as the active loop. The bq24250C supports a precision Li-Ion or Li-Polymer charging system for single-cell applications. The Dynamic Power Path Management (DPPM) feature regulates the system voltage to a minimum of V_{MINSYS}, so that startup is enabled even with a missing or deeply discharged battery. This provides a much better overall user experience in mobile applications. The figure below illustrates a typical charge profile while also demonstrating the minimum system output voltage regulation.

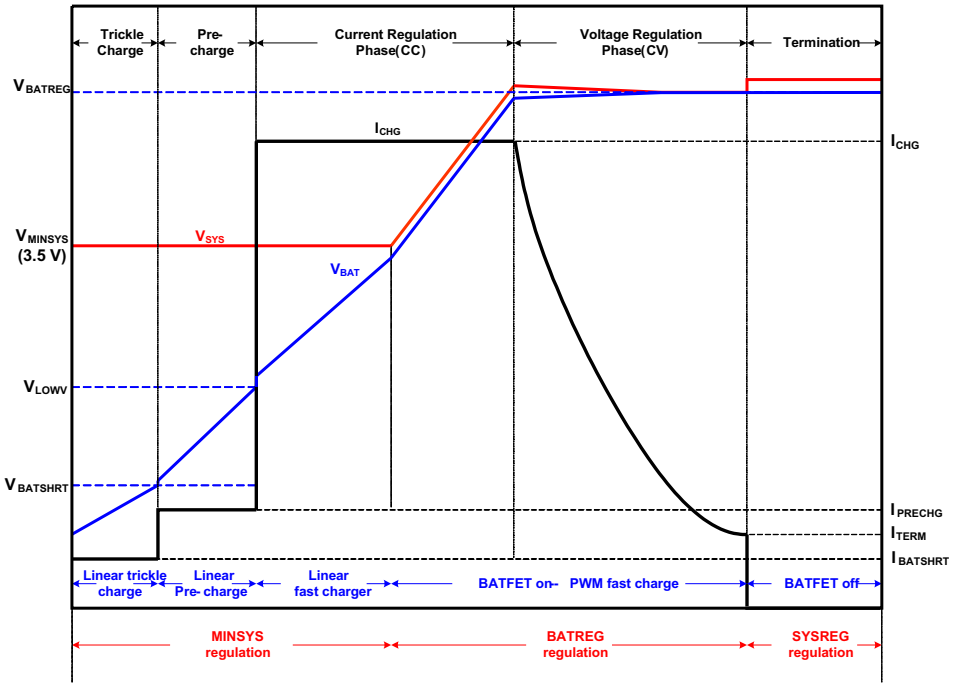

Figure 15. Typical Charge Profile

Figure 16 demonstrates a measured charge profile with the bq24250C while charging a 2700mAh Li-Ion battery at a charge rate of 1A.

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Device Functional Modes (continued)

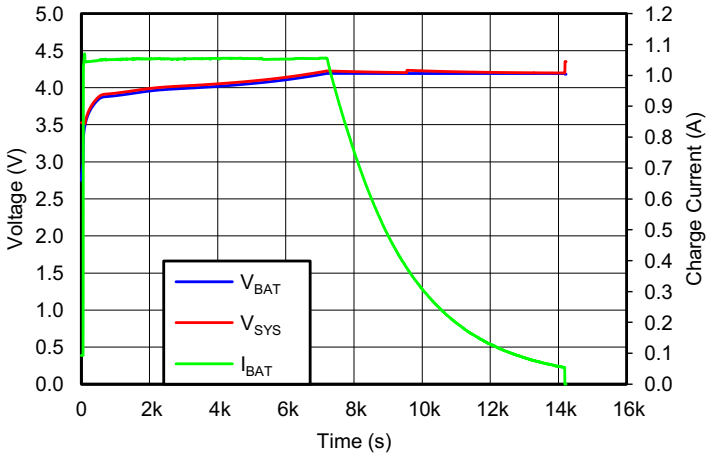

Figure 16. bq24250C Charge Profile while Charging a 2700 mAh Battery at a 1A Charge Rate

Figure 17 illustrates the precharge behavior of the above charge profile by narrowing the time axis to 0 – 120 seconds.

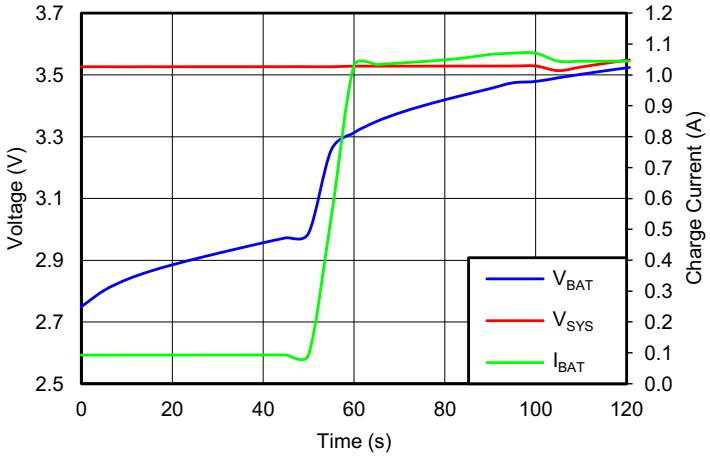

Figure 17. bq24250C Charge Profile While Charging a 2700-mAh Battery at a 1A Charge During Precharge

8.4.2 EN1/EN2 Pins

The bq24250C is I^2C and Stand Alone part. The EN1 and EN2 pins are available in this IC spin to support USB 2.0 compliance. These pins are used for Input Current Limit Configuration I. Set EN1 and EN2 to control the maximum input current and enable USB compliance. See Table 1 below for programming details.

When the input current limit pins change state, the V_{IN_DPM} threshold changes as well. See Table 1 for the detailed truth table:

Table 1. EN1, and EN2 Truth Table(1)

EN2	EN1	Input Current Limit	V_{IN_DPM} Threshold
0	0	500mA	4.36V
0	1	Externally programmed by ILIM (up to 2.0A)	Externally programmed VDPM
1	0	100mA	4.36V
1	1	Input Hi-Z	None

(1) USB3.0 support available. Contact your local TI representative for details.

8.4.3 I²C Operation (Host Mode / Default Mode)

There are two primary modes of operation when interacting with the charge parameters of the bq24250C charger: 1) *Host mode* operation where the I²C registers set the charge parameters, and 2) *Default mode* where the register defaults set the charge parameters.

Figure 18 illustrates the behavior of the bq24250C when transitioning between host mode and stand alone mode:

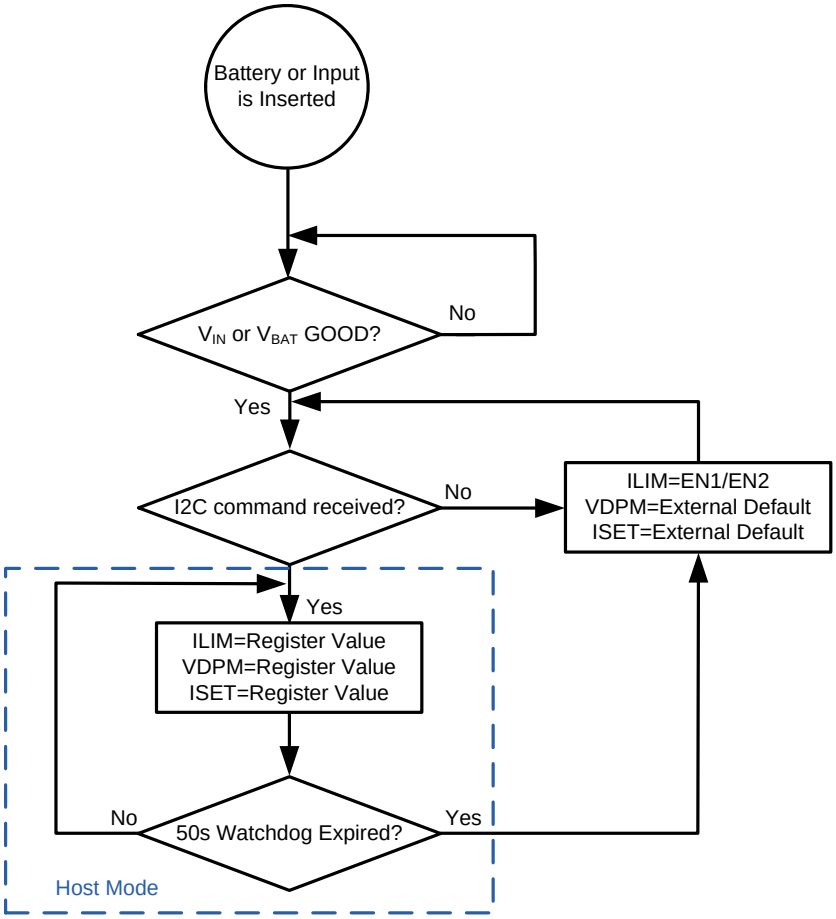

Figure 18. Host Mode and Stand Alone Mode Handoff

Once the battery or input is inserted and above the good thresholds, the device determines if an I²C command has been received in order to discern whether to operate from the I²C registers or the internal register defaults. In stand-alone mode the input current limit is set by the EN1/EN2 pins. If the watch dog timer is enabled, the device will enter stand alone operation once the watchdog timer expires and re-initiate the default charge settings.

8.4.4 External Settings: ISET, ILIM and VIN_DPM

If the external resistor settings are used, the following equations can be followed to configure the charge settings.

The fast charge current resistor (R_{ISET}) can be set by using the following formula:

$$R_{ISET} = \frac{K_{ISET}}{I_{FC}} = \frac{250}{I_{FC}} \quad (1)$$

Where I_{FC} is the desired fast charge current setting in Amperes.

The input current limit resistor (R_{ILIM}) can be set by using the following formula:

$$R_{ILIM} = \frac{K_{ILIM}}{I_{IC}} = \frac{270}{I_{IC}} \quad (2)$$

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Where I_{IC} is the desired input current limit in Amperes.

Based on the application diagram reference designators, the resistor R1 and R2 can be calculated as follows to set V_{IN_DPM}:

$$V_{IN_DPM} = V_{REF_DPM} \times \frac{R_1 + R_2}{R_2} = 1.2V \times \frac{R_1 + R_2}{R_2} \quad (3)$$

V_{IN_DPM} should be chosen first along with R_1. Choosing R_1 first will ensure that R_2 will be greater than the resistance chosen. This is the case since V_{IN_DPM} should be chosen to be greater than 2x V_{REF_DPM}.

If external resistors are not desired in order to reduce the BOM count, the VDPM and the ILIM pins can be shorted to set the internal defaults. The ISET resistor cannot be shorted in order to avoid an unstable charging state.Note that floating the ILIM pin will result in zero charge current if the external ISET is configured via the I^2C register. Table 2 summarizes the settings when the ILIM, ISET, and V_{IN_DPM} pins are shorted to GND:

Table 2. ILIM, VDPM, and ISET Short Behaviors

PIN SHORTED	BEHAVIOR
ILIM	Input current limit = 2A
VDPM	V_{IN_DPM} = 4.68V
ISET	Fault—Charging Suspended

8.4.5 Transient Response

The bq24250C includes an advanced hybrid switch mode control architecture. When the device is regulating the charge current (fast-charge), a traditional voltage mode control loop is used with a Type-3 compensation network. However, the bq24250C switches to a current mode control loop when the device enters voltage regulation. Voltage regulation occurs in three charging conditions: 1) Minimum system voltage regulation (battery below MINSYS), 2) Battery voltage regulation (I_{BAT} < I_{CHG}), and 3) Charge Done (V_{SYS} = V_{BAT} + 3.5%). This architecture allows for superior transient performance when regulating the voltage due to the simplification of the compensation when using current mode control. The below transient response plot illustrates a 0A to 2A load step with 4.7ms full cycle and 12% duty cycle. A 3.9V Li-Ion battery is used. The input voltage is set to 5V, charge current is set to 0.5A and the input current is limited to 0.5A. Note that a high line impedance input supply was used to indicate a realistic input scenario (adapter and cable). This is illustrated by the change in V_{IN} seen at the input of the IC.

Figure 19 shows a ringing at both the input voltage and the input current. This is caused by the input current limit speed up comparator.

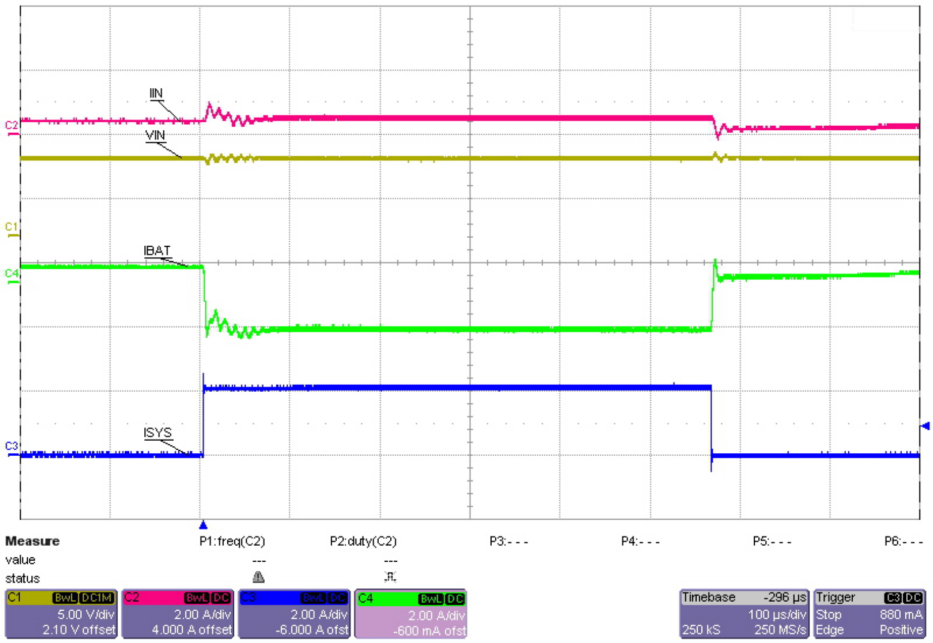

Figure 19. 2A Load Step Transient

8.4.6 Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage deceases. Once the supply drops to VIN_DPM, the input current limit is reduced down to prevent the further drop of the supply. When the IC enters this mode, the charge current is lower than the set. This feature ensures IC compatibility with adapters with different current capabilities without a hardware change.

8.4.7 Sleep Mode

The bq24250C enters the low-power sleep mode if the voltage on VIN falls below sleep-mode entry threshold, VBAT+VSLP, and VIN is higher than the under-voltage lockout threshold, VUVLO. This feature prevents draining the battery during the absence of VIN. When VIN < VBAT+VSLP, the bq24250C turns off the PWM converter, turns on the battery FET, sends a single 256µs pulse is sent on the STAT and INT outputs and the FAULT/STAT bits of the status registers are updated in the I^2C. Once VIN > VBAT+VSLP with the hysteresis, the FAULT bits are cleared and the device initiates a new charge cycle.

8.4.8 Input Over-Voltage Protection

The bq24250C provides over-voltage protection on the input that protects downstream circuitry. The built-in input over-voltage protection to protect the device and other components against damage from overvoltage on the input supply (Voltage from VIN to PGND). When VIN > VOVP, the bq24250C turns off the PWM converter, turns the battery FET, sends a single 256µs pulse is sent on the STAT and INT outputs and the FAULT/STAT bits of the status registers and the battery/supply status registers are updated in the I^2C. Once the OVP fault is removed, the FAULT bits are cleared and the device returns to normal operation. The OVP threshold for the bq24250 is programmable from 6.5V to 10.5V using VOVP bits in register #7.

8.4.9 NTC Monitor

The bq24250C includes the integration of an NTC monitor pin that complies with a modified JEITA specification (PSE also available upon request). The voltage based NTC monitor allows for the use of any NTC resistor with the use of the circuit shown in Figure 20.

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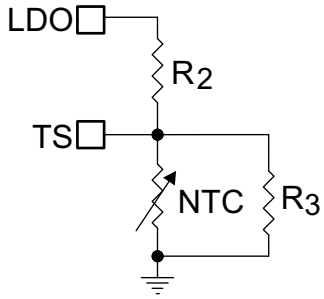

Figure 20. Voltage Based NTC circuit

The use of R3 is only necessary when the NTC does not have a beta near 3500K. When deviating from this beta, error will be introduced in the actual temperature trip thresholds. The trip thresholds are summarized below which are typical values provided in the specification table. Note that the T_{WARM} threshold is just a warning for the warm temperature, the device will generate an interrupt but it will not affect the charging process.

Table 3. Ratiometric TS Trip Thresholds

V_{HOT}	30.0%
V_{WARM}	38.3%
V_{COOL}	48.5%
V_{COLD}	60%

When sizing for R2 and R3, it is best to solve two simultaneous equations that ensure the temperature profile of the NTC network will cross the V_{HOT} and V_{COLD} thresholds. The accuracy of the V_{WARM} and V_{COOL} threshold will depend on the beta of the chosen NTC resistor. The two simultaneous equations are shown below:

$$\%V_{COLD} = \frac{\left(\frac{R_3 R_{NTC}|_{TCOLD}}{R_3 + R_{NTC}|_{TCOLD}}\right)}{\left(\frac{R_3 R_{NTC}|_{TCOLD}}{R_3 + R_{NTC}|_{TCOLD}}\right) + R2} \times 100$$

$$\%V_{HOT} = \frac{\left(\frac{R_3 R_{NTC}|_{THOT}}{R_3 + R_{NTC}|_{THOT}}\right)}{\left(\frac{R_3 R_{NTC}|_{THOT}}{R_3 + R_{NTC}|_{THOT}}\right) + R2} \times 100 \quad (4)$$

Where the NTC resistance at the V_{HOT} and V_{COLD} temperatures must be resolved as follows:

$$R_{NTC}|_{TCOLD} = R_o e^{\beta\left(1/T_{COLD} - 1/T_o\right)}$$

$$R_{NTC}|_{THOT} = R_o e^{\beta\left(1/T_{HOT} - 1/T_o\right)} \quad (5)$$

To be JEITA compliant, T_{COLD} must be 0°C and T_{HOT} must be 60°C. If an NTC resistor is chosen such that the beta is 4000K and the nominal resistance is 10kΩ, the following R2 and R3 values result from the above equations:

R_2 = 5 kΩ
R_3 = 9.82 kΩ

Figure 21 illustrates the temperature profile of the NTC network with R2 and R3 set to the above values.

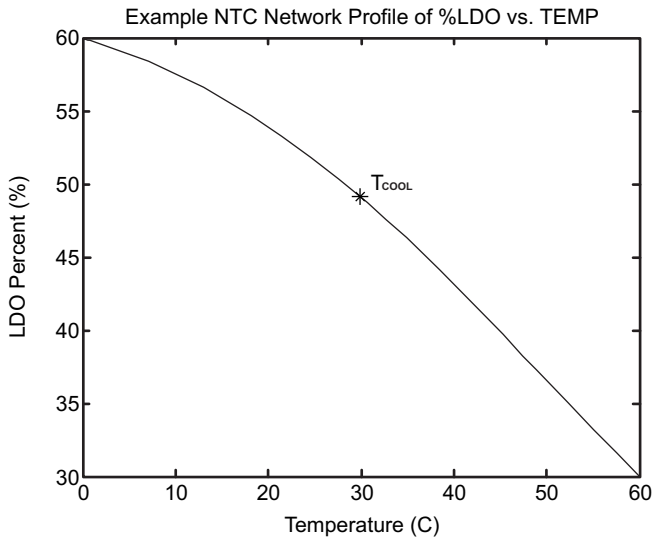

Figure 21. Voltage Based NTC Circuit Temperature Profile

Once the resistors are configured, the internal JEITA algorithm will apply the below profile at each trip point for battery voltage regulation and charge current regulation.

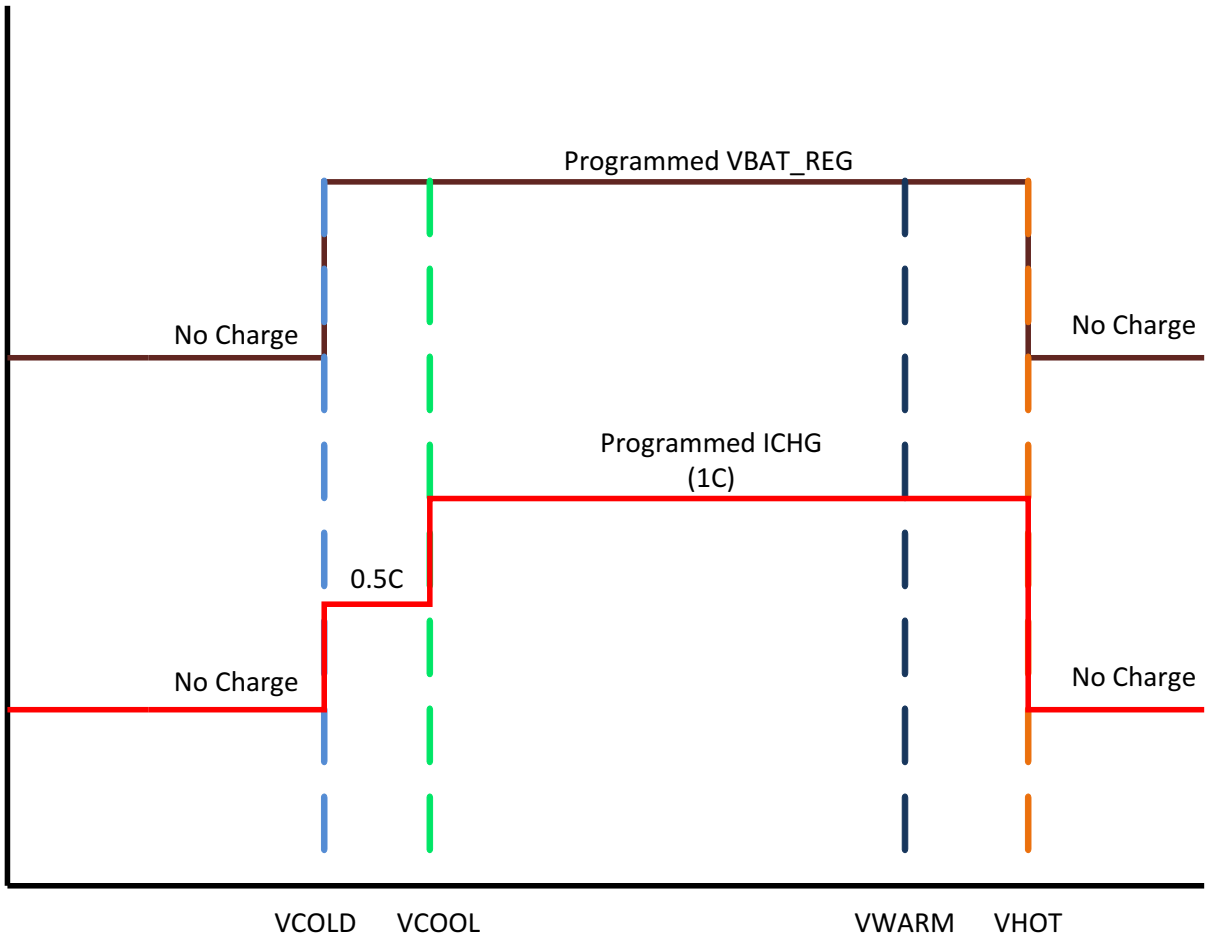

Figure 22. Modified JEITA Profile for Voltage and Current Regulation Loops

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8.4.10 Safety Timer

At the beginning of charging process, the bq24250C starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, the IC enters suspend mode where charging is disabled. The safety timer time is selectable using the I^2C interface. A single 256µs pulse is sent on the STAT and INT outputs and the FAULT/ bits of the status registers are updated in the I^2C. This function prevents continuous charging of a defective battery if the host fails to reset the safety timer. When 2xTMR_EN bit is set to "1", the safety timer runs at a rate 2x slower than normal (the timer is extended) under the following conditions:

- Pre-charge or linear mode (minimum system voltage mode),
- During thermal regulation where the charge current is reduced,
- During TS fault where the charge current is reduced

The safety timer is suspended during OVP, TS fault where charge is disabled, thermal shut down, and sleep mode.

8.4.11 Watchdog Timer

In addition to the safety timer, the bq24250C contains a 50-second watchdog timer that monitors the host through the I^2C interface. Once a write is performed on the I^2C interface, a watchdog timer is reset and started. The watchdog timer can be disabled by writing "0" on WD_EN bit of register #1. Writing "1" on that bit enables it and reset the timer.

If the watchdog timer expires, the IC enters DEFAULT mode where the default charge parameters are loaded and charging continues. The I^2C may be accessed again to re-initialize the desired values and restart the watchdog timer as long as the safety timer has not expired. Once the safety timer expires, charging is disabled.

8.4.12 Thermal Regulation and Thermal Shutdown

During the charging process, to prevent overheat of the chip, bq24250C monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, TREG. The charge current is reduced when the junction temperature increases above TREG. Once the charge current is reduced, the system current is reduced while the battery supplements the load to supply the system. This may cause a thermal shutdown of the IC if the die temperature rises too. At any state, if T_J exceeds TSHTDWN, bq24250C suspends charging and disables the buck converter. During thermal shutdown mode, PWM is turned off, all safety timers are suspended, and a single 256µs pulse is sent on the STAT and INT outputs and the FAULT/STAT bits of the status registers are updated in the I^2C. A new charging cycle begins when T_J falls below TSHTDWN by approximately 10°C.

8.4.13 Fault Modes

The bq24250C includes several hardware fault detections. This allows for specific conditions that could cause a safety concern to be detected. With this feature, the host can be alleviated from monitoring unsafe charging conditions and also allows for a "fail-safe" if the host is not present. The table below summarizes the faults that are detected and the resulting behavior.

FAULT CONDITION	CHARGER BEHAVIOR	SAFETY TIMER BEHAVIOR
Input OVP	VSYS and ICHG Disabled	Suspended
Input UVLO	VSYS and ICHG Disabled	Reset
Sleep (VIN < VBAT)	VSYS and ICHG Disabled	Suspended
TS Fault (Batter Over Temp)	VSYS Active and ICHG Disabled	Suspended
Thermal Shutdown	VSYS and ICHG Disabled	Suspended
Timer Fault	VSYS Active and ICHG Disabled	Reset
No Battery	VSYS Active and ICHG Disabled	Suspended
ISET Short	VSYS Active and ICHG Disabled	Suspended
Input Fault & LDO Low	VSYS and ICHG Disabled	Suspended

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8.4.14 Serial Interface Description

The bq24250C uses an I^2C compatible interface to program charge parameters. I^2C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor, see I^2C-Bus Specification, Version 5, October 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

Thebq24250C device works as a slave and supports the following data transfer modes, as defined in the I^2C Bus™ Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. The I^2C circuitry is powered from IN when a supply is connected.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The bq24250C device only supports 7-bit addressing. The device 7-bit address is defined as ‘1101010’ (0x6Ah).

To avoid I^2C hang-ups, a timer ($t_{I2CRESET}$) runs during I2C transactions. If the transaction takes longer than $t_{I2CRESET}$, any additional commands are ignored and the I2C engine is reset. The timeout is reset with START and repeated START conditions and stops when a valid STOP condition is sent.

8.4.14.1 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 23. All I^2C -compatible devices should recognize a start condition.

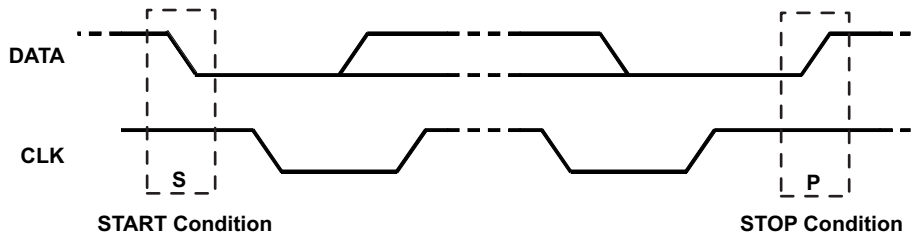

Figure 23. START and STOP Condition

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 24). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 25) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

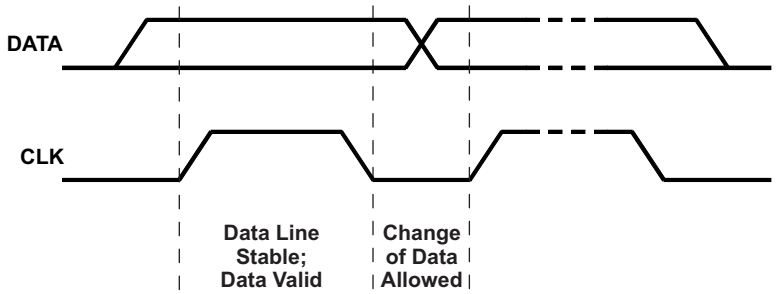

Figure 24. Bit Transfer on the Serial Interface

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The master generates further SCL cycles to either transmit data to the slave (R/W bit 0) or receive data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 23). This releases the bus and stops the communication link with the addressed slave. All I2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave I2C logic from remaining in a incorrect state. Attempting to read data from register addresses not listed in this section will result in 0xFFh being read out.

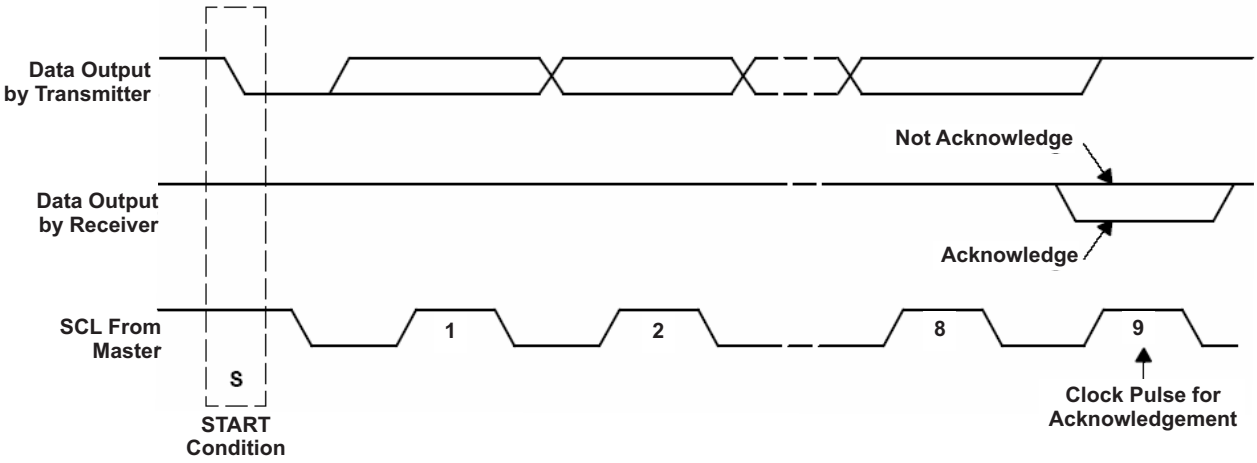

Figure 25. Acknowledge on the I2C Bus

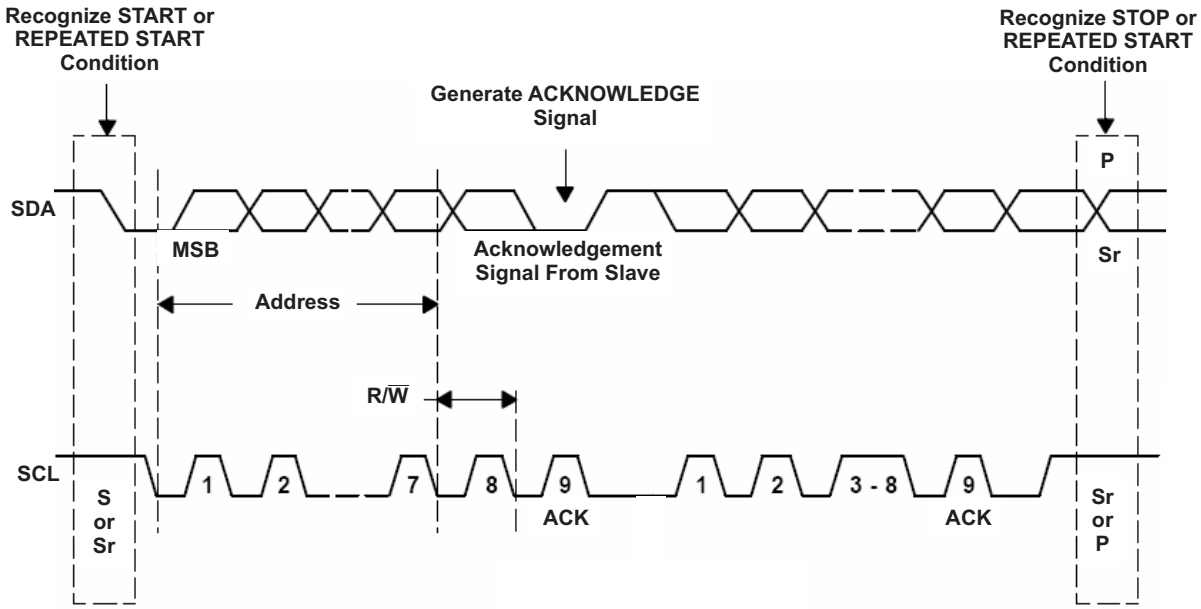

Figure 26. Bus Protocol

8.5 Register Maps

Register #1
Memory location: 00, Reset state: x0xx xxxx

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	WD_FAULT	Read only	Read:0 – No fault 1 – WD timeout if WD enabled
B6	WD_EN	Read/Write	0 – Disable 1 – Enable (also resets WC timer)
B5	STAT_1	Read only	00 – Ready 01 – Charge in progress 10 – Charge done 11 – Fault
B4	STAT_0	Read only	
B3	FAULT_3	Read only	0000 – Normal 0001 – Input OVP 0010 – Input UVLO 0011 – Sleep 0100 – Battery Temperature (TS) Fault 0101 – Battery OVP 0110 – Thermal Shutdown 0111 – Timer Fault 1000 – No Battery connected 1001 – ISET short 1010 – Input Fault and LDO low
B2	FAULT_2	Read only	
B1	FAULT_1	Read only	
B0(LSB)	FAULT_0	Read only	

WD_FAULT ‘0’ indicates no watch dog fault has occurred, where a ‘1’ indicates a fault has previously occurred.

WD_EN Enables or disables the internal watch dog timer. A ‘1’ enables the watch dog timer and a ‘0’ disables it. '1' is default for bq24251 only.

STAT Indicates the charge controller status.

FAULT Indicates the faults that have occurred. If multiple faults occurred, they can be read by sequentially addressing this register (e.g. reading the register 2 or more times). Once all faults have been read and the device is in a non-fault state, the fault register will show “Normal”. Regarding the "Input Fault & LDO Low" the IC indicates this if LDO is low and at the same time the input is below UVLO or coming out of UVLO with LDO still low.

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Register #2
Memory location: 01, Reset state: xxxx 1100

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	Reset	Write only	Write: 1 – Reset all registers to default values 0 – No effect
B6	$I_{IN_ILIMIT_2}$	Read/Write	000 – USB2.0 host with 100mA current limit 001 – USB3.0 host with 150mA current limit 010 – USB2.0 host with 500mA current limit 011 – USB3.0 host with 900mA current limit 100 – Charger with 1500mA current limit 101 – Charger with 2000mA current limit 110 – External ILIM current limit 111- No input current limit with internal clamp at 3A (PTM MODE)
B5	$I_{IN_ILIMIT_1}$	Read/Write	
B4	$I_{IN_ILIMIT_0}$	Read/Write	
B3	EN_STAT	Read/Write	0 – Disable STAT function 1 – Enable STAT function
B2	EN_TERM	Read/Write	0 – Disable charge termination 1 – Enable charge termination
B1	$\overline{CE}$	Read/Write	0 – Charging is enabled 1 – Charging is disabled
B0 (LSB)	HZ_MODE	Read/Write	0 – Not high impedance mode 1 – High impedance mode

I_{IN_LIMIT} Sets the input current limit level. When in host mode this register sets the regulation level. However, when in standalone mode (e.g. no I^2C writes have occurred after power up or the WD timer has expired) the external resistor setting for I_{ILIM} sets the regulation level.

EN_STAT Enables and disables the STAT pin. When set to a ‘1’ the STAT pin is enabled and function normally. When set to a ‘0’ the STAT pin is disabled and the open drain FET is in HiZ mode.

EN_TERM Enables and disables the termination function in the charge controller. When set to a ‘1’ the termination function will be enabled. When set to a ‘0’ the termination function will be disabled. When termination is disabled, there are no indications of the charger terminating (i.e. STAT pin or STAT registers).

$\overline{CE}$ The charge enable bit which enables or disables the charge function. When set to a ‘0’, the charger operates normally. With a valid input, when set the bit to a ‘1’, the charger is disabled by turning off the BAT FET between SYS and BAT. The SYS pin continues to stay active via the switch mode controller. Without a valid input, When set the bit to a '1', the BAT FET will not be turned off.

HZ_MODE Sets the charger IC into low power standby mode. When set to a ‘1’, the switch mode controller is disabled but the BAT FET remains ON to keep the system powered. When set to a ‘0’, the charger operates normally.

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Register #3
Memory location: 02, Reset state: 1000 1111

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	VBATREG_5 (1)	Read/Write	Battery Regulation Voltage: 640mV (default 1)
B6	VBATREG_4 (1)	Read/Write	Battery Regulation Voltage: 320mV (default 0)
B5	VBATREG_3 (1)	Read/Write	Battery Regulation Voltage: 160mV (default 0)
B4	VBATREG_2 (1)	Read/Write	Battery Regulation Voltage: 80mV (default 0)
B3	VBATREG_1 (1)	Read/Write	Battery Regulation Voltage: 40mV (default 1)
B2	VBATREG_0 (1)	Read/Write	Battery Regulation Voltage: 20mV (default 1)
B1(4)(5)	USB_DET_1/EN1	Read Only	Return USB detection result or pin EN1/EN0 status – 00 – DCP detected / EN1=0, EN0=0 01 – CDP detected / EN1=0, EN0=1 10 – SDP detected / EN1=1, EN0=0 11 – Apple/TT or non-standard adaptor detected / EN1=1, EN0=1
B0(LSB)	USB_DET_0/EN0	Read Only	

(1) Charge voltage range is 3.5V—4.44V with the offset of 3.5V and step of 20mV (default 4.2V)

V_{BATREG} Sets the battery regulation voltage

USB_DET/EN Provides status of the D+/D– detection-results for spins that include the D+/D– pins or the state of EN1/EN2 for spins that include the EN1/EN2 pins

Register #4
Memory location: 03, Reset state: 1111 1000

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	ICHG_4 (1) (2)	Read/Write	Charge current 800mA – (default 1)
B6	ICHG_3 (1) (2)	Read/Write	Charge current: 400mA – (default 1)
B5	ICHG_2 (1) (2)	Read/Write	Charge current: 200mA – (default 1)
B4	ICHG_1 (1) (2)	Read/Write	Charge current: 100mA – (default 1)
B3	ICHG_0 (1) (2)	Read/Write	Charge current: 50mA – (default 1)
B2	ITERM_2 (3)	Read/Write	Termination current sense threshold: 100mA (default 0)
B1	ITERM_1 (3)	Read/Write	Termination current sense threshold: 50mA (default 0)
B0(LSB)	ITERM_0 (3)	Read/Write	Termination current sense threshold: 25mA (default 0)

(1) Charge current offset is 500 mA and default charge current is external (maximum is 2.0A)
(2) When all bits are 1's, it is external ISET charging mode
(3) Termination threshold voltage offset is 50mA. The default termination current is 50mA if the charge is selected from I2C. Otherwise, termination is set to 10% of ICHG in external I_set mode with +/-10% accuracy.

I_{CHG} Sets the charge current regulation

I_{TERM} Sets the current level at which the charger will terminate

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Register #5
Memory location: 04, Reset state: xx00 x010

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	LOOP_STATUS1 (1)	Read Only	00 – No loop is active that slows down timer 01 – V_{IN_DPM} regulation loop is active 10 – Input current limit loop is active 11 – Thermal regulation loop is active
B6	LOOP_STATUS0 (1)	Read Only	
B5	LOW_CHG	Read/Write	0 – Normal charge current set by 03h 1 – Low charge current setting 330mA (default 0)
B4	DPDM_EN	Read/Write	0 – Bit returns to 0 after D+/D– detection is performed 1 – Force D+/D– detection (default 0)
B3	CE_STATUS	Read Only	0 – CE low 1 – CE high
B2	V_{INDPM_2} (2)	Read/Write	Input $V_{IN\text{-}DPM}$ voltage: 320mV (default 0)
B1	V_{INDPM_1} (2)	Read/Write	Input $V_{IN\text{-}DPM}$ voltage: 160mV (default 1)
B0(LSB)	V_{INDPM_0} (2)	Read/Write	Input $V_{IN\text{-}DPM}$ voltage: 80mV (default 0)

(1) LOOP_STATUS bits show if there are any loop is active that slow down the safety timer. If a status occurs, these bits announce the status and do not clear until read. If more than one occurs, the first one is shown.
(2) VIN-DPM voltage offset is 4.20V and default V_{IN_DPM} threshold is 4.36V.

LOOP_STATUS Provides the status of the active regulation loop. The charge controller allows for only one loop can regulate at a time.

LOW_CHG When set to a ‘1’, the charge current is reduced 330mA independent of the charge current setting in register 0x03. When set to ‘0’, the charge current is set by register 0x03.

DPDM_EN Forces a D+/D- detection routine to be executed once a ‘1’ is written. This is independent of the input being supplied.

CE_STATUS Provides the status of the $\overline{CE}$ pin level. If the $\overline{CE}$ pin is forced high, this bit returns a ‘1’. If the $\overline{CE}$ pin is forced low, this bit returns a ‘0’.

V_{INDPM} Sets the input VDPM level.

Register #6
Memory location: 05, Reset state: 101x 1xxx

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	2XTMR_EN	Read/Write	0 – Timer not slowed at any time 1 – Timer slowed by 2x when in thermal regulation, V_{IN_DPM} or DPPM (default 1)
B6	TMR_1	Read/Write	Safety Timer Time Limit 00 – 0.75 hour fast charge 01 – 6 hour fast charge (default 01) 10 – 9 hour fast charge 11 – Disable safety timers
B5	TMR_2	Read/Write	
B4	SYSOFF	Read/Write	0 – SYSOFF disabled 1 – SYSOFF enabled
B3	TS_EN	Read/Write	0 – TS function disabled 1 – TS function enabled (default 1)
B2	TS_STAT2	Read only	TS Fault Mode: 000 – Normal, No TS fault 100 – TS temp < T_{COLD} (Charging suspended for JEITA and Standard TS) 101 – T_{FREEZE} < TS temp < T_{COLD} (Charging at 3.9V and 100mA and only for PSE option only) 110 – TS temp < T_{FREEZE} (Charging suspended for PSE option only) 111 – TS open (TS disabled)
B1	TS_STAT1	Read only	
B0(LSB)	TS_STAT0	Read only	

2xTMR_EN When set to a ‘1’, the 2x Timer function is enabled and allows for the timer to be extended if a condition occurs where the charge current is reduced (i.e. V_{IN_DPM}, thermal regulation, etc.). When set to a ‘0’, this function is disabled and the normal timer will always be executed independent of the current reduce conditions.

SYSOFF When set to a ‘1’ and the input is removed, the internal battery FET is turned off in order to reduce the leakage from the BAT pin to less than 1µA. Note that this disconnects the battery from the system. When set to a ‘0’, this function is disabled.

TS_EN Enables and disables the TS function. When set to a ‘0’ the TS function is disabled otherwise it is enabled. Only applies to spins that have a TS pin.

TS_STAT Provides status of the TS pin state for spins that have a TS pin.

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Register #7
Memory location: 06, Reset state: 1110 0000

BIT	NAME	READ/WRITE	FUNCTION
B7(MSB)	VOVP_2	Read/Write	OVP voltage: 000 – 6.0V; 001 – 6.5V; 010 – 7.0V; 011 – 8.0V 100 – 9.0V; 101 – 9.5V; 110 – 10.0V; 111 –10.5V
B6	VOVP_1	Read/Write	
B5	VOVP_0	Read/Write	
B4	CLR_VDP	Read/Write	0 – Keep D+ voltage source on during DBP charging 1 – Turn off D+ voltage source to release D+ line
B3	FORCE_BAT DET	Read/Write	0 – Enter the battery detection routine only if TERM is true or Force PTM is true 1 – Enter the battery detection routine
B2	FORCE_PTM	Read/Write	0 – PTM mode is disabled 1 – PTM mode is enabled
B1	N/A	Read/Write	Not available. Keep set to 0.
B0(LSB)	N/A	Read/Write	Not available. Keep set to 0.

VOVP Sets the OVP level

CLR_VDP When the D+/D– detection has finished, some cases require the D+ pin to force a voltage of 0.6V. This bit allows the system to clear the voltage prior to any communication on the D+/D– pins. A ‘1’ clears the voltage at the D+ pin if present.

FORCE_BATDET Forces battery detection and provides status of the battery presence. A logic ‘1’ enables this function.

FORCE_PTM Puts the device in production test mode (PTM) where the input current limit is disabled. Note that a battery must not be present prior to using this function. Otherwise the function will not be allowed to execute. A logic ‘1’ enables the PTM function

9 Application and Implementation

9.1 Application Information

The bq24250C is a high-efficiency switch-mode charger. The device has integrated power FETs that are able to charge at up to a 2-A charging rate, and an integrated 50-mA LDO. In I2C mode, the device has programmable battery charge voltage (VBATREG), charge current (ICHG), input current limit (ILIM), and input over-voltage protection threshold (VOVP). The charge current and the input current limit are programmed using external resistors (RISET and RILIM) connected from the ISET and ILIM pins to ground. The range of these resistors can be found in the datasheet. Both of these currents can be programmed up to 2 A. The device also has complete system-level protection such as input under-voltage lockout (UVLO), input over-voltage protection (OVP), battery OVP, sleep mode, thermal regulation and thermal shutdown, voltage-based NTC monitoring input, and safety timers.

9.2 Typical Application

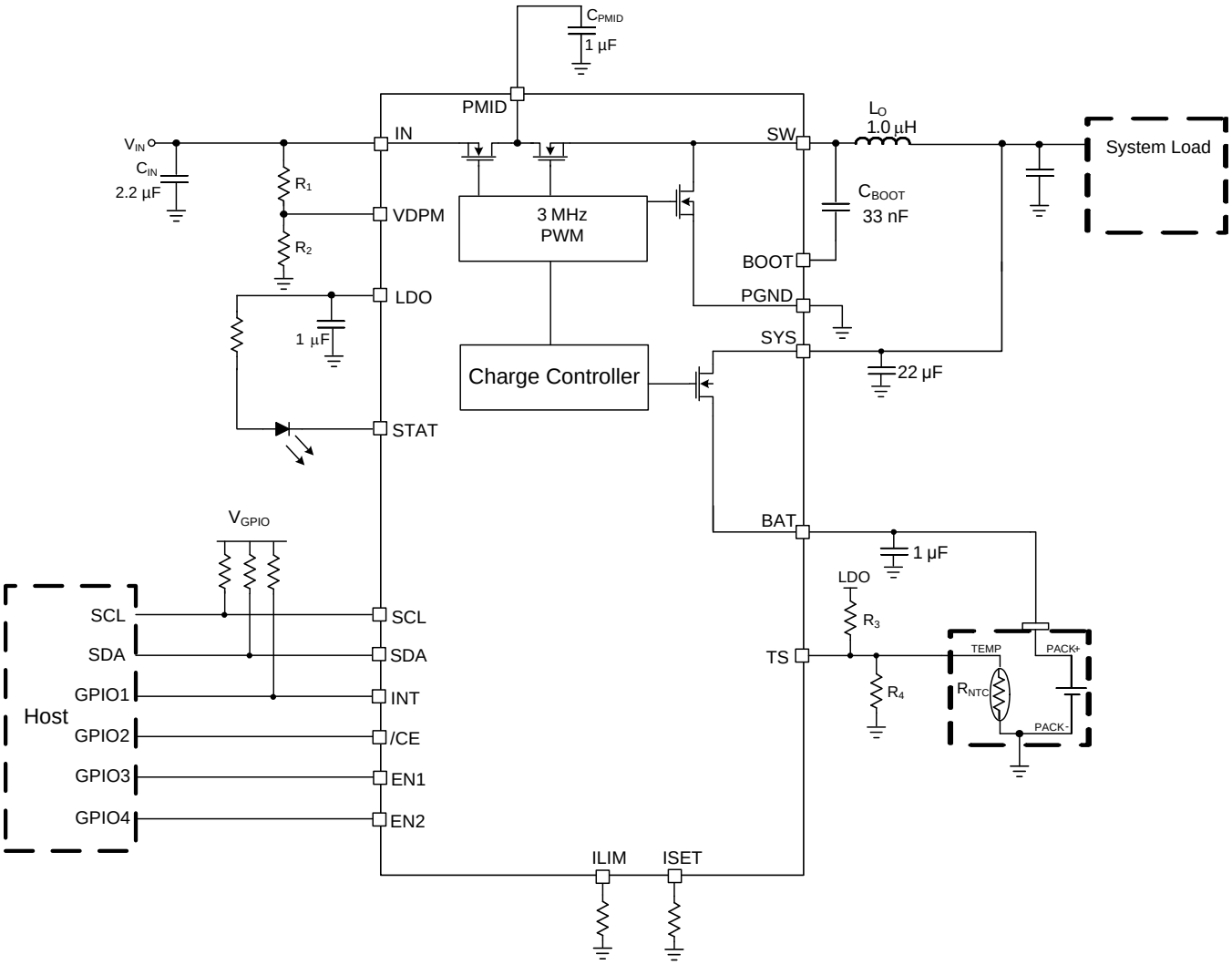

Figure 27. bq24250C Typical Application Circuit

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Typical Application (continued)

9.2.1 Design Requirements

Use the following typical application design procedure to select external components values for the bq24250C device.

Table 4. Design Parameters

SPECIFICATION	TEST CONDITION	MIN	TYP	MAX	UNIT
Input DC voltage, VIN	Recommended input voltage range	4.35		10.5	V
Input current	Recommended input current range			2	A
Charge current	Fast charge current range	0.5		2	A
Output regulation voltage	Standalone mode or I2C default mode		4.2		V
Output regulation voltage	I2C host mode: operating in voltage regulation, programmable range	3.5		4.44	V
LDO	LDO output voltage		4.9		V

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The inductor selection depends on the application requirements. The bq24250C is designed to operate at around 1 µH. The value will have an effect on efficiency, and the ripple requirements, stability of the charger, package size, and DCR of the inductor. The 1µH inductor provides a good tradeoff between size and efficiency and ripple.

Once the inductance has been selected, the peak current is needed in order to choose the saturation current rating of the inductor. Make sure that the saturation current is always greater than or equal to the calculated IPEAK. The following equation can be used to calculate the current ripple:

$$\Delta I_L = \{VBAT\ (VIN - VBAT)\}/(VIN \times f s \times L) \quad (6)$$

Then use current ripple to calculate the peak current as follows:

$$I_{PEAK} = Load \times (1 + \Delta I_L/2) \quad (7)$$

In this design example, the regulation voltage is set to 4.2V, the input voltage is 5V and the inductance is selected to be 1µH. The maximum charge current that can be used in this application is 1A and can be set by I2C command. The peak current is needed in order to choose the saturation current rating of the inductor. Using equation 6 and 7, ΔI_L is calculated to be 0.224A and the inductor peak current is 1.112A. A 1µF BAT cap is needed and 22µF SYS cap is needed on the system trace.

The default settings for external fast charge current and external setting of current limit are chosen to be IFC=500mA and ILIM=1A. RISET and RILIM need to be calculated using equation 1 and 2 in the data sheet.

The fast charge current resistor (RISET) can be set as follows:

RISET=250/0.5A=500Ω

The input current limit resistor (RILIM) can be set as follows:

RILIM= 270/1A=270Ω

The external settings of VIN_DPM can be designed by calculating R1 and R2 according to equation 3 in this data sheet and the typical application circuit. VIN_DPM should be chosen first along with R1. VIN_DPM is chosen to be 4.48V and R1 is set to 274KΩ in this design example. Using equation 3, the value of R2 is calculated to be 100KΩ.

In this design example, the application needs to be JEITA compliant. Thus, T_{COLD} must be 0°C and T_{HOT} must be 60°C. If an NTC resistor is chosen such that the beta is 4500K and the nominal resistance is 13KΩ, the calculated R3 and R4 values are 5KΩ and 8.8KΩ respectively. These results are obtained from equation 4 and 5 in this data sheet.

9.2.3 Application Curves

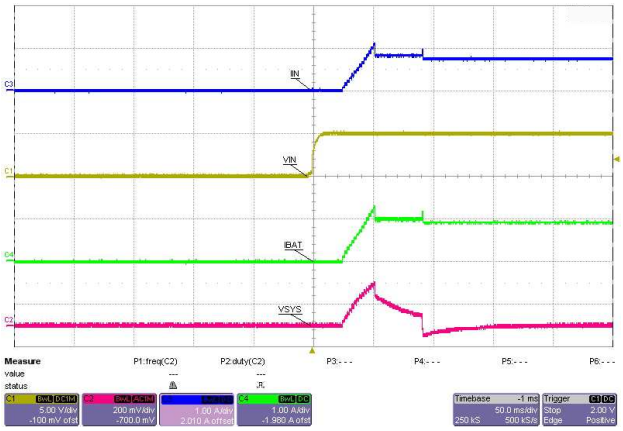

Figure 28. Startup

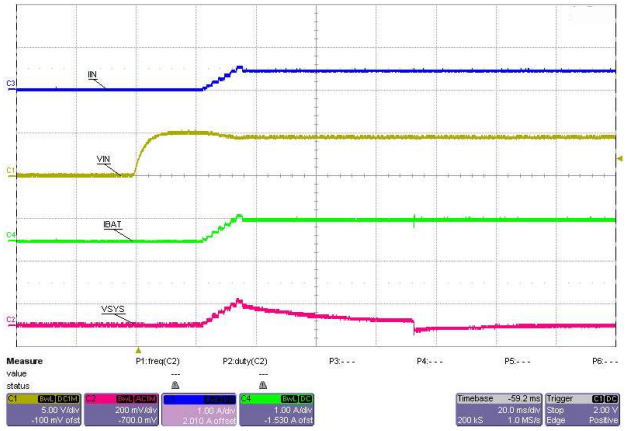

Figure 29. V_{DPM} Startup, 4.2 V

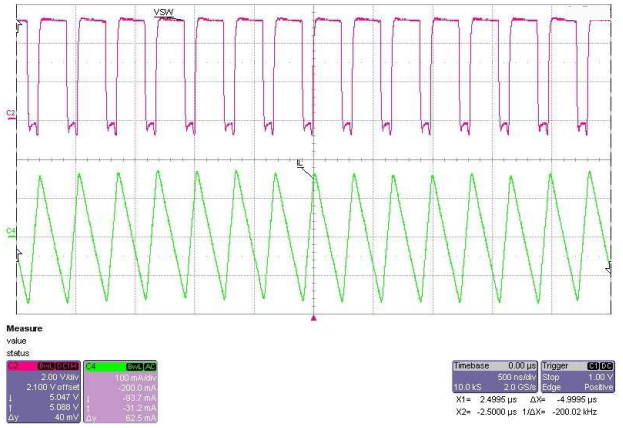

Figure 30. 1.0 µH CCM Operation

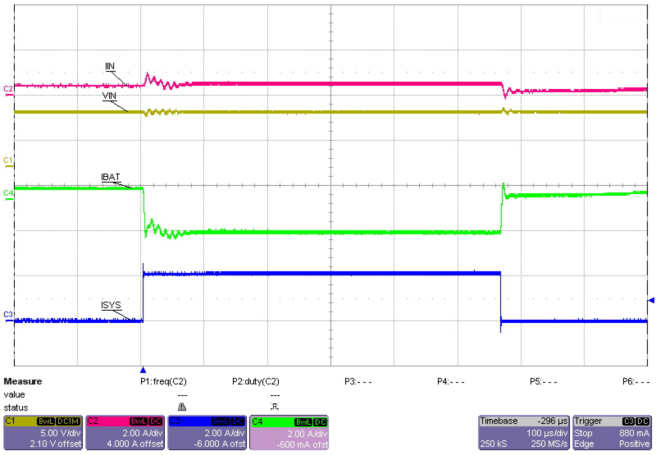

Figure 31. 2A Load Step Transient

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10 Power Supply Recommendations

The devices are designed to operate from an input voltage range between 4.35V and 10.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the bq24250C charger, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

1. Place the BOOT, PMID, IN, BAT, and LDO capacitors as close as possible to the IC for optimal performance.
2. Connect the inductor as close as possible to the SW pin, and the SYS cap as close as possible to the inductor minimizing noise in the path.
3. Place a 1-μF PMID capacitor as close as possible to the PMID and PGND pins, making the high frequency current loop area as small as possible.
4. The local bypass capacitor from SYS to GND must be connected between the SYS pin and PGND of the IC. This minimizes the current path loop area from the SW pin through the LC filter and back to the PGND pin.
5. Place all decoupling capacitors close to their respective IC pins and as close as possible to PGND (do not place components such that routing interrupts power-stage currents). All small control signals must be routed away from the high-current paths.
6. To reduce noise coupling, use a ground plane if possible, to isolate the noisy traces from spreading its noise all over the board. Put vias inside the PGND pads for the IC.
7. The high-current charge paths into IN, Micro-USB, BAT, SYS, and from the SW pins must be sized appropriately for the maximum charge current to avoid voltage drops in these traces.
8. For high-current applications, the balls for the power paths must be connected to as much copper in the board as possible. This allows better thermal performance because the board conducts heat away from the IC.

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11.2 Board Layout

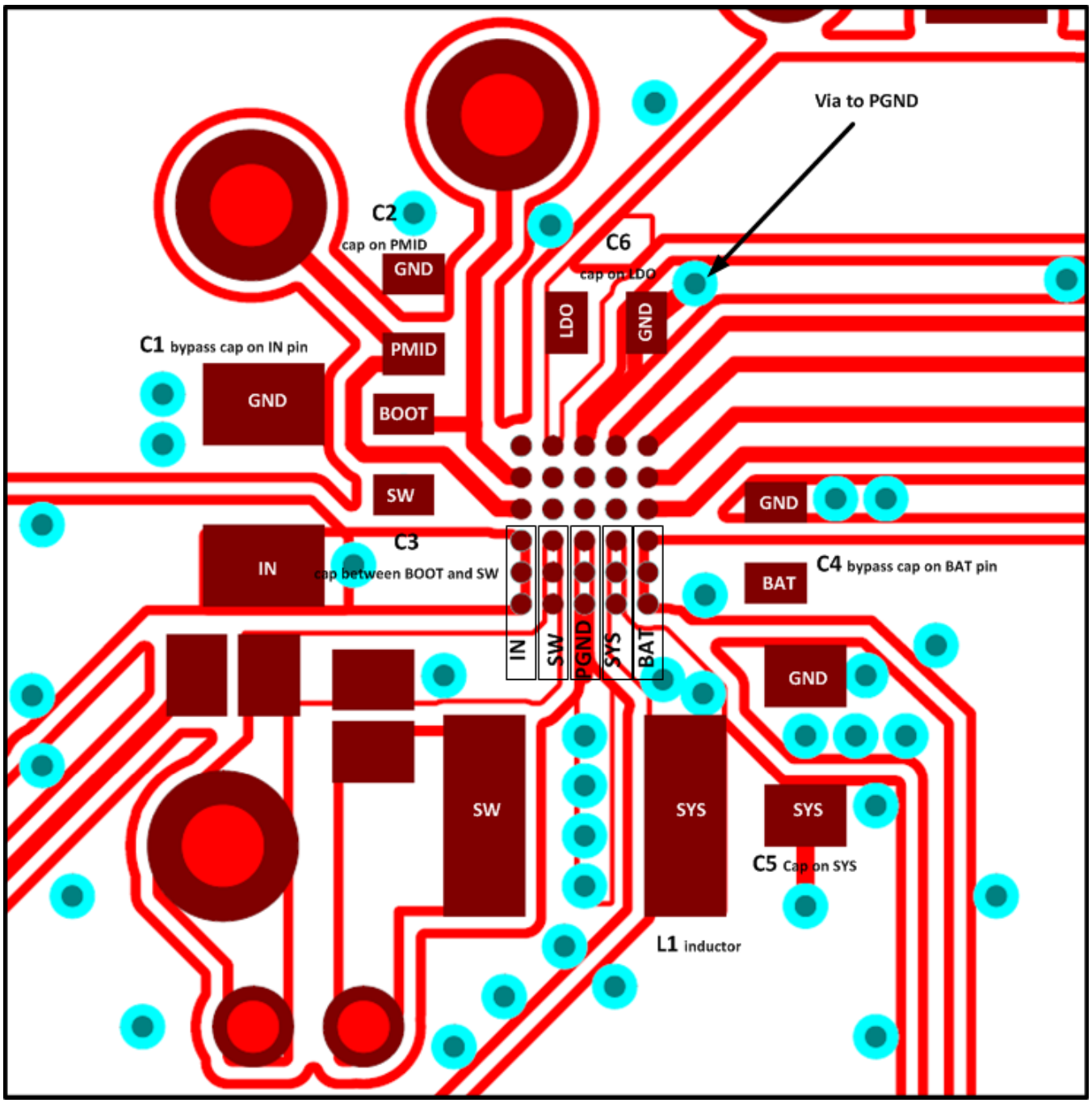

Figure 32. Recommended bq24250C PCB Layout for WCSP Package

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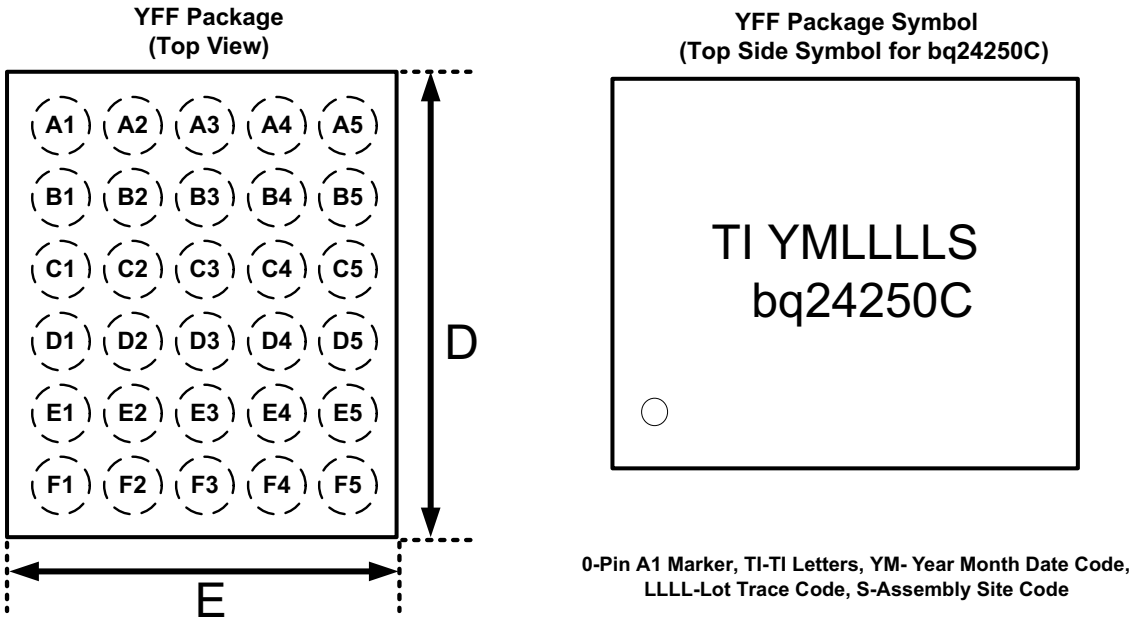
11.3 Package Summary



The bq24250C device is available in a 30-bump chip scale package (YFF, NanoFree™). The package dimensions are:

D – 2.427mm ±0.035mm

E – 2.027mm ±0.035mm

12 Device and Documentation Support

12.1 Trademarks

NanoFree is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24250CYFFR	ACTIVE	DSBGA	YFF	30	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24250C	Samples
BQ24250CYFFT	ACTIVE	DSBGA	YFF	30	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24250C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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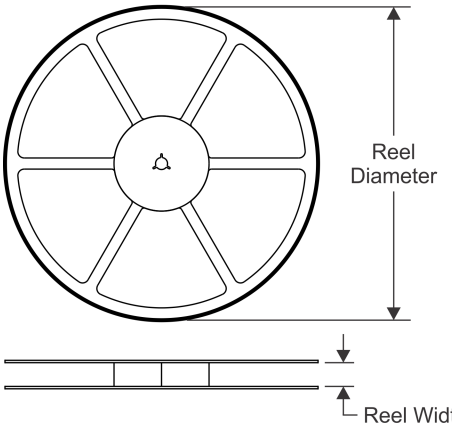
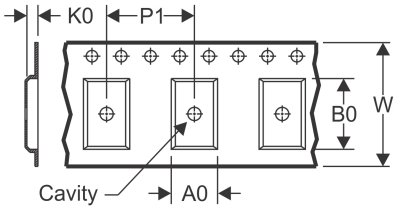
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

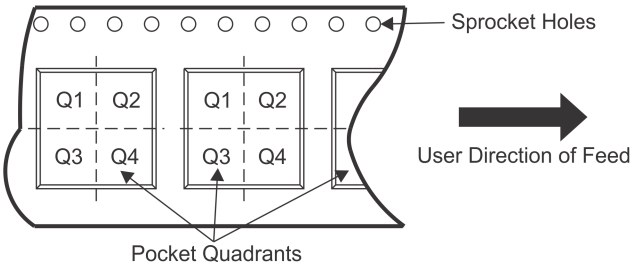


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

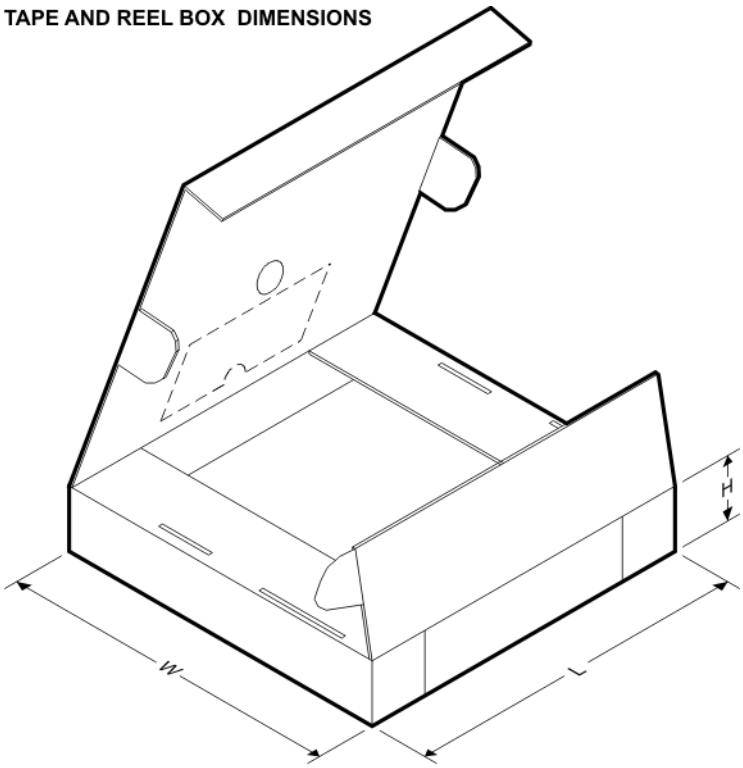
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

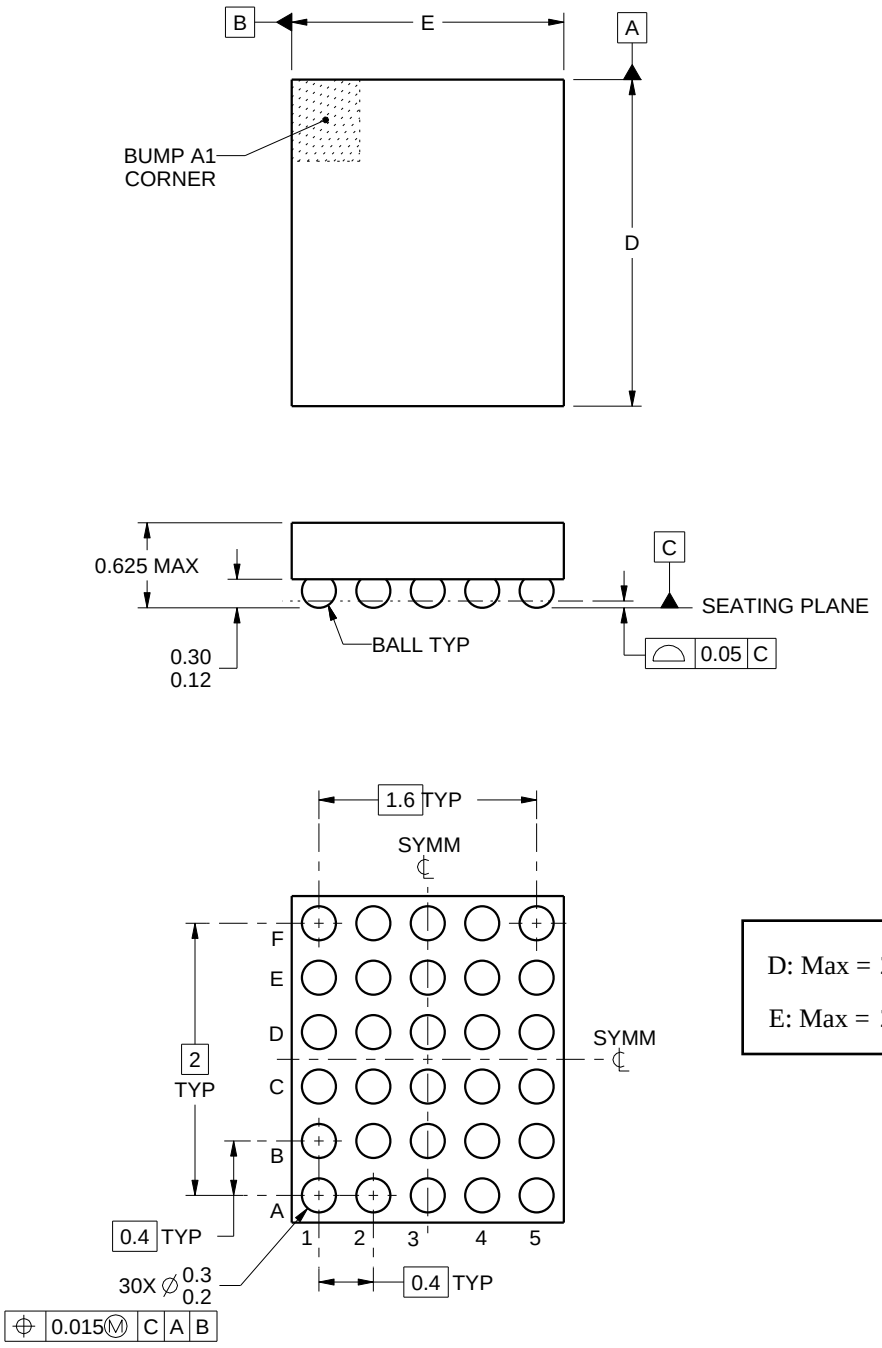
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24250CYFFR	DSBGA	YFF	30	3000	180.0	8.4	2.09	2.59	0.78	4.0	8.0	Q1
BQ24250CYFFT	DSBGA	YFF	30	250	180.0	8.4	2.09	2.59	0.78	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24250CYFFR	DSBGA	YFF	30	3000	182.0	182.0	20.0
BQ24250CYFFT	DSBGA	YFF	30	250	182.0	182.0	20.0



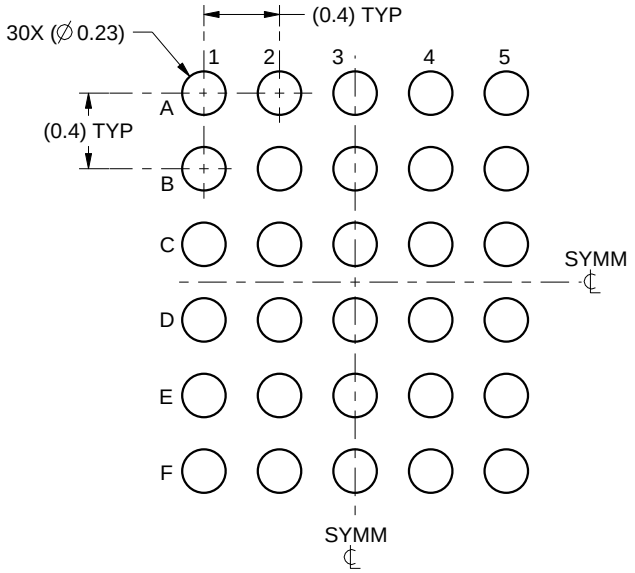
D: Max = 2.418 mm, Min =2.357 mm

E: Max = 2.018 mm, Min =1.957 mm

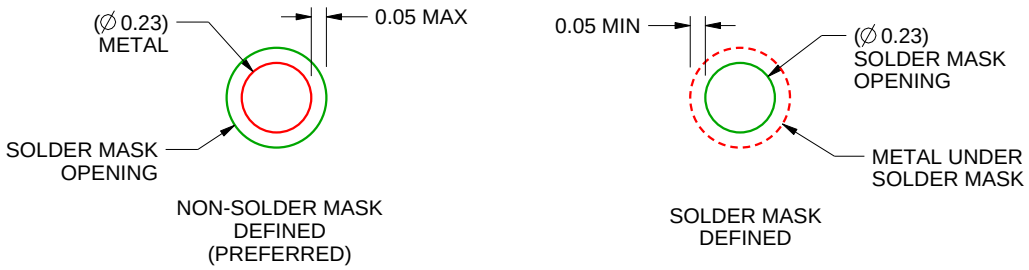
4219433/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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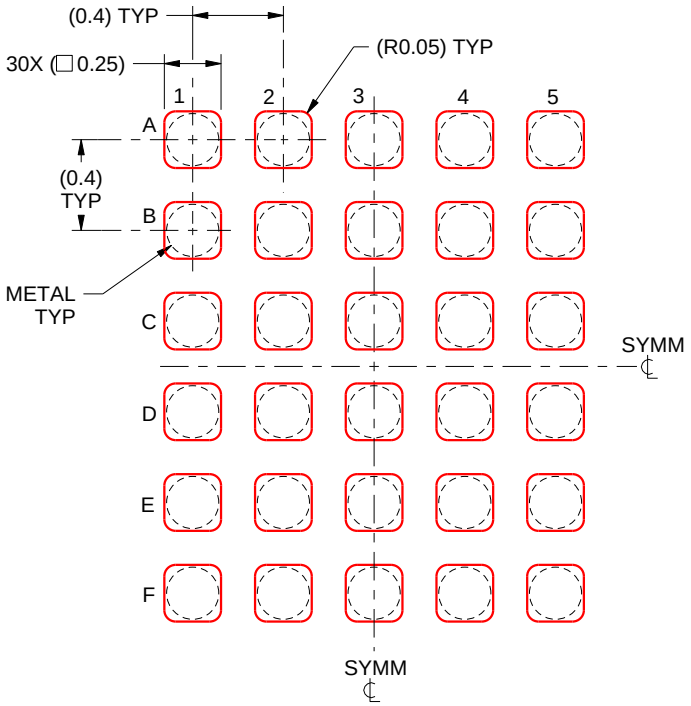
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219433/A 03/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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