



ALPHA & OMEGA
SEMICONDUCTOR

AO4474

N-Channel Enhancement Mode Field Effect Transistor

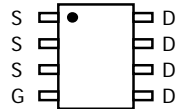


General Description

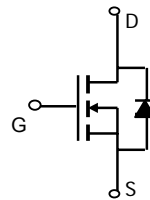
The AO4474 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. This device is suitable for use as a high side switch in SMPS and general purpose applications. *Standard Product AO4474 is Pb-free (meets ROHS & Sony 259 specifications). AO4474L is a Green Product ordering option. AO4474 and AO4474L are electrically identical.*

Features

V_{DS} (V) = 30V
 I_D = 13.4A (V_{GS} = 10V)
 $R_{DS(ON)}$ < 11.5m Ω (V_{GS} = 10V)
 $R_{DS(ON)}$ < 13.5m Ω (V_{GS} = 4.5V)



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^A	I_{DSM}	$T_A=25^\circ\text{C}$	13.4
		$T_A=70^\circ\text{C}$	10.7
Pulsed Drain Current ^B	I_{DM}	60	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3.7
		$T_A=70^\circ\text{C}$	2.4
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units	
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$	28	34	$^\circ\text{C/W}$
		Steady-State	57	71	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	16	23	$^\circ\text{C/W}$	

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±12V			0.1	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	1.55	2.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	60			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =13.4A T _J =125°C		9.5 16.2	11.5 18	mΩ
		V _{GS} =4.5V, I _D =10A		11	13.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =13.4A		40		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.74	1.0	V
I _S	Maximum Body-Diode Continuous Current				5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		1210	1452	pF
C _{oss}	Output Capacitance			330		pF
C _{riss}	Reverse Transfer Capacitance			85		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.2	1.6	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =13.4A		22	28	nC
Q _g (4.5V)	Total Gate Charge			10		nC
Q _{gs}	Gate Source Charge			3.7		nC
Q _{gd}	Gate Drain Charge			2.7		nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =15V, R _L =1.1Ω, R _{GEN} =3Ω		10		ns
t _r	Turn-On Rise Time			6.3		ns
t _{D(off)}	Turn-Off Delay Time			21		ns
t _f	Turn-Off Fall Time			2.8		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =13.4A, dI/dt=100A/μs		36	45	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =13.4A, dI/dt=100A/μs		47		nC

A: The value of R_{θJA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 ms pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

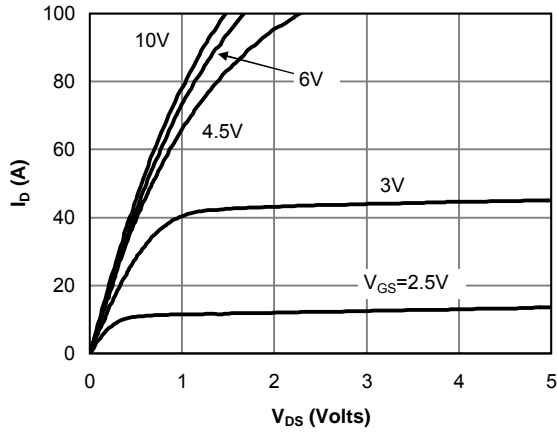


Fig 1: On-Region Characteristics

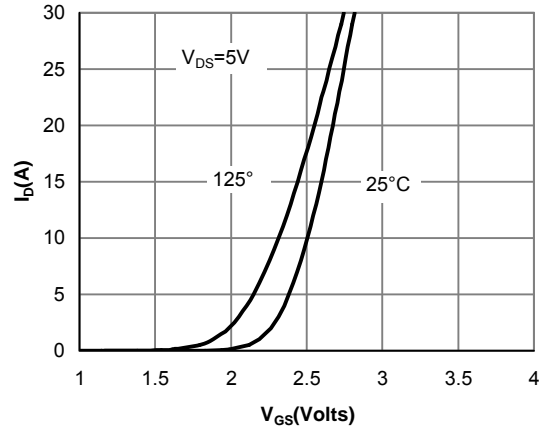


Figure 2: Transfer Characteristics

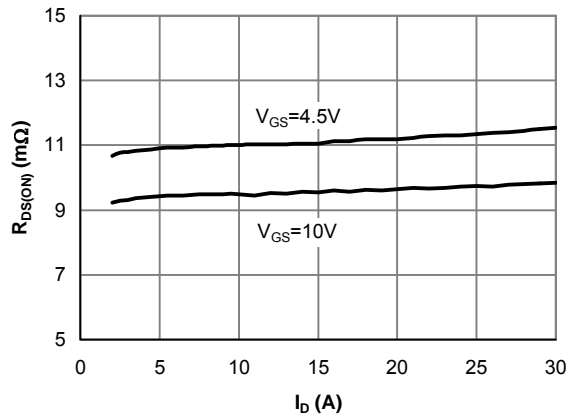


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

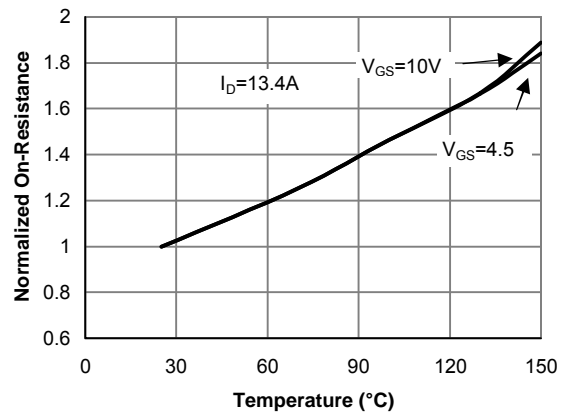


Figure 4: On-Resistance vs. Junction Temperature

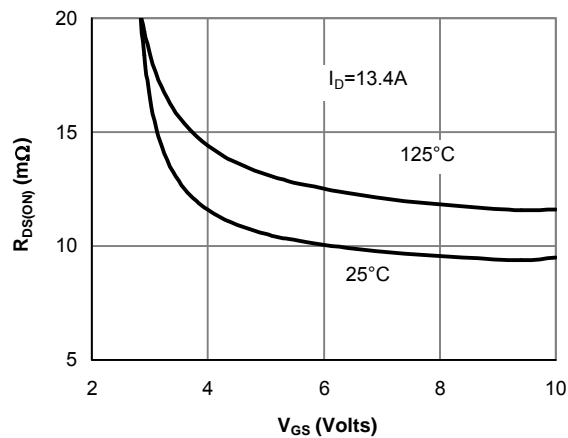


Figure 5: On-Resistance vs. Gate-Source Voltage

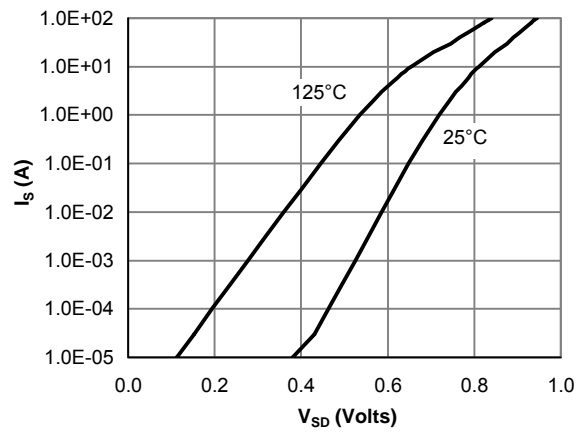


Figure 6: Body-Diode Characteristics

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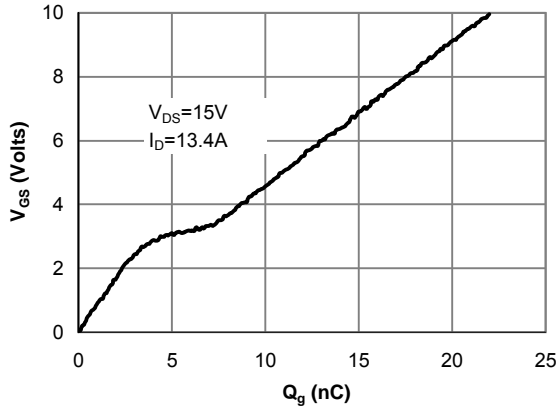


Figure 7: Gate-Charge Characteristics

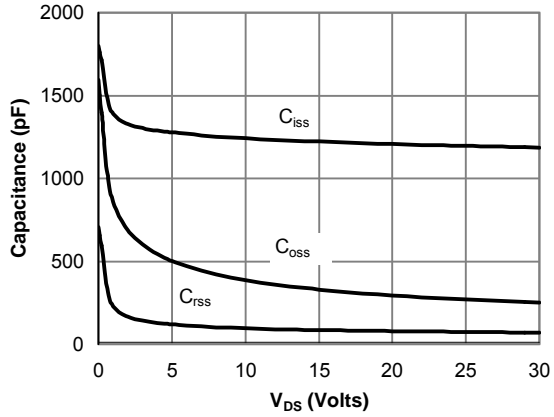


Figure 8: Capacitance Characteristics

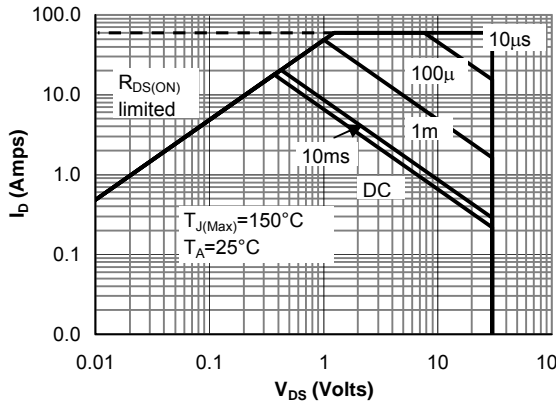


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

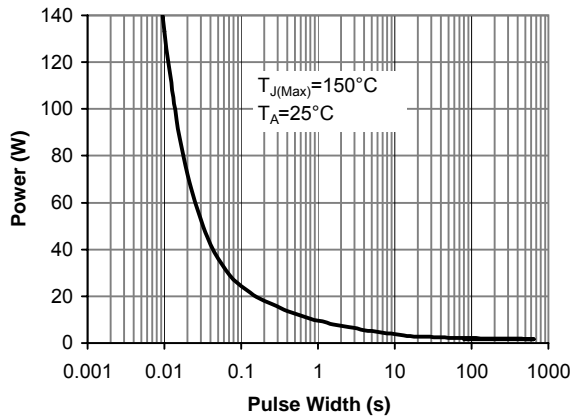


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note G)

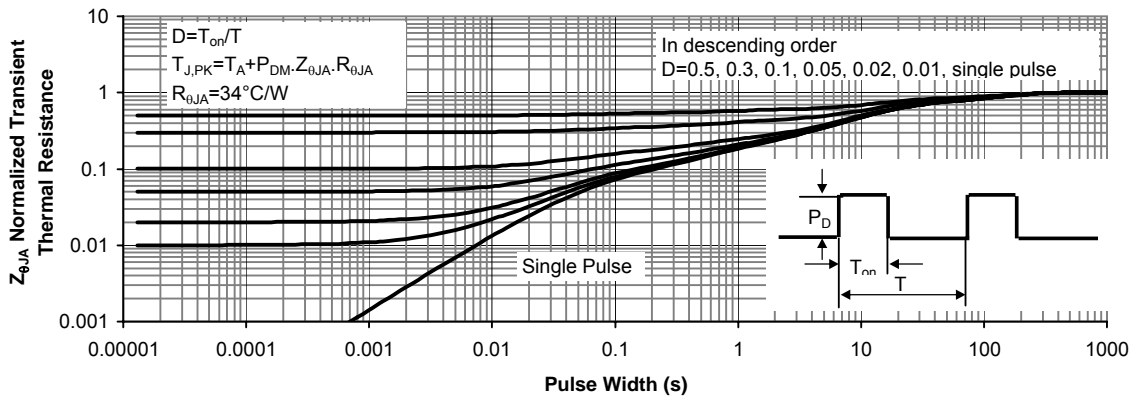


Figure 11: Normalized Maximum Transient Thermal Impedance (Note G)