



STV160NF02LA

N-CHANNEL 20V - 0.0018Ω - 160A PowerSO-10

STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STV160NF02LA	20 V	< 0.0027 Ω	160 A

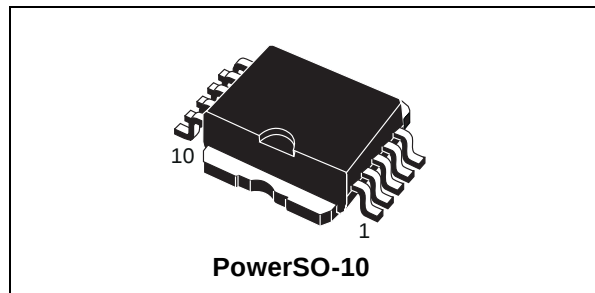
- TYPICAL R_{DS(on)} = 0.0018 Ω
- LOW THRESHOLD DRIVE
- ULTRA LOW ON-RESISTANCE
- ULTRA FAST SWITCHING
- 100% AVALANCHE TESTED
- VERY LOW GATE CHARGE
- LOW PROFILE, VERY LOW PARASITIC INDUCTANCE PowerSO-10 PACKAGE

DESCRIPTION

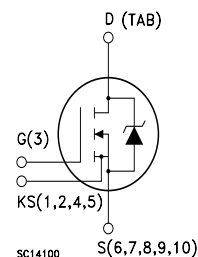
The **STV160NF02LA** represents the second generation of Application Specific STMicroelectronics well established STripFET™ process based on a very unique strip layout design. The resulting MOSFET shows unrivalled high packing density with ultra low on-resistance and superior switching characteristics. Process simplification also translates into improved manufacturing reproducibility. This device is particularly suitable for high current, low voltage switching application where efficiency is crucial

APPLICATIONS

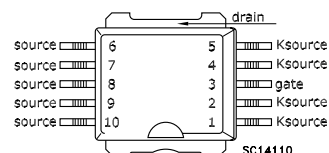
- BUCK CONVERTERS IN HIGH PERFORMANCE TELECOM AND VRMs DC-DC CONVERTERS



INTERNAL SCHEMATIC DIAGRAM



CONNECTION DIAGRAM (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	20	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	20	V
V _{GS}	Gate- source Voltage	± 15	V
I _D (**)	Drain Current (continuous) at T _C = 25°C	160	A
I _D	Drain Current (continuous) at T _C = 100°C	113	A
I _{DM} (●)	Drain Current (pulsed)	640	A
P _{TOT}	Total Dissipation at T _C = 25°C	210	W
	Derating Factor	1.4	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	330	mJ
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area
Note: Marking will be STV160NF02AL

(1) V_{DD} = 35V, I_D = 45A, R_G = 22Ω, L = 330μH, Starting T_j = 25°C
(**) Limited only maximum junction temperature allowed by PowerSO-10

STV160NF02LA

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.71	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	50	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	20			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 15 V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 80 A V _{GS} = 10 V, I _D = 45 A V _{GS} = 8 V, I _D = 80 A V _{GS} = 5 V, I _D = 40 A V _{GS} = 10 V, I _D =80 A; T _j = 175 °C V _{GS} = 8 V, I _D =80 A; T _j = 175 °C V _{GS} = 5 V, I _D =40 A; T _j = 125 °C		1.8 1.76 1.9 3.8	2.7 2.7 3.7 6.4 6 8 14	mΩ mΩ mΩ mΩ mΩ mΩ mΩ
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)} max, V _{GS} = 10V	160			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 80A		210		S
R _g	Gate resistance	V _{DS} = 0 V, f = 1 MHz, V _{GS} = 0		1.1		Ω
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 15 V, f = 1 MHz, V _{GS} = 0		5500 3210 750		pF pF pF
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 0 V, f = 1 MHz, V _{GS} = 0		8400 14500 5800		pF pF pF
L _S	Internal Source Inductance	From the Lead End (6mm from Package Body) to the Die Center		3		nH
L _D	Internal Drain Inductance		Not Available on Surface Mounting Package			

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 80\text{ A}$		30		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		650		ns
Q_g	Total Gate Charge	$V_{DD} = 16\text{ V}$, $I_D = 160\text{ A}$,		130	175	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10\text{ V}$		20		nC
Q_{gd}	Gate-Drain Charge			54		nC

SWITCHING OFF

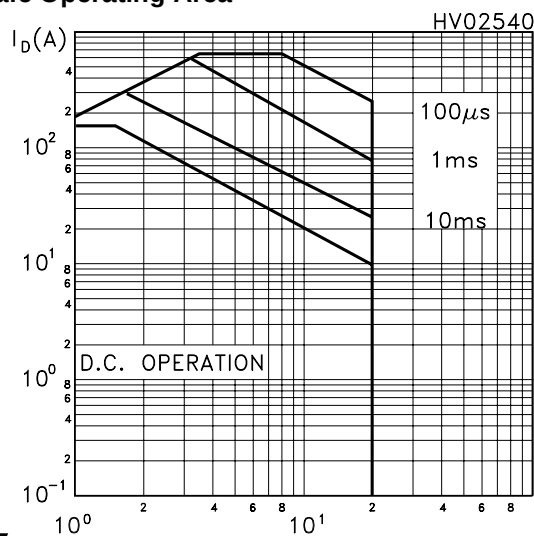
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 80\text{ A}$,		105		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		200		ns
$t_{d(off)}$	Turn-off Delay Time	$V_{clamp} = 16\text{ V}$, $I_D = 40\text{ A}$		90		ns
$t_{r(voff)}$	Off-voltage Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$		45		ns
t_f	Fall Time			125		ns
t_c	Cross-over Time			180		ns

SOURCE DRAIN DIODE

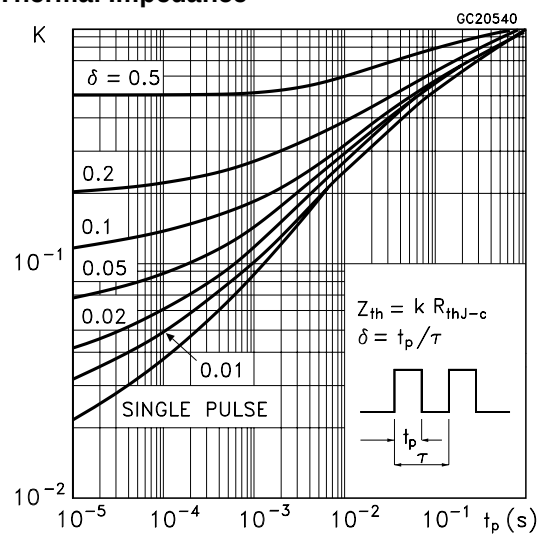
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				160	A
$I_{SDM(1)}$	Source-drain Current (pulsed)				640	A
$V_{SD(2)}$	Forward On Voltage	$I_{SD} = 160\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 160\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,		90		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 15\text{ V}$, $T_j = 25^\circ\text{C}$		225		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		5		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

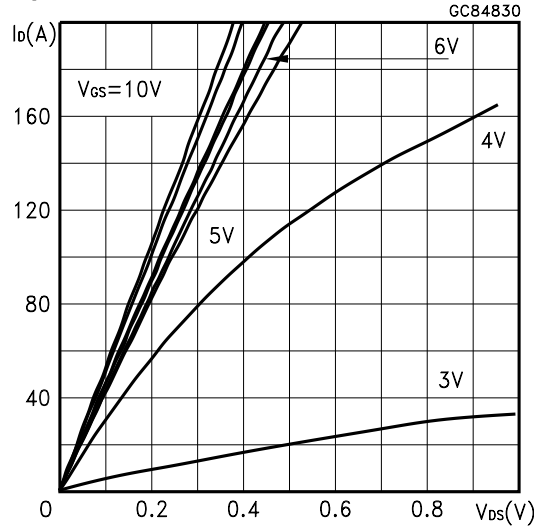
Safe Operating Area



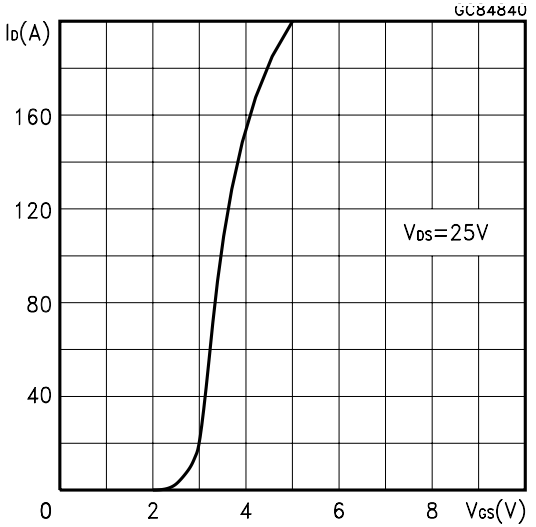
Thermal Impedance



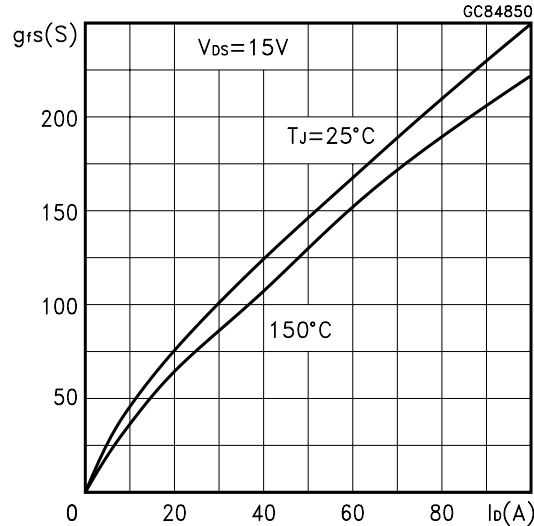
Output Characteristics



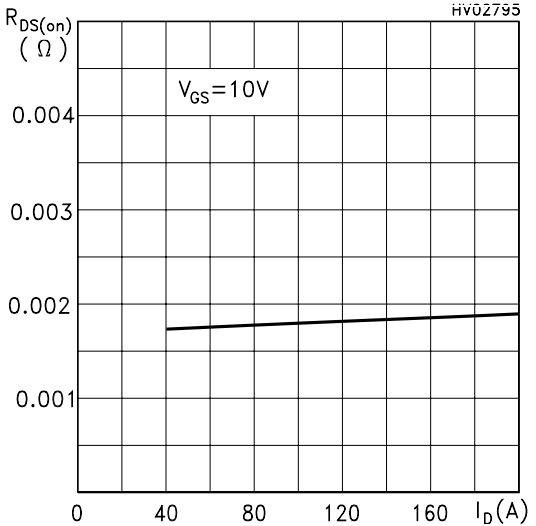
Transfer Characteristics



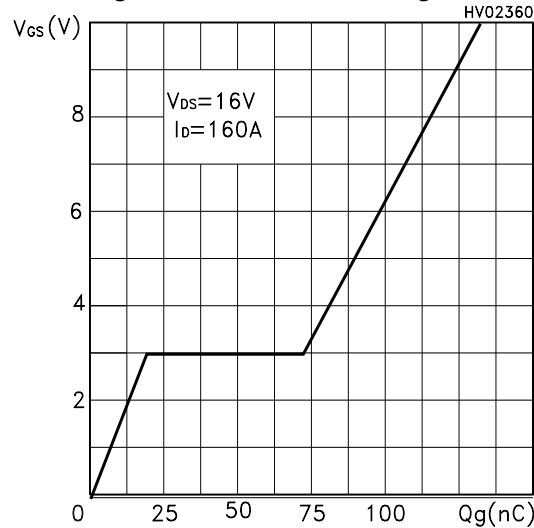
Transconductance



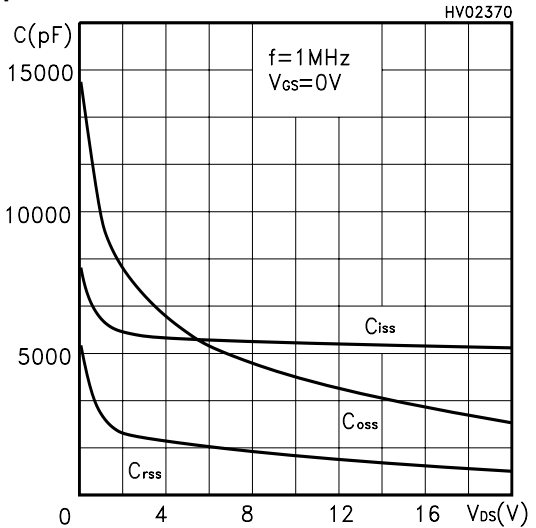
Static Drain-Source On Resistance



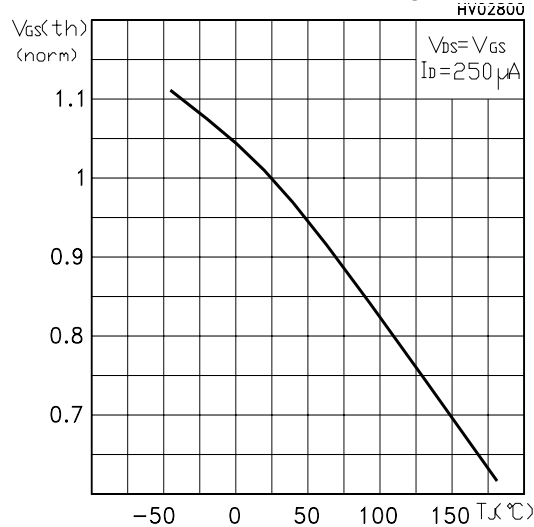
Gate Charge vs Gate-source Voltage



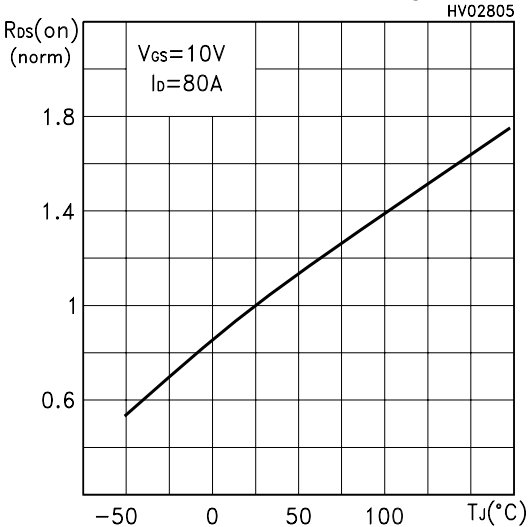
Capacitance Variations



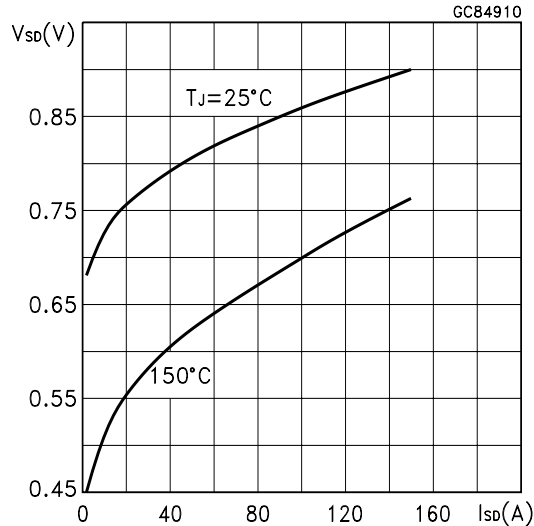
Normalized Gate Thereshold Voltage vs Temp.



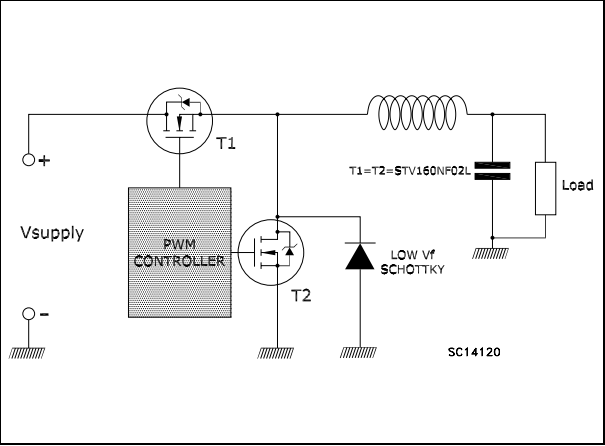
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Basic Schematic For Motherboard VRM With Synchronous Rectification



Basic Schematic Mosfets Switch Used In Secondary Side Of a Froward Convert

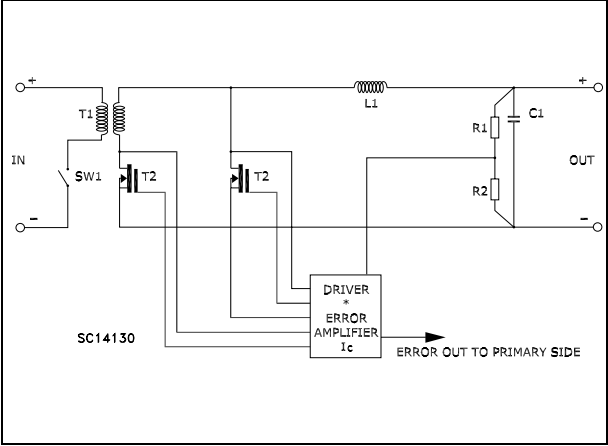


Fig. 1: Unclamped Inductive Load Test Circuit

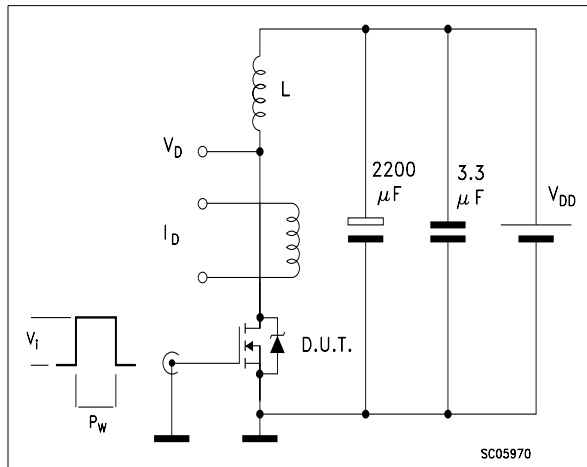


Fig. 2: Unclamped Inductive Waveform

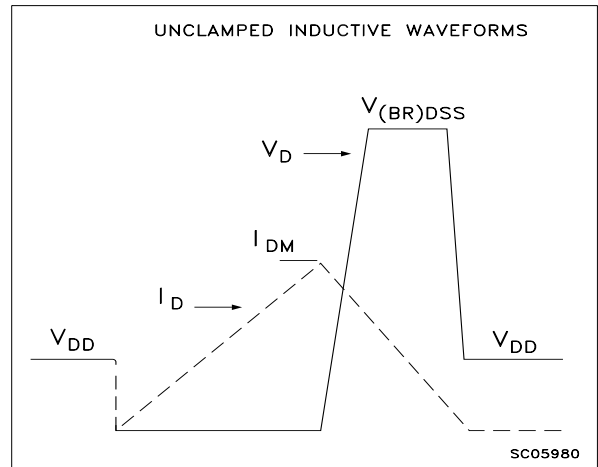


Fig. 3: Switching Times Test Circuit For Resistive Load

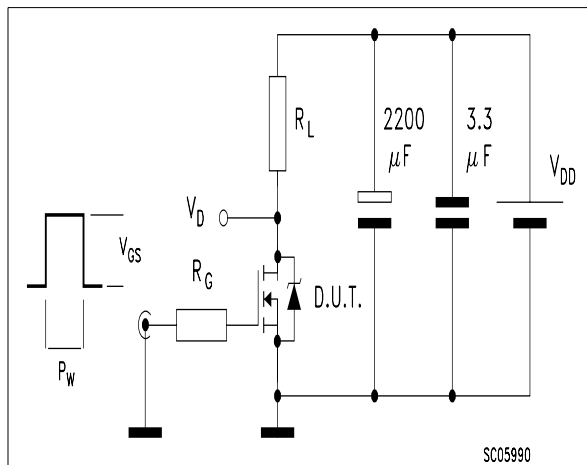


Fig. 4: Gate Charge test Circuit

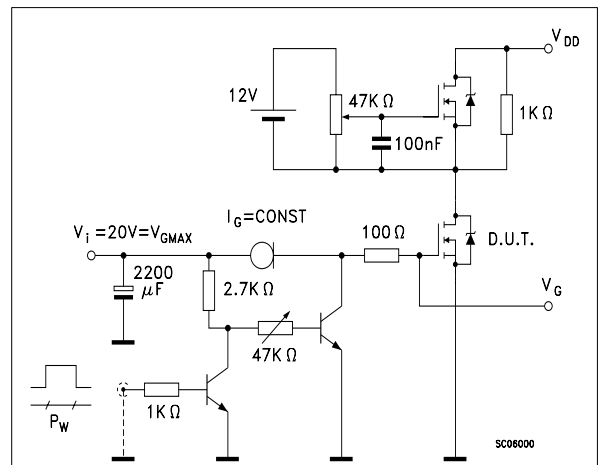
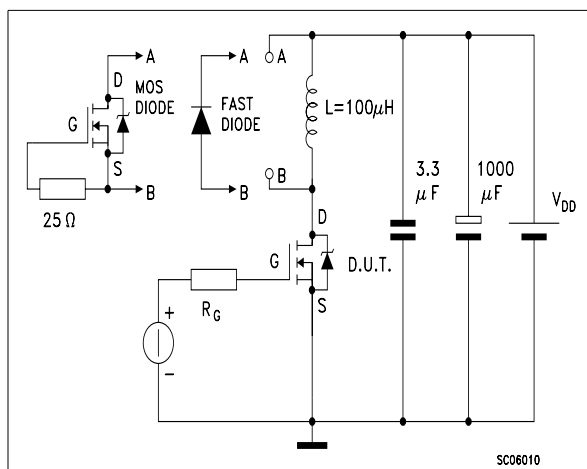
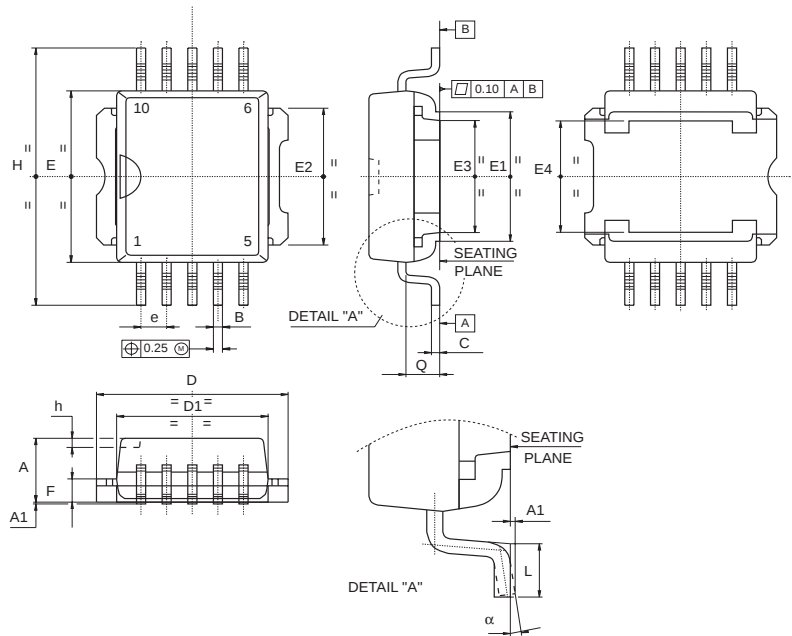


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



PowerSO-10 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
C	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
e		1.27			0.050	
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
F	1.25		1.35	0.049		0.053
h		0.50			0.002	
H	13.80		14.40	0.543		0.567
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			



0068039-C

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>