Integrated Multi-Channel DC-DC Converters for Panels

Description

The FP9928A offers a compact power supply solution to provide all voltages required by EPD panel. The FP9928A includes 2 high performance PFM DC-DC converters, one is for positive voltage and the other is for negative voltage used by EPD drivers, a VCOM buffer (unity-gain OPA), a positive charge pump and a negative charge pump to provide adjustable regulated output voltages.

The converters provide the regulated positive and negative supply voltage for the panel source driver ICs.

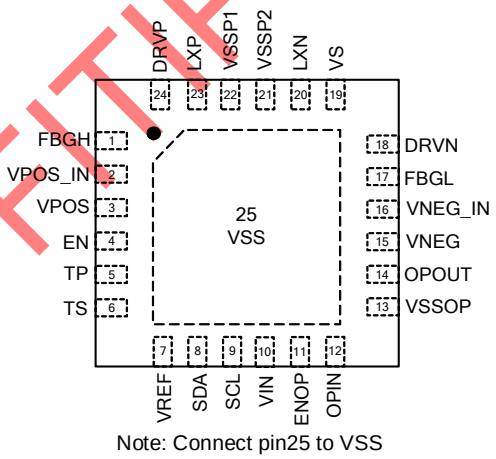
The positive charge pump controller provides regulated EPD gate-on voltage. The negative charge pump controller provides regulated EPD gate-off voltage.

Accurate back-plane biasing is provided by a linear amplifier and can be adjusted either by an external resistor or the I^{2}C interface. The VCOM driver can source or sink current depending on panel condition. For automatic VCOM adjustment in production line, VCOM can be set from -0.6V to -5V with 8 bit control through the serial interface.

The FP9928A provides precise temperature measurement function to monitor the panel temperature during operation. The FP9928A automatically updates the temperature every 60s.

Pin Assignments

WQ Package (TQFN-24)(4mm×4mm)



Note: Connect pin25 to VSS

Figure 1. Pin Assignment of FP9928A

Features

- High Efficiency
- Low Power Consumption
- 2.7V to 5.5V Input Supply Voltage
- I^{2}C Serial Interface
- Over-Temperature Protection

DC-DC Converters

- Fast Transient Response to Pulsed Load
- Built-In 20V, 800mA, 1Ω MOSFET
- Built-In Soft-Start
- Over-Current Protection

LDO Regulator

- Built-In ±15V LDO with ±0.15V accuracy for Source Driver Supply

Adjustable VCOM Driver for Accurate Panel-Backplane Biasing

- -0.6V to -5V
- 8-bit Control

Regulated Charge Pumps

- Charge Pump for VGH Regulation
- Charge Pump for VGL Regulation
- TQFN-24 (4mm×4mm) Package
- RoHS Compliant

Thermistor Monitoring

- -10°C to +85°C Temperature Range
- ±1°C Accuracy from 0°C to 50°C

Applications

- Electro-Phoretic Display (EPD) Panel
- E-Book
- P-DVD
- CAR TV

Ordering Information

FP9928A □□□

- TR: Tape/Reel
  Blank: Tube
- C: Green
- Package Type
  WQ: TQFN-24 (4mm×4mm)

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Typical Application Circuit

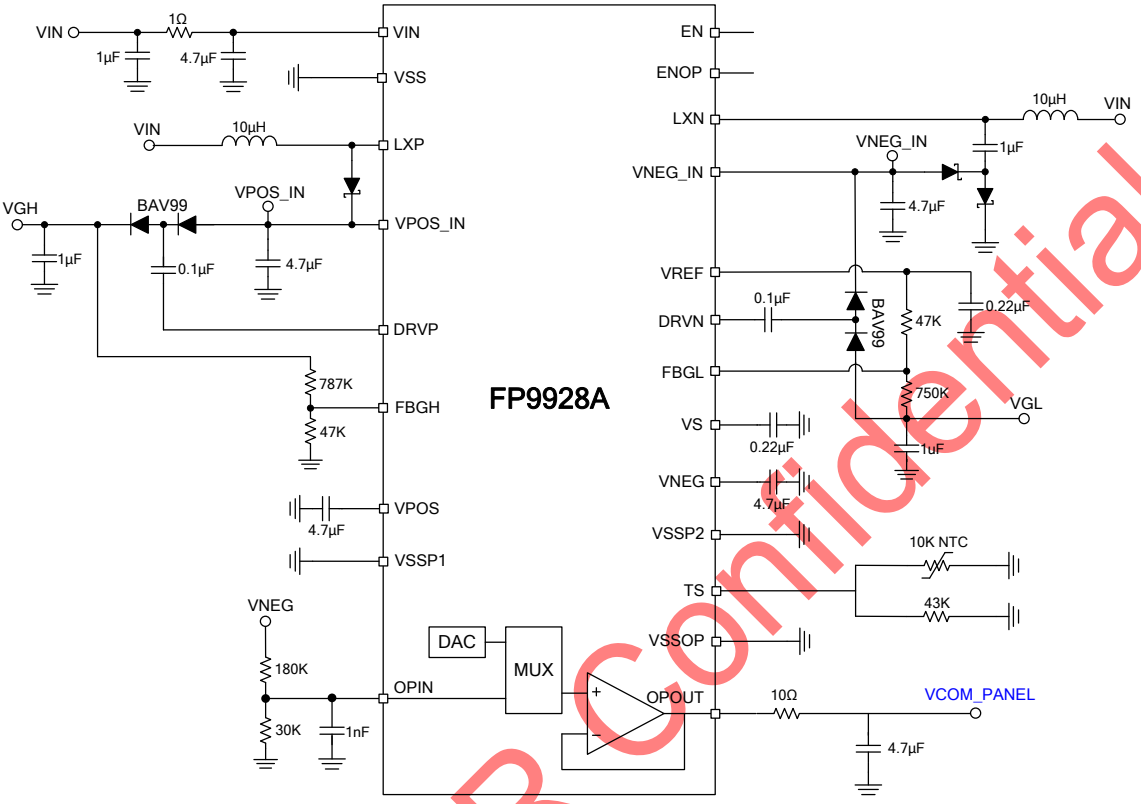


Figure 2. Typical Application Circuit of FP9928A

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Functional Pin Description

Pin Name	Pin No.	Pin Function
FBGH	1	Voltage Feedback to Determine Positive Charge Pump Output Voltage. FBGH is regulated to 1.25V.
VPOS_IN	2	Input pin for LDO (VPOS).
VPOS	3	Positive Source Driver Power.
EN	4	Enable Pin of Whole CHIP
TP	5	Test pin for testing, please do not connect to any signal.
TS	6	Thermistor input pin. Connect a 10K NTC thermistor and a 43K linearization resistor between this pin and system GND.
VREF	7	Internal Reference Bypass Terminal.
SDA	8	Serial interface (I^2C) data input/output.
SCL	9	Serial interface (I^2C) clock input.
VIN	10	Power Supply Input. The supply voltage powers all the control circuits.
ENOP	11	Enable Pin of Unity-Gain Operational Amplifier, active when EN is high.
OPIN	12	Unity-Gain Operational Amplifier Input Pin.
VSSOP	13	Positive Supply of Unity-Gain Operational Amplifier.
OPOUT	14	Unity-Gain Operational Amplifier Output Pin.
VNEG	15	Negative Source Driver Power, also ground of op-amp.
VNEG_IN	16	Input pin for LDO (VNEG).
FBGL	17	Voltage Feedback to Determine Negative Charge Pump Output Voltage. FBGL is regulated to 0V.
DRVN	18	Switching Pin. Driver for the negative charge pump.
VS	19	Regulated voltage for internal circuit.
LXN	20	Switching Pin. Drain of the internal power NMOS for the inverting regulator.
VSSP2	21	Power Ground. VSSP2 is the source of positive or Inverting boost converter power NMOS.
VSSP1	22	Power Ground. VSSP1 is the source of positive or Inverting boost converter power NMOS.
LXP	23	Switching Pin. Drain of the internal power NMOS for the positive regulator.
DRVP	24	Switching Pin. Driver for the positive charge pump.
VSS	25	Chip Digital Ground Pin must be connected to System GND.

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Block Diagram

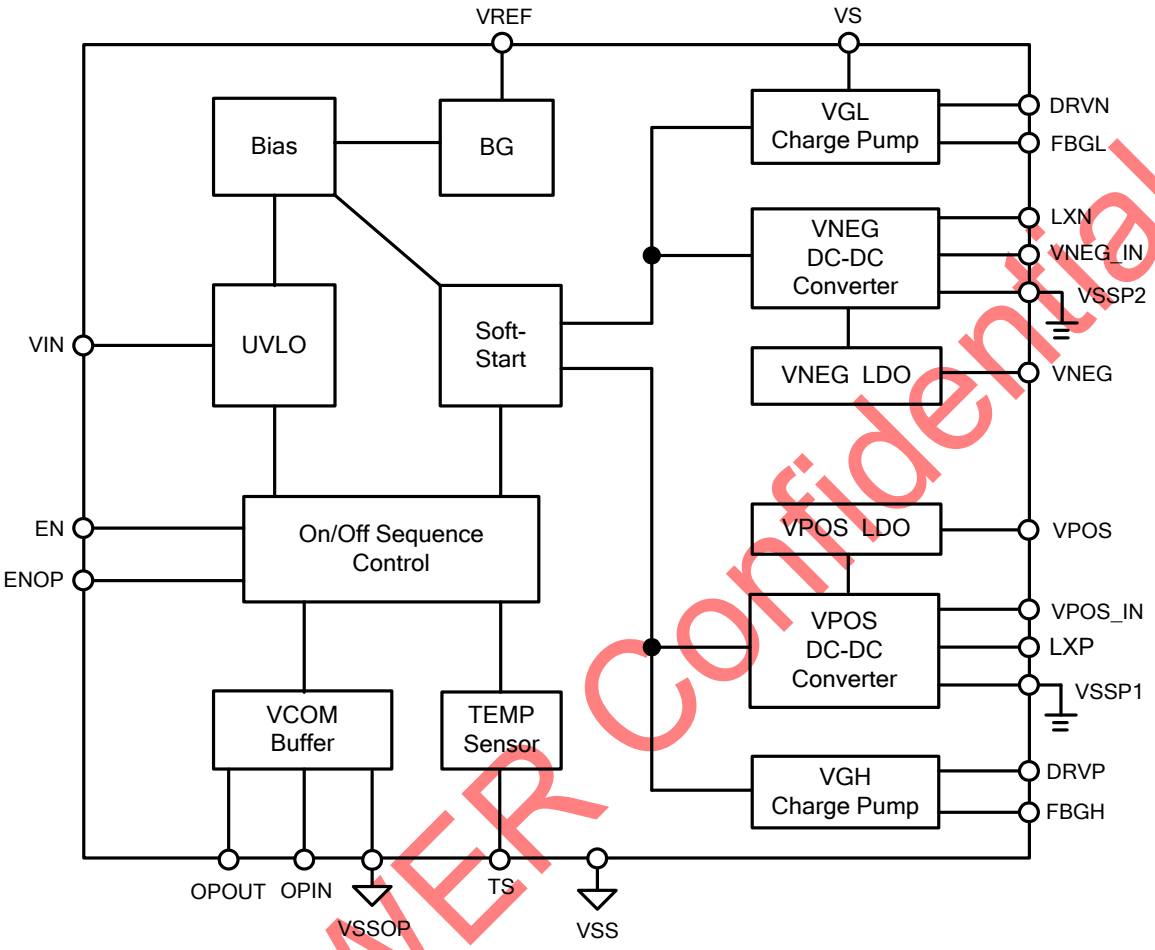


Figure 3. Block Diagram of FP9928A

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Absolute Maximum Ratings

- LXP, LXN, DRVP, DRVN, VPOS_IN, VPOS, VS ---------- -0.3V to +22V
- VIN, EN, ENOP, FBGH, FBGL,VREF ---------- -0.3V to +6V
- VNEG_IN, VNEG, OPIN, OPOUT ---------- -24V to +0.3V
- VSS,VSSP1, VSSP2, VSSOP ---------- -0.3V to +0.3V
- Power Dissipation @T_A=25°C, (P_D)

  TQFN-24 (4mm×4mm) ---------- 2.0W
- Package Thermal Resistance, (θ_{JA})

  TQFN-24 (4mm×4mm) ---------- 50°C/W
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_{STG}) ---------- -65°C to +150°C

Note：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (VIN) ---------- +2.7V to +5.5V
- Operating Junction Temperature Range ---------- -40°C to +85°C

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Electrical Characteristics

(V_{IN}=3.7V, T_A=0 to 85°C, typical values are at T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
System Supply						
Input Voltage Range	V_{IN}		2.7	3.7	5.5	V
V_{IN} UVLO Threshold	V_{UVLO}	V_{IN} Rising	-	2.5	-	V
		Hysteresis	-	0.2	-	
V_{IN} Supply Current	I_{IN}		-	1.5	-	mA
V_{IN} Shutdown Current	I_{SD}		-	0.1	1	µA
REF Output Voltage	V_{REF}		1.225	1.25	1.275	V
Thermal Shutdown Threshold	T_{SD}		-	140	-	°C
		Hysteresis	-	20	-	°C
Boost Regulator						
NMOS Switch ON-Resistance	R_{ONNMOS}		-	1	-	Ω
NMOS Switch Current Limit	$I_{LIMNMOS}$		-	800	-	mA
NMOS Switch Leakage Current	I_{LXNMOS}	V_{LXP}=18V	-	0.1	-	µA
VPOS LDO						
Input Voltage Range	V_{POS_IN}		15.3	-	17	V
Output Voltage Range	V_{POS}	I_{LOAD}=20mA	14.85	15	15.15	V
Inverting Regulator						
NMOS Switch ON-Resistance	R_{ONNMOS}		-	1	-	Ω
NMOS Switch Current Limit	$I_{LIMNMOS}$		-	800	-	mA
Switch Leakage Current	I_{LXNMOS}	V_{LXN}=18V	-	0.1	-	µA
VNEG LDO						
Input Voltage Range	V_{NEG_IN}		-17	-	-15.3	V
Output Voltage Range	V_{NEG}	I_{LOAD}=-20mA	-15.15	-15	-14.85	V
VCOM Buffer						
Accuracy	V_{COMACC}	VCOM_SET[7:0]=0x74h(-1.25V) VIN=3.4V to 4.2V, No load	-0.8	-	0.8	%
		VCOM_SET[7:0]=0x74h(-1.25V) VIN=2.7V to 5.5V, No load	-1.5	-	1.5	%
Output voltage range	V_{COM}		-5		-0.6	V
Resolution	V_{RES}	VCOM_ADJ=1, 1 LSB	-	22	34	mV
VCOM Gain (OPOUT/OPIN)	V_G	VCOM_ADJ=0	-	1	-	V/V

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Electrical Characteristics

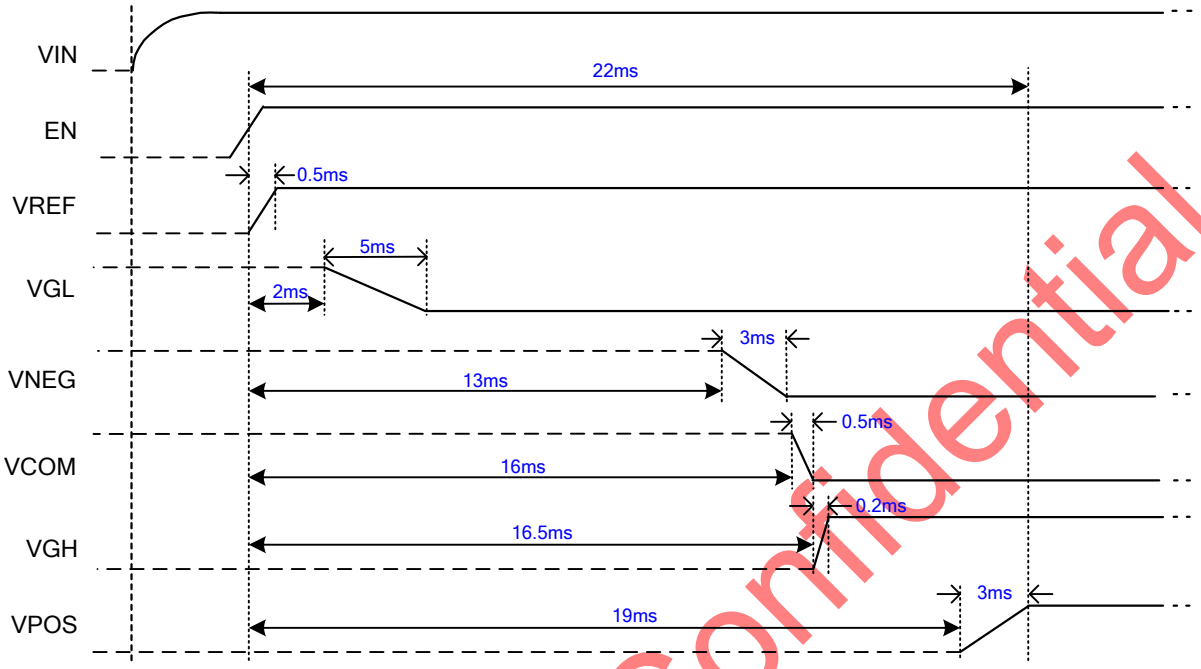
(V_{IN}=3.7V, T_A=0 to 85°C, typical values are at T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOGIC LEVELS AND TIMING CHARACTERISTIC (SCL, SDA)						
Input Low Threshold Level	V_{IL}		-	-	0.4	V
Input High Threshold Level	V_{IH}		1.2	-	-	V
Output Low Threshold Level	V_{OL}	I_O=3mA, Sink Current.	-	-	0.4	V
SCL Clock Frequency	f_{SCL}		-	-	400	kHz
Thermal Sensor (Note 1)						
Offset	OffsetTMS	Temperature = 25°C	-	1.18	-	V
Maximum Input Level	VTMS_MAX		-	2.25	-	V
Internal Pull Up Resistor	RNTC_UP		-	7.307	-	KΩ
External Linearization Resistor	RLINEAR		-	43	-	KΩ

Note 1: 10KΩ Murata NCP18XH103F03RB thermistor (1%) in parallel with a linearization resistor (43kΩ, 1%) are used at TS pin for panel temperature measurement.

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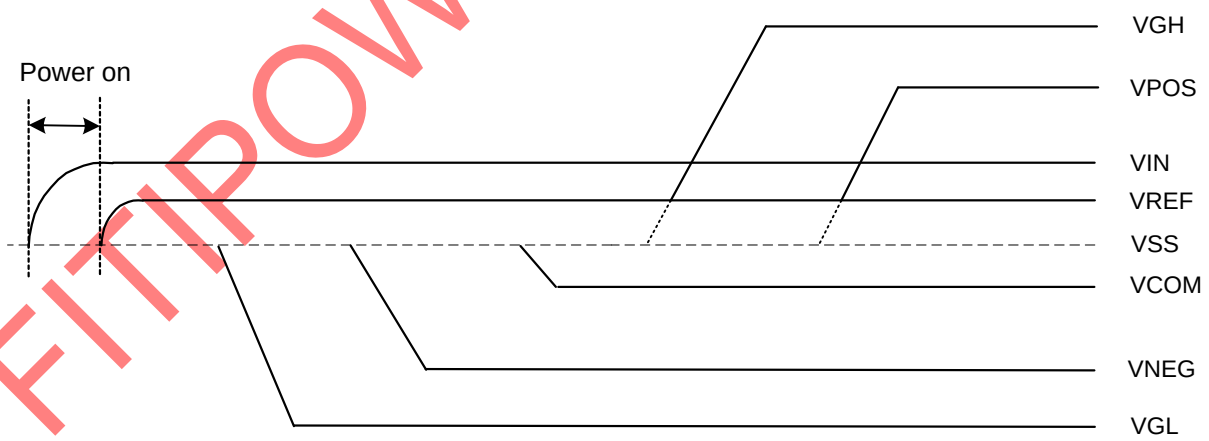
Power On Sequence



Note : VIN UVLO → EN → VREF → VGL → VNEG → VCOM → VGH → VPOS

Figure 4. Power-on Sequence

Power Level



Note : VGL < VNEG < VCOM < VSS < VREF < VIN < POS < VGH

Figure 5. Power Level

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Power Off Sequence

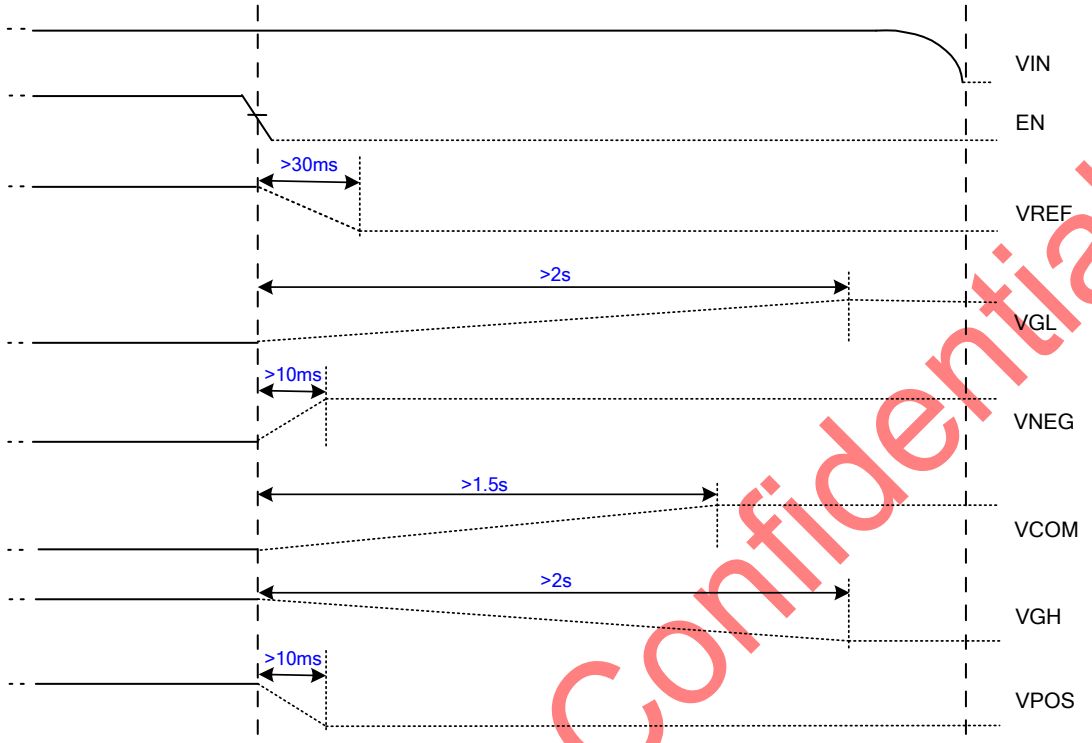


Figure 6. Power Off Sequence

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VCOM Adjustment

Through the I^{2}C interface, the user can select between two methods of VCOM voltage adjustment:

(1) Use the internal 8-bit DAC and register control
(2) Use an external voltage source (resistor divider) connected to the OPIN pin.

The VCOM adjustment method is selected by the VCOM_ADJ bit of the FUNC_ADJUST register (0x01h), and both methods have the same adjustment voltage range. The block diagram for VCOM is shown in Figure 7.

VCOM Adjustment through Register Control

By default the FP9928A is setup for internal VCOM control through the I^{2}C interface. The default setting for the 8-bit DAC is 0x74h which results in 1.25V +/- 0.8% for VCOM. VCOM can be adjusted up or down in steps of 22mV (typ.) by writing to the VCOM_SETTING register (0x02h). The output range for VCOM is limited to -0.6 to -5V.

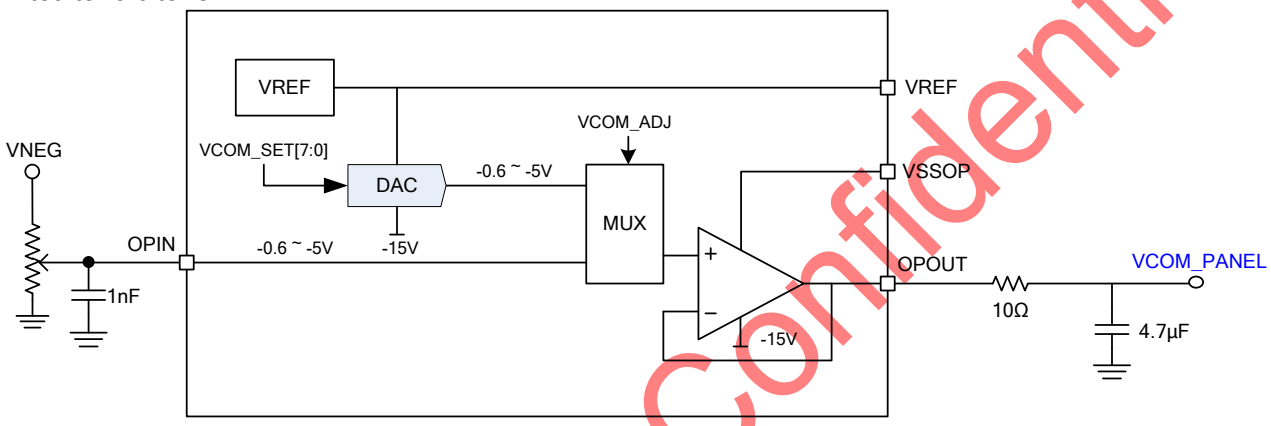


Figure 7. Block Diagram of VCOM Circuit

VCOM Adjustment through External Potentiometer

VCOM can be adjusted by an external potentiometer by setting the VCOM_ADJ bit of the FUNC_ADJUST register to 0 and connecting a potentiometer to the OPIN pin. The potentiometer must be connected between ground and a negative supply as shown in Figure 7. The gain from OPIN to OPOUT is 1, and therefore the voltage applied to OPIN pin should range from -0.6 to -5V.

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Temperature Sensor

The FP9928A is specifically designed to operate in multi-host systems where one of I^2C host, e.g. the display controller, has limited I^2C capability. Standard I^2C protocol requires the following steps to read data from a register:

1. Send device and register address, R/nW bit set low (write command).
2. Send device address, R/nW set high (read command).
3. The slave will respond with data from the specified register address.

Some display controllers support I^2C read commands only and need to access the temperature data form the FP9928A TMST_VALUE register. To support these systems, the FP9928A automatically triggers temperature acquisition every 60s and stores the result in TMST_VALUE register. With the FIX_RD_PTR bit in the FUNC_ADJUST register set to 1 the device will respond to any I^2C read command with data from the TMST_VALUE register. No write command with the register address is required and address auto increment feature is disabled in this mode. Therefore reading the temperature data is reduced to two steps:

1. Send device address, R/nW set high (read command).
2. Read the data from the Slave. The slave will respond with data from TMST_VALUE register address.

The FIX_RD_PTR Bit

The FP9928A supports a special I^2C mode making it compatible with the EPSON Broadsheet S1D13521 timing controller. Standard I^2C protocol requires the following steps to read data from a register:

1. Send device slave address, R/nW bit set low (write command)
2. Send register address
3. Send device slave address, R/n/W set high (read command)
4. The slave will respond with data from the specified register address.

The EPSON Broadsheet S1D13521 controller does not support I^2C writes nor I^2C reads from addressed register (step 1. and step 2. above) but needs to access the temperature data from the FP9928A's TMST_VALUE register. To support Broadsheet based systems, the FP9928A automatically triggers temperature acquisition every 60s and stores the result in TMST_VALUE register. With the FIX_RD_PTR bit in the FUNC_ADJUST register set to 1 the device will respond to any I^2C read command with data from the TMST_VALUE register. No write command with the register address is required and address auto increment feature in the mode. Therefore reading the temperature data is reduced to two steps:

1. Send device address, R/nW set high (read command).
2. Read the data from the Slave. The slave will respond with data from TMST_VALUE register address.

At system power-up the main processor sets up the PMIC by accessing the I^2C registers and setting the control parameters as needed. When the system is setup correctly, the main controller sets the FIX_RD_PTR bit and the display controller can start accessing the temperature information. During normal operation, the main controller can write to the PMIC at any time but before it can read access registers the FIX_RD_PTR bit must be written 0.

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NTC BIAS Circuit

Figure 8 shows the block diagram of the NTC bias and measurement circuit. The NTC is biased from an internally generated 2.25V reference voltage through an integrated 7.307ΩK bias resistor. A 43ΩK resistor is connected parallel to the NTC to linearize the temperature response curse. The circuit is designed to work with a nominal 10ΩK NTC and achieves accuracy of ±1°C from 0°C to 50°C. The voltage drop across the NTC is digitized by a 10-bit SAR ADC and translated into an 8-bit two's complement by digital per Table 1.

Table 1. ADC Output Value vs Temperature

TEMPERATURE	TMST_VALUE [7:0]
< -10°C	1111 0110
-10°C	1111 0110
-9°C	1111 0111
---	---
-2°C	1111 1110
-1°C	1111 1111
0°C	0000 0000
1°C	0000 0001
2°C	0000 0010
---	---
25°C	0001 1001
---	---
85°C	0101 0101
> 85°C	0101 0101

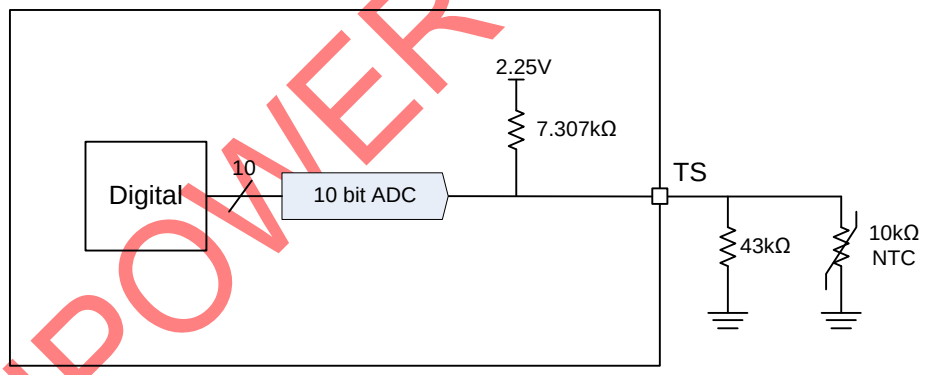


Figure 8. NTC Bias and Measurement Circuit

FP9928A Temperature Acquisition

The FP9928A triggers temperature acquisition every 60s. The FP9928A can be accessed at any time, and reading the Temperature Register will yield result from the last temperature conversion. When the FP9928A is accessed, the conversion that is in process will be interrupted and it will be restarted after the end of the communication. Accessing the FP9928A continuously without waiting at least one conversion time between communications will prevent the device from updating the Temperature Register with a new temperature conversion result.

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I²C Interafce Specification

Serial Interface

The serial interface is compatible with the standard and fast mode I²C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and the PMIC status to be monitored. The E Ink® PMIC has a 7bit address: '1001000', other addresses are available upon contact with the factory. Attempting to read data from register addresses not listed in this section will result in 00h being read out. For normal data transfer, SDA is allowed to change only when SCL is low. Changes when SCL is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the –PMIC generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The –PMIC will pull down the SDA line during the acknowledge clock pulse so that the SDA line is a stable low during the high period of the acknowledge clock pulse. The SDA line is a stable low during the high period of the acknowledge–related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave –PMIC device must leave the data line high to enable the master to generate the stop condition.

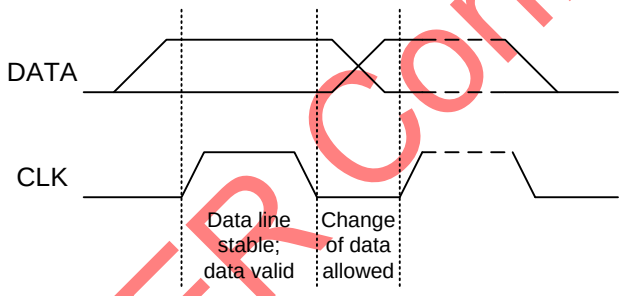


Figure 9. bit transfer on the serial interface

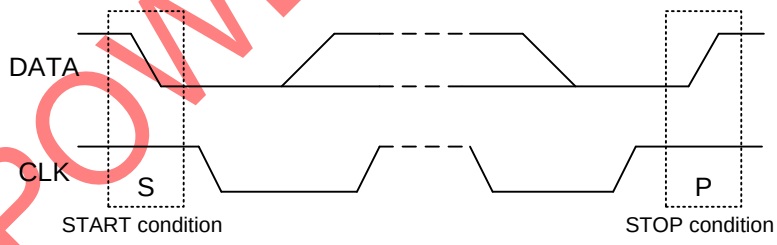


Figure 10. START and STOP conditions

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I²C Timing Diagrams

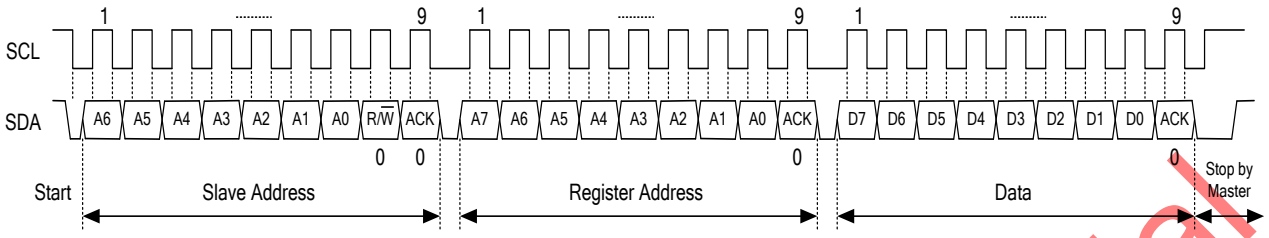


Figure 11. Serial interface WRITE to the device.

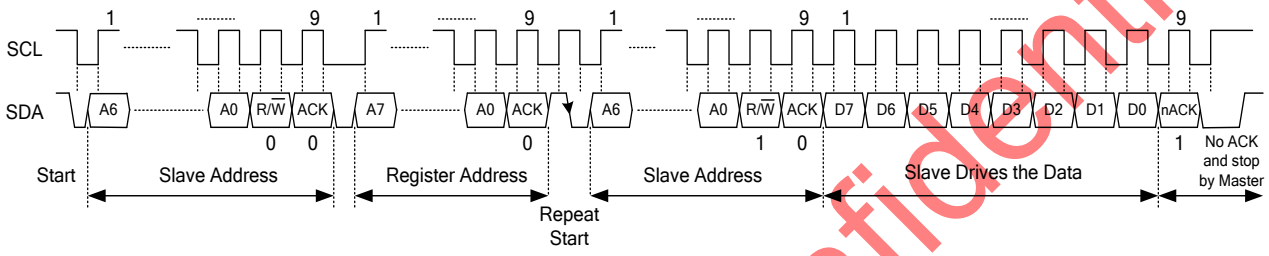


Figure 12. Serial interface READ from the device.

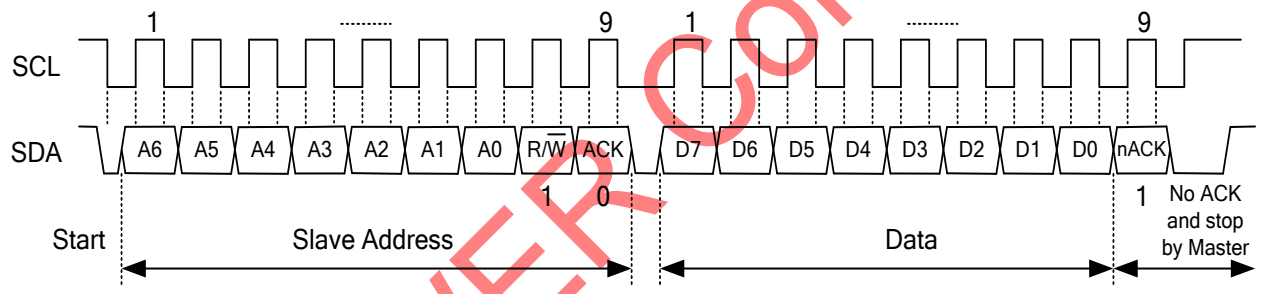


Figure 13. Serial interface READ from the device for EPSON Broadsheet support.

Figure 13. I²C READ data transmission with FIX_RD_PTR bit set for EPSON Broadsheet support. Only address 0x00h can be read. FIX_RD_PTR bit has no impact on WRITE transaction.

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I²C Data Transmission Timing

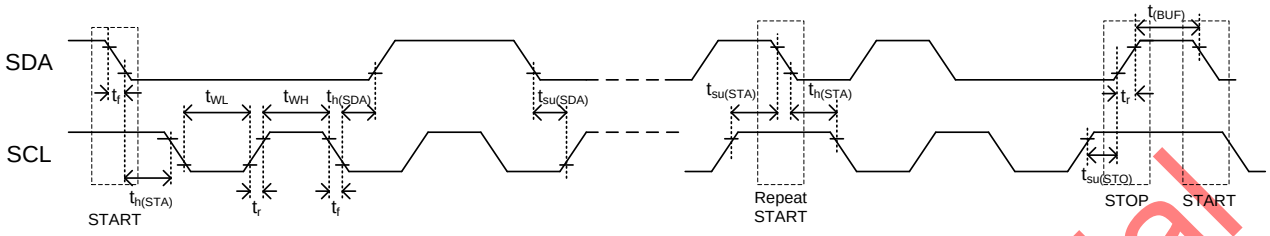


Figure 14. Serial I/F Timing Diagram

Data Transmission Timing

VBAT=3.7V±5%, TA=25°C, CL=100pF, SCL=400KHz (unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Serial clock frequency	f_{SCL}		-	-	400	kHz
HIGH period of the SCL clock	t_{WH}		600	-	-	nS
LOW period of the SCL clock	t_{WL}		1300	-	-	nS
SDA and SCL rise time	t_r		-	-	300	nS
SDA and SCL fall time	t_f		-	-	300	nS
Data input setup time	tsu(SDA)		100	-	-	nS
Data input hold time	th(SDA)		0	-	900	nS
Setup time for a repeated START condition.	tsu(STA)		600	-	-	nS
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	th(STA)		600	-	-	nS
Setup time for STOP condition	tsu(STO)		600	-	-	nS
Bus free time between stop and start condition	t(BUF)		1300	-	-	nS

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Register Address Map

Register	Address (Hex)	Name	Default Value	Description
0	0x00	TMST_VALUE	N/A	Thermistor value read by ADC
1	0x01	FUNC_ADJUST	0000 0001	Vcom output adjustment method and I^2C read pointer control
2	0x02	VCOM_SETTING	0111 0100	Voltage setting for Vcom

THERMISTOR READOUT (TMST_VALUE)
Address – 0x00h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TMST_VALUE [7:0]							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	NA	NA	NA	NA	NA	NA	NA	NA

Field Name	Bit Definition
TMST_VALUE [7:0]	Temperature read-out 1111 0110 – < -10°C 1111 0110 – -10°C 1111 0111 – -9°C --- 1111 1110 – -2°C 1111 1111 – -1°C 0000 0000 – 0°C 0000 0001 – 1°C 0000 0010 – 2°C --- 0001 1001 – 25°C --- 0101 0101 – 85°C 0101 0101 – > 85°C

VCOM ADJUSTMENT METHOD and I^2C read pointer control (FUNC_ADJUST)
Address – 0x01h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Not Used						FIX_RD_PTR	VCOM_ADJ
Read/Write	R	R	R	R	R	R	R./W	R./W
Reset Value	NA	NA	NA	NA	NA	NA	0	1

Field Name	Bit Definition
FIX_RD_PTR	I^2C read pointer control **0 – Read pointer is controlled through I^2C (Default)** 1 – Read pointer is fixed to 0x00h
VCOM_ADJ	VCOM output adjustment method 0 – OPIN pin **1 – I^2C interface (Default)**

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VCOM ADJUSTMENT (VCOM_SETTING)
Address – 0x02h

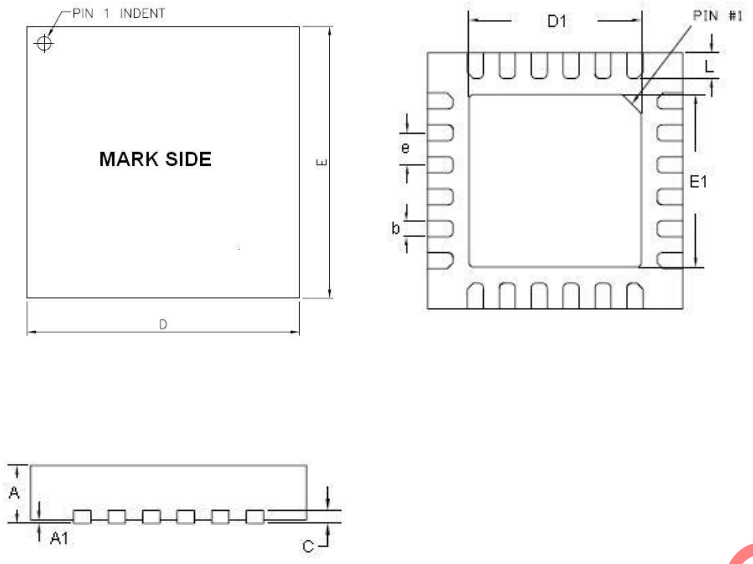
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOM_SET[7:0]							
Read/Write	R./W	R./W	R./W	R./W	R./W	R./W	R./W	R./W
Reset Value	0	1	1	1	0	1	0	0

Field Name	Bit Definition
VCOM_SET[7:0]	VCOM voltage adjustment 0000 0000 – Reserved --- 0001 1011 – Reserved 0001 1100 – 604mV 0001 1101 – 626mV --- 0111 0011 – 2480mV **0111 0100 – 2500mV (Default)** 0111 0101 – 2522mV --- 1110 1000 – 5002mV 1110 1001 – Reserved --- 1111 1111 – Reserved Note: Step size is rounded to 11mV. Theoretical step size is 5500mV / 255 = 21.57mV.

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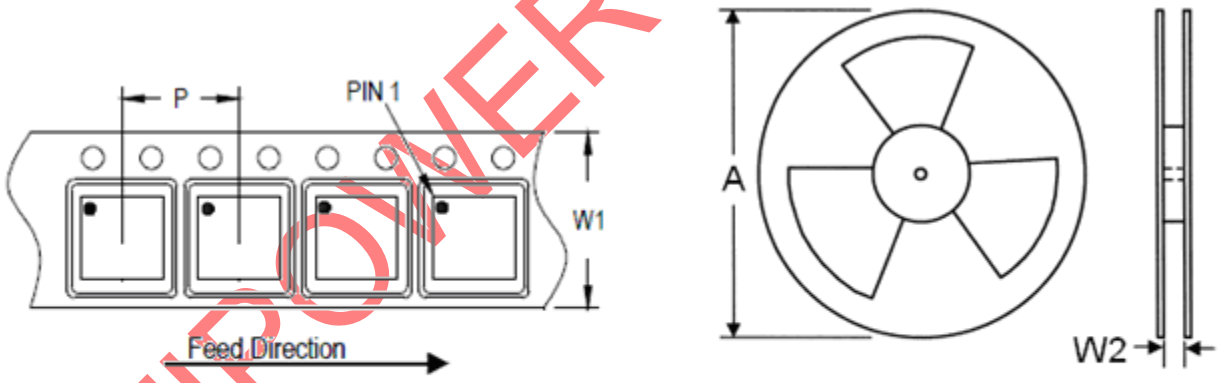
Outline Information

TQFN-24 4mm×4mm (pitch: 0.5mm) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
C	0.18	0.25
E	3.90	4.10
D	3.90	4.10
L	0.30	0.45
b	0.18	0.30
e	0.45	0.55
E1	2.20	2.80
D1	2.20	2.80

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000

FITIPOWER Confidential

Life Support Policy
Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.