NCS6415

Bus-Controlled Video Matrix Switch

ON Semiconductor®

http://onsemi.com

Description

The main function of the NCS6415 is to switch 8 video input sources to the 6 outputs.

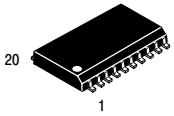
Each output can be switched to only one of the inputs, whereas any single input may be connected to several outputs.

All switching possibilities are controlled through the I^2C bus.

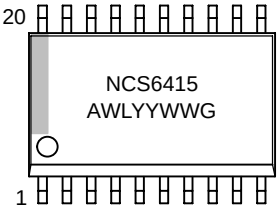
Features

- Cascadable with another NCS6415 (Internal Address can be changed by Pin 7 Voltage)
- 8 Inputs (CVBS, RGB, Chroma, ...)
- 6 Outputs with Low Impedance Driver
- Possibility of Chroma Signal for each Input by Switching off the Clamp with an External Resistor Bridge
- Bus Controlled
- 6.5 dB Gain between any Input and Output
- −45 dB Crosstalk at 5 MHz
- Compatible with TEA6415C
- Full ESD Protection
- These are Pb−Free Devices

MARKING DIAGRAMS*

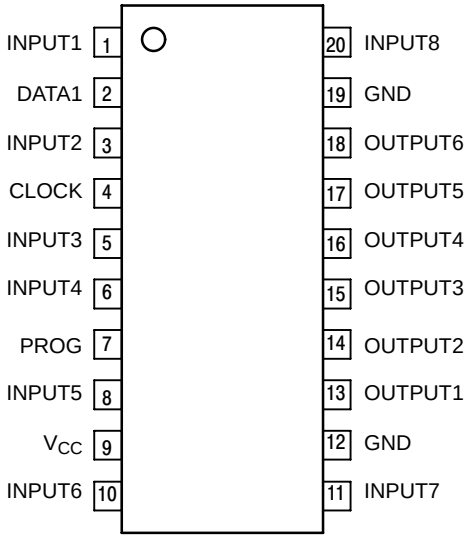


SO−20 WB
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.



ORDERING INFORMATION

Device	Package	Shipping†
NCS6415DWG	SO−20 (Pb−Free)	38 Units / Rail
NCS6415DWR2G	SO−20 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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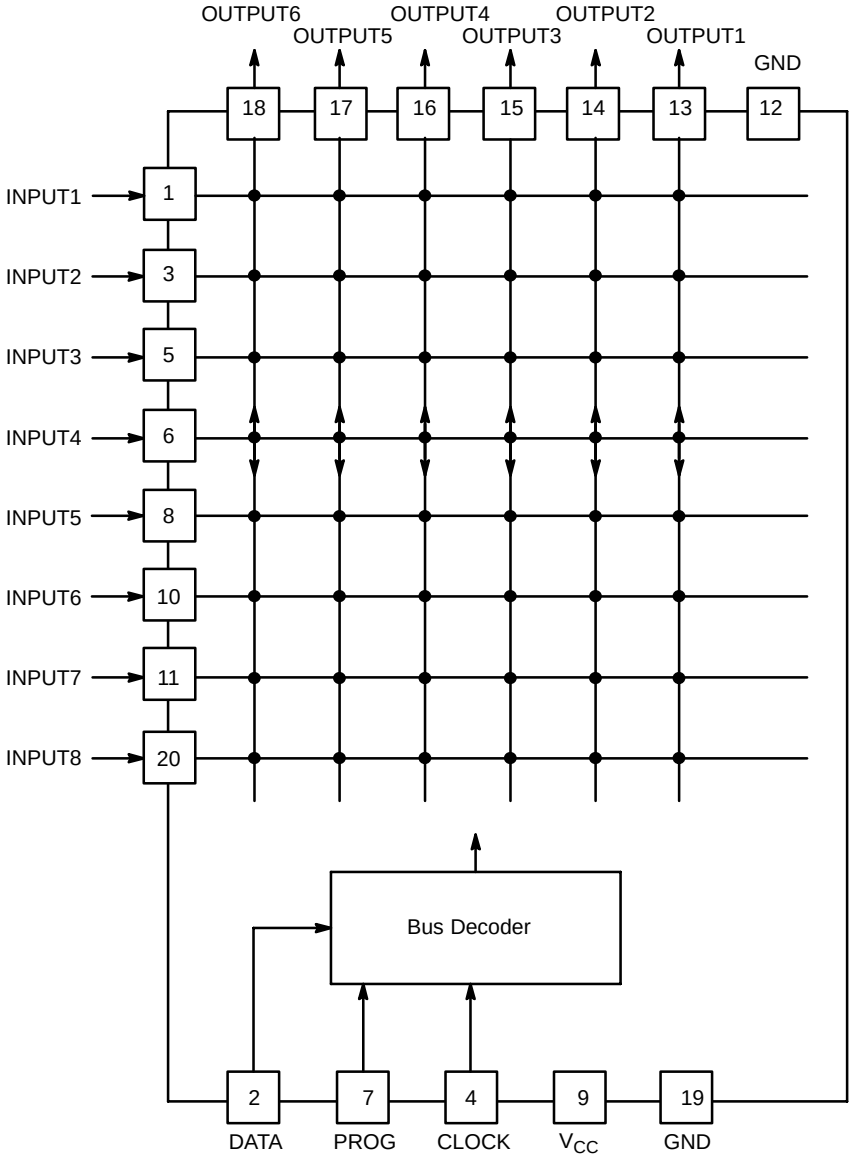


Figure 1. Block Diagram

The main function of the NCS6415 is to switch 8 video input sources to the 6 outputs.

Each output can be switched to only one of the inputs, whereas any single input may be connected to several outputs. The lowest level of each signal is aligned on each input (bottom of sync pulse for CVBS or Black Level for RGB signals).

The nominal gain between any input and output is 6 dB. For Chroma signals, the alignment is switched off by forcing, with an external 5‘ VDC resistor bridge on the input. Each input can be used as a normal input or as a Chroma input (with external resistor bridge). All the switching possibilities are changed through the I^2C bus.

The switches configuration is defined by words of 16 bits: one word of 16 bits for each output channel.

So, 6 words of 16 bits are necessary to determine the starting configuration upon power−on (power supply: 0 to 10 V). But a new configuration needs only the words of the changed output channels. Driving a 75 Ω load requires an external transistor.

Table 1. ATTRIBUTES

Characteristics		Value
ESD	Human Body Model Machine Model	4 kV 400 V
Moisture Sensitivity (Note 1)		Level 3
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in.

1. For additional information, see Application Note AND8003/D

Table 2. MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	12	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Thermal Resistance, Junction−to−Air SO−20	θ_{JA}	 30 to 35	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. DC & AC Characteristics (T_A = 25°C, V_{CC} = 10 V, R_L = 10 kΩ, C_L = 3 pF)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	8	10	11	V
I_{CC}	Power Supply Current (No Load)	20	30	40	mA
INPUTS					
	Signal Amplitude (CVBS signal) (Note 2)		1.5	2	V_{PP}
	Input Current (per output connected, V_{IN} = 5 V_{DC})		1	3	μA
	DC Level	3.3	3.6	3.9	V
	DC Level Shift (0°C to 70°C)		5	100	mV
R_{IN}	Input Resistance		1		MΩ
C_{IN}	Input Capacitance		2		pF
OUTPUTS					
	Dynamic (V_{IN} = 2.5 V_{PP})		5		V_{PP}
	Output Impedance (Note 2)		25	50	Ω
A_V	Gain (Note 2)	6	6.5	7	dB
BW	Bandwidth (Note 2) −1 dB Attenuation −3 dB Attenuation	7	 15 20		MHz
	0.1 dB Gain Flatness (Note 2)	6			MHz
	Crosstalk f = 3.58 MHz f = 5 MHz		−48 −45		dB
	DC Level	2.4	2.75	3.1	V
I^2C BUS INPUT: DATA, CLOCK AND PROG					
	Threshold Voltage	1.5	2	3	V

2. Guaranteed by design and/or characterization.

Table 4. I²C Bus Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Unit
SCL					
V_{IL}	Low Level Input Voltage		−0.3	+1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} +0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	−10	+10	μA
f_{SCL}	Clock Frequency (Note 3)		0	100	kHz
t_R	Input Rise Time (Note 3)	1.5 V to 3 V		1000	ns
t_F	Input Fall Time (Note 3)	3 V to 1.5 V		300	ns
C_I	Input Capacitance (Note 3)			10	pF
SDA					
V_{IL}	Low Level Input Voltage		−0.3	+1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} +0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	−10	+10	μA
C_I	Input Capacitance (Note 3)			10	pF
t_R	Input Rise Time (Note 3)	1.5 V to 3 V		1000	ns
t_F	Input Fall Time (Note 3)	3 V to 1.5 V		300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3 mA		0.4	V
t_F	Output Fall Time (Note 3)	3V to 1.5 V		250	ns
C_L	Load Capacitance			400	pF
TIMING					
t_{LOW}	Clock Low Period (Note 4)		4.7		μs
t_{HIGH}	Clock High Period (Note 4)		4.0		μs
$t_{SU,DAT}$	Data Setup Time (Note 4)		250		ns
$t_{HD,DAT}$	Data Hold Time (Note 4)		0	340	ns
$t_{SU,STO}$	Setup Time from Clock High to Stop (Note 4)		4.0		μs
t_{BUF}	Start Setup Time following a Stop (Note 4)		4.7		μs
$t_{HD,STA}$	Start Hold Time (Note 4)		4.0		μs
$t_{SU,STA}$	Start Setup Time following Clock Low to High Transition (Note 4)		4.7		μs

3. Guaranteed by design and/or characterization.
4. Functionality guaranteed by design and/or characterization.

I²C Bus Selections

The I²C chip address is defined by the first byte. The second byte defines the input/output configuration.

Table 5. CHIP ADDRESS BYTE (1ST BYTE OF TRANSMISSION)

HEX	BINARY	Comment
86	1000 0110	When PROG pin is connected to Ground
06	0000 0110	When PROG pin is connected to V_{CC}

Input/Output Selection Byte (2nd byte of transmission)

Table 6. I²C BUS OUTPUT SELECTIONS

Output Address (MSB)	Input Address (LSB)	Selected Output	
00000	XXX	Pin 18	Output is selected by the 5 MSBs.
00100	XXX	Pin 14	
00010	XXX	Pin 16	
00110	–	Not Used	
00001	XXX	Pin 17	
00101	XXX	Pin 13	
00011	XXX	Pin 15	
00111	–	Not Used	

Table 7. I²C BUS INPUT SELECTIONS

Output Address (MSB)	Input Address (LSB)	Selected Input	
00XXX	000	Pin 5	Input is selected by the 3 LSBs.
00XXX	100	Pin 8	
00XXX	010	Pin 3	
00XXX	110	Pin 20	
00XXX	001	Pin 6	
00XXX	101	Pin 10	
00XXX	011	Pin 1	
00XXX	111	Pin 11	

Example: 0010 0101 (Binary) or 25 (Hex) connects Pin 10 (input) to Pin 14 (output)

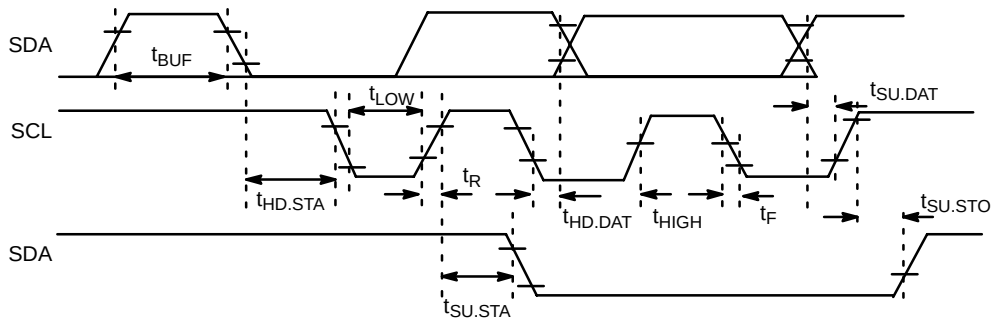


Figure 2. I²C Timing Diagram

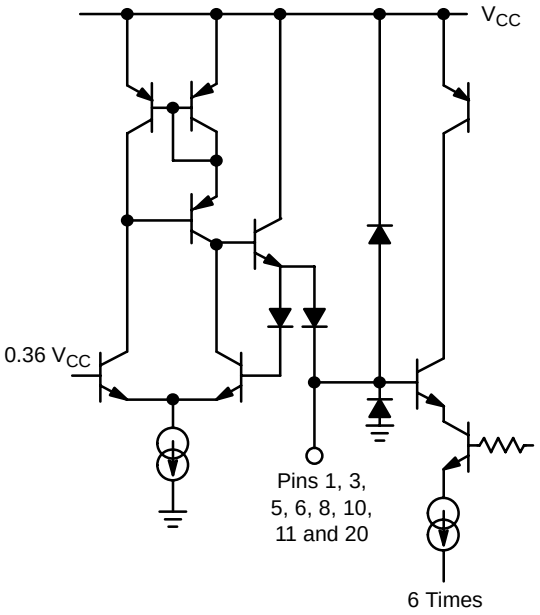


Figure 3. Input Configuration

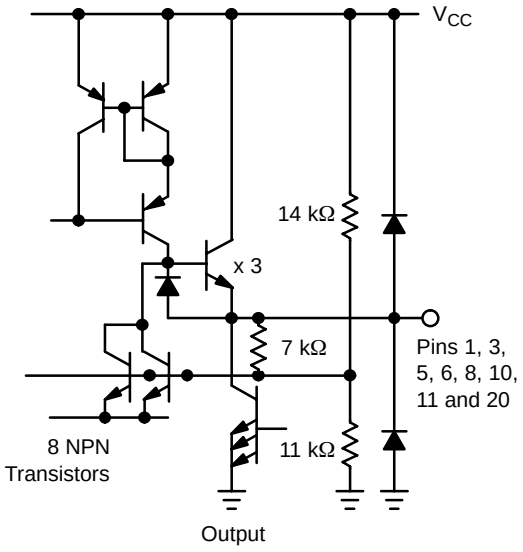


Figure 4. Output Configuration

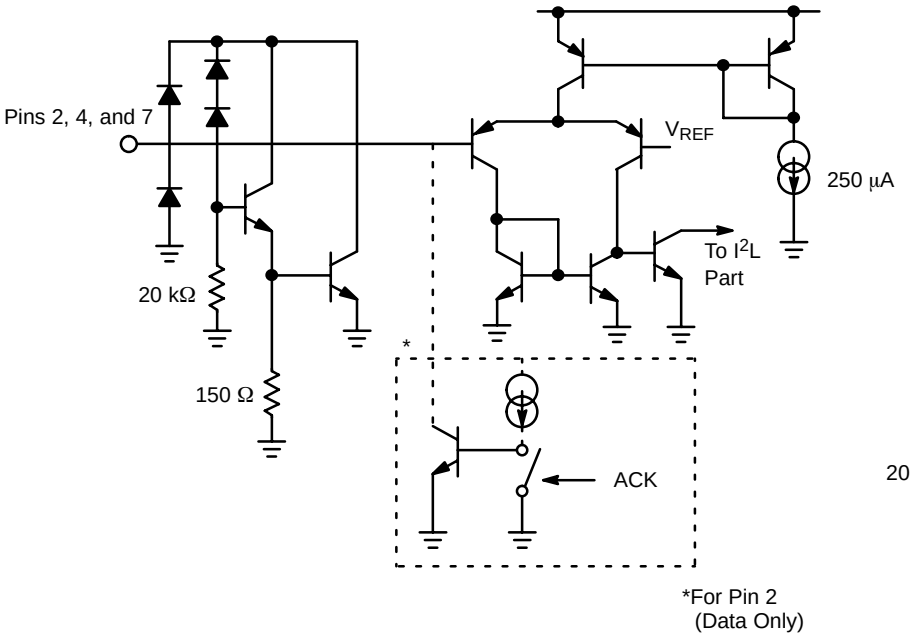


Figure 5. Bus I/O Configuration

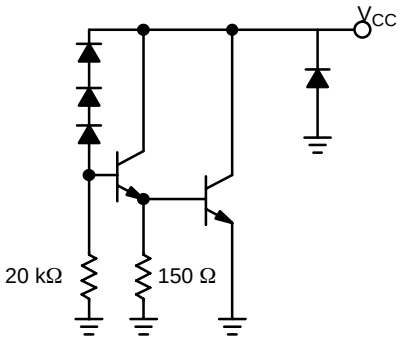


Figure 6. V_{CC} Pin Configuration

USING A SECOND NCS6415

The programming input pin (PROG) allows two NCS6415 circuits to operate in parallel and to select them independently through the I^2C bus by modifying the address byte. Consequently, the switching capabilities are doubled, or IC1 and IC2 can be cascaded (see Figure 7).

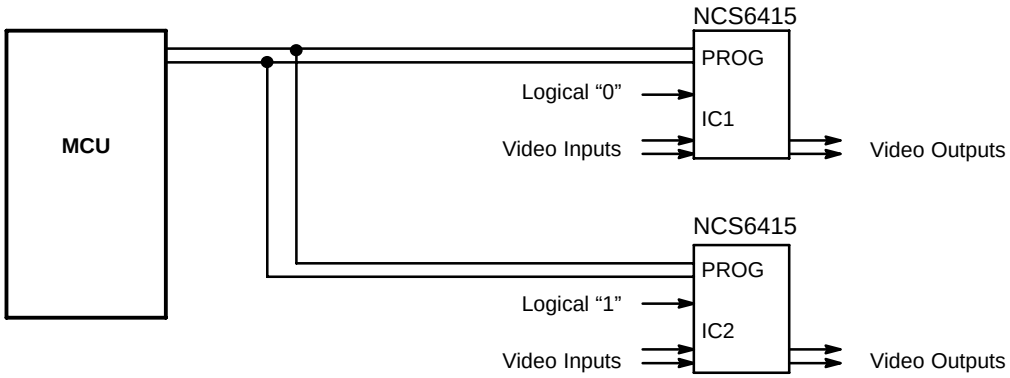


Figure 7. Cascaded NCS6415

TYPICAL APPLICATION DIAGRAM

NCS6415 is suited for single supply system, running on a single +10 V supply. The high quality of the output stage and excellent linearity provides video signal comparable to broadcast studio quality signals. The layout is not as critical to the design and it can be easily realized on a single sided board.

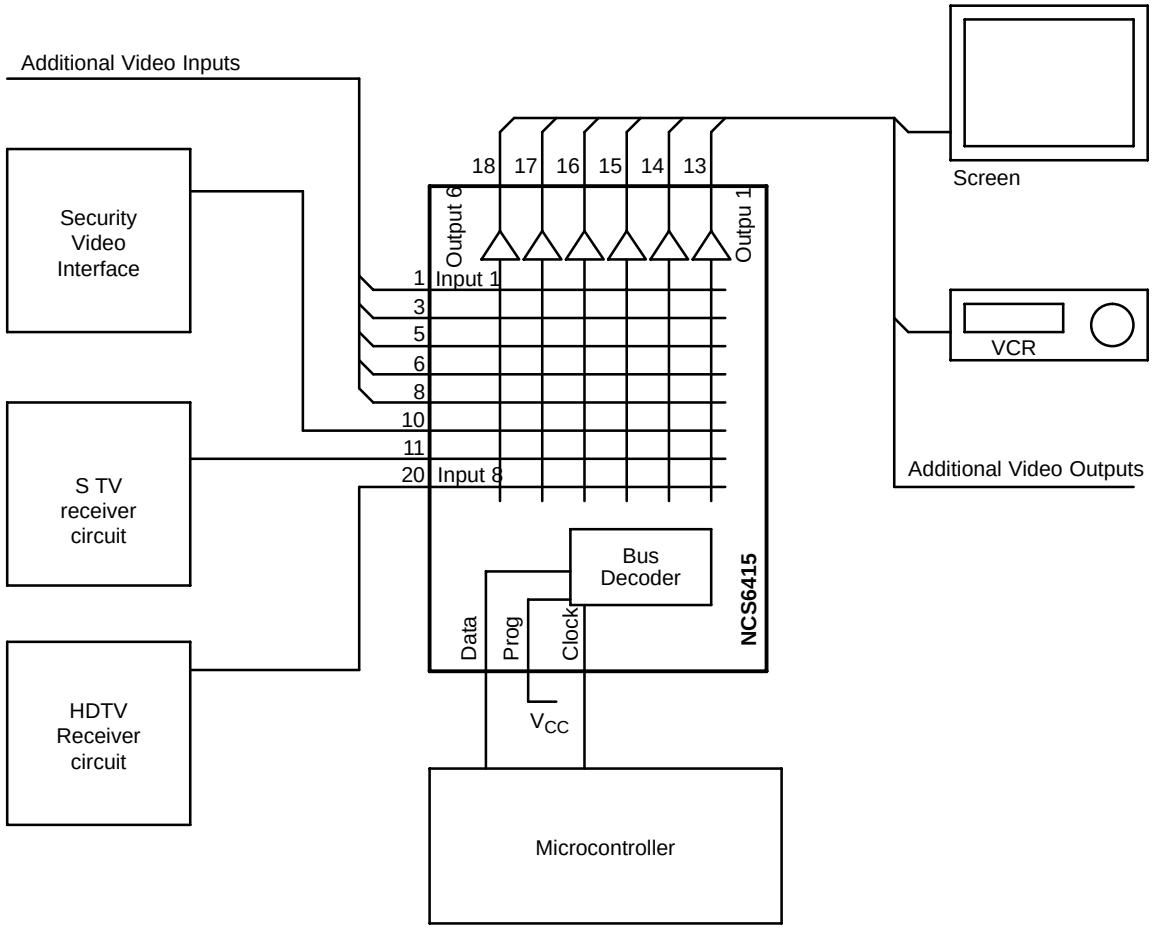


Figure 8. Typical Application Diagram

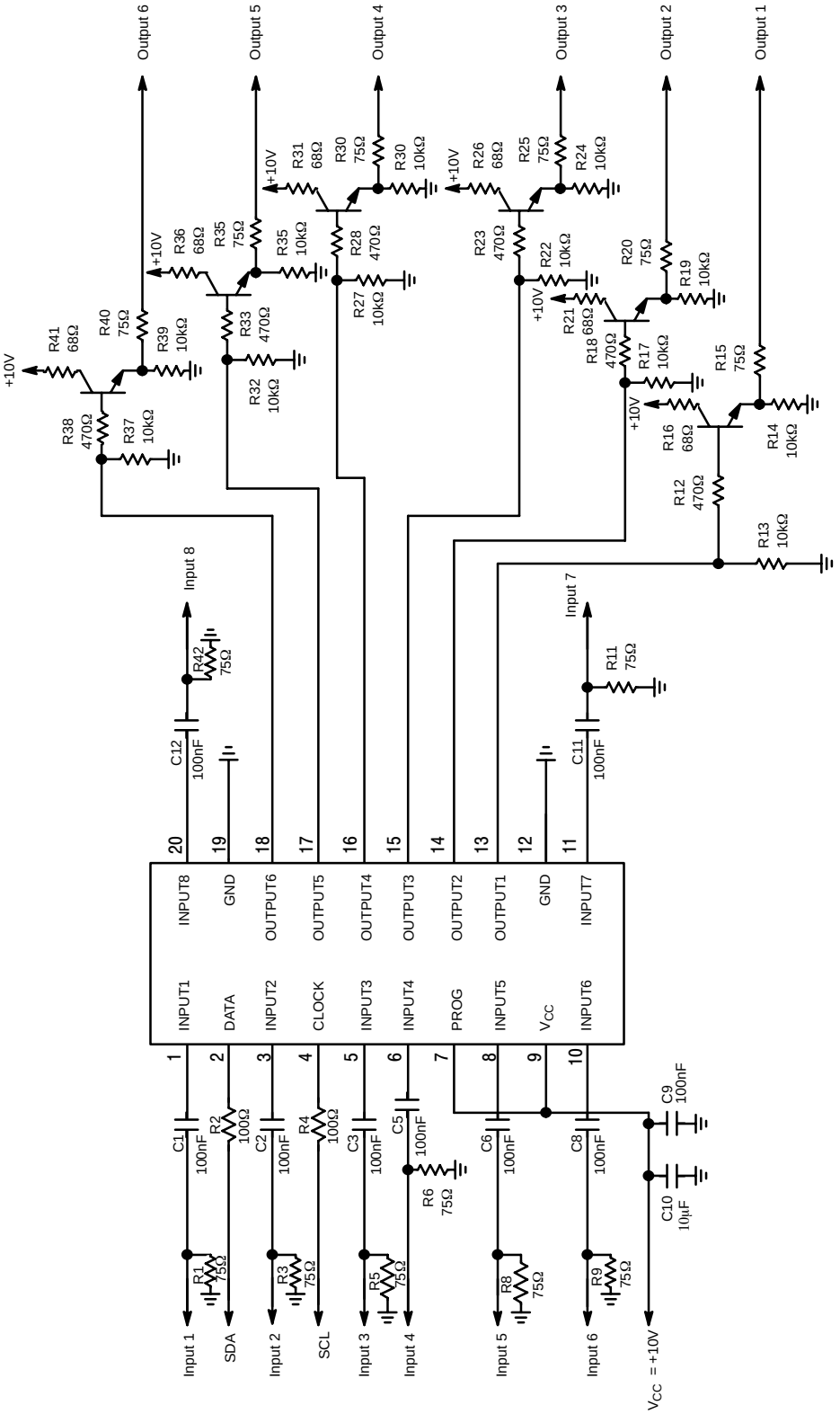
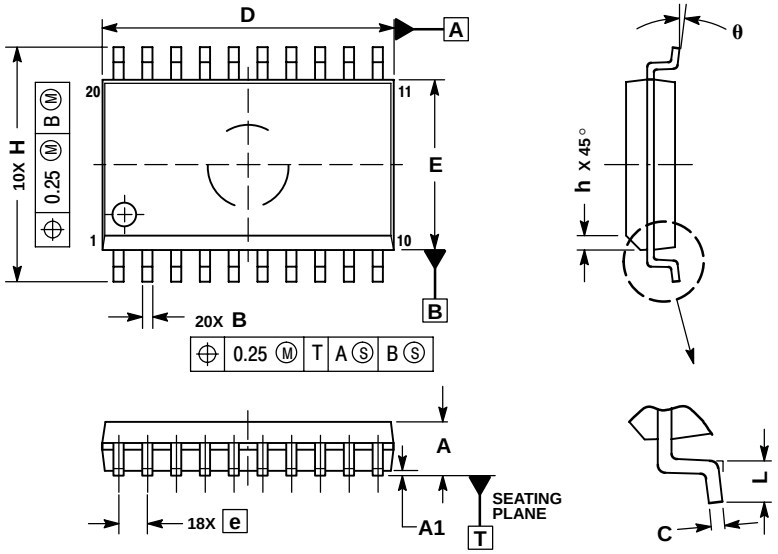


Figure 9. Typical Application Circuit

PACKAGE DIMENSIONS

SO−20 WB
CASE 751D−05
ISSUE G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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