Synchronous-Rectified Buck MOSFET Drivers

General Description

The RT9603 is a high frequency, dual MOSFET drivers specifically designed to drive two power N-MOSFETs in a synchronous-rectified buck converter topology. The device combined with the RT924x series of multi-phase PWM controllers and MOSFETs form a complete core voltage regulator solution for advanced microprocessors.

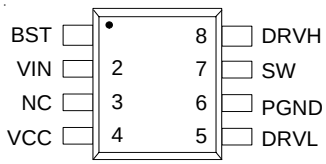
The output drivers in the RT9603 can efficiently switch power MOSFETs at frequencies up to 500kHz. It shall be taken into account the thermal consideration when the switching frequency above 500kHz. Each driver is capable of driving a 3nF load in 30/40ns rise/fall time with fast propagation delay from input transition to the gate of the power MOSFET. The device implements boot-strapping on the upper gate with only an external capacitor and a diode required. This reduces implementation complexity and allows the use of higher performance, cost effective N-MOSFETs.

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply.

An unique feature of the RT9603 driver is the addition of over-voltage protection in the event of upper MOSFET direct shorted before power-on. The RT9603 detects the fault condition during initial start-up, the internal power-on OVP sense circuitry will rapidly drive the output lower MOSFET on before the multi-phase PWM controller takes control. As a result, the input supply will latch into the shutdown state, thereby prevent the processor from damaged.

Pin Configurations

(TOP VIEW)



SOP-8

Features

- **Drives Two N-MOSFETs**
- **Adaptive Shoot-Through Protection**
- **Supports High Switching Frequency**
  - **Fast Output Rise Time**
  - **Propagation Delay 40ns**
- **Tri-State Input for Bridge Shutdown**
- **Supply Over-Voltage Protection above Maximum Voltage Rating**
- **Supply Under-Voltage Protection**
- **Upper MOSFET Direct Shorted Protection**
- **Small SOP-8 Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Core Voltage Supplies for Intel Pentium® 4, AMD® Athlon™ Microprocessors
- High Frequency Low Profile DC-DC Converters
- High Current Low Voltage DC-DC Converters
- IA Equipments

Ordering Information

RT9603 □ □

Package Type
S : SOP-8

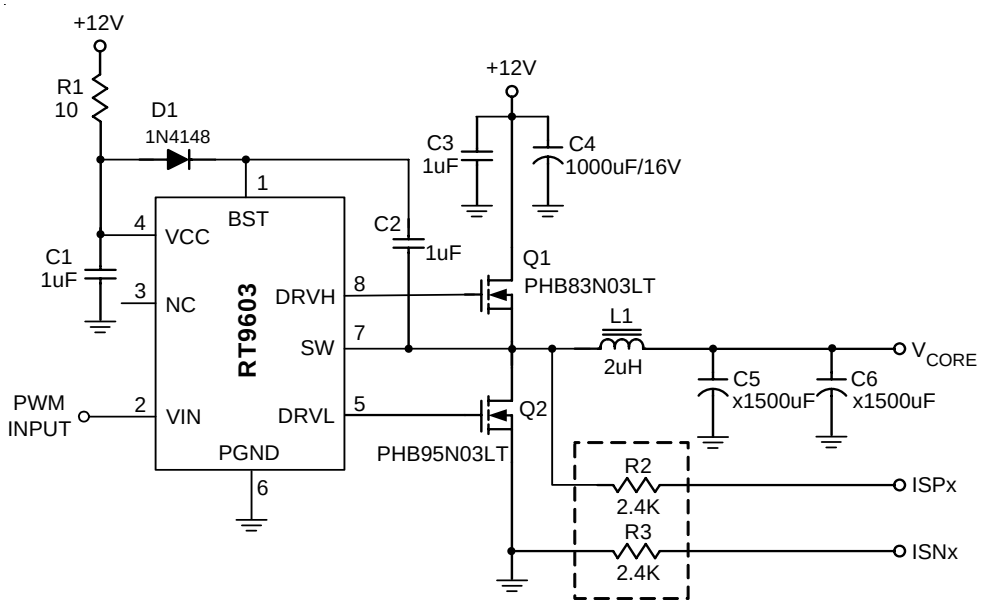
Operating Temperature Range
P : Pb Free with Commercial Standard
G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100%matte tin (Sn) plating.

Typical Application Circuit

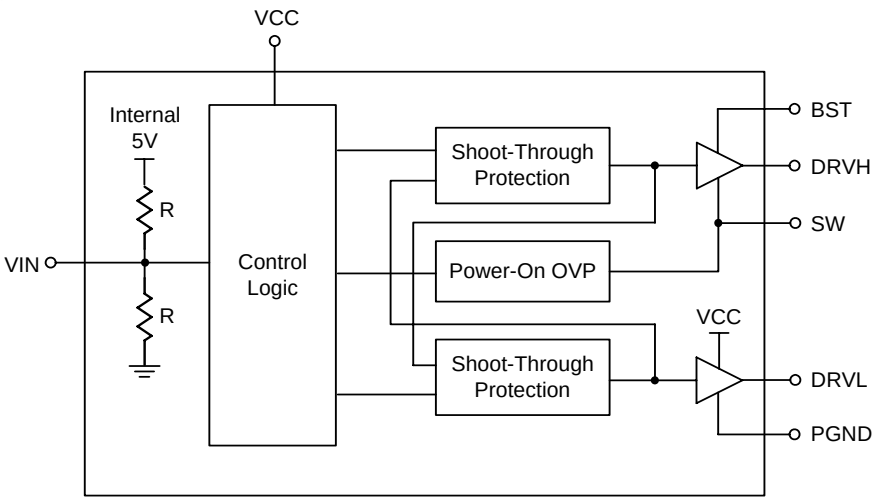


Note: The traces that run from the controller ISPx and ISNx pins, should be run together next to each other and Kelvin connected to the Q2. Place both R2 and R3 as close to the PWM Controller as possible.

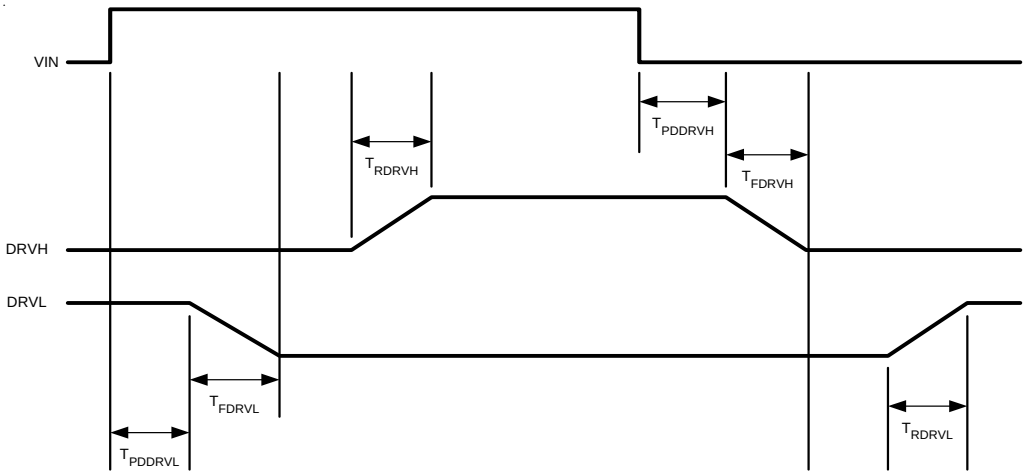
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BST	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the SW pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
2	VIN	Accepts a logic control signal. Connect this pin to the PWM output of the controller. If the PWM signal enters and remains within the shutdown window, the output drivers are disabled and both MOSFET gates are pulled and held low.
3	NC	No Internal Connection.
4	VCC	Supply Input. Connect to +12V supply. Place a bypass capacitor from this pin to PGND.
5	DRVL	Lower gate drive output. Should be connected to the lower MOSFET gate.
6	PGND	Common Ground.
7	SW	Upper driver return. Should be connected to the common node of upper and lower MOSFETs. The SW voltage is monitored for adaptive shoot-through protection.
8	DRVH	Upper gate drive output. Should be connected to the upper MOSFET gate.

Function Block Diagram



Timing Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 15V
- BST to SW ---------- 15V
- SW to GND
  - DC ---------- –5V to 15V
  - < 200ns ---------- –10V to 30V
- BST to GND
  - DC ---------- –0.3V to V_{CC}+15V
  - < 200ns ---------- –0.3V to 42V
- PWM Input Voltage ---------- GND - 0.3V to 7V
- DRVH ---------- V_{SW} - 0.3V to V_{BST} + 0.3V
- DRVL ---------- GND - 0.3V to V_{VCC} + 0.3V
- Power Dissipation, P_D @ T_A = 25°C
- SOP-8 ---------- 0.625W
- Package Thermal Resistance (Note 4)
  - SOP-8, θ_{JA} ---------- 160°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –40°C to 150°C
- ESD Susceptibility (Note 2)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{CC} ---------- 12V ±10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(Recommended Operating Conditions, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Supply Current						
Power Supply Current	I_{VCC}	V_{BST} = 12V, V_{PWM_IN} = 0V	--	5	7	mA
Power-On Reset						
POR Threshold	V_{VCCRTH}	V_{CC} Rising	8.6	9.9	10.7	V
Hysteresis	V_{VCCHYS}		--	1.35	--	V
PWM Input						
Input Current	I_{PWM_IN}	V_{PWM_IN} = 0V or 5V	80	127	150	μA
Floating Voltage	V_{PWMFL}	V_{CC} = 12V	1.1	2.1	3.7	V
PWM_IN Threshold	V_{PWMRTH}	PWM_IN Rising	3.3	3.7	4.3	V
	V_{PWMFTH}	PWM_IN Falling	1.0	1.26	1.5	V
DRVH Rise Time	T_{RDRVH}	V_{VCC} = 12V, 3nF load	--	30	--	ns
DRVH Fall Time	T_{FDRVH}	V_{VCC} = 12V, 3nF load	--	40	--	ns

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DRVL Rise Time	T_{RDRVL}	V_{VCC}= 12V, 3nF load	--	30	--	ns
DRVL Fall Time	T_{FDRVL}	V_{VCC} = 12V, 3nF load	--	30	--	ns
DRVH Turn-Off Propagation Delay	T_{PDDRVH}	V_{VCC} = 12V, 3nF load	--	40	--	ns
DRVL Turn-Off Propagation Delay	T_{PDDRVL}	V_{VCC} = 12V, 3nF load	--	35	--	ns
Shutdown Window			1.0	--	4.3	V
Output						
Upper Drive Source	R_{DRVH}	V_{VCC} = 12V	--	2	--	Ω
Upper Drive Sink	R_{DRVH}	V_{VCC} = 12V	--	2.8	--	Ω
Lower Drive Source	R_{DRVL}	V_{VCC} = 12V	--	1.9	--	Ω
Lower Drive Sink	R_{DRVL}	V_{VCC} = 12V	--	1.6	--	Ω

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended. The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Application Information

The RT9603 is designed to drive both high side and low side N-MOSFET through externally input PWM control signal. It has power-on protection function which held DRVH and DRVL low before VCC up across the rising threshold voltage. After the initialization, the PWM signal takes the control. The rising PWM signal first forces the DRVL signal turns low then DRVH signal is allowed to go high just after a non-overlapping time to avoid shoot-through current. The falling of PWM signal first forces DRVH to go low. When DRVH and SW signal reach a predetermined low level, DRVL signal is allowed to turn high. The non-overlapping function is also presented between DRVH and DRVL signal transient.

The PWM signal is acted as "High" if above the rising threshold and acted as "Low" if below the falling threshold. Any signal level enters and remains within the shutdown window is considered as "tri-state", the output drivers are disabled and both MOSFET gates are pulled and held low. If left the PWM signal (IN) floating, the pin will be kept at 2.1V by the internal divider and provide the PWM controller with a recognizable level.

The RT9603 typically operates at frequency of 200kHz to 250kHz. It shall be noted that to place a 1N4148 or schottky diode between the VCC and BST pin as shown in the typical application circuit.

Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs} at 12V (or 5V), the gate draws the current only few nano-amperes. Thus once the gate has been driven up to "ON" level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

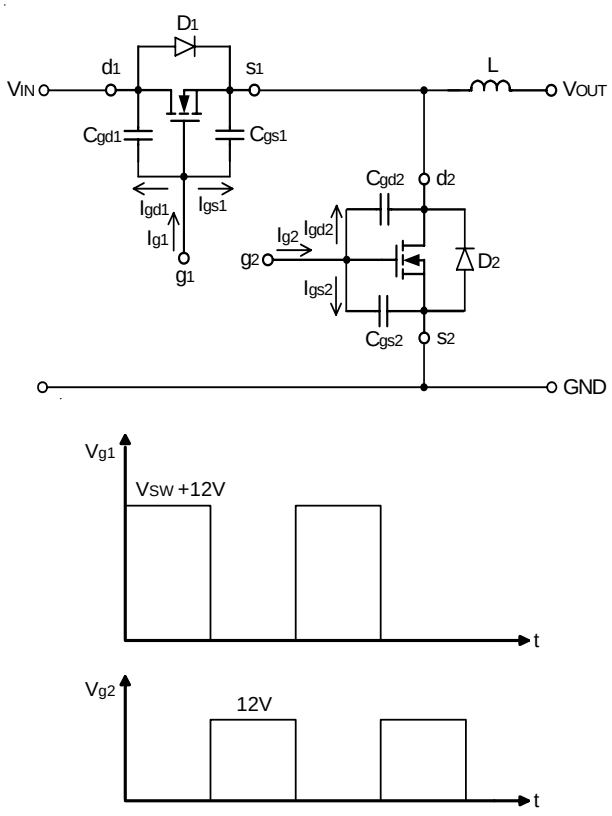


Figure 1. Equivalent Circuit and Associated Waveforms

In Figure 1, the current I_{g1} and I_{g2} are required to move the gate up to 12V. The operation consists of charging C_{gd} and C_{gs}. C_{gs1} and C_{gs2} are the capacitances from gate to source of the high side and the low side power MOSFETs, respectively. In general data sheets, the C_{gs} is referred as "C_{rss}" which is the input capacitance. C_{gd1} and C_{gd2} are the capacitances from gate to drain of the high side and the low side power MOSFETs, respectively and referred to the data sheets as "C_{rss}" the reverse transfer capacitance. For example, t_{r1} and t_{r2} are the rising time of the high side and the low side power MOSFETs respectively, the required current I_{gs1} and I_{gs2} are showed below:

$$I_{gs1} = C_{gs1} \frac{dVg1}{dt} = \frac{C_{gs1} \times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs2} \frac{dVg2}{dt} = \frac{C_{gs2} \times 12}{t_{r2}} \quad (2)$$

Before driving the gate of the high side MOSFET up to 12V (or 5V), the low side MOSFET has to be off; and the high side MOSFET is turned off before the low side is turned on. From Figure 1, the body diode "D_2" had been turned on before high side MOSFETs turned on.

$$I_{gd1} = C_{g1}\frac{dV}{dt} = C_{gd1}\frac{12V}{t_{r1}} \qquad (3)$$

Before the low side MOSFET is turned on, the C_{gd2} have been charged to V_{IN}. Thus, as C_{gd2} reverses its polarity and g_2 is charged up to 12V, the required current is

$$I_{gd2} = C_{gd2}\frac{dV}{dt} = C_{gd2}\frac{Vi+12V}{t_{r2}} \qquad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified buck converter, input voltage V_{IN} = 12V, $V_{g1} = V_{g2}$ = 12V. The high side MOSFET is PHB83N03LT whose C_{iss} = 1660pF, C_{rss} = 380pF, and t_r = 14ns. The low side MOSFET is PHB95N03LT whose C_{iss} = 2200pF, C_{rss} = 500pF and t_r = 30ns, from the equation (1) and (2) we can obtain

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 1.428 \quad (A) \qquad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 12}{30 \times 10^{-9}} = 0.88 \quad (A) \qquad (6)$$

from equation. (3) and (4)

$$I_{gs1} = \frac{380 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 0.326 \quad (A) \qquad (7)$$

$$I_{gd2} = \frac{500 \times 10^{-12} \times (12+12)}{30 \times 10^{-9}} = 0.4(A) \qquad (8)$$

the total current required from the gate driving source is

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.745(A) \qquad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28(A) \qquad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

Layout Consideration

Figure 2 shows the schematic circuit of a two-phase synchronous buck converter to implement the RT9603. The converter operates from 5V to 12V of V_{IN}.

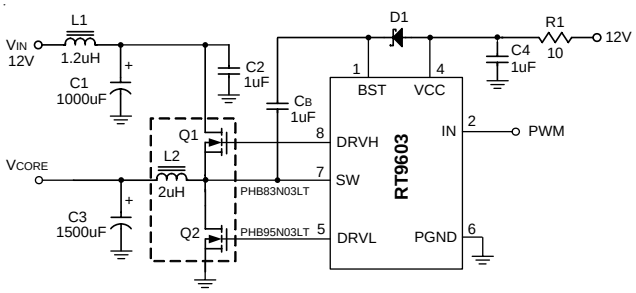


Figure 2. Two-Phase Synch. Buck Converter Circuit

When layout the PCB, it should be very careful. The power-circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The junction of Q1, Q2, L2 should be very close.

Next, the trace from DRVH, and DRVL should also be short to decrease the noise of the driver output signals. SW signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor C4 should be connected to PGND directly. Furthermore, the bootstrap capacitors (C_B) should always be placed as close to the pins of the IC as possible.

Select the Bootstrap Capacitor

Figure 3 shows part of the bootstrap circuit of RT9603. The V_{CB} (the voltage difference between BST and SW on RT9603) provides a voltage to the gate of the high side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance C_B has to be selected properly. It is determined by following constraints.

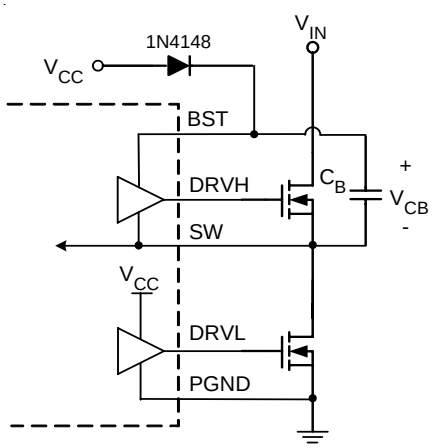


Figure 3. Part of Bootstrap Circuit of RT9603

In practice, a low value capacitor C_B will lead the over-charging that could damage the IC. Therefore to minimize the risk of overcharging and reducing the ripple on V_{CB}, the bootstrap capacitor should not be smaller than 0.1µF, and the larger the better. In general design, using 1µF can provide better performance. At least one low-ESR capacitor should be used to provide good local de-coupling. Here, to adopt either a ceramic or tantalum capacitor is suitable.

Power Dissipation

For not exceeding the maximum allowable power dissipation to drive the IC beyond the maximum recommended operating junction temperature of 125°C, it is necessary to calculate power dissipation appropriately. This dissipation is a function of switching frequency and total gate charge of the selected MOSFET. Figure 4 shows the power dissipation test circuit. C_L and C_U are the DRVH and DRVL load capacitors, respectively. The bootstrap capacitor value is 0.01µF.

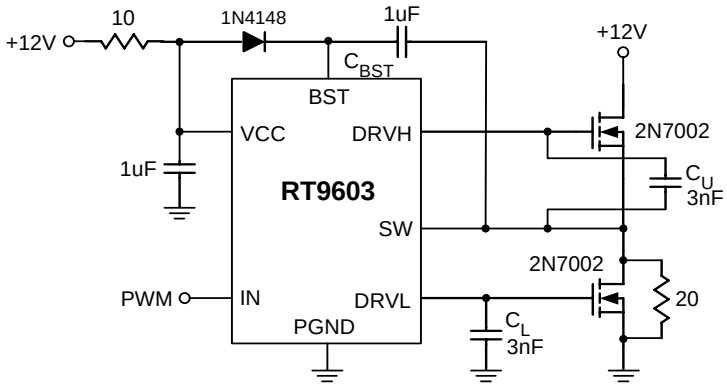


Figure 4. Test Circuit

Figure 5 shows the power dissipation of the RT9603 as a function of frequency and load capacitance. The value of the C_U and C_L are the same and the frequency is varied from 100kHz to 1MHz.

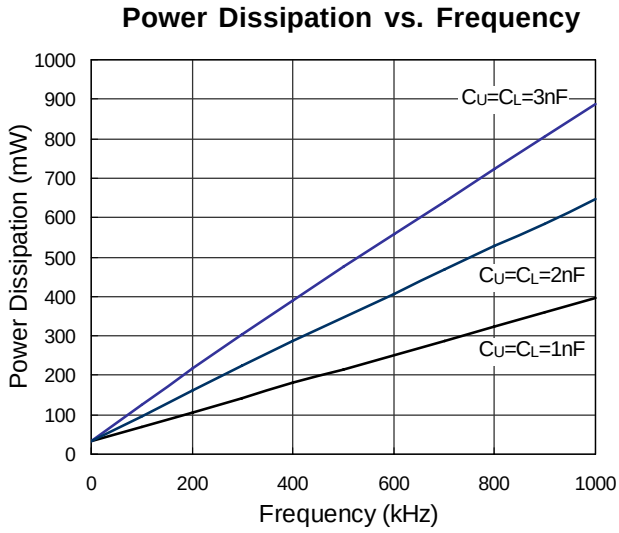


Figure 5. Power Dissipation vs. Frequency

The operating junction temperature can be calculated from the power dissipation curves (Figure 5). Assume VCC=12V, operating frequency is 200kHz and the C_U=C_L=1nF which emulate the input capacitances of the high side and low side power MOSFETs. From Figure 5, the power dissipation is 100mW. For RT9603, the package thermal resistance θ_{JA} is 160°C/W, the operating junction temperature is calculated as :

T_J = (160°C/W x 100mW) + 25°C = 41°C (11)

where the ambient temperature is 25°C.

The method to improve the thermal transfer is to increase the PCB copper area around the RT9603 first. Then, adding a ground pad under IC to transfer the heat to the peripheral of the board.

Over-Voltage Protection Function at Power-On

An unique feature of the RT9603 driver is the addition of over-voltage protection in the event of upper MOSFET direct shorted before power-on. The RT9603 detects the fault condition during initial start-up, the internal power-on OVP sense circuitry will rapidly drive the output lower MOSFET on before the multi-phase PWM controller takes control.

Figure 6 shows the measured waveforms with the high side MOSFET directly shorted to 12V.

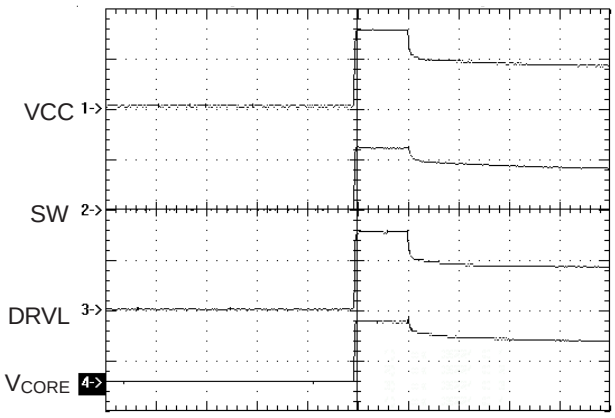
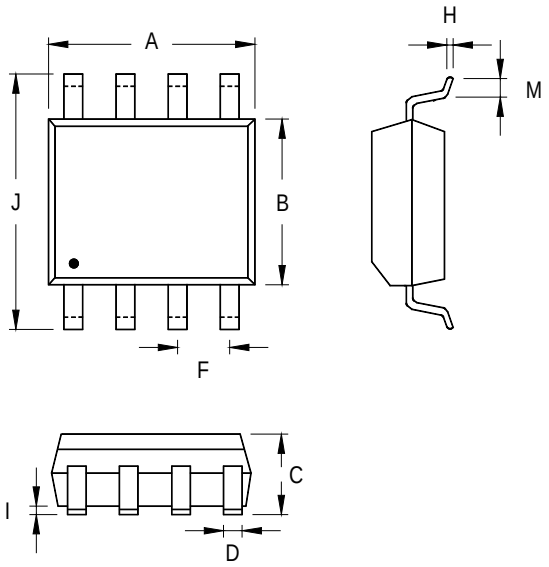


Figure 6. Waveforms at High Side MOSFET Shorted

Please note that the VCC trigger point to RT9603 is at 3V, and the clamped level on SW pin is at about 2.4V. Obviously since the SW pin voltage increases during initial start-up, the V_{CORE} increases correspondingly, but it would quickly drop-off followed by DRVL and VCC decreased.

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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