DATA SHEET

Part No.	MN662793
Package Code No.	LQFP100-P-1414

SEMICONDUCTOR COMPANY
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

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MN662793

Silicon CMOS IC

■ Overview

■ Features

(Optical Servo)

- Focus, tracking, and traverse servos
- Automatic adjustment functions
  (Focus / Tracking gain, Focus / Tracking offset, Focus / Tracking balance)
- Provided with a countermeasure for dropout
- Provided with an anti-shock detection function
- Provided with a track-cross function
- Drive output PWM drive function supported
- Provided with supply voltage monitoring and a servo gain automatic adjustment function

(Digital Signal Processing)

- Containing DSL and analog / digital PLL
- Provided with a frame synchronous detection / protection / interpolation
- Subcode data processing
  Q-data CRC check
  On-chip Q-data register
  On-chip CD-TEXT data register

- CIRC error correction
  C1 decoder: double error correction
  C2 decoder: triple / quadruple error correction
  On-chip deinterleaving 16-K RAM
- CD-ROM error correction
  Q decoder: an error correction
  P decoder: an error correction
  Mode1 and Mode 2 compatible
- Audio data interpolation processing
  4-sampling average value interpolation and previous value hold

(Spindle Motor Servo)

- CLV digital servo
- Servo gain setting function
- Shaft loss compensation setting function

(Audio Circuit)

- Soft muting
- Digital attenuation (2048 levels)
- Soft attenuation (2048 levels)
- Digital audio interface (EIAJ format)
- 8 × -oversampling digital filter
- On-chip low-voltage OP amp
- Bass boost filter, high-band notch filter, and surround function
- On-chip digital de-emphasis

■ Features (continued)

(MP3 Decoding)

- Decoding of asignals recorded in MPEG1-layer3 or MPEG2-layer3 format
- Decoding of asignals recorded in MPEG1-layer2 or MPEG2-layer2 format
- Decoding of asignals recorded in MPEG2.5 format
- Sampling rate conversion from signals recorded at Fs = 32 kHz or 48 kHz to 44.1 kHz

(WMA Decoding)

- Decoding of signals recorded in WMA Ver. 8 format (Sampling rate: 48 kHz to 22.05 kHz)
- Supporting special playback (forward, reverse, and resume playback)

(SD Interface)

- Stream serial input from SD available

(Anti-shock Memory Controller)

- ADPCM 4-bit compression or expansion / decompression in full-bit (16 bits) mode
- External DRAM selectable

  Async DRAM (Data bus width: 4 bits)
  - 64M-bit DRAM × 1
  - 16M-bit DRAM × 2
  - 16M-bit DRAM × 1 + 4M-bit DRAM × 1
  - 16M-bit DRAM × 1
  - 4M-bit DRAM × 2
  - 4M-bit DRAM × 1
  - 1M-bit DRAM × 2
  - 1M-bit DRAM × 1

  Async DRAM (Data bus width: 16 bits)
  - 128M-bit DRAM × 1
  - 64M-bit DRAM × 1
  - 16M-bit DRAM × 1
  - 4M-bit DRAM × 1

  SDRAM (Data bus width: 16 bits)
  - 128M-bit DRAM × 1
  - 64M-bit DRAM × 1
  - 16M-bit DRAM × 1
  - 4M-bit DRAM × 1

(Others)

- Disc rotation mechanism has a synchronous playback (jitter-free) mode (– 50 % to + 50 %)
- 8 × -speed playback (when using jitter-free function)
- TX output (1 × -, 2 × -, 3 ×-and 4 ×-speed) supported
- Serial data output pitch shift function

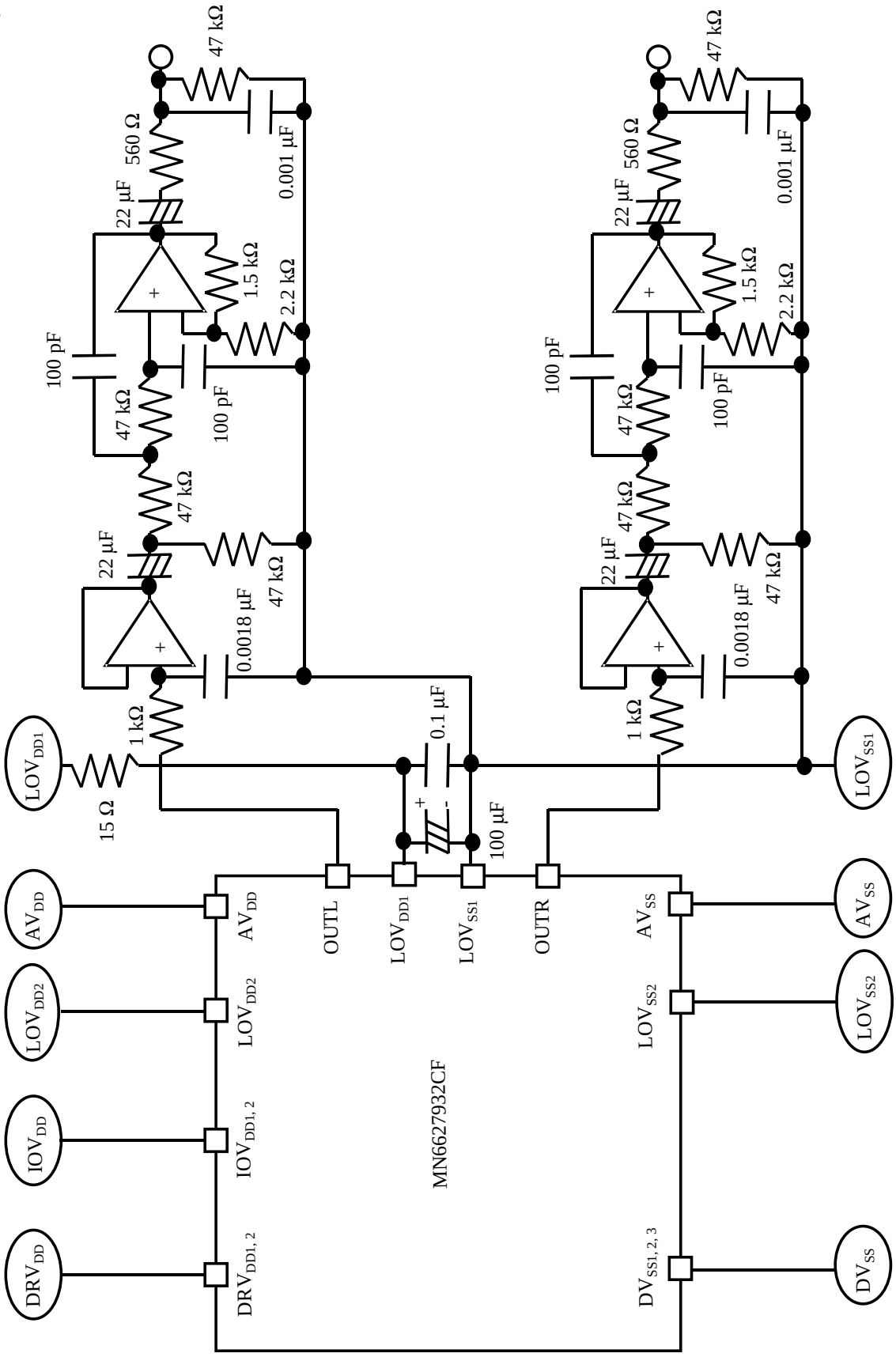
A patent license must be acquired from the management company when using MPEG Layer3 products.

■ Applications

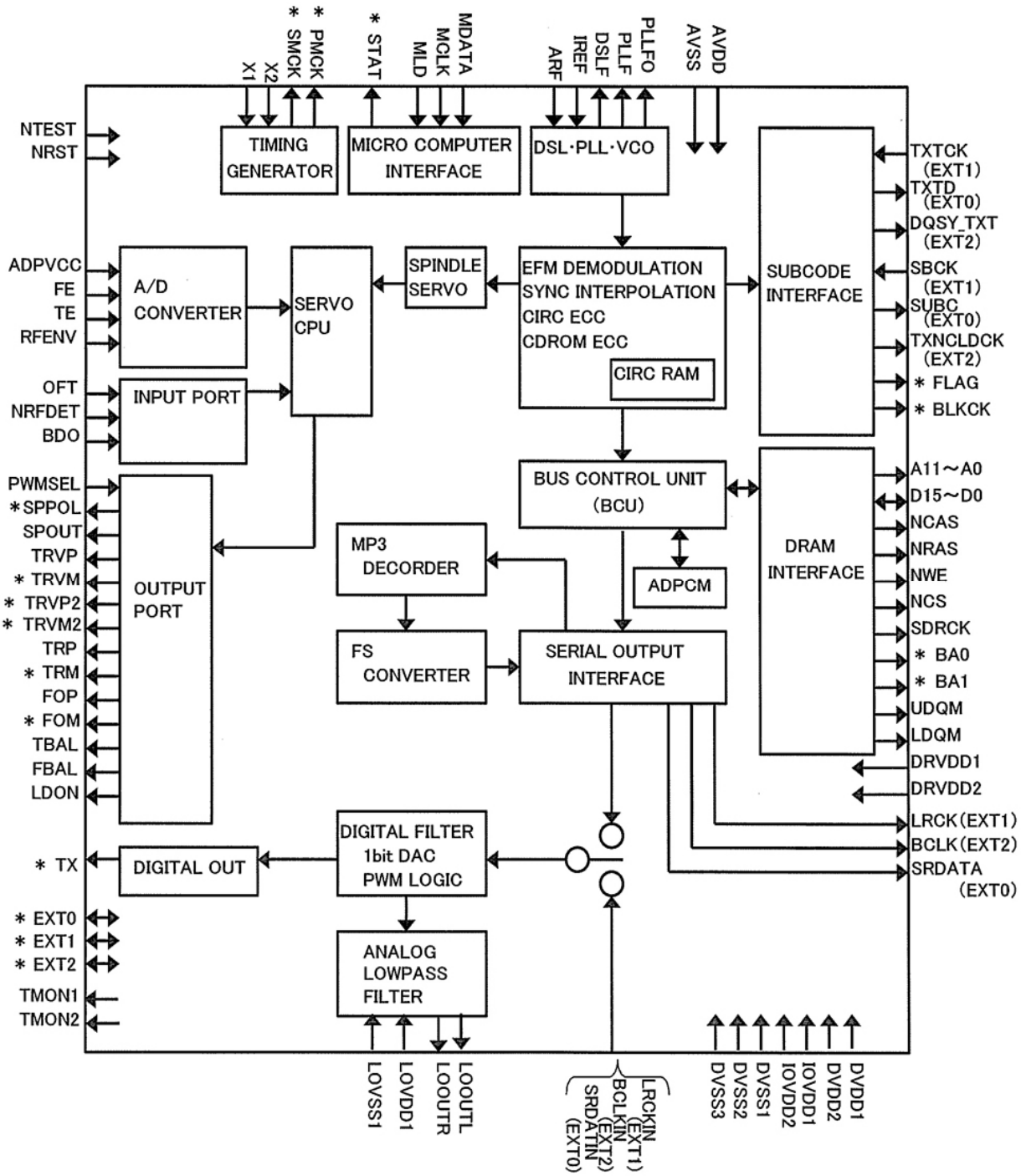
- Signal processing LSI for CDs (Compact Discs)

■ Application Circuit

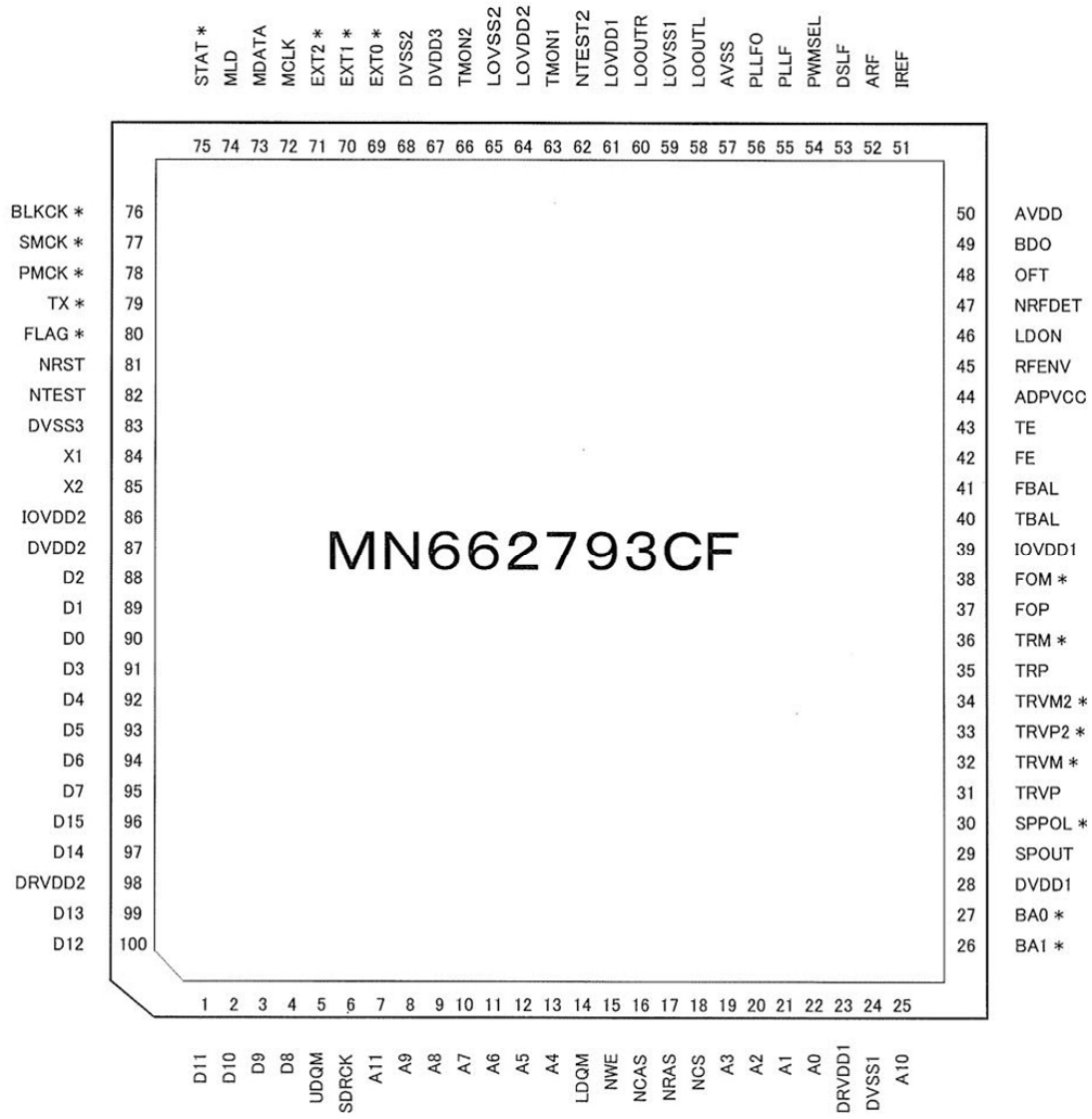
• D/A Converter



■ Block Diagram



■ Pin Arrangement



Note) Pins marked with an asterisk can be switched to different signals by using microcontroller commands.

■ Pin Descriptions

Pin No.	Symbol	I/O	Function
1	D11	I/O	DRAM data signal I/O 11
2	D10	I/O	DRAM data signal I/O 10
3	D9	I/O	DRAM data signal I/O 9
4	D8	I/O	DRAM data signal I/O 8
5	UDQM	O	SDRAM upper byte data mask signal output
6	SDRCK	O	SDRAM clock signal output
7	A11	O	DRAM address signal output 11
8	A9	O	DRAM address signal output 9
9	A8	O	DRAM address signal output 8
10	A7	O	DRAM address signal output 7
11	A6	O	DRAM address signal output 6
12	A5	O	DRAM address signal output 5
13	A4	O	DRAM address signal output 4
14	LDQM	O	SDRAM lower byte data mask signal output
15	NWE	O	DRAM write enable signal output
16	NCAS	O	DRAM CAS control signal output
17	NRAS	O	DRAM RAS control signal output
18	NCS	O	SDRAM chip select signal output
19	A3	O	DRAM address signal output 3
20	A2	O	DRAM address signal output 2
21	A1	O	DRAM address signal output 1
22	A0	O	DRAM address signal output 0
23	DRV_{DD1}	I	Power supply 1 for DRAM interface I/O
24	DV_{SS1}	I	Ground 1 for digital circuits
25	A10	O	DRAM address signal output 10
26	*BA1	O	SDRAM bank selection signal output 1
27	*BA0	O	SDRAM bank selection signal output 0
28	DV_{DD1}	I	Power supply 1 for internal digital circuits
29	SPOUT	O	Spindle drive signal output (absolute value)
30	*SPPOL	O	Spindle drive signal output (polarity)
31	TRVP	O	Traverse drive signal output (positive polarity)

Note) Pins marked with an asterisk can be switched to different signals by using microcontroller commands. The specifications of the DRAM pins depend on their type and capacitance.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function
32	*TRVM	O	Traverse drive signal output (negative polarity)
33	*TRVP2	O	Traverse drive signal output 2 (positive polarity)
34	*TRVM2	O	Traverse drive signal output 2 (negative polarity)
35	TRP	O	Tracking drive signal output (positive polarity)
36	*TRM	O	Tracking drive signal output (negative polarity)
37	FOP	O	Focus drive signal output (positive polarity)
38	*FOM	O	Focus drive signal output (negative polarity)
39	IOV_{DD1}	I	Power supply 1 for digital I/O
40	TBAL	O	Tracking balance adjustment signal output
41	FBAL	O	Focus balance adjustment signal output
42	FE	I	Focus error signal input
43	TE	I	Tracking error signal input
44	$ADPV_{CC}$	I	Voltage input for supply voltage monitor
45	RFENV	I	RF envelope signal input
46	LDON	O	Laser ON signal output
47	NRFDET	I	RF detection signal input
48	OFT	I	Off-track signal input
49	BDO	I	Dropout signal input
50	AV_{DD}	I	Power supply for analog circuits
51	I_{REF}	I	Analog reference current input
52	ARF	I	RF signal input
53	DSLF	O	DSL loop filter pin
54	PWMSEL	I	PWM output mode selection input Low: Direct High: 3-state
55	PLLF	O	PLL loop filter pin (for phase comparison output)
56	PLLFO	O	PLL loop filter pin (for speed comparison output)
57	AV_{SS}	I	Ground for analog circuits
58	LOOUTL	O	L-ch. audio output for line-out output
59	LOV_{SS1}	I	Ground for line-out output
60	LOOUTR	O	R-ch. audio output for line-out output
61	LOV_{DD1}	I	Power supply for line-out output
62	NTEST2	I	Test mode setting input (L fix)
63	TMON1	O	Test monitor output 1

Note) Pins marked with an asterisk can be switched to different signals by using microcontroller commands.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function
64	LOV_{DD2}	I	Power supply for Audio output
65	LOV_{SS2}	I	Ground for Audio output
66	TMON2	O	Test monitor output 2
67	DV_{DD3}	I	Power supply 3 for digital circuits
68	DV_{SS2}	I	Ground 2 for digital circuits
69	*EXT0	I/O	Expansion I/O port 0
70	*EXT1	I/O	Expansion I/O port 1
71	*EXT2	I/O	Expansion I/O port 2
72	MCLK	I	Microcontroller command clock signal input
73	MDATA	I	Microcontroller command data signal input
74	MLD	I	Microcontroller command load signal input
75	*STAT	O	Status signal output
76	*BLKCK	O	Subcode block clock signal output
77	*SMCK	O	4.2336 MHz / 8.4672 MHz clock signal output
78	*PMCK	O	88.2 kHz clock signal output
79	*TX	O	Digital audio interface signal output
80	*FLAG	O	Flag signal output
81	NRST	I	LSI reset signal input
82	NTEST	I	Test mode setting input
83	DV_{SS3}	I	Ground 3 for digital circuits
84	X1	I	Crystal oscillator circuit input
85	X2	O	Crystao oscillator circuit output
86	IOV_{DD2}	I	Power supply 2 for digital I/O
87	DV_{DD2}	I	Power supply 2 for internal digital circuits
88	D2	I/O	DRAM data signal I/O 2
89	D1	I/O	DRAM data signal I/O 1
90	D0	I/O	DRAM data signal I/O 0
91	D3	I/O	DRAM data signal I/O 3
92	D4	I/O	DRAM data signal I/O 4
93	D5	I/O	DRAM data signal I/O 5
94	D6	I/O	DRAM data signal I/O 6
95	D7	I/O	DRAM data signal I/O 7

Note) Pins marked with an asterisk can be switched to different signals by using microcontroller commands.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function
96	D15	I/O	DRAM data signal I/O 15
97	D14	I/O	DRAM data signal I/O 14
98	DRV_{DD2}	I	Power supply 2 for DRAM interface I/O
99	D13	I/O	DRAM data signal I/O 13
100	D12	I/O	DRAM data signal I/O 12

Note) Pins marked with an asterisk can be switched to different signals by using microcontroller commands. The specifications of the DRAM pins depend on their type and capacitance.

■ Absolute Maximum Ratings T_a = 25°C±2°C

Parameter		Symbol	Rating	Unit	Note
A1	Supply voltage	$DRV_{DD1, 2}$ $IOV_{DD1, 2}$ AV_{DD} $LOV_{DD1, 2}$	– 0.3 to + 4.6	V	$DV_{SS1, 2, 3}$ = 0 V AV_{SS} = 0 V $LOV_{SS1, 2}$ = 0 V
A2	Internal supply voltage	$DV_{DD1, 2, 3}$	– 0.3 to + 2.0	V	$DV_{SS1, 2}$ = 0 V $AV_{SS1, 2}$ = 0 V $LOV_{SS1, 2}$ = 0 V
A3	Input voltage	V_I	$DV_{SS1, 2, 3}$ – 0.3 to $DRV_{DD1, 2}$ + 0.3 (Upper limit: 4.6 V) $DV_{SS1, 2, 3}$ – 0.3 to $IOV_{DD1, 2}$ + 0.3 (Upper limit: 4.6 V) AV_{SS} – 0.3 to AV_{DD} + 0.3 (Upper limit: 4.6 V) $LOV_{SS1, 2}$ – 0.3 to $LOV_{DD1, 2}$ + 0.3 (Upper limit: 4.6 V)	V	$DV_{SS1, 2, 3}$ = 0 V AV_{SS} = 0 V $LOV_{SS1, 2}$ = 0 V
A4	Output voltage	V_O	$DV_{SS1, 2, 3}$ – 0.3 to $DRV_{DD1, 2}$ + 0.3 (Upper limit: 4.6 V) $DV_{SS1, 2, 3}$ – 0.3 to $IOV_{DD1, 2}$ + 0.3 (Upper limit: 4.6 V) AV_{SS} – 0.3 to AV_{DD} + 0.3 (Upper limit: 4.6 V) $LOV_{SS1, 2}$ – 0.3 to $LOV_{DD1, 2}$ + 0.3 (Upper limit: 4.6 V)	V	$DV_{SS1, 2, 3}$ = 0 V AV_{SS} = 0 V LOV_{SS1} = 0 V
A5	Power dissipation	P_D	560	mW	$DV_{SS1, 2, 3}$ = 0 V AV_{SS} = 0 V $LOV_{SS1, 2}$ = 0 V
A6	Operating ambient temperature	T_{OPR}	– 30 to + 85	°C	
A7	Storage temperature	T_{STG}	– 50 to + 125	°C	

Note) 1. The absolute maximum ratings are the limit values beyond which the IC may be broken. They do not assure operations.

2. Connect each of the DV_{SS1} , DV_{SS2} , DV_{SS3} , AV_{SS} and $LOV_{SS1, 2}$ pins directly to ground and use at the same voltage.

3. Connect each of the DRV_{DD1} , DRV_{DD2} , IOV_{DD1} , IOV_{DD2} , AV_{DD} and $LOV_{DD1, 2}$ pins directly to the specified power supply and use at the same voltage.

4. DRV_{DD} , IOV_{DD1} , IOV_{DD2} , AV_{DD1} and AV_{DD2} should be powered up at the same time before power up the DV_{DD1} , DV_{DD2} , DV_{DD3} pins at the same time when not using an internal regulator.

5. Connect a bypass capacitor of 0.1 µF or larger between each of the power supply pins and ground.

■ Operating Supply Voltage Range T_a = –30°C ~ +85°C, $DV_{SS1, 2, 3}$ = 0 V, AV_{SS} = 0 V, $LOV_{SS1, 2}$ = 0 V

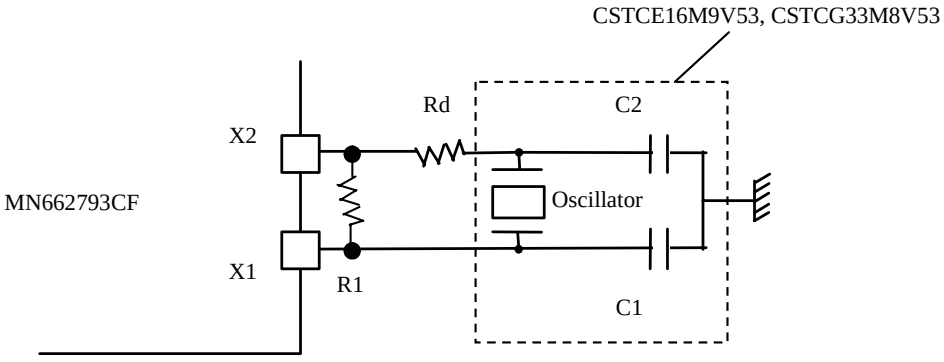
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
B1	I/O system supply voltage	$IOV_{DD1, 2}$		2.2	3.3	3.6	V
B2	Digital system supply voltage	$DV_{DD1, 2, 3}$		1.35	1.5	1.65	V
B3	Analog system supply voltage	AV_{DD}		2.4	3.3	3.6	V
B4	Audio system 1 supply voltage	LOV_{DD1}		2.4	3.3	3.6	V
B5	Audio system 2 supply voltage	LOV_{DD2}		2.0	2.5	3.6	V
B6	D-RAM interface voltage	$DRV_{DD1, 2}$		2.2	3.3	3.6	V

■ Operating Supply Voltage Range (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Self-excited Oscillation 1 *1							
B7	Oscillator frequency	fxtal	16.9344 MHz Oscillator *2		16.9344		MHz
B8	Recommended external capacitance 1	C1			15		pF
B9	Recommended external capacitance 2	C2			15		
B10	Recommended external feedback resistance	R1			1		MΩ
B11	Recommended external dumping resistance	Rd			470		Ω
Self-excited Oscillation 2 *1							
B12	Oscillator frequency	fxtal	33.8688 MHz Oscillator *3		33.8688		MHz
B13	Recommended external capacitance 1	C1			15		pF
B14	Recommended external capacitance 2	C2			15		
B15	Recommended external feedback resistance	R1			1		MΩ
B16	Recommended externaldumping resistance	Rd			100		Ω

Note) *1: Oscillation circuit



*2: Values for C1 and C2 specified above are standard values when use CSTCE16M9V53 made in Murata Manufacturing Co., Ltd. as an oscillator. However, CSTCE16M9V53 builds in C1 and C2 of the above standard value. The appropriate capacitors' values differ according to the oscillator used. Use the values specified by the oscillator manufacturer.

*3: Values for C1 and C2 specified above are standard values when use CSTCG33M8V53 made in Murata Manufacturing Co., Ltd. as an oscillator. However, CSTCG33M8V53builds in C1 and C2 of the above standard value. The appropriate capacitors' values differ according to the oscillator used. Use the values specified by the oscillator manufacturer.

■ Electrical Characteristics

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(1) DC Characteristics

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
C1	Supply current	I_{DD}	Anti-shock memory function used. No external load connected. (in 2x-speed playback mode) ADPCM compression: ON MP3 decode: OFF CD-ROM decode: OFF Digital PLL: OFF		22	65	mA
C2	I/O / analog system supply current	$I_{DD(A, L1)}$			12	24	mA
C3	Audio system 2 current	$I_{DD(L2)}$			8	20	mA
C4	Total power consumption	P_T			92.6	227	mW
C5	Supply current	I_{DD}	Anti-shock memory function used. No external load connected. (in 4x-speed playback mode) MP3 decode: ON CD-ROM decode: ON Digital PLL: OFF		24	70	mA
C6	I/O / analog system supply current	$I_{DD(A, L1)}$			14	28	mA
C7	Audio system 2 current	$I_{DD(L2)}$			2	20	mA
C8	Total power consumption	P_T			102.2	247	mW
C9	Supply current	I_{DD}	Anti-shock memory function used. No external load connected. (in 4x-speed playback mode) WMA decode: ON CD-ROM decode: ON Digital PLL: OFF		25	75	mA
C10	I/O / analog system supply current	$I_{DD(A, L1)}$			16	32	mA
C11	Audio system 2 current	$I_{DD(L2)}$			8	20	mA
C12	Total power consumption	P_T			110.3	278	mW
C13	Supply current	I_{DD}	Anti-shock memory function used. No external load connected. (in 8x-speed playback mode) MP3 decode: OFF CD-ROM decode: OFF Digital PLL: OFF		24	70	mA
C14	I/O / analog system supply current	$I_{DD(A, L1)}$			16	32	mA
C15	Audio system 2 current	$I_{DD(L2)}$			8	20	mA
C16	Total power consumption	P_T			108.8	261	mW

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(1) DC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Input Pins 1 DRV_{DD} voltage type		D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15					
C17	High-level input voltage	V_{IH1}		2.31		3.30	V
C18	Low-level input voltage	V_{IL1}		0.0		0.99	V
C19	Input leakage current	I_{LK1}	V_{IN} = 0 V or 3.3 V			± 1	µA
Input Pins 2 IOV_{DD} voltage type		EXT0, EXT1, EXT2, MCLK, MDATA, MLD, NRST, TEST					
C20	High-level input voltage	V_{IH2}		2.31		3.30	V
C21	Low-level input voltage	V_{IL2}		0.0		0.99	V
C22	Input leakage current	I_{LK2}	V_{IN} = 0 V or 3.3 V			± 1	µA
Input Pins 3 AV_{DD} voltage type		NRFDET, OFT , BDO, PWMSEL					
C23	High-level input voltage	V_{IH3}		2.31		3.30	V
C24	Low-level input voltage	V_{IL3}		0.0		0.99	V
C25	Input leakage current	I_{LK3}	V_{IN} = 0 V or 3.3 V			± 1	µA

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(1) DC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Output Pins 1 DRV_{DD} voltage type D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, UDQM, LDQM, SDRCK, NWE, NCAS, NRAS, NCS							
C26	High-level output voltage	V_{OH1}	I_{OH1} = – 1.0 mA	2.7			V
C27	Low-level output voltage	V_{OL1}	I_{OL1} = 1.0 mA			0.4	V
Output Pins 2 DRV_{DD} voltage type BA0, BA1							
C28	High-level output voltage	V_{OH2}	I_{OH2} = – 1.0 mA	2.7			V
C29	Low-level output voltage	V_{OL2}	I_{OL2} = 1.0 mA			0.4	V
C30	Output leakage current	O_{LK2}	Hi-Z state V_O = 0 V or 3.3 V			± 1	μΩ
Output Pins 3 IOV_{DD} voltage type SPPOL, TRVM, TRM, FOM, STAT, TX							
C31	High-level output voltage	V_{OH3}	I_{OH3} = – 1.0 mA	2.7			V
C32	Low-level output voltage	V_{OL3}	I_{OL3} = 1.0 mA			0.4	V
Output Pin 4 IOV_{DD} voltage type SPOUT, TRVP, TRVP2, TRVM2, TRP, FOP, TMON1, TMON2, EXT0, EXT1, EXT2, BLKCK, SMCK, PMCK, FLAG							
C33	High-level output voltage	V_{OH4}	I_{OH4} = – 1.0 mA	2.7			V
C34	Low-level output voltage	V_{OL4}	I_{OL4} = 1.0 mA			0.4	V
C35	Output leakage current	O_{LK4}	Hi-Z state V_O = 0 V or 3.3 V			± 1	μA
Output Pins 5 AV_{DD} voltage type LDON							
C36	High-level output voltage	V_{OH5}	I_{OH5} = – 1.0 mA	2.7			V
C37	Low-level output voltage	V_{OL5}	I_{OL5} = 1.0 mA			0.4	V
C38	Output leakage current	O_{LK5}	Hi-Z state V_O = 0 V or 3.3 V			± 1	μA

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(1) DC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Analog System Input Pin 1 I_{REF}							
C39	Input current	I_{REF}	When pulled up with an 82-k Ω resistor.	18	29	41	μA
Analog System Input Pin 2 ARF							
C40	nput signal amplitude	V_{ARF}	EFM signal input level in an application circuit of DSL block.	0.5	1.0		V[P-P]
C41	Internal resistance between ARF and DSLF pins	R_{ARF}	REGSEL: R1 + R2 + R3 setting	65	100	135	kΩ
			REGSEL: R2 + R3 setting	26	40	54	
			REGSEL: R3 setting	13	20	27	
			REGSEL: R1 + R2 + R3 and RFSW = ON setting	32	50	68	
Analog System Input Pin 3 TE, FE, RFENV, $ADPV_{CC}$							
C42	High-level input voltage	V_{IH4}				2.97	V
C43	Low-level input voltage	V_{IL4}		0.33			V
LOV_{DD2} System Input Pin 5 NTEST2							
C44	High-level input voltage	V_{IH5}		1.75		2.50	V
C45	Low-level input voltage	V_{IL5}		0.00		0.75	V
C46	Input leakage current	I_{LK5}				± 1.0	μA
A/D Converter (for servo)							
C47	Resolution	RES				8	bit
C48	Integral nonlinearity	INL	A/D output = 99 to 66 (2's complement)			± 2	LSB
C49	Differential nonlinearity	DNL				± 3	

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

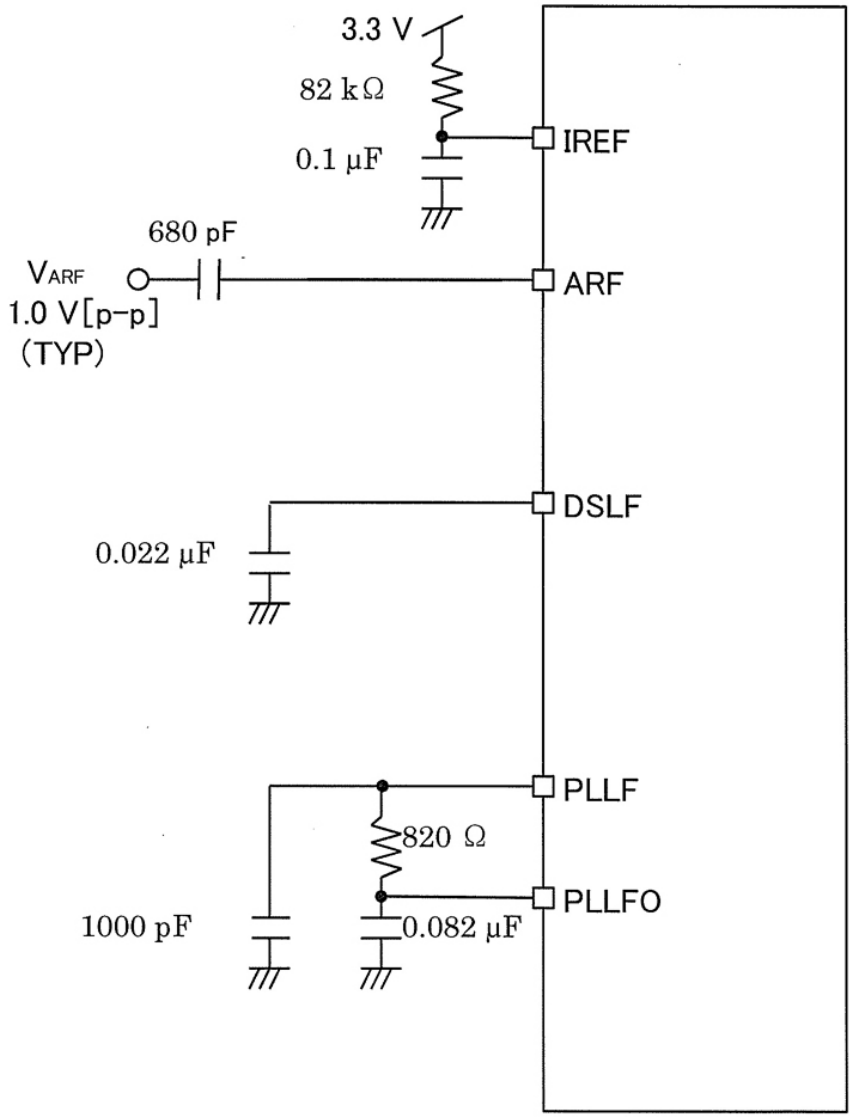
(1) DC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Analog System Output Pin 1		DSLF (I_{REF} pin is pulled up to AV_{DD} with an 82 kΩ resistor)					
C50	Output current (N)	I_{DSH}	BDO: Low, Tracking ON state DSLF = 1.65 V	56	80	104	µA
C51	Output current (P)	I_{DSH}	BDO: Low, Tracking ON state DSLF = 1.65 V	– 104	– 80	– 56	
C52	Output unbalance current	I_{DSEL}	BDO: Low, Tracking ON state Normal current mode	– 7	0	7	
Analog System Output Pin 2		PLLF (I_{REF} pin is pulled up to AV_{DD} with an 82 kΩ resistor)					
C53	Phase comparator output current (N)	I_{PFH}	PLLF = 1.65 V	56	80	104	µA
C54	Phase comparator output current (P)	I_{PFH}	PLLF = 1.65 V	– 104	– 80	– 56	
C55	Input leakage current	I_{LKP}	Hi-Z state			± 1	
C56	Output unbalance current	I_{PLBL}	PLLF = 1.65 V	– 10	0	10	
C57	VCO oscillator frequency for PLL	$f_{VCO}1$		25.9		103.7	MHz
Analog System Output Pin 3		PLLFO (I_{REF} pin is pulled up to AV_{DD} with an 82 kΩ resistor)					
C58	Output current (N)	I_{PFHO}		59	85	111	µA
C59	Output current (P)	I_{PFHO}		– 111	– 85	– 59	
C60	Input leakage current	I_{LKPO}	Hi-Z state			± 1	
Analog System Output Pin 4		TBAL, FBAL (I_{REF} pin is pulled up to AV_{DD} with an 82 kΩ resistor)					
C61	Output current (N)	I_{BAH}	At default setting (× 1)	15	22	29	µA
C62	Output current (P)	I_{BAL}	At default setting (× 1)	– 29	– 22	– 15	

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(1) DC Characteristics (continued)



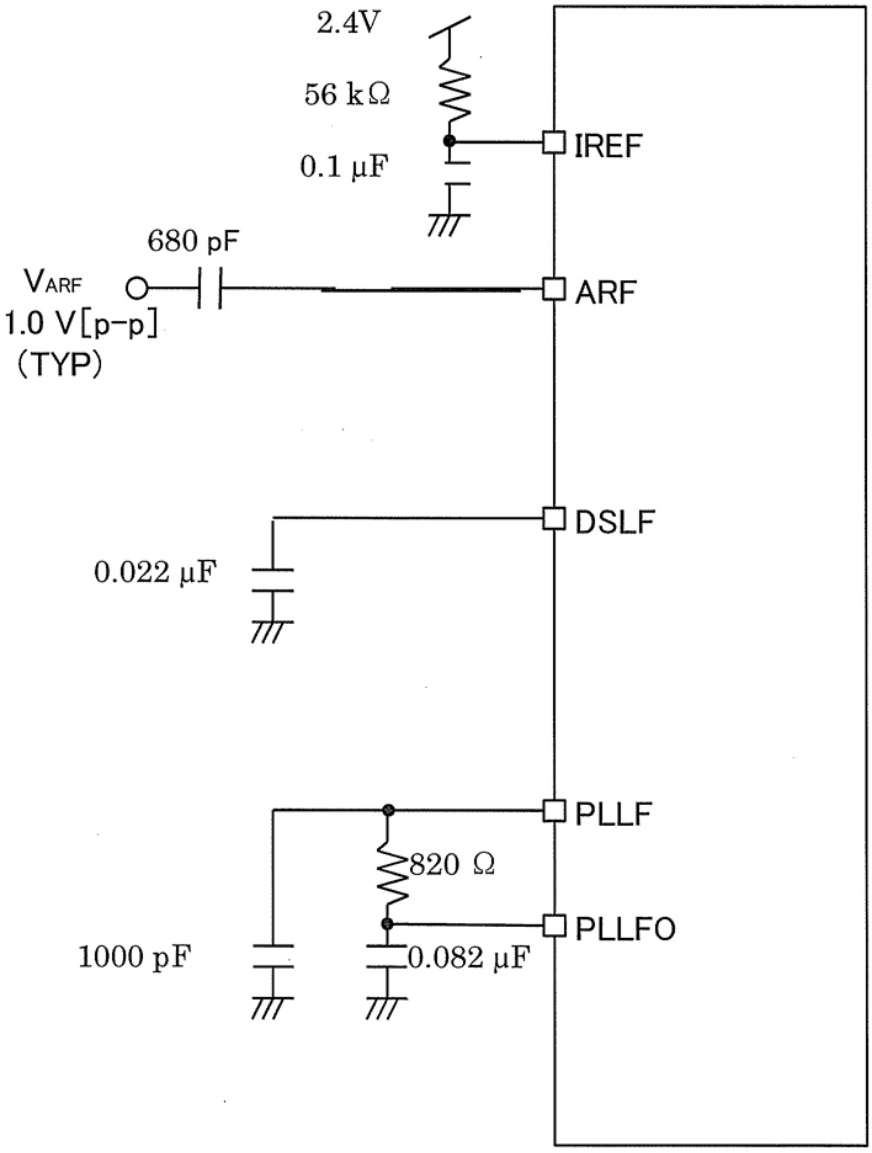
Recommended Circuit for DSL and PLL Blocks (AVDD = 3.3V)

Note) The above is a basic circuit. Calculate the constants and other factors of the circuit in consideration of playability when making use of this circuit for actual applications.

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(1) DC Characteristics (continued)



Recommended Circuit for DSL and PLL Blocks (AVDD = 2.4 V)

Note) The above is a basic circuit. Calculate the constants and other factors of the circuit in consideration of playability when making use of this circuit for actual applications.

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(1) DC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D/A Converter Analog Characteristics							
C63	Signal-to-noise ratio	S/N	EIAJ	90	97		dB
C64	Dynamic range	D. R.	EIAJ	86	94		dB
C65	Total harmonic distortion ratio	THD + N	EIAJ		0.005	0.009	%
C66	Crosstalk		EIAJ	80	85		dB
C67	Output level 1		1 kHz F. S. *1	1.04	1.33	1.62	V[rms]
C68	Output level difference		Difference between OUTL and OUTR pins at output level 20 log (VR / VL)	– 0.99		+ 0.99	dB
C69	Output level 2		1 kHz F.S. *2	0.69	0.88	1.07	V[rms]

Note) 1. The analog characteristics show the measured values when inserting a 15 0Ω resistor between LOV_{DD1} and power supply.
The analog characteristics is prescribed when LOVDD1 voltage is 3.3V.
The above typical values are only reference values and not guaranteed.

2. With no anti-shock memory function used, the operation of the D/A converter will not be guaranteed in modes other than normal-speed playback.

3. *1: The output level 1 shows the measured value at the output pin of the application circuit below.
*2: The output level 2 shows a value at the output pin of the IC and is calculated by taking the measured value of output level 1, dividing it by the circuit gain.

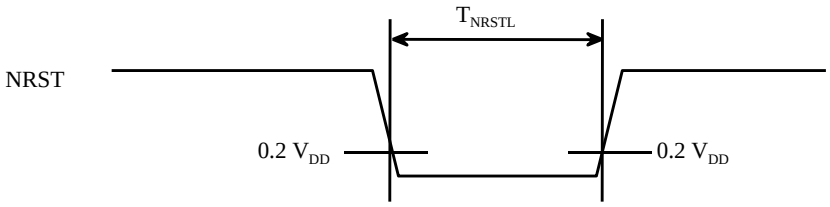
■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

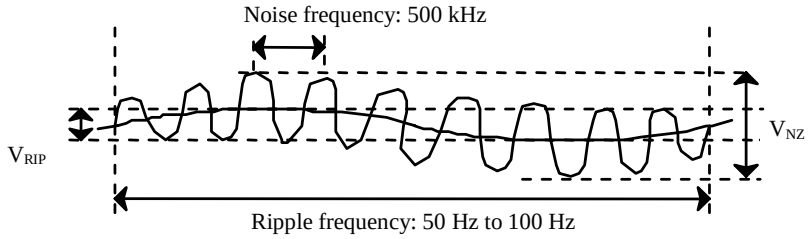
(2) AC Characteristics

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Reset Timing *1							
C70	NRST pulse width	T_{NRSTL}		200			µs
Power Supply Ripple Noise *2							
C71	Ripple amplitude	V_{RIP}				15	mV[p-p]
C72	Ripple noise amplitude	V_{NZ}				30	mV[p-p]

Note) *1: When the power is turned on, reset with the NRST pulse which is equal to or exceeds the above pulse width only after the clock oscillation is stabilized within ±10% of error of the specified oscillator frequency. Keep noise on the reset line as low as possible.



*2: The standard ripple noise values of the IC are guaranteed on condition that the values apply to typical 50-Hz to 100-Hz ripples with 500 kHz typical noise and that both the ripples and noise are in sine waveform as shown below.
The values, however, vary under the influence of other parts located on the PCB.
Therefore, be sure to apply the IC to practical applications and check the actual ripple noise values.

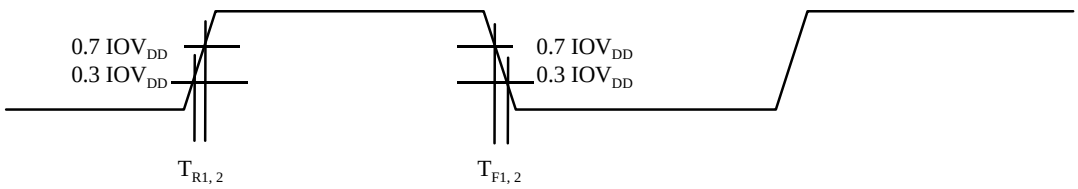


■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Transition Time 1 MCLK, MLD							
C73	Rise time	T_{R1}				250	ns
C74	Fall time	T_{F1}				250	ns
Transition Time 2 * SBCK, TXTCK							
C75	Rise time	T_{R2}				50	ns
C76	Fall time	T_{F2}				50	ns



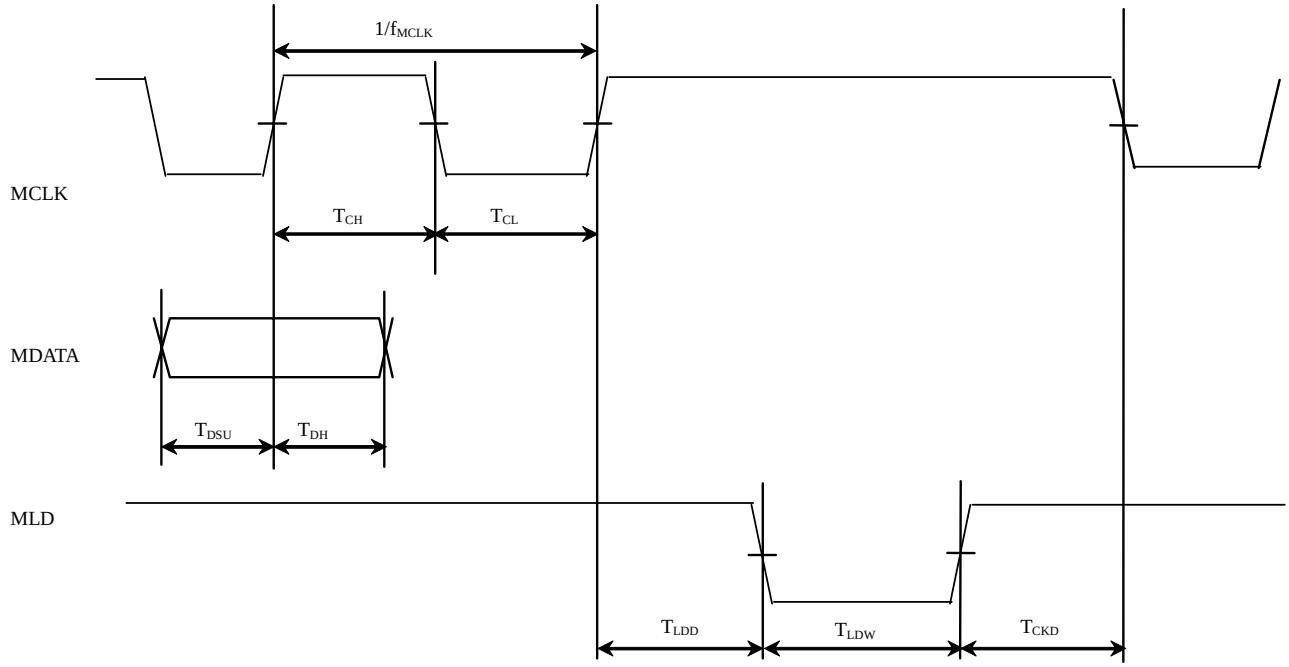
Note) *: SBCK and TXTCK are output from EXT1.

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Microcontroller Command Input Timing							
C77	Clock frequency	f_{MCLK}				2	MHz
C78	Clock pulse width	$T_{CH,CL}$		150			ns
C79	Data setup time	T_{DSU}		150			ns
C80	Data hold time	T_{DH}		150			ns
C81	MLD delay time	T_{LDD}		150			ns
C82	Latch pulse time	T_{LDW}		0.5		10	µs
C83	MCLK delay time	T_{CKD}		300			ns

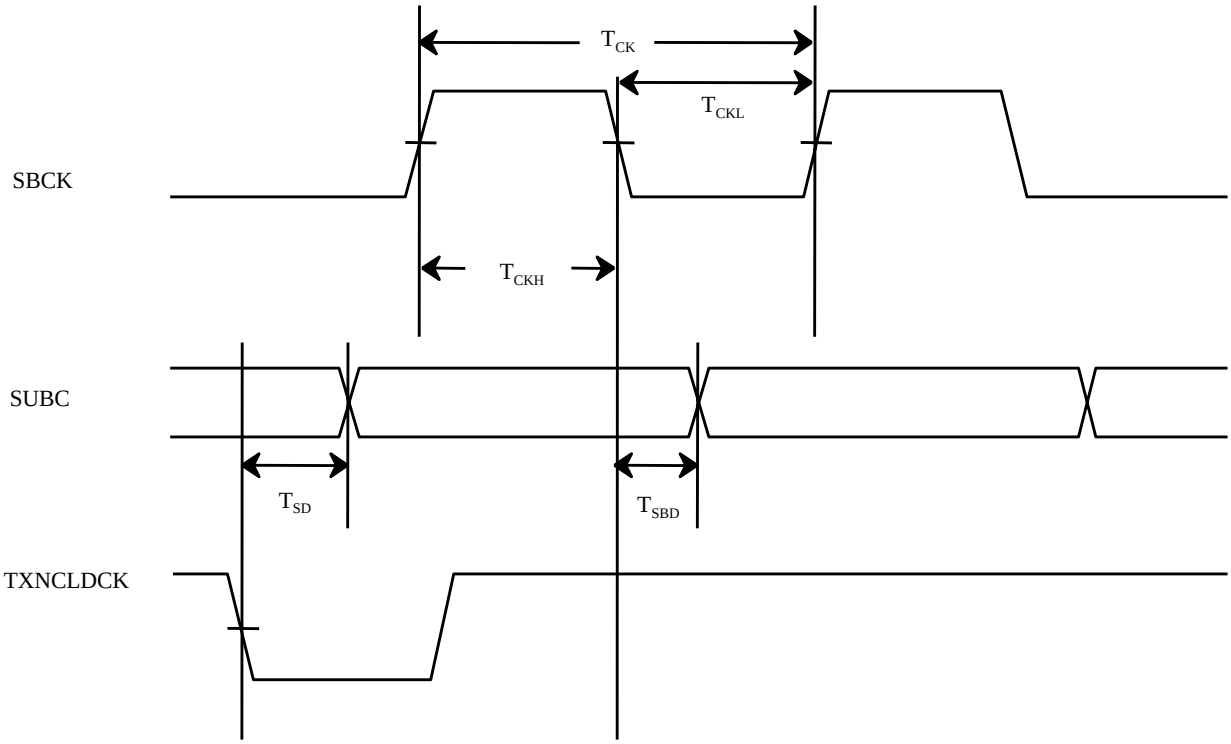


■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Sub code Interface *1 SBCK, SUBC, TXNCLDCK							
C84	Clock width	T_{CK}		909			ns
C85	High-level pulse width	T_{CKH}		400			ns
C86	Low-level pulse width	T_{CKL}		400			ns
C87	Delay time	T_{SBD}	When digital filter is used. *2			350	ns
			When no filter is used. *2			173	ns
C88	Setup delay time	T_{SD}				150	ns



Note) *1: SBCK is output from EXT1, SUBC is output from EXT0, and TXNCLDCK is output from EXT2.

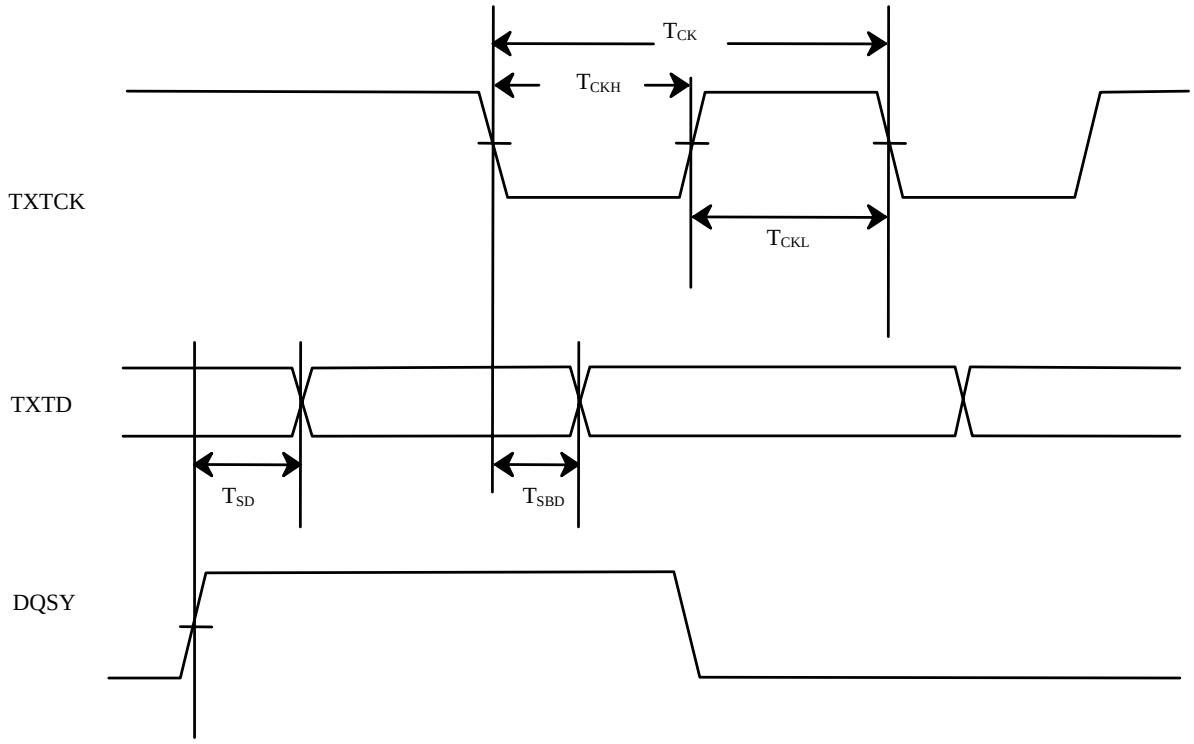
*2: SBCK,TXTCK noise filter command is SBCKNF (by setting the D5 and D4 bits of the 67 command) .

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Subcode Interface TXTCK, TXTD, DQSY							
C89	Clock frequency	T_{CK}		2500			ns
C90	High-level pulse width	T_{CKH}		1200			ns
C91	Low-level pulse width	T_{CKL}		1200			ns
C92	Delay time	T_{SBD}				1150	ns
C93	Setup delay time	T_{SD}				1100	ns



Note) 1. TXTCK is input or output from EXT1, TXTD is input or output from EXT0, and DQSY is input or output from EXT2.

2. The cycle width of the readout clock TXTCK is proportional to disc rotation speed. High-speed readout such as high-speed CLV playback or high-speed jitter-free playback using MSON (Memory system setting) is possible.

Example) When in 2x speed mode

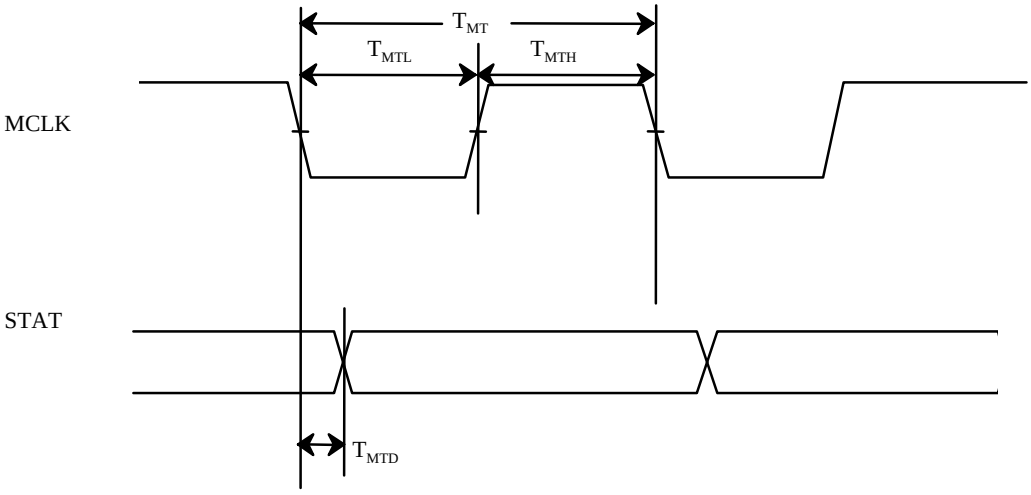
T_{SBD2} = 450 ns (Typ.)

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
STAT Output Interface (When analog filter 1 is used.)							
C94	Clock width	T_{MT}		909			ns
C95	High-level pulse width	T_{MTH}		300			ns
C96	Low-level pulse width	T_{MTL}		300			ns
C97	Delay time	T_{MTD}				225	ns
STAT Output Interface (When analog filter 2 is used.)							
C98	Clock width	T_{MT}		500			ns
C99	High-level pulse width	T_{MTH}		220			ns
C100	Low-level pulse width	T_{MTL}		220			ns
C101	Delay time	T_{MTD}				200	ns
STAT Output Interface (When no noise filter is used.)							
C102	Clock width	T_{MT}		500			ns
C103	High-level pulse width	T_{MTH}		220			ns
C104	Low-level pulse width	T_{MTL}		220			ns
C105	Delay time	T_{MTD}				173	ns



Note) 1. In multiple-byte read mode using REGRD command (96h), VWA_ID command (97h), or VWAIDRD command (98h), it is necessary to set the high-level pulse width T_{MTH} to more than 450 ns in 1-byte increments.

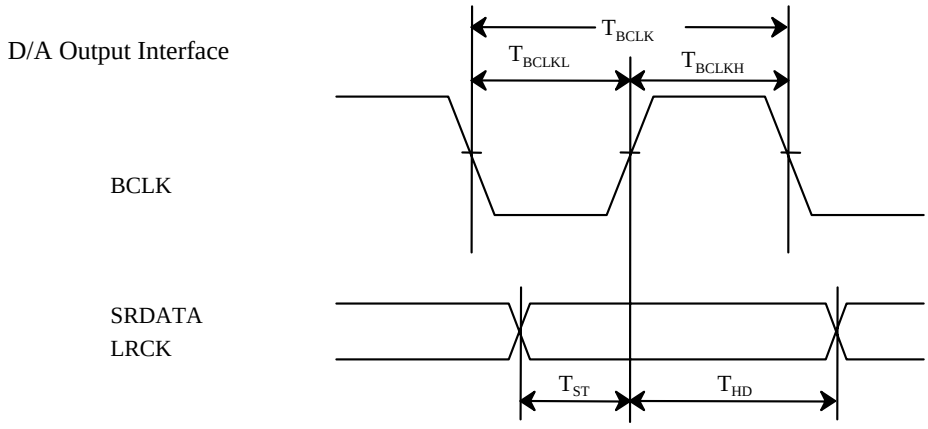
2. MCLK,MDATA,MLD noise filter command is MCIFNF (by setting the D5 and D4 bits of the 67 command) .

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D/A Output Interface 1							
C106	Clock width	T_{BCLK}	In normal-speed playback mode (64fs)		354		Ns
C107	High-level pulse width	T_{BCLKH}			177		Ns
C108	Low-level pulse width	T_{BCLKL}			177		Ns
C109	Setup time	T_{ST}		70			Ns
C110	Hold time	T_{HD}		70			Ns
D/A Output Interface 2							
C111	Clock width	T_{BCLK}	In 4x-speed playback mode (48fs)		118		Ns
C112	High-level pulse width	T_{BCLKH}			59		Ns
C113	Low-level pulse width	T_{BCLKL}			59		Ns
C114	Setup time	T_{ST}		30			Ns
C115	Hold time	T_{HD}		30			Ns
D/A Output Interface 3							
C116	Clock width	T_{BCLK}	In 8x-speed playback mode (48fs)		59		Ns
C117	High-level pulse width	T_{BCLKH}			29.5		Ns
C118	Low-level pulse width	T_{BCLKL}			29.5		Ns
C119	Setup time	T_{ST}		15			Ns
C120	Hold time	T_{HD}		15			Ns



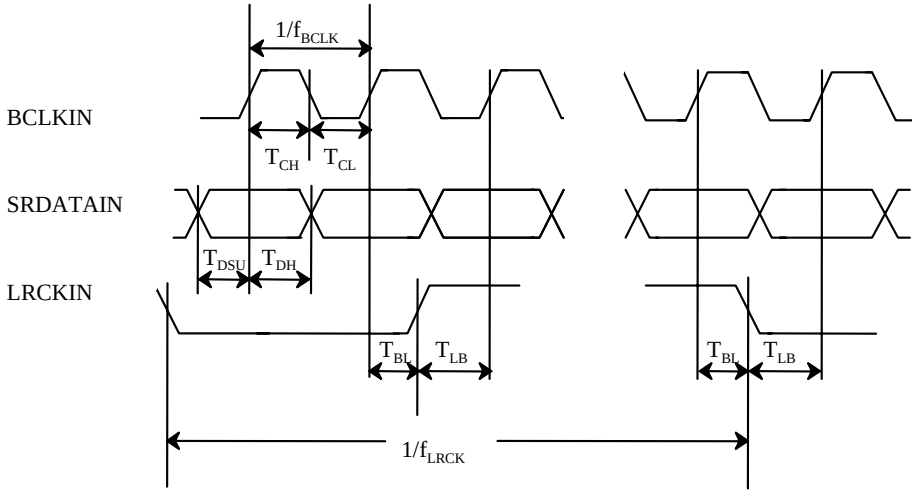
Note) SRDATA, BCLK, and LRCK are output in combination with PMCK (BCLK), FLAG (SRDATA), and SMCK (LRCK) or EXT0 (SRDATA), EXT1 (LRCK), and EXT2 (BCLK).

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D/A Converter Input Timing 1 (When no noise filter is used.)							
C121	BCLK frequency	f_{BCLK}			2.8		Ns
C122	SCLK pulse width	$T_{CH,CL}$		100			Ns
C123	Data setup time	T_{DSU}		100			Ns
C124	Data hold time	T_{DH}		100			Ns
C125	LRCK frequency	f_{LRCK}			44.1		KHz
C126	BCLK-LRCK timing	$T_{BL,}T_{LB}$		100			Ns
D/A Converter Input Timing 2 (When digital filter is used.)							
C127	BCLK frequency	f_{BCLK}			2.8		Ns
C128	SCLK pulse width	$T_{CH,CL}$		150			Ns
C129	Data setup time	T_{DSU}		100			Ns
C130	Data hold time	T_{DH}		100			Ns
C131	LRCK frequency	f_{LRCK}			44.1		KHz
C132	BCLK-LRCK timing	$T_{BL,}T_{LB}$		100			Ns



Note) 1. SRDATAIN,BCLK,LRCK noise filter command is SRDATANF (by setting the D7 and D6 bits of the 67 command) .

2. SRDATAIN, LRCKIN, and BCLKIN are input from EXT0 (SRDATAIN), EXT1 (LRCKIN), and EXT2 (BCLKIN) respectively.

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued) In BCKSEL = 0 mode

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
EDO, First-Page DRAM Interface Read / Write Cycle							
C133	A0 to A11 row address setup time	t_{ASR}			2		cycle
C134	A0 to A11 row address hold time	t_{RAH}			1		cycle
C135	A0 to A11 column address setup time	t_{ASC}			1		cycle
C136	A0 to A11 column address hold time	t_{CAH}			2		cycle
C137	RAS-CAS delay time (NCAS0, NCAS1)	t_{RCD}			2		cycle
C138	RAS access time	t_{RAC}			4		cycle
C139	CAS access time	t_{CAC}			2		cycle
C140	Write enable signal NWE setup time	t_{WCS}			2		cycle
C141	Write enable signal NWE hold time	t_{WCH}			2		cycle
C142	D0 to D15 write data setup time	t_{DWDS}			1		cycle
C143	D0 to D15 write data hold time	t_{DWDH}			2		cycle
EDO, First-Page DRAM Interface Page Mode Data Transfer							
C144	CAS pre-charge pulse width	t_{CP}			1		cycle
C145	CAS low-level pulse width	t_{CAS}			2		cycle
C146	RAS hold time	t_{RSH}			2		cycle
EDO, First-Page DRAM Interface CAS Before RAS Refresh							
C147	CAS-RAS delay time	t_{CRD}			1		cycle
C148	Refresh RAS low-level pulse width	t_{RRAS}			4		cycle
C149	Refresh CAS low-level pulse width	t_{RCAS}			5		cycle

Note) One cycle is the system clock cycle of 1 / (16.9344 MHz or 33.8688 MHz) [s].
The system clock frequencies, 16.9344 MHz and 33.8688 MHz, are determined according to the DCKSEL command (65h command D6 and D5).

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued) In BCKSEL = 1 mode

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
EDO, First-Page DRAM Interface Read / Write Cycle							
C150	A0 to A11 row address setup time	t_{ASR}			2		cycle
C151	A0 to A11 row address hold time	t_{RAH}			1		cycle
C152	A0 to A11 column address setup time	t_{ASC}			1		cycle
C153	A0 to A11 column address hold time	t_{CAH}			1		cycle
C154	RAS-CAS delay time (NCAS0, NCAS1)	t_{RCD}			2		cycle
C155	RAS access time	t_{RAC}			4		cycle
C156	CAS access time	t_{CAC}			1		cycle
C157	Write enable signal NWE setup time	t_{WCS}			2		cycle
C158	Write enable signal NWE hold time	t_{WCH}			1		cycle
C159	D0 to D15 write data setup time	t_{DWDS}			1		cycle
C160	D0 to D15 write data hold time	t_{DWDH}			1		cycle
EDO, First-Page DRAM Interface Page Mode Data Transfer							
C161	CAS pre-charge pulse width	t_{CP}			1		cycle
C162	CAS low-level pulse width	t_{CAS}			1		cycle
C163	RAS hold time	t_{RSH}			1		cycle
EDO, First-Page DRAM Interface CAS Before RAS Refresh							
C164	CAS-RAS delay time	t_{CRD}			1		cycle
C165	Refresh RAS low-level pulse width	t_{RRAS}			4		cycle
C166	Refresh CAS low-level pulse width	t_{RCAS}			5		cycle

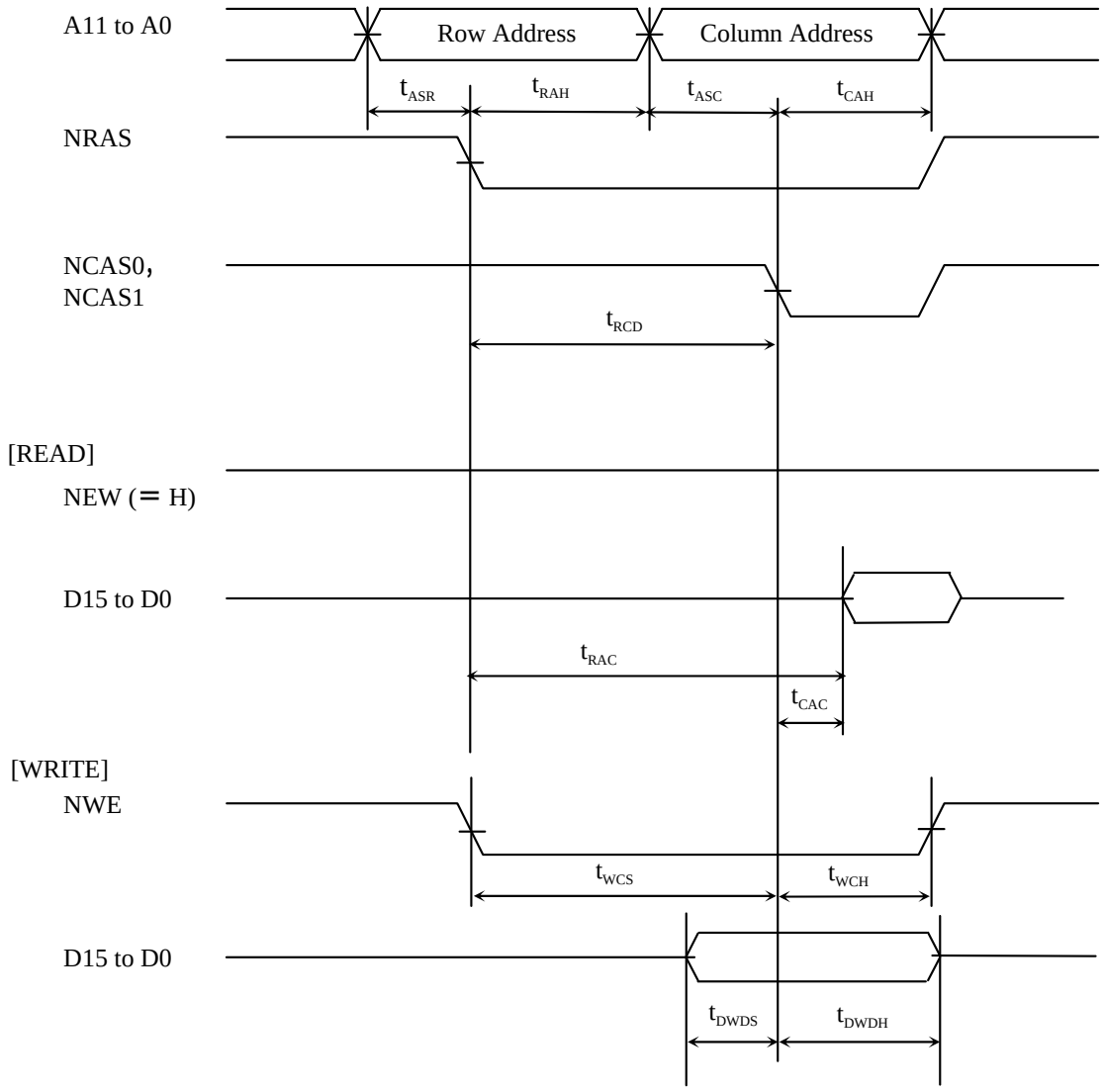
Note) One cycle is the system clock cycle of 1 / (16.9344 MHz or 33.8688 MHz) [s].
The system clock frequencies, 16.9344 MHz and 33.8688 MHz, are determined according to the DCKSEL command (65h command D6 and D5).

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

- EDO, First-Page DRAM Access Timing (NRAS, NCAS0, NCAS1, NWE, A0 to A11, D0 to D15) (Normal mode)



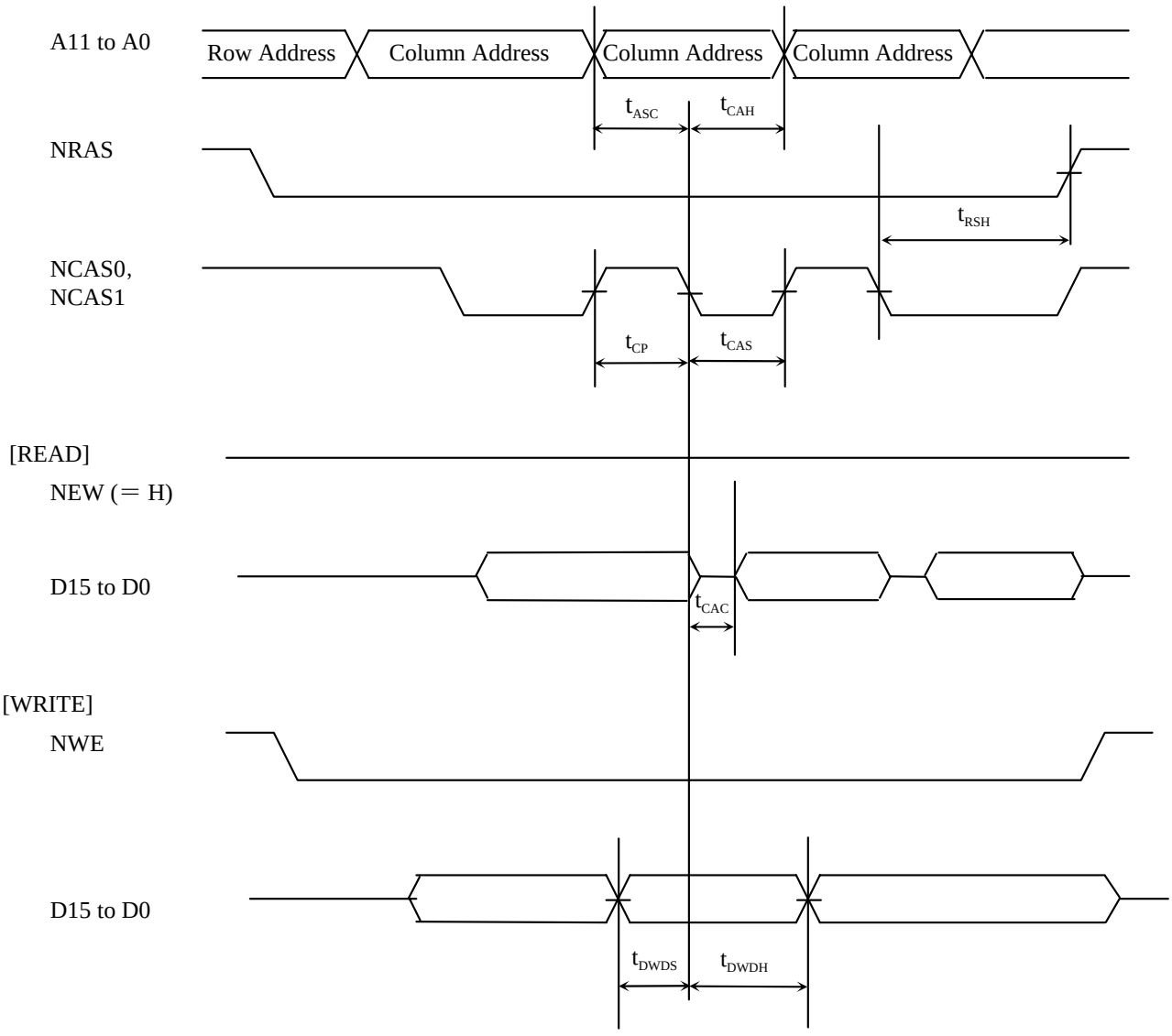
■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

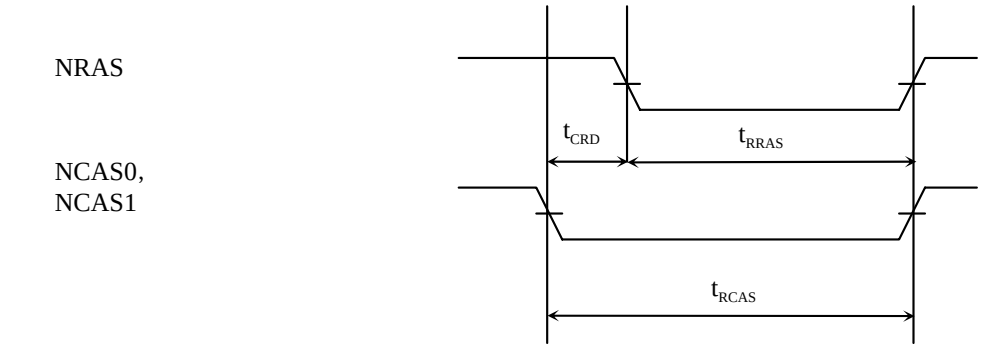
(2) AC Characteristics (continued)

- EDO, First-Page DRAM Access Timing (NRAS, NCAS0, NCAS1, NWE, A0 to A11, D0 to D15)

(Page mode)



(CAS Before RAS Refresh Mode)



■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
SDRAM Interface							
C167	SDRCK cycle time	t_{CLK}			1		cycle
C168	SDRCK high-level pulse width	t_{CH}			0.5		cycle
C169	SDRCK low-level pulse width	t_{CL}			0.5		cycle
C170	NCS input setup time	t_{CSS}			0.5		cycle
C171	NCS input hold time	t_{CSH}			0.5		cycle
C172	NRAS input setup time	t_{RAS}			0.5		cycle
C173	NRAS input hold time	t_{RAH}			0.5		cycle
C174	NCAS input setup time	t_{CAS}			0.5		cycle
C175	NCAS input hold time	t_{CAH}			0.5		cycle
C176	New input setup time	t_{WES}			0.5		cycle
C177	New input hold time	t_{WEH}			0.5		cycle
C178	LDQM, UDQM input setup time	t_{DMS}			0.5		cycle
C179	LDQM, UDQM input hold time	t_{DMH}			0.5		cycle
C180	D0 to D15 input setup time	t_{DQS}			1		cycle
C181	D0 to D15 input hold time	t_{DQH}			1		cycle
C182	A0 to A11, BA0,BA1 input setup time	t_{AS}			1		cycle
C183	A0 to A11, BA0, BA1 input hold time	t_{AH}			1		cycle

Note) 1. One cycle is the system clock cycle of 1 / (16.9344 MHz or 33.8688 MHz) [s].

2. Connect SDRAM near this LSI as much as possible.
Connect the wiring load of the SDRCK pin specially within 5pF.

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
SDRAM Interface							
C184	access time from SDRCK	t_{AC}				15	ns
C185	Hi-Z output time from SDRCK	t_{OH}			0		ns
C186	low impedance output time from SDRCK	t_{OLZ}			0		ns
C187	high impedance output time from SDRCK	t_{OHZ}			0		ns

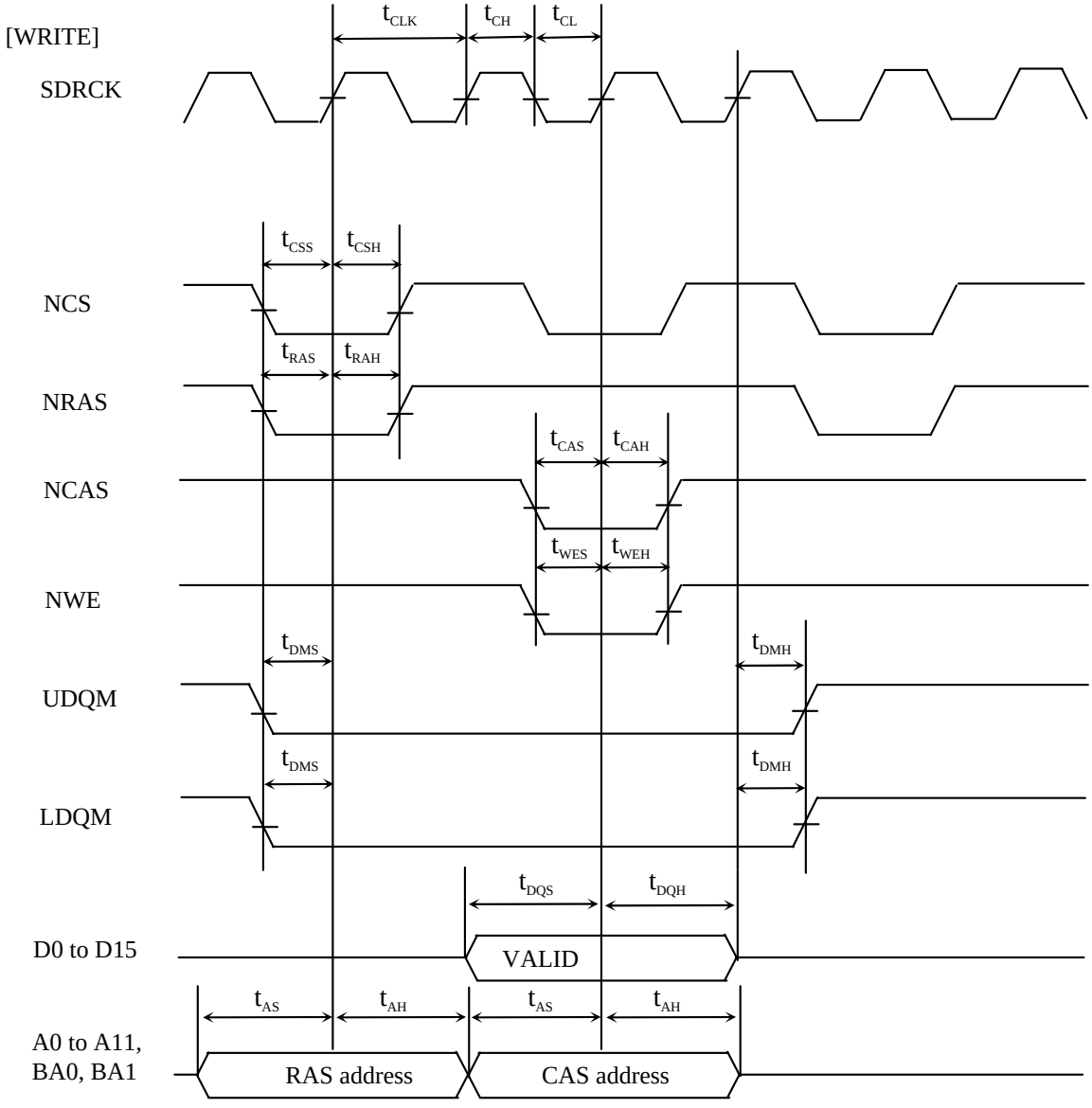
Note) One cycle is the system clock cycle of 1 / (16.9344 MHz or 33.8688 MHz) [s].

■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

- SDRAM Access Timing
  (SDRCK, NCS, NCAS, NWE, LDQM, UDQM, A0 to A11, BA0, BA1, D0 to D15)

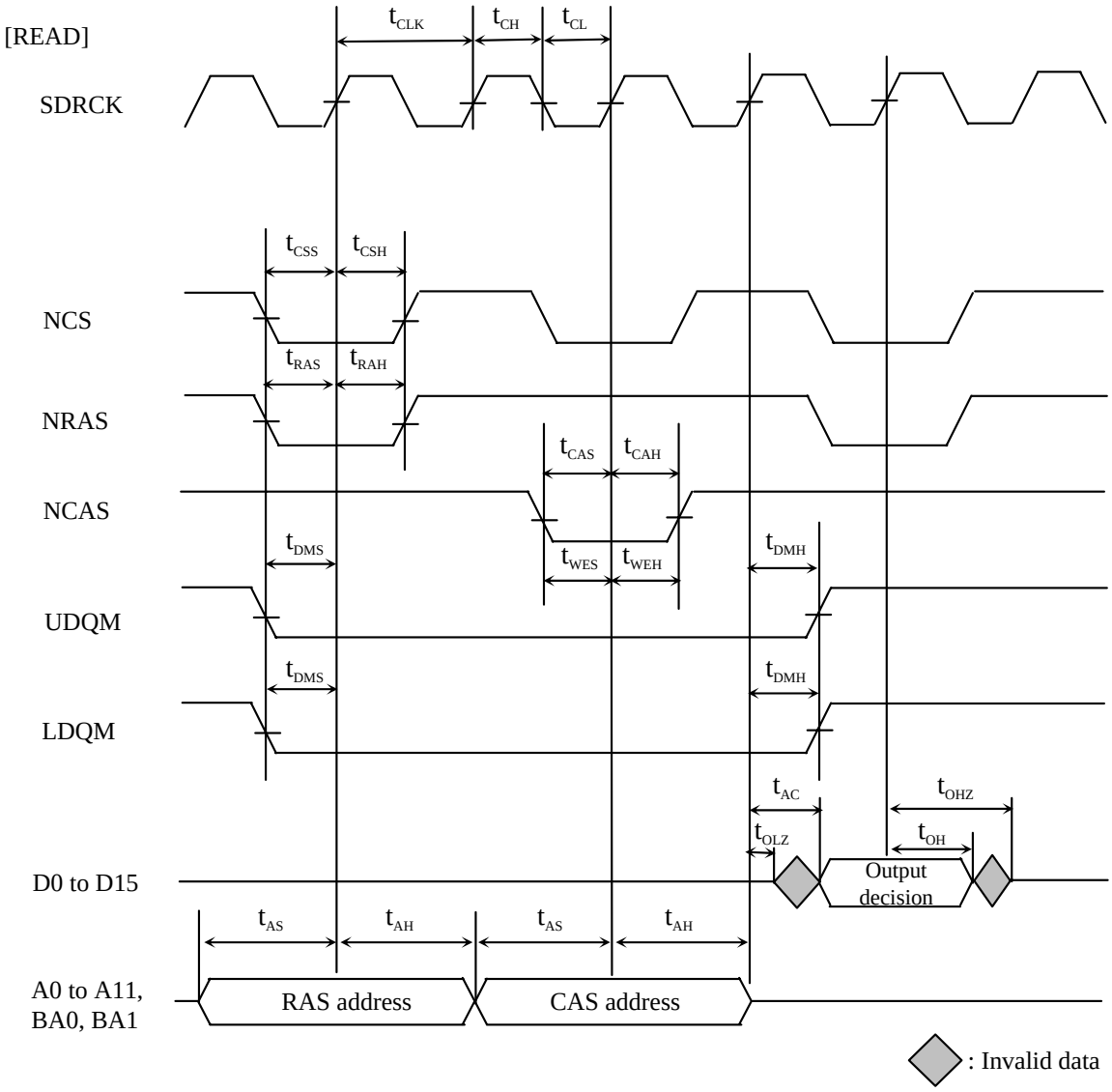


■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

- SDRAM Access Timing (continued)
  (SDRCK, NCS, NCAS, NWE, LDQM, UDQM, A0 to A11, BA0, BA1, D0 to D15)

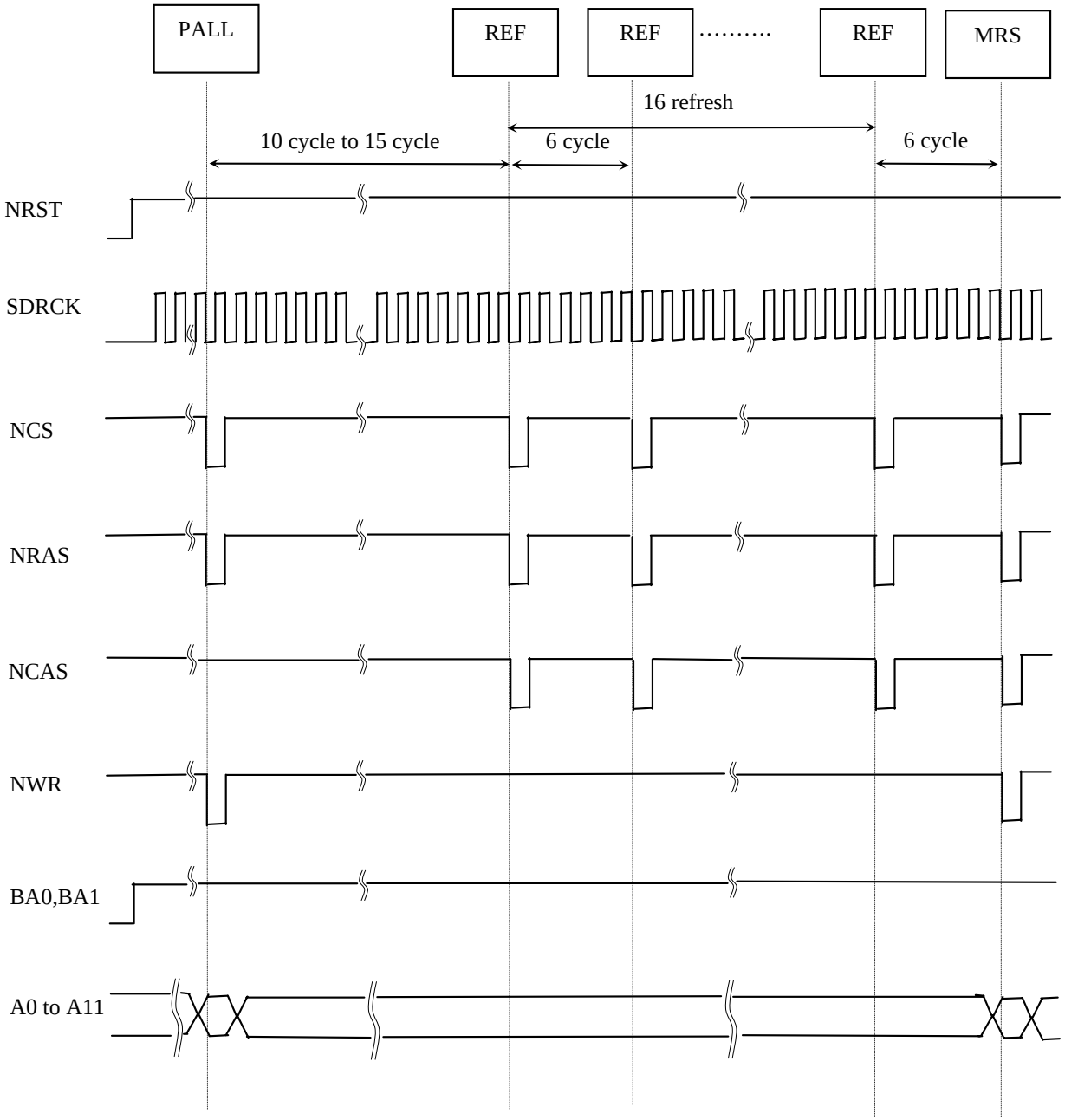


■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

- SDRAM Initialize Sequence
  (SDRCK, NCS, NCAS, NWE, A0 to A11, BA0, BA1)

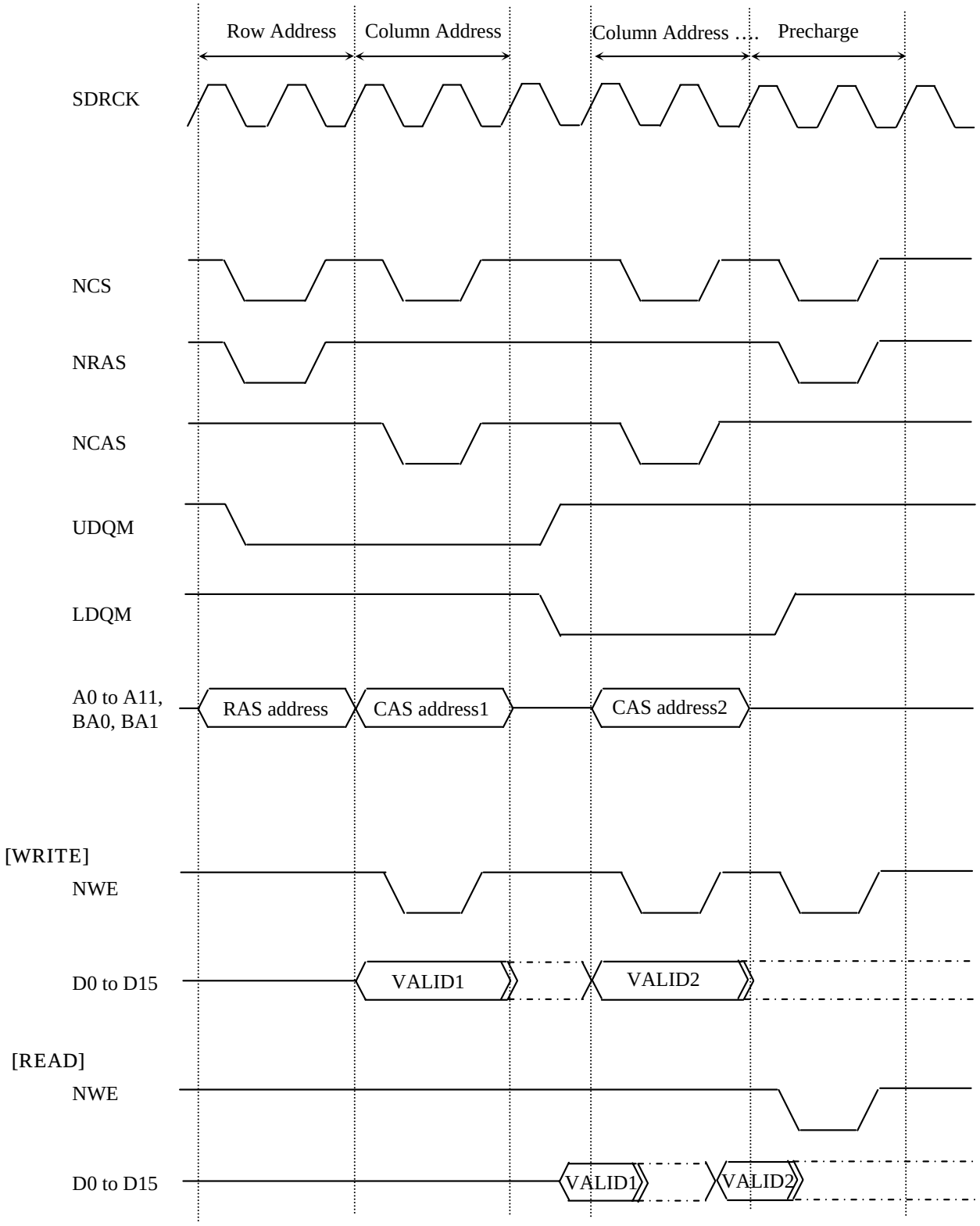


■ Electrical Characteristics (continued)

$DV_{DD1, 2, 3}$ = 1.5 V, $DRV_{DD1, 2}$ = 3.3 V, $IOV_{DD1, 2}$ = 3.3 V, $DV_{SS1, 2, 3}$ = 0 V, AV_{DD} = 3.3 V, AV_{SS} = 0 V, LOV_{DD1} = 3.3 V, LOV_{DD2} = 2.5 V, $LOV_{SS1, 2}$ = 0 V

(2) AC Characteristics (continued)

- SDRAM Page Access Timing
  (SDRCK, NCS, NRAS, NCAS, NWE, A0 to A11, BA0, BA1)



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