



# U74AHCT02

CMOS IC

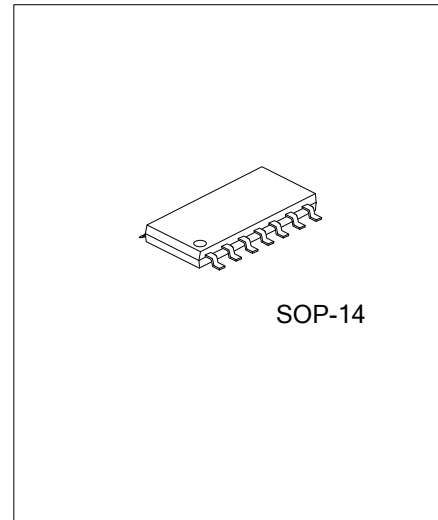
## QUADRUPLE 2-INPUT POSITIVE-NOR GATES

### DESCRIPTION

The **U74AHCT02** contains four independent 2-input NOR gates. Each gate provides the function  $Y = \overline{A+B}$  in positive logic.

### FEATURES

- \* Inputs Are TTL-Voltage Compatible
- \* Low Power Dissipation
- \* Balanced Propagation Delays

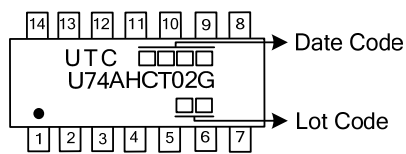


### ORDERING INFORMATION

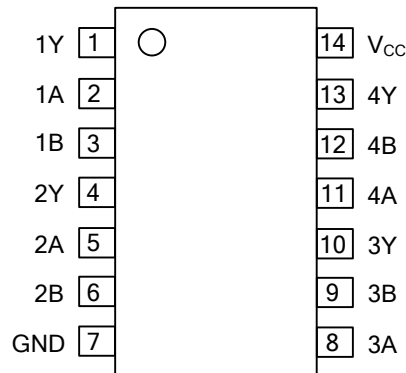
Ordering Number	Package	Packing
U74AHCT02G-S14-R	SOP-14	Tape Reel

<p>U74AHCT02G-S14-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) S14: SOP-14</li> <li>(3) G: Halogen Free and Lead Free</li> </ul>
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### MARKING



■ PIN CONFIGURATION

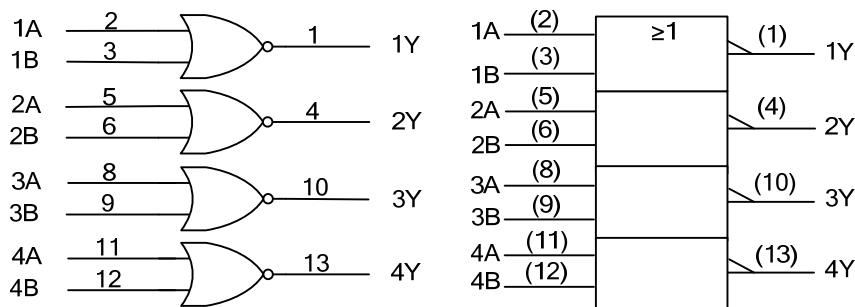


■ FUNCTION TABLE (Each Gate)

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	L
H	L	L
H	H	L

Note: H: HIGH voltage level; L: LOW voltage level.

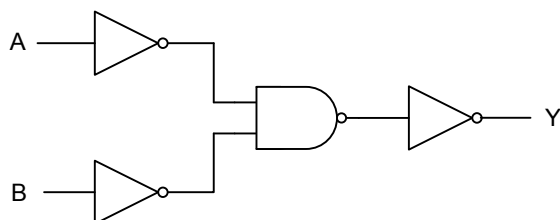
■ LOGIC SYMBOL (Positive Logic)



Logic Symbol

IEC Logic Symbol

■ LOGIC DIAGRAM (One Gate)



## ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	-0.5 ~ +7	V
Input Voltage	$V_{IN}$	-0.5 ~ +7	V
Output Voltage	$V_{OUT}$	-0.5 ~ $V_{CC} + 0.5$	V
$V_{CC}$ or GND Current	$I_{CC}$	±50	mA
Output Current ( $V_{OUT}=0 \sim V_{CC}$ )	$I_{OUT}$	±25	mA
Input Clamping Current ( $V_{IN} < 0V$ )	$I_{IK}$	-20	mA
Output Clamping Current ( $V_{OUT} < 0$ or $V_{OUT} > V_{CC}$ )	$I_{OK}$	±20	mA
Storage Temperature	$T_{STG}$	-65 ~ + 150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	76	°C/W

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$		4.5	5.0	5.5	V
Input Voltage	$V_{IN}$		0		5.5	V
Output Voltage	$V_{OUT}$		0		$V_{CC}$	V
High-Level Input Voltage	$V_{IH}$	$V_{CC} = 4.5V$ to $5.5V$	2.0			V
Low-Level Input Voltage	$V_{IL}$	$V_{CC} = 4.5V$ to $5.5V$			0.8	V
High-Level Input Current	$I_{OH}$				-8	mA
Low-Level Input Current	$I_{OL}$				8	mA
Input Transition Rise or Fall Rate	$t_R / t_F$	$V_{CC} = 5.0 \pm 0.5V$			20	ns/V
Ambient Operating Temperature	$T_{OPR}$		-40		+85	°C

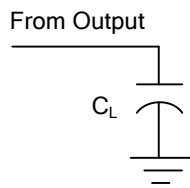
## ■ STATIC CHARACTERISTICS ( $T_A = 25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	$V_{OH}$	$I_{OH} = -50\mu A$ , $V_{CC} = 4.5V$	4.4	4.5		V
		$I_{OH} = -8mA$ , $V_{CC} = 4.5V$	3.94			V
Low-Level Output Voltage	$V_{OL}$	$I_{OL} = 50\mu A$ , $V_{CC} = 4.5V$			0.1	V
		$I_{OL} = 8mA$ , $V_{CC} = 4.5V$			0.36	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 0V$ to $5.5V$			±0.1	μA
Quiescent Supply Current	$I_Q$	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ , $V_{CC} = 5.5V$			2	μA
Additional Quiescent Supply Current Per Input Pin	$\Delta I_Q$	One input at 3.4V, other inputs at $V_{CC}$ or GND, $I_{OUT} = 0$ , $V_{CC} = 5.5V$			1.35	mA
Input Capacitance	$C_{IN}$	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5V$		4	10	pF

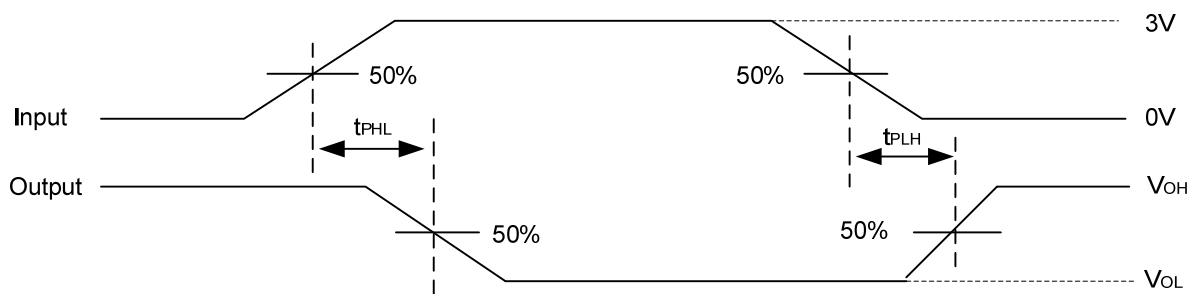
## ■ SWITCHING CHARACTERISTICS ( $T_A = 25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay, From Input(A and B) To Output(Y)	$t_{PLH} / t_{PHL}$	$V_{CC} = 5 \pm 0.5V$			5.5	ns
					$C_L = 15 pF$	
Power Dissipation Capacitance	$C_{PD}$	$f = 1MHz$ , No load		17		pF
					$C_L = 50 pF$	

■ TEST CIRCUIT AND WAVEFORMS



Test circuit for measuring propagation delay



Waveforms showing the Input(A and B) to Output(Y) propagation delays

- Notes: 1.  $C_L$  includes probe and jig capacitance.  
 2. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$ MHz,  $Z_o = 50\Omega$ ,  $t_R \leq 3$ ns,  $t_F \leq 3$ ns.

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