Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations



L7556, L7557 Low-Power SLICs with Battery Switch

Features

- Auxiliary input for second battery, and internal switch to enable its use to save power
- Low active power (typical 125 mW during on-hook transmission)
- Supports meter pulse injection
- Spare op amp for meter pulse filtering
- –16 V to –60 V power supply operation
- Distortion-free on-hook transmission
- Convenient operating states:
  — Forward powerup
  — Disconnect (high impedance)
  — 2-wire wink (zero loop voltage)
- Adjustable supervision functions:
  — Off-hook detector with longitudinal rejection
  — Ground key detector
  — Ring trip detector
- Independent, adjustable, dc and ac parameters:
  — dc feed resistance
  — Loop current limit
  — Termination impedance
- Thermal protection

Description

These electronic subscriber loop interface circuits (SLICs) are optimized for low power consumption while providing an extensive set of features.

The SLICs include an auxiliary battery input and a built-in switch. In short-loop applications, they can be used in high battery to present a high on-hook voltage, and then switched to low battery to reduce off-hook power.

The SLICs also include a summing node for meter pulse injection to 2.2 Vrms. A spare, uncommitted op amp is included for meter pulse filtering.

The switched battery is applied to the power amplifiers of the device. There are two versions. The L7556 has the battery switch completely under processor control. The L7557 can automatically switch to lower battery when appropriate and includes hysteresis to avoid frequent switching. To make the switch silent, an external capacitor can be added to slow the transition.

The L7556 is suited for applications serving only short loops, where a high on-hook voltage is required for compatibility with preexisting standards.

The L7557 is suited for applications where a full loop range is needed, but low short-loop power is desired. It is a much lower-cost solution than a switching regulator, and also occupies much less PCB area, needing only a battery filter capacitor and a diode for implementation.

The device is available in a 32-pin PLCC package. It is built by using a 90 V complementary bipolar integrated circuit (CBIC) process.

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Description (continued)

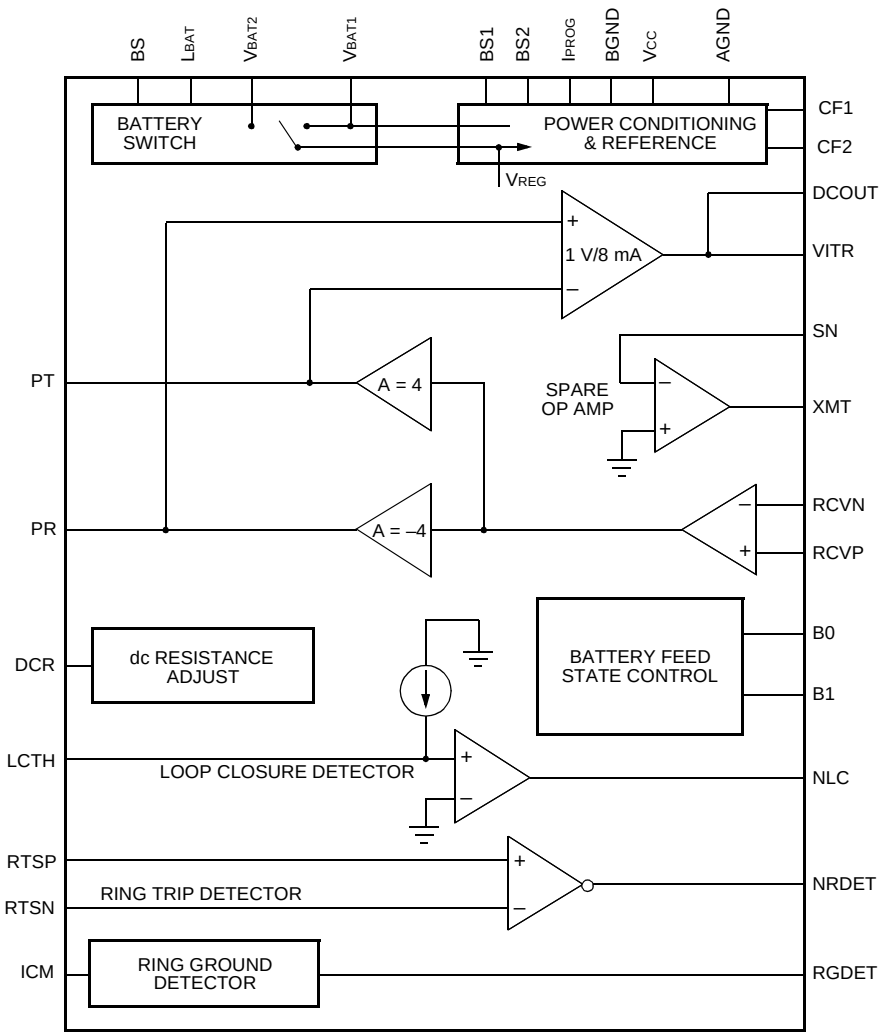
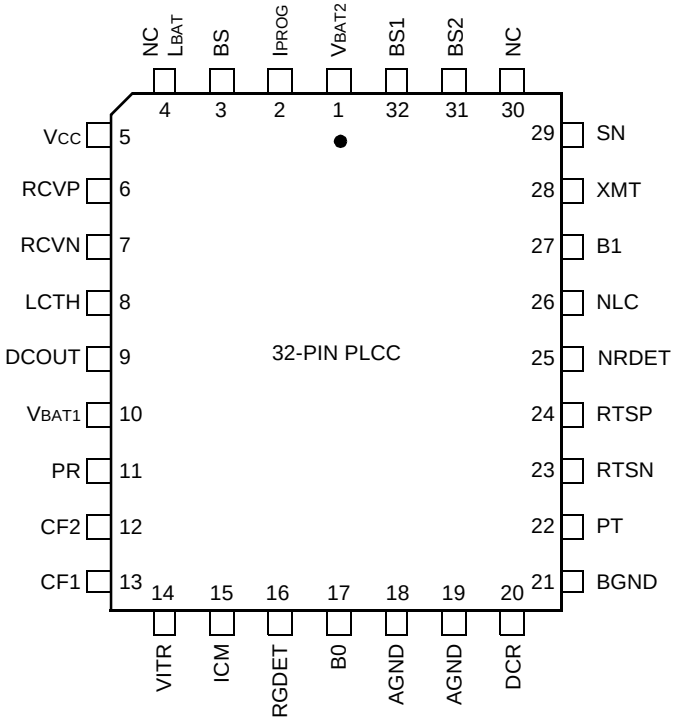


Figure 1. Functional Diagram

Pin Information



12-2548.q (F)

Figure 2. Pin Diagram (PLCC Chip)

Table 1. Pin Descriptions

Pin	Symbol	Type	Description
1	V_{BAT2}	—	**Auxiliary Battery Supply.** Negative high-voltage battery, lower in magnitude than V_{BAT1}, used to reduce power dissipation on short loops.
2	I_{PROG}	I	**Current-Limit Program Input.** A resistor to DCOUT sets the dc current limit of the device.
3	BS	I	**Battery Switch.** See Table 2 for description.
4	NC	—	**No Connection (L7556 Only).** Do not use as a tie point.
4	L_{BAT}	O	**Lower Battery in Use (L7557 Only).** When high, this open-collector output indicates the device has switched to V_{BAT2}. To use, connect a 100 kΩ resistor to V_{CC}.
5	V_{CC}	—	**+5 V Power Supply.**
6	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls the ac differential voltage on tip and ring.
7	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls the ac differential voltage on tip and ring.
8	LCTH	I	**Loop Closure Threshold Input.** Connect a resistor to DCOUT to set off-hook threshold.
9	DCOUT	O	**dc Output Voltage.** This output is a voltage that is directly proportional to the absolute value of the differential tip/ring current.
10	V_{BAT1}	—	**Battery Supply.** Negative high-voltage power supply, higher in magnitude than V_{BAT2}.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Description
11	PR	I/O	**Protected Ring.** The output of the ring driver amplifier and input to loop sensing circuitry. Connect to loop through overvoltage protection.
12	CF2	—	**Filter Capacitor 2.** Connect a 0.1 µF capacitor from this pin to AGND.
13	CF1	—	**Filter Capacitor 1.** Connect a 0.47 µF capacitor from this pin to pin CF2.
14	VITR	O	**Transmit ac Output Voltage.** This output is a voltage that is directly proportional to the differential tip/ring current.
15	ICM	I	**Common-Mode Current Sense.** To program ring ground sense threshold, connect a resistor to V_{CC} and connect a capacitor to AGND to filter 50/60 Hz. If unused, the pin can be left unconnected.
16	RGDET	O	**Ring Ground Detect.** When high, this open-collector output indicates the presence of a ring ground. To use, connect a 100 kΩ resistor to V_{CC}.
17	B0	I	**State Control Input.** B0 and B1 determine the state of the SLIC. See Table 2.
18	AGND	—	**Analog Signal Ground.**
19	AGND	—	**Analog Signal Ground.**
20	DCR	I	**dc Resistance for Low Loop Currents.** Leave open for dc feed resistance of 115 Ω, or short to DCOUT for 615 Ω. Intermediate values can be set by a simple resistor divider from DCOUT to ground with the tap at DCR.
21	BGND	—	**Battery Ground.** Ground return for the battery supply.
22	PT	I/O	**Protected Tip**. The output of the tip driver amplifier and input to loop sensing circuitry. Connect to loop through overvoltage protection.
23	RTSN	I	**Ring Trip Sense Negative**. Connect this pin to the ringing generator signal through a high-value resistor.
24	RTSP	I	**Ring Trip Sense Positive**. Connect this pin to the ring relay and the ringer series resistor through a high-value resistor.
25	NRDET	O	**Ring Trip Detector Output**. When low, this logic output indicates that ringing is tripped.
26	NLC	O	**Loop Detector Output**. When low, this logic output indicates an off-hook condition.
27	B1	I/O	**State Control Input**. B0 and B1 determine the state of the SLIC. See Table 2. Pin B1 has a 40 kΩ pull-up. It goes low in the event of thermal shutdown.
28	XMT	O	**Transmit ac Output Voltage**. The output of the uncommitted operational amplifier.
29	SN	I	**Summing Node**. The inverting input of the uncommitted operational amplifier. A resistor or network to XMT sets the gain.
30	NC	—	**No Connection.** Do not use as a tie point.
31	BS2	—	**Battery Switch Slowdown.** A 0.1 µF capacitor from BS1 to BS2 will ramp the battery switch transition for applications requiring quiet transition. If not needed, the pin can be left open.
32	BS1	—	**Battery Switch Slowdown.** A 0.1 µF capacitor from BS1 to BS2 will ramp the battery switch transition for applications requiring quiet transition. If not needed, the pin can be left open.

Functional Description

Table 2. Input State Coding

B0	B1	BS	State/Definition
1	1	1	**Powerup, Forward Battery.** Normal talk and battery feed state. Pin PT is positive with respect to PR. On-hook transmission is enabled. V_{BAT1} is applied to entire circuit.
1	1	0	**Powerup, Forward Battery.** Normal talk and battery feed state. Pin PT is positive with respect to PR. On-hook transmission is enabled. For the L7556 only, V_{BAT2} is applied to tip/ring drive amplifiers. For the L7557 only, the device compares the magnitude of V_{BAT2} to the voltage necessary to maintain proper loop current. Then the device automatically applies V_{BAT2} to tip/ring drive amplifiers when possible, not affecting the desired dc template.
1	0	1	**2-Wire Wink.** Pins PT and PR are put at the same potential (near ground). V_{BAT1} is applied to entire circuit.
0	0	1	**Disconnect.** The tip and ring amplifiers are turned off, and the SLIC goes to a high-impedance state (>100 kΩ).V_{BAT1} is applied to entire circuit.

Table 3. Supervision Coding

Pin NLC	Pin NRDET	Pin RGDET
0 = off-hook 1 = on-hook	0 = ring trip 1 = no ring trip	1 = ring ground 0 = no ring ground

Absolute Maximum Ratings (T_A = 25 °C)

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Value	Unit
5 V Power Supply	V_{CC}	7.0	V
Battery (Talking) Supply	V_{BAT1}	–63	V
Auxiliary Battery Supply	V_{BAT2}	–63	V
Logic Input Voltage	—	–0.5 to +7.0	V
Analog Input Voltage	—	–7.0 to +7.0	V
Maximum Junction Temperature	T_J	165	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Relative Humidity Range	R_H	5 to 95	%
Ground Potential Difference (BGND to AGND)	—	±3	V
PT or PR Fault Voltage (dc)	V_{PT}, V_{PR}	(V_{BAT1} – 5) to +3	V
PT or PR Fault Voltage (10 x 1000 µs)	V_{PT}, V_{PR}	(V_{BAT1} – 15) to +15	V
Current into Ring Trip Inputs	I_{RTSP}, I_{RTSN}	±240	µA

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. Some of the known examples of conditions that cause such potentials during powerup are the following:
1. An inductor connected to tip and ring can force an overvoltage on V_{BAT} through the protection devices if the V_{BAT} connections chatter.
2. Inductance in the V_{BAT} leads could resonate with the V_{BAT} filter capacitors to cause a destructive overvoltage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature	–40	—	85	°C
V_{CC} Supply Voltage	4.75	5.0	5.25	V
V_{BAT1} Supply Voltage	–24	–48	–60	V
V_{BAT2} Supply Voltage	–16	–28	V_{BAT1}	V
Loop Closure Threshold-detection Programming Range	—	10	I_{LIM}	mA
dc Loop Current-limit Programming Range	5	22	45	mA
On- and Off-hook 2-wire Signal Level	—	1	2.2	Vrms
ac Termination Impedance Programming Range	150	600	1300	Ω

Electrical Characteristics

Minimum and maximum values are testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements. Minimum and maximum values apply across the entire temperature range (–40 °C to +85 °C) and the entire battery range unless otherwise specified. Typical is defined as 25 °C, V_{CC} = 5.0 V, V_{BAT1} = –48 V, V_{BAT2} = –48 V, and I_{LIM}= 40 mA. Positive currents flow into the device. Test circuit is Figure 4 unless noted.

Table 4. Power Supply

Parameter	Min	Typ	Max	Unit
Power Supply—Powerup, No Loop Current:				
I_{CC}	—	2.8	—	mA
I_{BAT} (V_{BAT} = –48 V)	—	–2.3	—	mA
Power Dissipation (V_{BAT} = –48 V)	—	125	155	mW
Power Supply Rejection 500 Hz to 3 kHz (See Figures 5, 6, 15, and 16.)[1]:				
V_{CC}	35	—	—	dB
V_{BAT}	45	—	—	dB
Thermal Protection Shutdown (Tjc)	—	175	—	°C
Thermal Resistance, Junction to Ambient (θ_{JA})	—	60	—	°C/W

1. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Table 5. 2-Wire Port

Parameter	Min	Typ	Max	Unit
Tip or Ring Drive Current: = dc + Longitudinal + Signal Currents	65	—	—	mA
Signal Current	15	—	—	mArms
Longitudinal Current Capability per Wire[1]	8.5	15	—	mArms
dc Loop Current Limit[2]: R_{LOOP} = 100 Ω Programmability Range Accuracy (20 mA < I_{LIM} < 40 mA)	— 5 —	I_{LIM} — —	— 45 ±12	mA mA %
Powerup Open Loop Voltage Levels (includes external diode): Differential Voltage	$\lvert V_{BAT} + 8.4 \rvert$	$\lvert V_{BAT} + 7.9 \rvert$	$\lvert V_{BAT} + 7.4 \rvert$	V
Disconnect State: PT Resistance (V_{BAT} < V_{PT} < 0 V) PR Resistance (V_{BAT} < V_{PR} < 0 V)	100 100	143 133	— —	kΩ kΩ
Ground Start State: PT Resistance	100	143	—	kΩ
dc Feed Resistance (for I_{LOOP} below regulation level)	95	115	135	Ω
Loop Resistance Range (–3.17 dBm overload into 600 Ω; not including protection): I_{LOOP} = 20 mA at V_{BAT2} = –48 V I_{LOOP} = 20 mA at V_{BAT2} = –24 V	1885 685	— —	— —	Ω Ω
Longitudinal to Metallic Balance—*IEEE*[3] Std. 455 (See Figure 6.)[4]: 50 Hz to 1 kHz 1 kHz to 3 kHz	64 60	75 70	— —	dB dB
Metallic to Longitudinal Balance: 200 Hz to 4 kHz	46	—	—	dB
RFI Rejection (See Figure 7.)[5]: 0.5 Vrms, 50 Ω Source, 30% AM Mod 1 kHz 500 kHz to 100 MHz	—	–55	–45	dBV

1. The longitudinal current is independent of dc loop current.
2. Current-limit I_{LIM} is programmed by a resistor, R_{PROG}, from pin I_{PROG} to DCOUT. I_{LIM} is specified at the loop resistance where current limiting begins (see Figure 19). Select R_{PROG} (kΩ) =1.67 x I_{LIM} (mA).
3. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
4. Longitudinal balance of circuit card will depend on loop series resistance matching (see Figure 23 and Figure 24).
5. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Table 6. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
Differential PT/PR Current Sense (DCOUT): Gain (PT/PR to DCOUT)	 –123	 –125	 –127	 V/A
Loop Closure Detector Threshold[1]: Programming Accuracy	 —	 —	 ±20	 %
Ring Ground Detector Threshold[2]: R_{ICM} = 154 kΩ Programming Accuracy	 3 —	 6 —	 10 ±25	 kΩ %
Ring Trip Comparator: Input Offset Voltage	 —	 —	 ±10	 mV
RCVN, RCVP: Input Bias Current	 —	 –0.2	 –1	 µA

1. Loop closure threshold is programmed by resistor RLCTH from pin LCTH to pin DCOUT.
2. Ring ground threshold is programmed by resistor RICM2 from pin ICM to V_{CC}.

Table 7. Uncommitted Op Amp Characteristics

Parameter	Min	Typ	Max	Unit
Input Offset Voltage	—	±5	—	mV
Input Offset Current	—	±10	—	nA
Input Bias Current	—	200	—	nA
Differential Input Resistance	—	1.5	—	MΩ
Output Voltage Swing (R_L = 10 kΩ)	—	±3.5	—	Vpk
Output Resistance (A_{VCL} = 1)	—	2.0	—	Ω
Small Signal GBW	—	700	—	kHz

Electrical Characteristics (continued)

Table 8. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]:	150	—	1300	Ω
Longitudinal Impedance[2] (See Figure 8.)	—	40	46	Ω
Total Harmonic Distortion—200 Hz to 4 kHz[2]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain, f = 1 kHz (PT/PR to VITR)	–122	–125	–128	V/A
Transmit Accuracy in dB	–0.18	0	0.18	dB
Receive + Gain, f = 1 kHz (RCVP to PT/PR)	7.84	8.00	8.16	—
Receive – Gain, f = 1 kHz (RCVN to PT/PR)	–7.84	–8.00	–8.16	—
Receive Accuracy in dB	–0.18	0	0.18	dB
Gain vs. Frequency (transmit and receive) (600 Ω termination; reference 1 kHz[2]):				
200 Hz to 300 Hz	–1.00	0.0	0.05	dB
300 Hz to 3.4 kHz	–0.3	0.0	0.05	dB
3.4 kHz to 16 kHz	–3.0	–0.1	0.3	dB
16 kHz to 266 kHz	—	—	2.0	dB
Gain vs. Level (transmit and receive)(reference 0 dBV[2]):				
–50 dB to +3 dB	–0.05	0	0.05	dB
Return Loss[3]:				
200 Hz to 500 Hz	20	24	—	dB
500 Hz to 3400 Hz	26	29	—	dB
2-wire Idle-channel Noise (600 Ω termination):				
Psophometric	—	–87	–77	dBmp
C-message	—	2	12	dBrnC
3 kHz Flat	—	10	20	dBrn
Transmit Idle-channel Noise:				
Psophometric	—	–82	–77	dBmp
C-message	—	7	12	dBrnC
3 kHz flat	—	15	20	dBrn
Transhybrid Loss[3]:				
200 Hz to 500 Hz	21	24	—	dB
500 Hz to 3400 Hz	26	29	—	dB

1. Set by external components. Any complex impedance R1 + R2 || C between 150 Ω and 1300 Ω can be synthesized.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Return loss and transhybrid loss are functions of device gain accuracies and the external hybrid circuit. Guaranteed performance assumes 1% tolerance external components.

Electrical Characteristics (continued)

Table 9. Logic Inputs and Outputs

All outputs except RGDET and L_{BAT} are open collectors with internal, 30 kΩ pull-up resistor. RGDET and L_{BAT} are open collectors without internal pull-up. Input pin B1 has a 40 kΩ pull-up; it goes low in the event of thermal shutdown.

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level (permissible range)	V_{IL}	–0.5	0.4	0.7	V
High Level (permissible range)	V_{IH}	2.0	2.4	V_{CC}	V
Input Currents:					
Low Level (V_{CC} = 5.25 V, V_I = 0.4 V)	I_{IL}	–75	–115	–200	µA
High Level (V_{CC} = 5.25 V, V_I = 2.4 V)	I_{IH}	–40	–60	–100	µA
Output Voltages (open collector with internal pull-up resistor):					
Low Level (V_{CC} = 4.75 V, I_{OL} = 360 µA)	V_{OL}	0	0.2	0.4	V
High Level (V_{CC} = 4.75 V, I_{OH} = –20 µA)	V_{OH}	2.4	—	V_{CC}	V

Ring Trip Requirements

- Ringing signal:
  - — Voltage, minimum 35 Vrms, maximum 100 Vrms.
  - — Frequency, 17 Hz to 23 Hz.
  - — Crest factor, 1.4 to 2.
- Ringing trip:
  - — ≤100 ms (typical), ≤250 ms (V_{BAT} = –33 V, loop length = 530 Ω).
- Pretrip:
  - — The circuits in Figure 3 will not cause ringing trip.

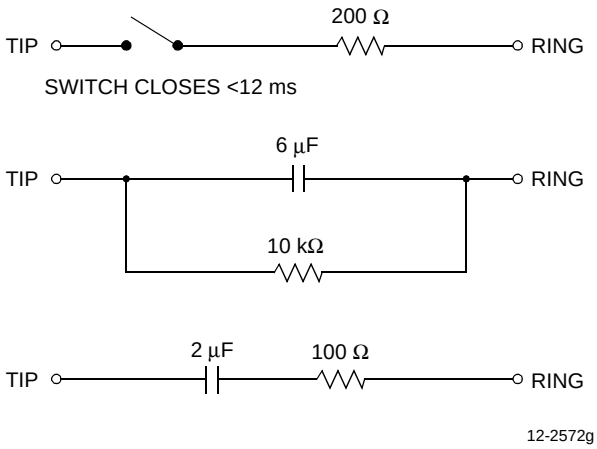
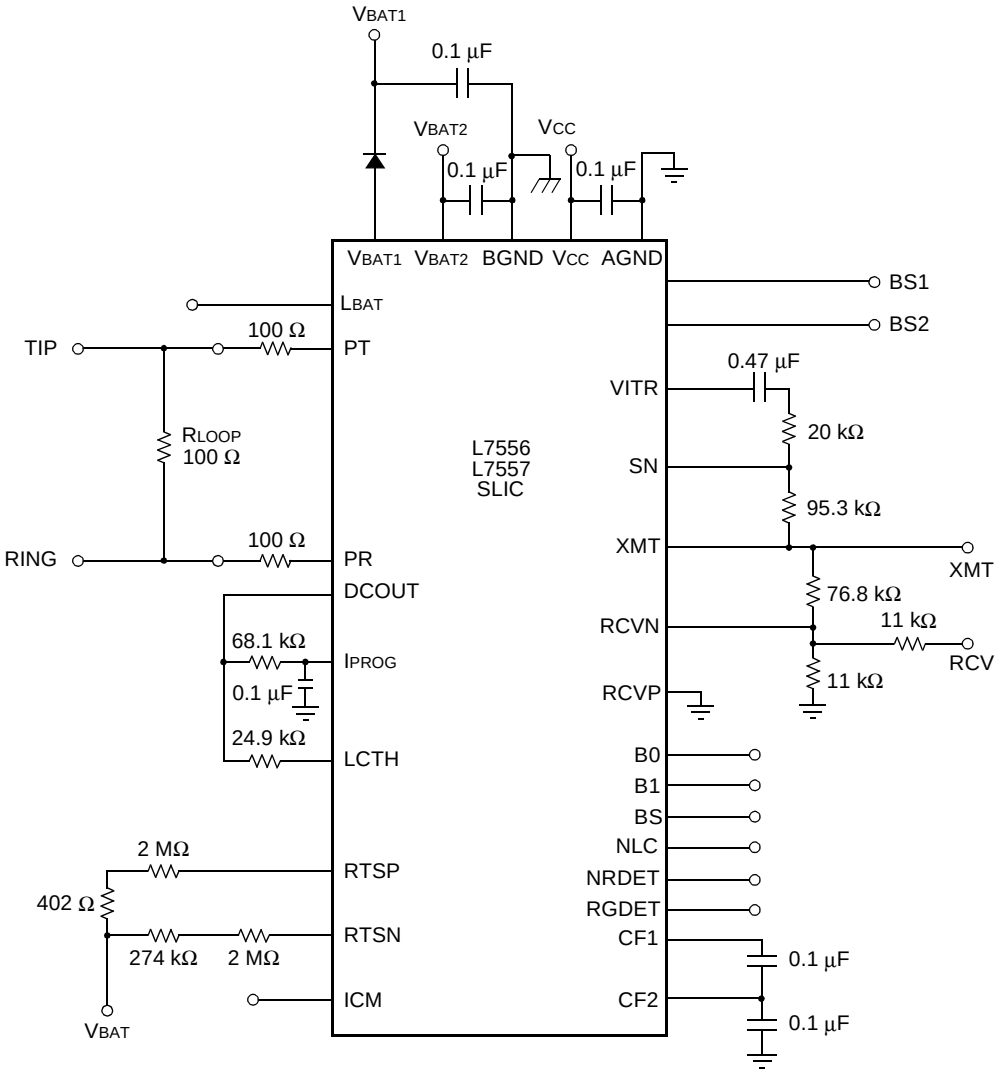


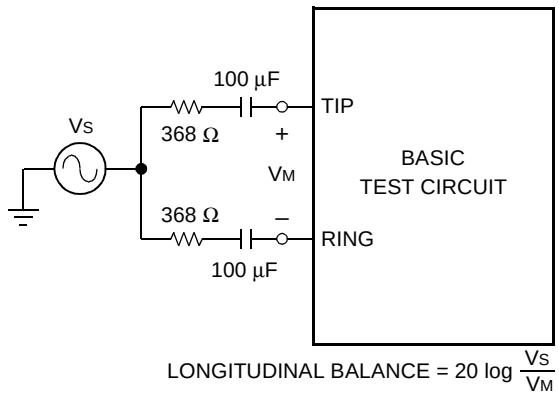
Figure 3. Ring Trip Circuits

Test Configurations



12-2564.a (F)

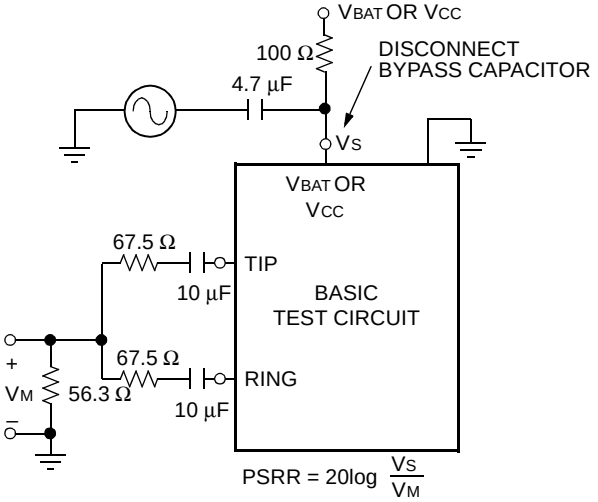
Figure 4. Basic Test Circuit



12-2584.c (F)

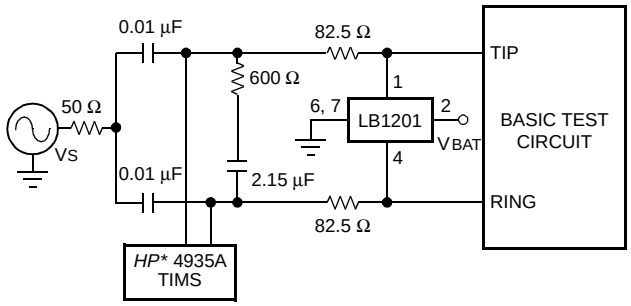
Figure 5. Longitudinal Balance

Test Configurations (continued)



12-2583.b (F)

Figure 6. Longitudinal PSRR

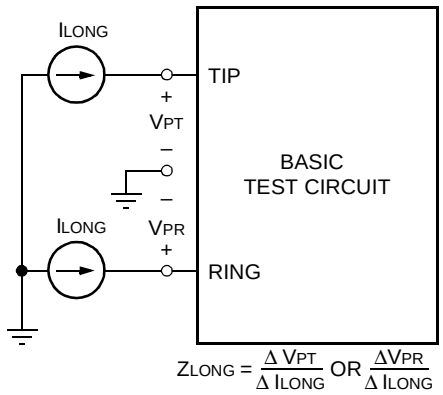


VS = 0.5 Vrms 30% AM 1 kHz MODULATION,
f = 500 kHz—1 MHz
DEVICE IN POWERUP MODE, 600 Ω TERMINATION

5-6756.b (F)

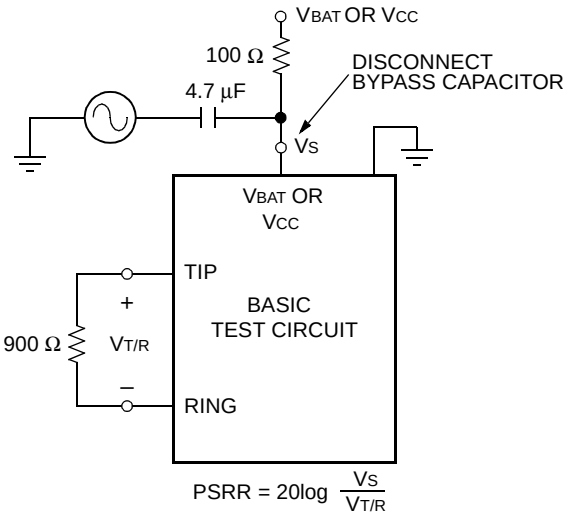
* *HP* is a registered trademark of Hewlett-Packard Company.

Figure 7. RFI Rejection



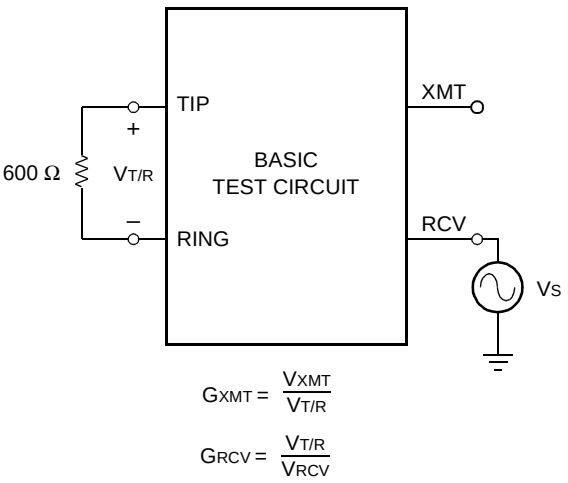
12-2585.a (F)

Figure 8. Longitudinal Impedance



12-2582.b (F)

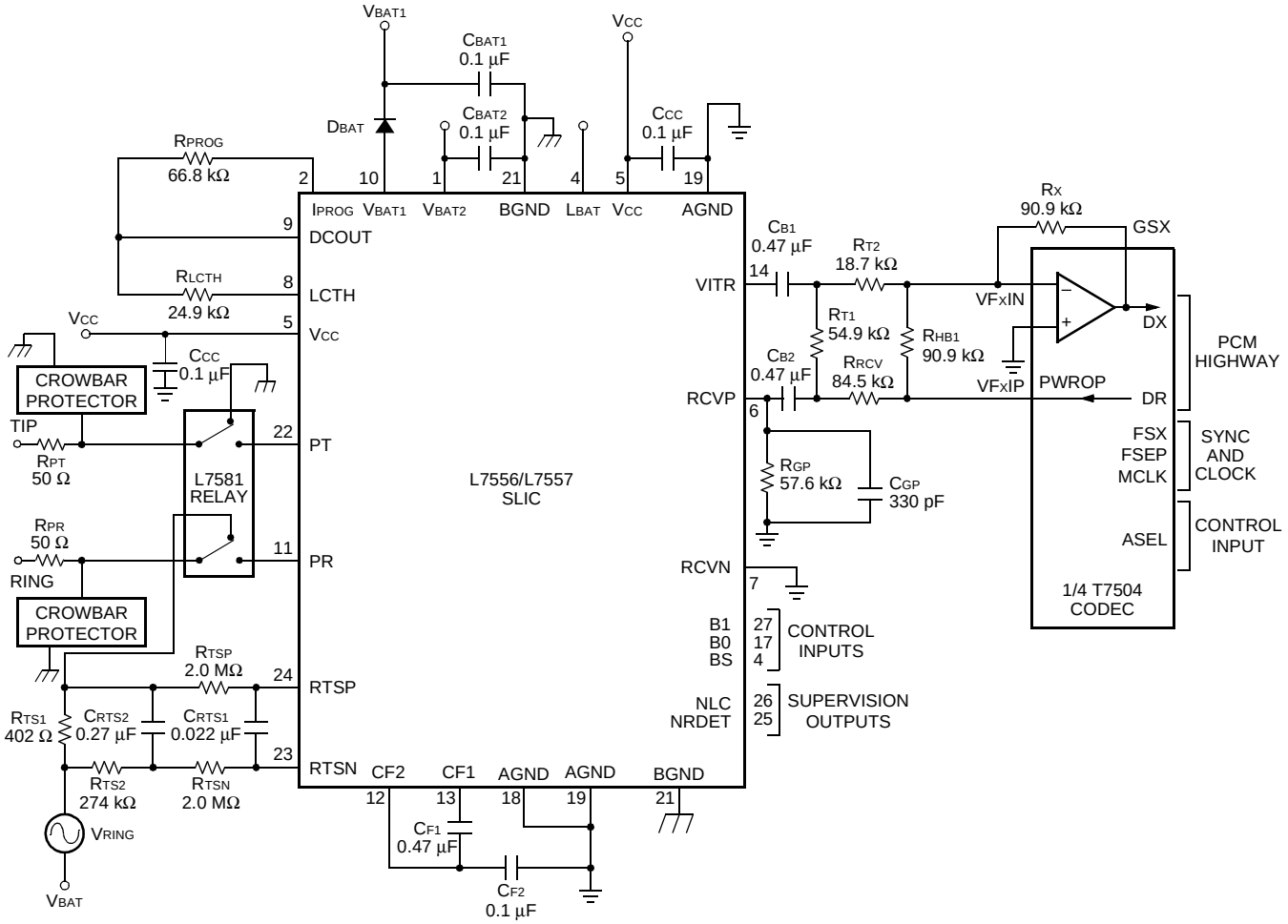
Figure 9. Metallic PSRR



12-2587.e (F)

Figure 10. ac Gains

Applications



12-2573.Y(F)

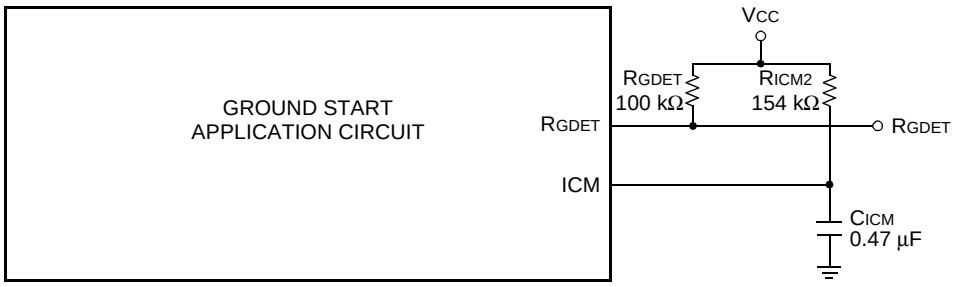
Notes:
Tx = 0 dB.

Rx = 0 dB.

Termination = 600 Ω.

Transhybrid = 600 Ω.

Figure 11. Basic Loop Start Application Circuit Using T7504 Type Codec



12-3547(F)

Figure 12. Ring Ground Detection Circuit

Applications (continued)

Table 10. Parts List for Loop Start and Ground Start Applications

Name	Value	Function
Integrated Circuits		
SLIC	L7556/7557	Subscriber loop interface circuit (SLIC).
Protector	Crowbar protector*	Secondary protection.
Ringing Relay	L7581	Switches ringing signals.
Codec	T7504	First-generation codec.
Overvoltage Protection		
R_{PT}	50 Ω, PTC or Fusible	Protection resistor.
R_{PR}	50 Ω, PTC or Fusible	Protection resistor.
Power Supply		
C_{BAT1}	0.1 µF, 20%, 100 V	V_{BAT1} filter capacitor.
C_{BAT2}	0.1 µF, 20%, 100 V	V_{BAT2} filter capacitor.
C_{CC}	0.1 µF, 20%, 10 V	V_{CC} filter.
C_{F1}	0.47 µF, 20%, 100 V	With C_{F2}, improves idle channel noise.
C_{F2}	0.1 µF, 20%, 100 V	With C_{F1}, improves idle channel noise.
D_{BAT}	100 V, 150 mA	Transient protection diode.
dc Profile		
R_{PROG}	66.8 kΩ, 1%, 1/16 W	Sets dc loop current limit.
ac Characteristics		
C_{B1}	0.47 µF, 20%, 10 V	ac/dc separation capacitor.
C_{B2}	0.47 µF, 20%, 10 V	ac/dc separation capacitor.
R_{T1}	54.9 kΩ, 1%, 1/16 W	With R_{GP} and R_{RCV}, sets ac termination impedance.
R_{RCV}	84.5 kΩ, 1%, 1/16 W	With R_{GP} and R_{T1}, sets receive gain.
R_{GP}	57.6 kΩ, 1%, 1/16 W	With R_{T1} and R_{RCV}, sets ac termination impedance and receive gain.
C_{GP}	330 pF, 10 V, 20%	Loop stability.
R_{T2}	18.7 kΩ, 1%, 1/16 W	With R_X, sets transmit gain in codec.
R_X	90.9 kΩ, 1%, 1/16 W	With R_{T2}, sets transmit gain in codec.
R_{HB1}	90.9 kΩ, 1%, 1/16 W	Sets hybrid balance.

* Contact your Lucent Technologies account representative for protector recommendations. Choice of this (and all) component(s) should be evaluated and confirmed by the customer prior to use in any field or laboratory system. Lucent does not recommend use of this part in the field without performance verification by the customer. This device is suggested by Lucent for customer evaluation. The decision to use a component should be based solely on customer evaluation.

Applications (continued)

Table 10. Parts List for Loop Start and Ground Start Applications (continued)

Name	Value	Function
Supervision		
R_{LCTH}	24.9 kΩ, 1%, 1/16 W	Sets loop closure (off-hook) threshold.
R_{TS1}	402 Ω, 5%, 2 W	Ringing source series resistor.
R_{TS2}	274 kΩ, 1%, 1/16 W	With C_{RTS2}, forms first pole of a double pole, 2 Hz ring trip sense filter.
C_{RTS1}	0.022 µF, 20%, 5 V	With R_{TSN}, R_{TSP}, forms second 2 Hz filter pole.
C_{RTS2}	0.27 µF, 20%, 100 V	With R_{TS2}, forms first 2 Hz filter pole.
R_{TSN}	2 MΩ, 1%, 1/16 W	With C_{RTS1}, R_{TSP}, forms second 2 Hz filter pole.
R_{TSP}	2 MΩ, 1%, 1/16 W	With C_{RTS1}, R_{TSN}, forms second 2 Hz filter pole.
Ground Start		
C_{ICM}	0.47 µF, 20%, 10 V	Provides 60 Hz filtering for ring ground detection.
R_{GDET}	100 kΩ, 20%, 1/16 W	Digital output pull-up resistor.
R_{ICM2}	82.5 kΩ, 1%, 1/16 W	Sets ring ground detection threshold.

Design Considerations

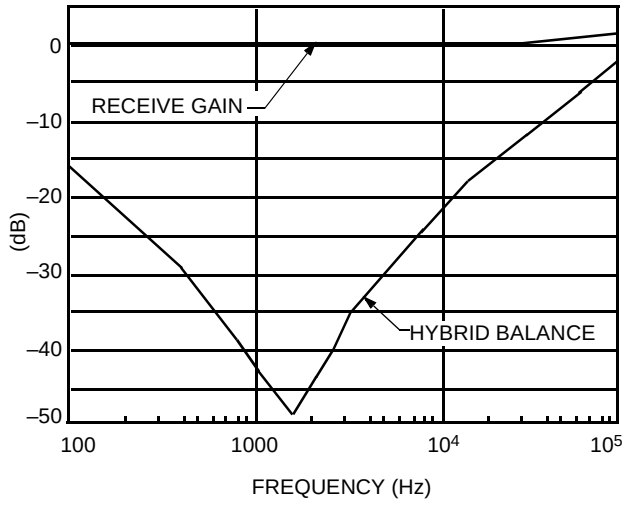
Table 11 shows the design parameters of the application circuit shown in Figure 11. Components that are adjusted to program these values are also shown.

Table 11. 600 Ω Design Parameters

Design Parameter	Parameter Value	Components Adjusted
Loop Closure Threshold	10 mA	R_{LCTH}
dc Loop Current Limit	40 mA	R_{PROG}
dc Feed Resistance	180 Ω	R_{PT}, R_{PR}
2-wire Signal Overload Level	3.14 dBm	—
ac Termination Impedance	600 Ω	R_{T1}, R_{GP}, R_{RCV}
Hybrid Balance Line Impedance	600 Ω	R_{HB1}
Transmit Gain	0 dB	R_{T2}, R_X
Receive Gain	0 dB	R_{RCV}, R_{GP}, R_{T1}

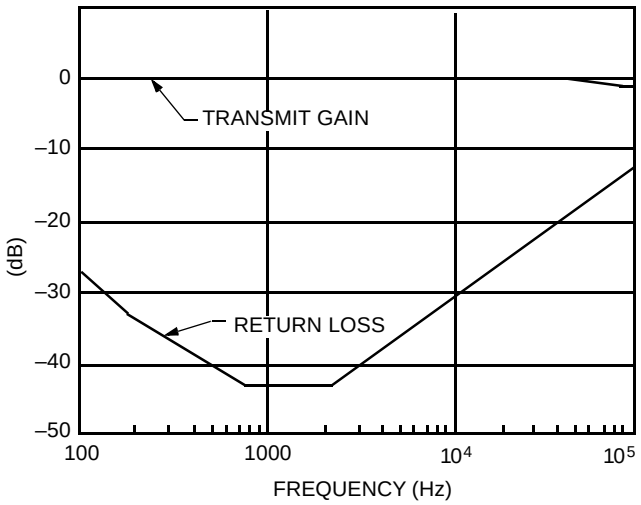
Applications (continued)

Characteristic Curves



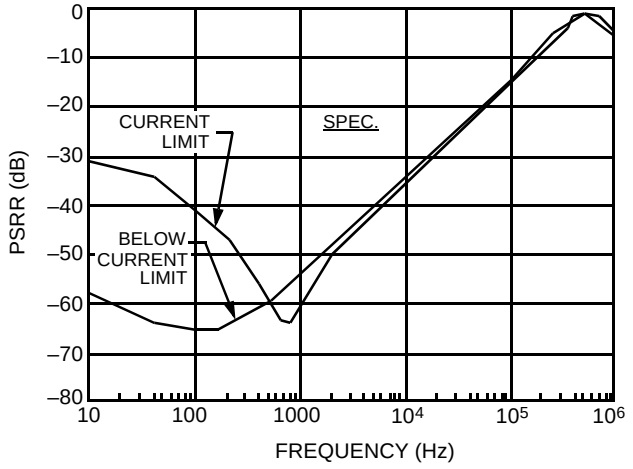
12-2828.c (F)

Figure 13. Receive Gain and Hybrid Balance vs. Frequency



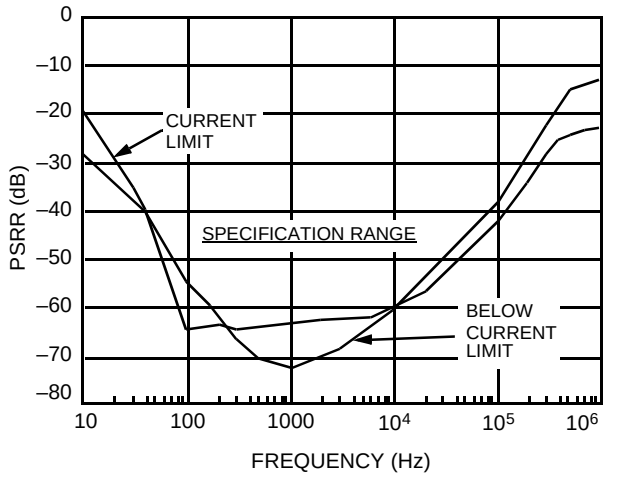
12-2829.b (F)

Figure 14. Transmit Gain and Return Loss vs. Frequency



12-2830.a (F)

Figure 15. Typical V_{CC} Power Supply Rejection

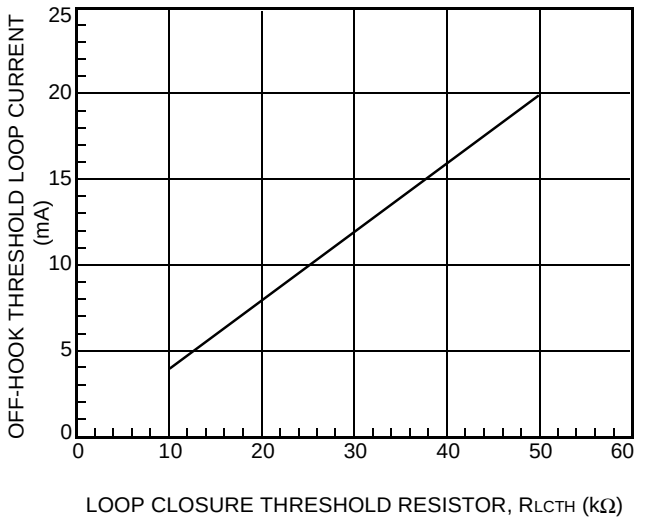


12-2871.a (F)

Figure 16. Typical V_{BAT} Power Supply Rejection

Applications (continued)

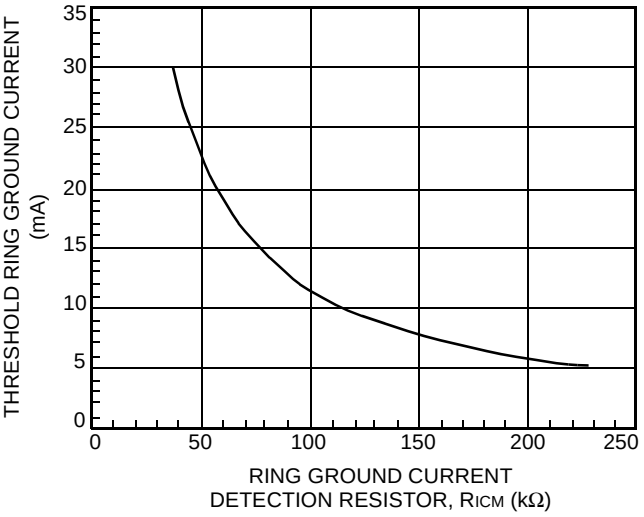
Characteristic Curves (continued)



12-3015 (F)

Note: V_{BAT} = –48 V.

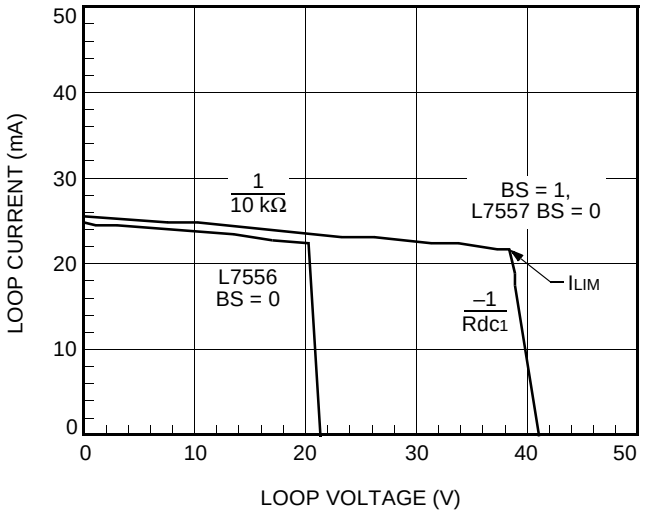
Figure 17. Loop Closure Program Resistor Selection



12-3016a (F)

Notes:
Tip lead is open.
V_{BAT} = –48 V.

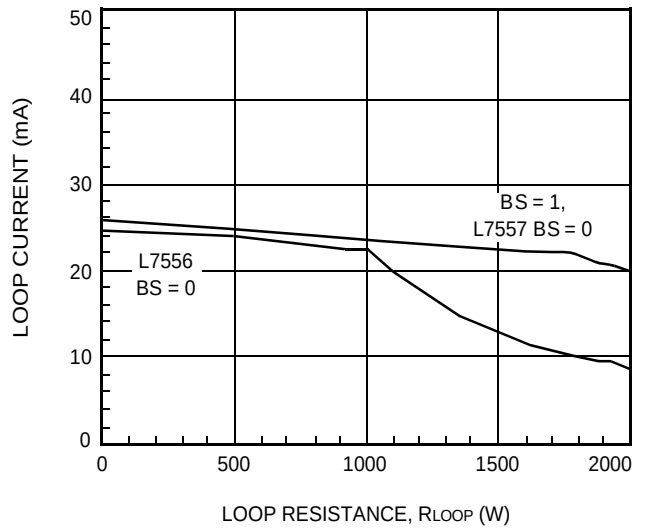
Figure 18. Ring Ground Detection Programming



12-3050.a(F)

Notes:
V_{BAT1} = –48 V.
V_{BAT2} = –28 V.
I_{LIM} = 22 mA.
R_{dc1} = 115 Ω.

Figure 19. Loop Current vs. Loop Voltage



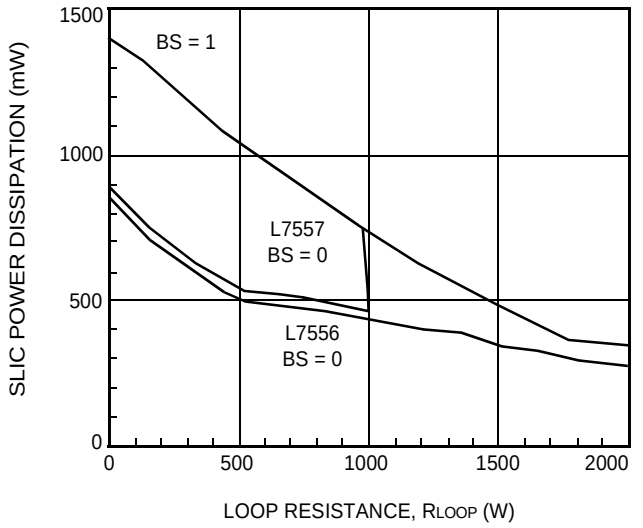
12-3051.a(F)

Notes:
V_{BAT1} = –48 V.
V_{BAT2} = –28 V.
I_{LIM} = 22 mA.
R_{dc1} = 115 Ω.

Figure 20. Loop Current vs. Loop Resistance

Applications (continued)

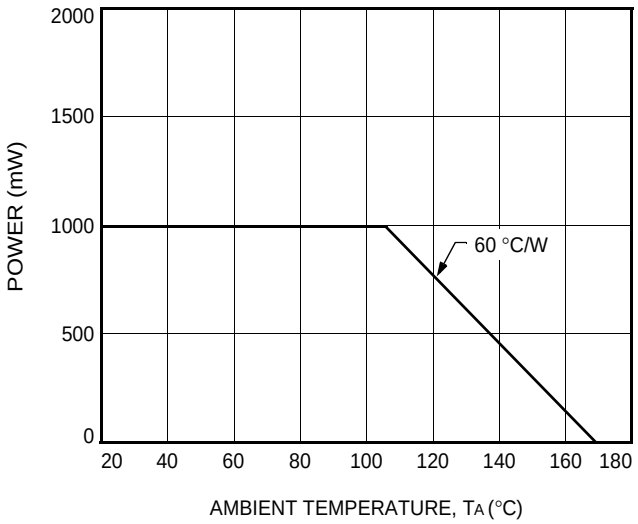
Characteristic Curves (continued)



12-3052.a (F)

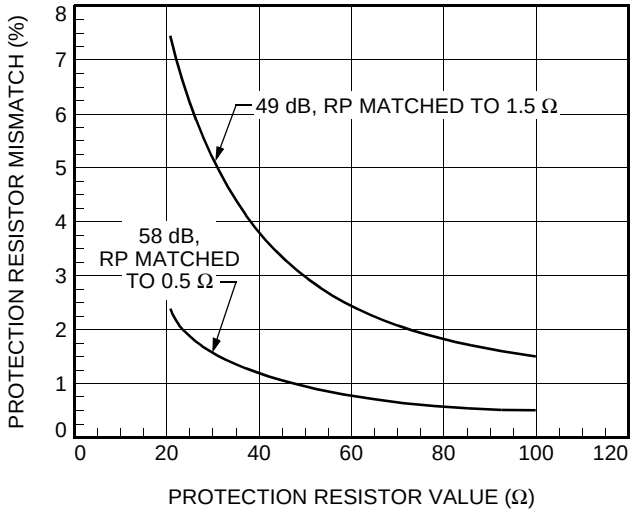
Notes:
V_{BAT1} = –48 V.
V_{BAT2} = –28 V.
I_{LIM} = 22 mA.
R_{dc1} = 115 Ω.

Figure 21. Typical SLIC Power Dissipation vs. Loop Resistance



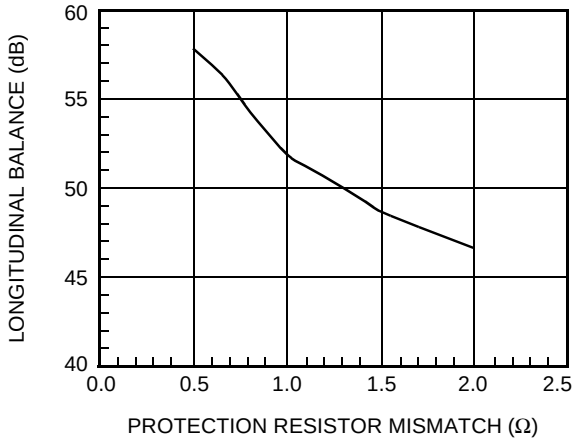
12-2825.c (F)

Figure 22. Power Derating



12-2559.b (F)

Figure 23. Longitudinal Balance Resistor Mismatch Requirements



12-3021 (F)

Figure 24. Longitudinal Balance vs. Protection Resistor Mismatch

Applications (continued)

dc Applications

Battery Feed

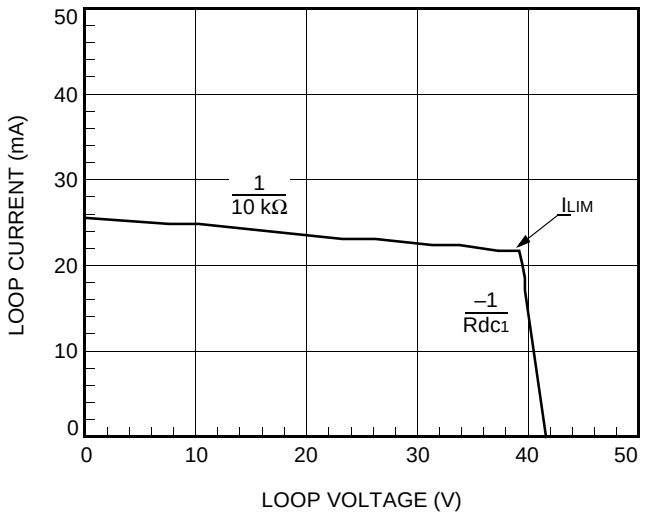
The dc feed characteristic can be described by:

$$I_L = \frac{|V_{BAT}| - V_{OH}}{R_L + 2R_P + R_{dc}}$$

$$V_{T/R} = \frac{(|V_{BAT}| - V_{OH}) \times R_L}{R_L + 2R_P + R_{dc}}$$

where:
I_L = dc loop current.
$V_{T/R}$ = dc loop voltage.
$|V_{BAT}|$ = battery voltage magnitude applied to the power amplifier stage (V_{BAT1} or V_{BAT2}).
V_{OH} = overhead voltage. This is the difference between the battery voltage and the open loop tip/ring voltage.
R_L = loop resistance, not including protection resistors.
R_P = protection resistor value.
R_{dc} = SLIC internal dc feed resistance.

The design begins by drawing the desired dc template. An example is shown in Figure 25.



Notes:
V_{BAT1} = –48 V.

V_{BAT2} = –28 V.

I_{LIM} = 22 mA.

R_{dc1} = 115 Ω.

Figure 25. Loop Current vs. Loop Voltage

Starting from the on-hook condition and going through to a short circuit, the curve passes through two regions:

Region 1; On-hook and low loop currents. The slope corresponds to the dc resistance of the SLIC, R_{DC1} (default is 115 Ω typical). The open circuit voltage is the battery voltage less the overhead voltage of the device, V_{OH} (default is 7.9 V typical). These values are suitable for most applications, but can be adjusted if needed. For more information, see the sections entitled Adjusting dc Feed Resistance or Adjusting Overhead Voltage.

Region 2; Current limit. The dc current is limited to a value determined by external resistor R_{PROG}. This region of the dc template has a high resistance (10 kΩ).

Calculate the external resistor as follows:

$$R_{PROG}\ (k\Omega) = 1.67\ I_{LIM}\ (mA)$$

Switching the Battery

The L7556 and L7557 SLICs provide an input for an auxiliary battery. Called V_{BAT2}, this power supply should be lower in magnitude than the primary battery, V_{BAT1}. Under an acceptable loop condition, V_{BAT2} can be switched to provide the loop power through the output amplifiers of the SLIC. The dc template, described in the last section, is determined by the battery that is activated—either V_{BAT1} or V_{BAT2}.

Which device will be best for you? That mainly depends on your loop range requirements. If you have only short loops and no on-hook voltage requirements, you don't need a battery switch at all. Use the L7551 instead. If you have only to guarantee a short loop range, e.g., 22 mA into 530 Ω, consider the L7556. The minimum V_{BAT2} can be determined by the standard dc equations.

In these applications, the off-hook detector can be used to indicate when to switch the battery. Just make sure the off-hook detector will also function as required with V_{BAT2} as well as V_{BAT1}.

Consider an off-hook threshold of 10 mA. This could represent a 1000 Ω loop with a 48 V V_{BAT1} active or a 2000 Ω loop with a 28 V V_{BAT2} active. In this case, if the loop is below 1000 Ω or above 2000 Ω, off-hook detection will be accurate. Between 1000 Ω and 2000 Ω, the detector is battery-dependent. This condition must be avoided. In our example, since the maximum loop is 530 Ω, the 10 mA detector is perfectly acceptable.

If the PTT would like a short loop system that can also serve long loops, the off-hook detector is not the best indicator, and better loop intelligence is needed. In this case, the L7557 can be used. It has an internal comparator that senses when there is enough potential at V_{BAT2} to switch without affecting the loop current. In this case, the loop range is determined by V_{BAT1}, and V_{BAT2} is only switched in when the loop is short enough to use it. This switching is automatic and includes hysteresis to avoid oscillation when the loop length is close to the V_{BAT2} switch threshold.

Applications (continued)

dc Applications (continued)

Overhead Voltage

In order to drive an on-hook ac signal, the SLIC must set up the tip and ring voltage to a value less than the battery voltage. The amount that the open loop voltage is decreased relative to the battery is referred to as the overhead voltage. Expressed as an equation:

$$V_{OH} = |V_{BAT}| - (V_{PT} - V_{PR})$$

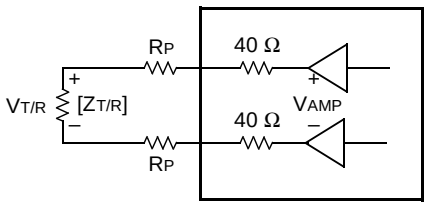
Without this buffer voltage, amplifier saturation will occur and the signal will be clipped. The device is automatically set at the factory to allow undistorted on-hook transmission of a 3.17 dBm signal into a 900 Ω loop impedance. For applications where higher signal levels are needed, e.g., periodic pulse metering, the 2-wire port of the SLIC can be programmed with pin DCR.

The drive amplifiers are capable of 4 Vrms minimum (VAMP). Referring to Figure 26, the internal resistance has a worst-case value of 46 Ω. So, the maximum signal the device can guarantee is:

$$V_{T/R} = 4\ V\left(\frac{|Z_{T/R}|}{|Z_{T/R}| + 2(R_P + 46)}\right)$$

Thus, $R_P \leq 35\ \Omega$ allows 2.2 Vrms metering signals. The next step is to determine the amount of overhead voltage needed. The peak voltage at output of tip and ring amplifiers is related to the peak signal voltage by:

$$\hat{V}amp = \hat{V}_{T/R}\left(1 + \frac{2(R_P + 40\,\Omega)}{|Z_{T/R}|}\right)$$



12-2560.e (F)

Figure 26. SLIC 2-Wire Output Stage

In addition to the required peak signal level, the SLIC needs about 2 V from each power supply to bias the amplifier circuitry. It can be thought of as an internal saturation voltage. Combining the saturation voltage and the peak signal level, the required overhead can be expressed as:

$$V_{OH} = V_{SAT} + \left(1 + \frac{2(R_P + 40\,\Omega)}{|Z_{T/R}|}\right)\hat{V}_{T/R}$$

where V_{SAT} is the combined internal saturation voltage between the tip/ring amplifiers and V_{BAT} (5.4 V typ.). R_P (Ω) is the protection resistor value, and 40 Ω is the output series resistance of each internal amplifier. $Z_{T/R}$ (Ω) is the ac loop impedance.

Example 1, on-hook transmission of a meter pulse:

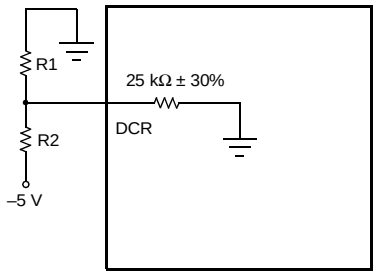
Signal level: 2.2 Vrms into 200 Ω
35 Ω protection resistors
I_{LOOP} = 0 (on-hook transmission of the metering signal)

$$V_{OH} = 5.4 + \left(1 + \frac{2(35 + 40)}{200}\right)\sqrt{2}\ (2.2) = 10.8\ V$$

Accounting for V_{SAT} tolerance of 0.5 V, a nominal overhead of 11.3 V would ensure transmission of an undistorted 2.2 V metering signal.

Adjusting Overhead Voltage

To adjust the open loop 2-wire voltage, pin DCR is programmed at the midpoint of a resistive divider from ground to either –5 V or V_{BAT}. In the case of –5 V, the overhead voltage will be independent of the battery voltage. Figure 27 shows the equivalent input circuit to adjust the overhead voltage.



12-2562 (F)

Figure 27. Equivalent Circuit for Adjusting the Overhead Voltage

The overhead voltage is programmed by using the following equation:

$$V_{OH} = 7.9 - 4\ V_{DCR}$$

$$= 7.9 - 4\left(-5 \times \left(\frac{R_1 \parallel 25\ k\Omega}{R_2 + R_1 \parallel 25\ k\Omega}\right)\right)$$

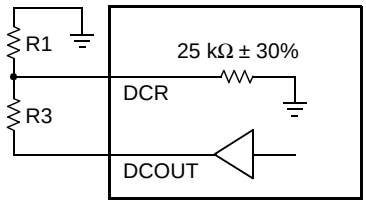
$$= 7.9 + 20\left(\frac{R_1 \parallel 25\ k\Omega}{R_2 + R_1 \parallel 25\ k\Omega}\right)$$

Applications (continued)

dc Applications (continued)

Adjusting dc Feed Resistance

The dc feed resistance may be adjusted with the help of Figure 28.



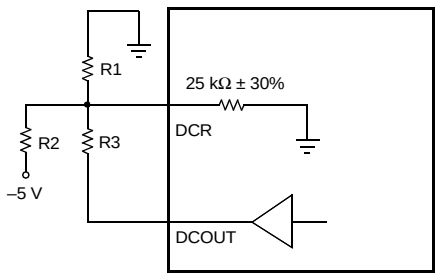
12-2560 (F)

Figure 28. Equivalent Circuit for Adjusting the dc Feed Resistance

$$R_{dc} = 115\,\Omega + 500\,\Omega\frac{\Delta V_{DCR}}{\Delta V_{DCOUT}}$$

$$= 115\,\Omega + 500\,\Omega\left(\frac{R_1 \| 25\,k\Omega}{R_3 + R_1 \| 25\,k\Omega}\right)$$

The above paragraphs describe the independent setting of the overhead voltage and the dc feed resistance. If both need to be set to customized values, combine the two circuits as shown in Figure 29.



12-2561 (C)

Figure 29. Adjusting Both Overhead Voltage and dc Feed Resistance

This is an equivalent circuit for adjusting both the dc feed resistance and overhead voltage together.

The adjustments can be made by a simple superposition of the overhead and dc feed equations:

$$V_{OH} = 7.9 + 20\left(\frac{R_1 \| 25\ k\Omega \| R_3}{R_2 + R_1 \| \ 25\ k\Omega \| R_3}\right)$$

$$R_{DC} = 115\ \Omega + 500\ \Omega\left(\frac{R_1 \ \| 25\ k\Omega}{R_2 + R_1 \| 25\,k\Omega}\right)$$

When selecting external components, select R1 on the order of 5 kΩ to minimize the programming inaccuracy caused by the internal 25 kΩ resistor. Lower values can be used; the only disadvantage is the power consumption of the external resistors.

Loop Range

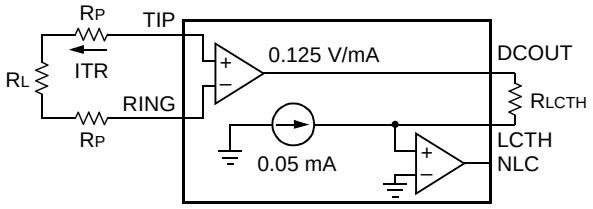
The equation below can be rearranged to provide the loop range for a required loop current:

$$R_L = \frac{|V_{BAT}| - V_{OH}}{I_L} - 2R_P - R_{dc}$$

Off-Hook Detection

The loop closure comparator has built-in longitudinal rejection, eliminating the need for an external 60 Hz filter. The loop closure detection threshold is set by resistor R_{LCTH}. Referring to Figure 30, NLC is high in an on-hook condition (I_{TR} = 0, V_{DCOUT} = 0) and V_{LCTH} = 0.05 mA x R_{LCTH}. The off-hook comparator goes low when V_{LCTH} crosses zero and then goes negative:

$$V_{LCTH} = 0.05\ mA \times R_{LCTH} + V_{DCOUT}$$
$$= 0.05\ mA \times R_{LCTH} - 0.125\ V/mA \times I_{TR}$$
$$R_{LTCH}\ (k\Omega) = 2.5 \times I_{TR}\ (mA)$$



12-2553g(F)

Figure 30. Off-Hook Detection Circuit Applications

Applications (continued)

dc Applications (continued)

Ring Trip Detection

The ring trip circuit is a comparator that has a special input section optimized for this application. The equivalent circuit is shown in Figure 31, along with its use in an application using unbalanced, battery-backed ringing.

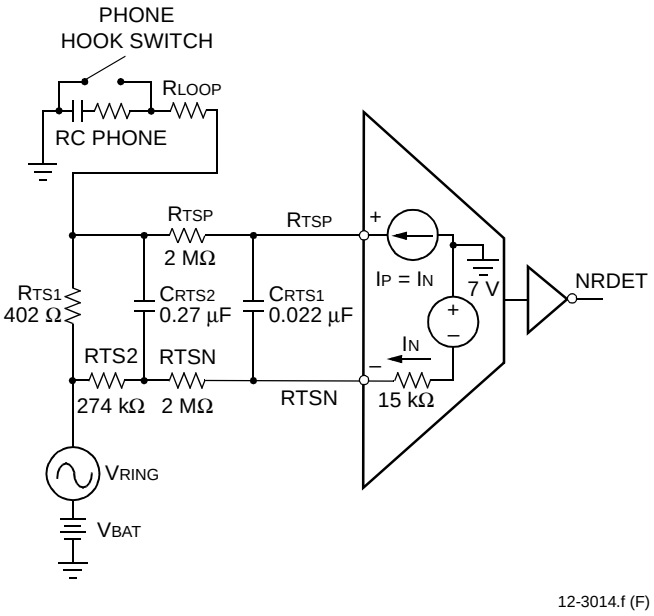


Figure 31. Ring Trip Equivalent Circuit and Equivalent Application

The comparator input voltage compliance is V_{CC} to V_{BAT}, and the maximum current is 240 µA in either direction. Its application is straightforward. A resistance (R_{TSN} + R_{TS2}) in series with the R_{TSN} input establishes a current which is repeated in the R_{TSP} input. A slightly lower resistance (R_{TSP}) is placed in series with the R_{TSP} input. When ringing is being injected, no dc current flows through R_{TS1}, and so the R_{TSP} input is at a lower potential than R_{TSN}. When enough dc loop current flows, the R_{TSP} input voltage increases to trip the comparator. In Figure 31, a low-pass filter with a double pole at 2 Hz was implemented to prevent false ring trip.

The following example illustrates how the detection circuit of Figure 31 will trip at 12.5 mA dc loop current using a –48 V battery.

$$I_N = \frac{-7-(-48)}{2.289\ k\Omega}$$
$$= 17.9\ \mu A$$

The current I_N is repeated as I_P in the positive comparator input. The voltage at comparator input R_{TSP} is:

$$V_{RTSP} = V_{BAT} + I_{LOOP(dc)} \times R_{TS1} + I_P \times R_{TSP}$$

Using this equation and the values in the example, the voltage at input R_{TSP} is –12 V during ringing injection ($I_{LOOP(dc)}$ = 0). Input R_{TSP} is therefore at a level of 5 V below R_{TSN}. When enough dc loop current flows through R_{TS1} to raise its dc drop to 5 V, the comparator will trip. In this example,

$$I_{LOOP(dc)} = \frac{5\ V}{402\ \Omega}$$
$$= 12.5\ mA$$

Ring Ground Detection

Pin ICM sinks a current proportional to the longitudinal loop current. It is also connected to an internal comparator whose output is pin RGDET. In a ground start application where tip is open, the ring ground current is half differential and half common mode. In this case, to set the ring ground current threshold, connect a resistor R_{ICM} from pin ICM to V_{CC}. Select the resistor according to the following relation:

$$R_{ICM}(k\Omega) = \frac{V_{CC} \times 228}{I_{RG}(mA)}$$

The above equation is shown graphically in Figure 18. It applies for the case of tip open. The more general equation can be used in ground key application to detect a common-mode current I_{CM}:

$$R_{ICM}(k\Omega) = \frac{V_{CC} \times 114}{I_{CM}(mA)}$$

Applications (continued)

ac Design

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is done from the PCM highway to the transmit port. Finally, the **hybrid balance** network cancels the unwanted amount of the receive signal that appears at the transmit port.

At this point in the design, the codec needs to be selected. The discrete network between the SLIC and the codec can then be designed. Here is a brief codec feature and selection summary.

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and µ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, and µ-law/A-law selectability. This generation of codecs has the lowest cost. They are most suitable for applications with fixed gains, termination impedance, and hybrid balance.

Second-Generation Codecs

This class of devices includes a microprocessor interface for software control of the gains and hybrid balance. The hybrid balance is included in the device. ac programmability adds application flexibility and saves several passive components and also adds several I/O latches that are needed in the application. However, it does not have the transmit op amp, since the transmit gain and hybrid balance are set internally.

Third-Generation Codecs

This class of devices includes the gains, termination impedance, and hybrid balance—all under microprocessor control. Depending on the device, it may or may not include latches.

Selection Criteria

In the following examples, use of a first-generation codec is shown. The equations for second- and third-generation codecs are simply subsets of these. There are two examples. The first shows the simplest circuit, which uses a minimum number of discrete components to synthesize a real termination impedance. The second example shows the use of the uncommitted op amp to synthesize a complex termination. The design has been automated in a DOS based program, available on request.

In the codec selection, increasing software control and flexibility are traded for device cost. To help decide, it may be useful to consider the following. Will the application require only one value for each gain and impedance? Will the board be used in different countries with different requirements? Will several versions of the board be built? If so, will one version of the board be most of the production volume? Does the application need only real termination impedance? Does the hybrid balance need to be adjusted in the field?

Applications (continued)

ac Design (continued)

Selection Criteria (continued)

ac equivalent circuits using a T7513 Codec are shown in Figures 32 and 33.

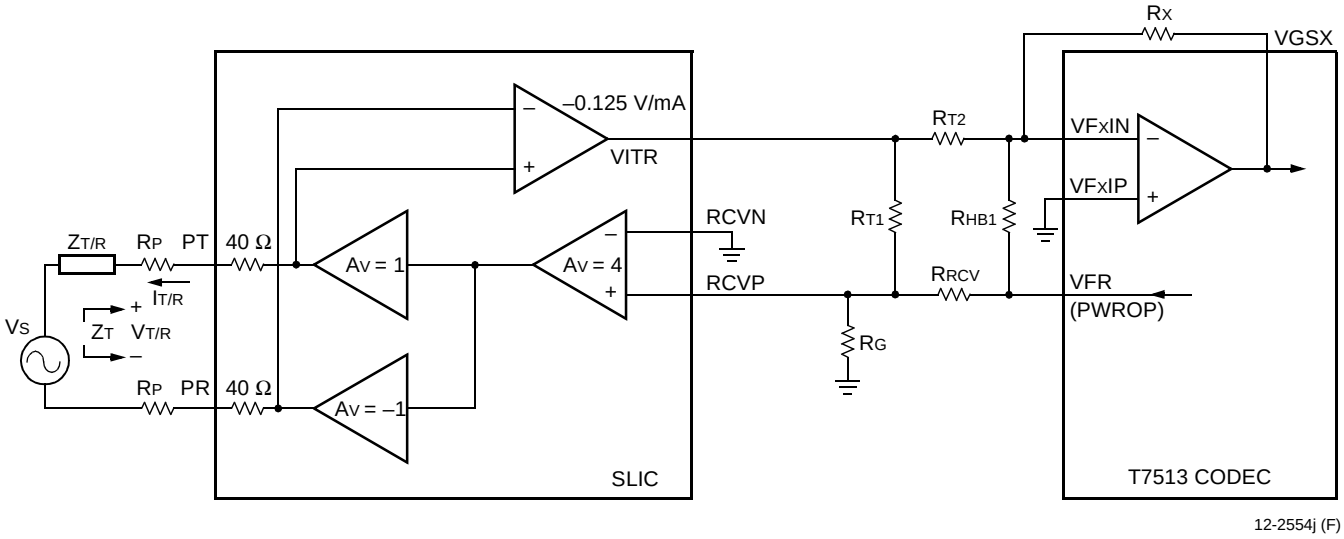


Figure 32. ac Equivalent Circuit Not Including Spare Op Amp

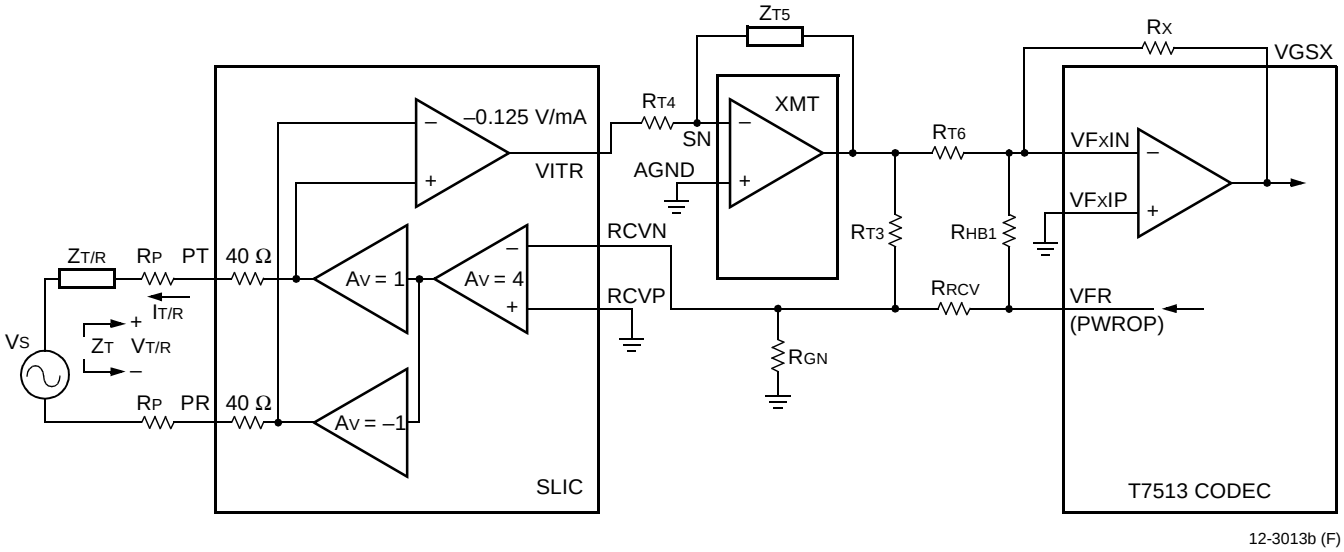


Figure 33. ac Equivalent Circuit Including Spare Op Amp

Applications (continued)

ac Design (continued)

Selection Criteria (continued)

Example 1, Real Termination:

The following design equations refer to the circuit in Figure 32. Use these to synthesize real termination impedance.

Termination Impedance:

$$Z_T = \frac{V_{T/R}}{-I_{T/R}}$$

$$Z_T = R_P + 80\ \Omega + \frac{1000}{1 + \frac{R_{T1}}{R_{GP}} + \frac{R_{T1}}{R_{RCV}}}$$

Receive Gain:

$$g_{rcv} = \frac{V_{T/R}}{V_{FR}}$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T1}} + \frac{R_{RCV}}{R_{GP}}\right)\left(1 + \frac{Z_T}{Z_{T/R}}\right)}$$

Transmit Gain:

$$g_{tx} = \frac{V_{GSX}}{V_{T/R}}$$

$$g_{tx} = \frac{-R_X}{R_{T2}} \times \frac{125}{Z_{T/R}}$$

Hybrid Balance:

$$h_{bal} = 20\log\frac{V_{GSX}}{V_{FR}}$$

To optimize the hybrid balance, the sum of the currents at the VFX input of the codec op amp should be set to 0. The following expressions assume the test network is the same as the termination impedance.

$$h_{bal} = 20\log\left(\frac{R_X}{R_{HB}} - g_{tx} \times g_{rcv}\right)$$

$$R_{HB} = \frac{R_X}{g_{tx} \times g_{rcv}}$$

Example 2, Complex Termination:

For complex termination, the spare op amp is used (see Figure 33).

$$Z_T = 2R_P + 80\ \Omega + \frac{1000}{1 + \frac{R_{T3}}{R_{GN}} + \frac{R_{T3}}{R_{RCV}}}\left(\frac{Z_{T5}}{R_{T4}}\right)$$

$$= 2R_P + 80\ \Omega + k(Z_{T5})$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GN}}\right)\left(1 + \frac{Z_T}{Z_{T/R}}\right)}$$

$$g_{tx} = \frac{-R_X}{R_{T6}} \times \frac{125}{Z_{T/R}} \times \frac{Z_{T5}}{R_{T4}}$$

The hybrid balance equation is the same as in Example 1.

PCB Layout Information

Make the leads to BGND and V_{BAT} as wide as possible for thermal and electrical reasons. Also, maximize the amount of PCB copper in the area of—and specifically on—the leads connected to this device for the lowest operating temperature.

When powering the device, ensure that no external potential creates a voltage on any pin of the device that exceeds the device ratings. In this application, some of the conditions that cause such potentials during powerup are the following: 1) an inductor connected to PT and PR (this can force an overvoltage on V_{BAT} through the protection devices if the V_{BAT} connection chatters), and 2) inductance in the V_{BAT} lead (this could resonate with the V_{BAT} filter capacitor to cause a destructive overvoltage).

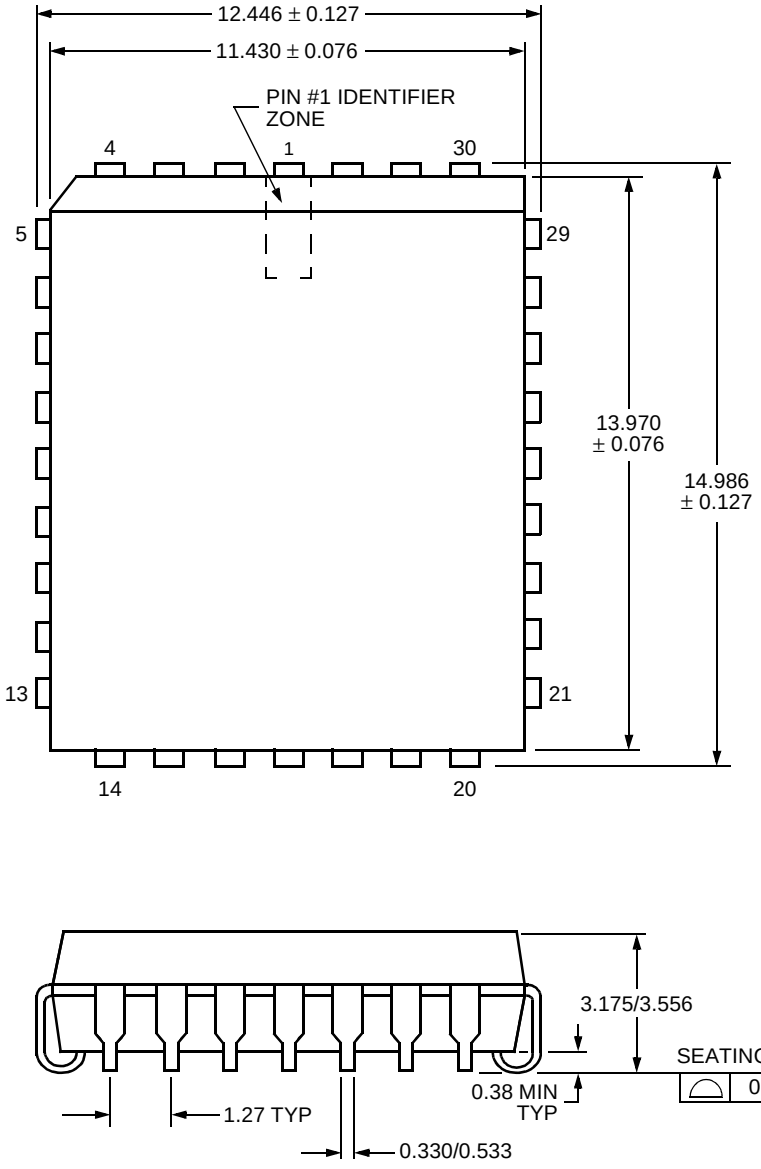
This device is normally used on a circuit card that is subjected to hot plug-in, meaning the card is plugged into a biased backplane connector. In order to prevent damage to the IC, all ground connections must be applied before, and removed after, all other connections.

Outline Diagram

32-Pin PLCC

Dimensions are in millimeters.

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.



5-3813F

Ordering Information

Device Part No.	Description	Package	Comcode
ATTL7556AAU	Low-Power SLIC with Battery Switch	32-Pin PLCC	107385668
ATTL7556AAU-TR	Low-Power SLIC with Battery Switch	32-Pin PLCC (Tape and Reel)	107749509
ATTL7557AAU	Low-Power SLIC with Battery Switch	32-Pin PLCC	107385841
ATTL7557AAU-TR	Low-Power SLIC with Battery Switch	32-Pin PLCC (Tape and Reel)	107749517

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