独立的控制器局域网 (CAN) 收发器

查询样品: ISO1050

特性

- 满足符合 **ISO11898-2** 标准的要求
- **5000 V_{RMS}**隔离 **(ISO1050DW)**
- **2500 V_{RMS}**隔离
- 故障安全输出
- 低环路延迟：**150ns**（典型值），**210ns**（最大值）
- **50kV/μs** 典型瞬态抗扰度
- **-27V** 至 **40V** 的总线故障保护
- 驱动器 **(TXD)** 主超时功能
- **IEC 60747-5-2** （**VDE 0884**，修订版本 **2**）和 **IEC 61010-1** 已被批准
- **UL 1577** 双重保护已获批准；请见管理信息
- **IEC 60601-1**（医疗用）和 **CSA** 已通过检验
- **5 KV_{RMS}**针对 **EN/UL/CSA 60950-1 (ISO1050DW)** 根据 **TUV** 认可的增强型隔离
- **I/O** 电压范围支持 **3.3V** 和 **5V** 微处理器
- 额定工作电压下典型值为 **25** 年使用寿命到特性（参见应用报告**SLLA197**和**Figure 18**）

应用范围

- 工业自动化、控制、传感器和驱动系统
- 楼宇和温室环境控制（暖通空调 **(HVAC)**）控制自动化
- 安防系统
- 运输
- 医疗
- 电信
- 诸如 **CANopen**，**DeviceNet**，**NMEA2000**，**ARNIC825**，**ISO11783**，**CAN Kingdom**，**CANaerospace** 的 **CAN** 总线标准

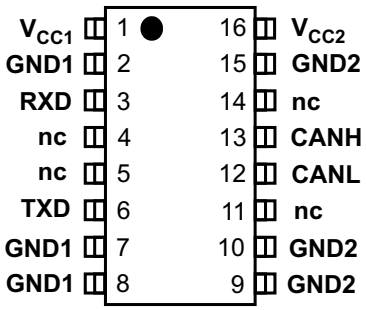
说明

ISO1050 是一款电镀隔离的 CAN 转发器，此转发器符合或者优于 ISO11898-2 标准的技术规范。 此器件有几个由氧化硅 (SiO_2) 绝缘隔栅分开的逻辑输入和输出缓冲器，此绝缘隔栅为说明第一段中的 ISO1050DW 和针对 ISO1050DUB 的 2500 V_{RMS}。 与隔离式电源一起使用，此器件可防止数据总线或者其它电路上的噪音电流进入本地接地并干扰和损坏敏感电路。

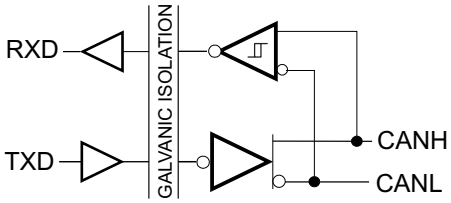
作为一个 CAN 转发器，此器件为总线和信令速度高达 1 兆比特每秒 (Mbps) 的 CAN 控制器分别提供差分发射能力和差分接收能力。 设计运行在特别恶劣的环境中，此器件特有串线，过压，-27V 至 40V 的接地损失保护和过热关断，以及 -12V 到 12V 的共模范围。

ISO1050 额定运行环境温度范围为 –55°C 至 105°C。

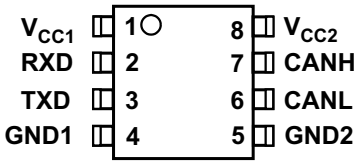
DW PACKAGE



FUNCTION DIAGRAM



DUB PACKAGE



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

PRODUCT	RATED ISOLATION	PACKAGE	MARKED AS	ORDERING NUMBER
ISO1050DUB	2500 V_{RMS}	DUB-8	ISO1050	ISO1050DUB (rail)
				ISO1050DUBR (reel)
ISO1050DW	5000 V_{RMS}	DW-16	ISO1050	ISO1050DW (rail)
				ISO1050DWR (reel)

PIN FUNCTIONS

PIN			TYPE	DESCRIPTION
NAME	PACKAGE			
	DW	DUB		
V_{CC1}	1	1	Supply	Digital side supply voltage (3 to 5.5V)
GND1	2	NA	GND1	Digital side ground connection
RXD	3	2	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
NC	4	NA	NC	No connect
NC	5	NA	NC	No connect
TXD	6	3	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND1	7	4	GND1	Digital side ground connection
GND1	8	NA	GND1	Digital side ground connection
GND2	9	5	GND2	Transceiver side ground connection
GND2	10	NA	GND2	Transceiver side ground connection
NC	11	NA	NC	No connect
CANL	12	6	I/O	Low level CAN bus line
CANH	13	7	I/O	High level CAN bus line
NC	14	NA	NC	No connect
GND2	15	NA	GND2	Transceiver side ground connection
V_{CC2}	16	8	Supply	Transceiver side supply voltage (5V)

FUNCTIONAL DESCRIPTION

CAN BUS STATES

The CAN bus has two states during operation: *dominant* and *recessive*. A dominant bus state, equivalent to logic low, is when the bus is driven differentially by a driver. A recessive bus state is when the bus is biased to a common mode of V_{CC} / 2 via the high-resistance internal input resistors of the receiver, equivalent to a logic high. The host microprocessor of the CAN node will use the TXD pin to drive the bus and will receive data from the bus on the RXD pin. See Figure 1 and Figure 2.

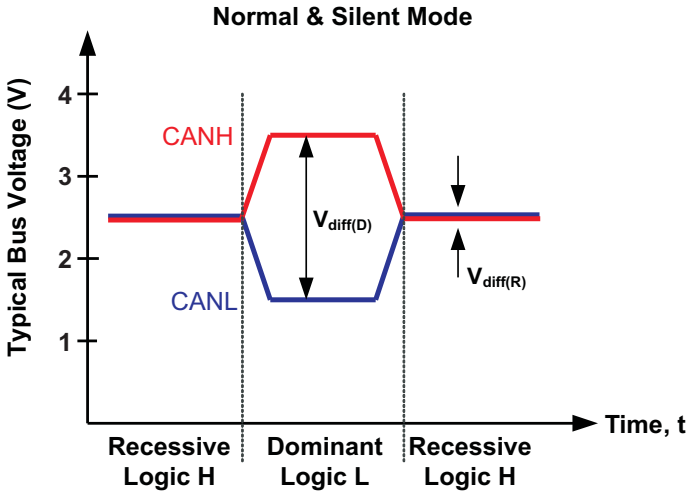


Figure 1. Bus States (Physical Bit Representation)

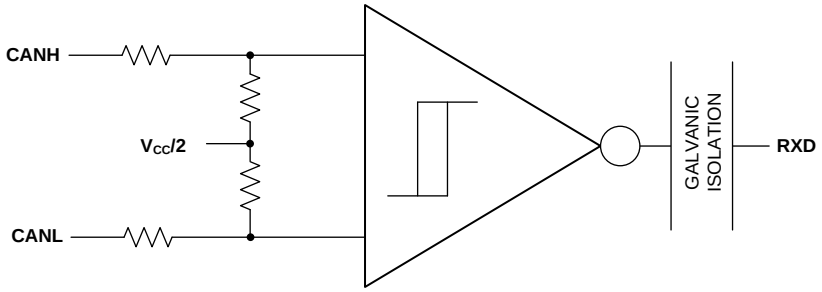


Figure 2. Simplified Recessive Common Mode Bias and Receiver

DRIVER AND RECEIVER FUNCTION TABLES

Table 1. Driver Function Table

INPUT	OUTPUTS		DRIVEN BUS STATE
TXD(1)	CANH(1)	CANL(1)	
L	H	L	Dominant
H	Z	Z	Recessive

(1) H = high level, L = low level, Z = common mode (recessive) bias to V_{CC} / 2. See Figure 1 and Figure 2 for bus state and common mode bias information.

Table 2. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD PIN(1)
Normal or Silent	$V_{ID} \geq 0.9$ V	Dominant	L
	0.5 V < V_{ID} < 0.9 V	?	?
	$V_{ID} \leq 0.5$ V	Recessive	H
	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level, ? = indeterminate.

DIGITAL INPUTS AND OUTPUTS

TXD (Input) and RXD (Output):

V_{CC1} for the isolated digital input and output side of the device maybe supplied by a 3.3 V or 5 V supply and thus the digital inputs and outputs are 3.3 V and 5 V compatible.

NOTE

TXD is very weakly internally pulled up to V_{CC1}. An external pull up resistor should be used to make sure that TXD is biased to recessive (high) level to avoid issues on the bus if the microprocessor doesn't control the pin and TXD floats. TXD pullup strength and CAN bit timing require special consideration when the device is used with an open-drain TXD output on the microprocessor's CAN controller. An adequate external pullup resistor must be used to ensure that the TXD output of the microprocessor maintains adequate bit timing input to the input on the transceiver.

PROTECTION FEATURES

TXD Dominant Timeout (DTO)

TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit timer starts on a falling edge on TXD. The TXD DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on the TXD pin, thus clearing the TXD DTO condition. The receiver and RXD pin still reflect the CAN bus, and the bus pins are biased to recessive level during a TXD dominant timeout.

NOTE

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate by: Minimum Data Rate = 11 / t_{TXD_DTO}.

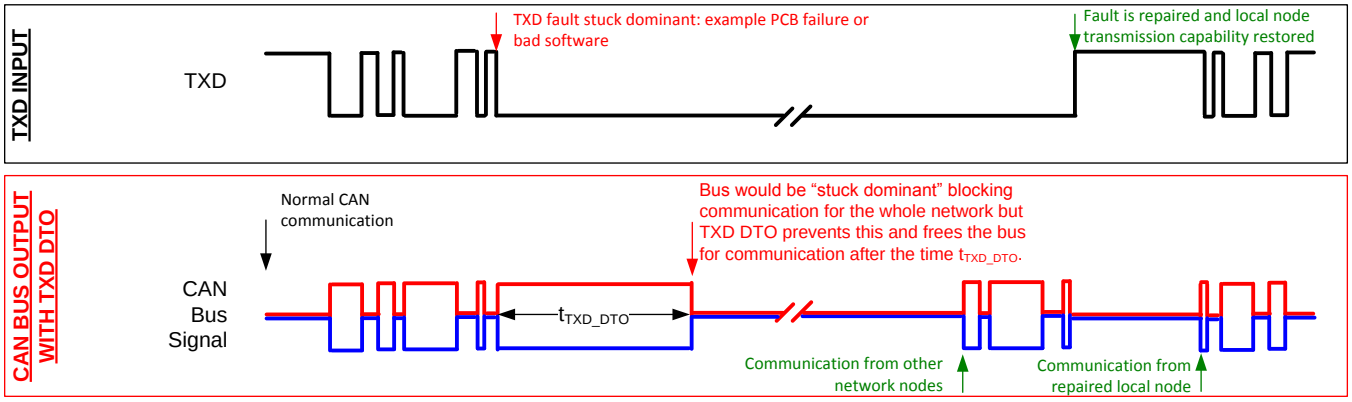


Figure 3. Example Timing Diagram for Devices With TXD DTO

Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device. If the fault condition is still present, the temperature may rise again and the device would enter thermal shut down again. Prolonged operation with thermal shutdown conditions may affect device reliability.

NOTE

During thermal shutdown the CAN bus drivers turn off; thus no transmission is possible from TXD to the bus. The CAN bus pins are biased to recessive level during a thermal shutdown, and the receiver to RXD path remains operational.

Undervoltage Lockout and Failsafe

The supply pins have undervoltage detection that places the device in protected or failsafe mode. This protects the bus during an undervoltage event on V_{CC1} or V_{CC2} supply pins. If the bus-side power supply Vcc2 is lower than about 2.7V, the power shutdown circuits in the ISO1050 will disable the transceiver to prevent false transmissions due to an unstable supply. If Vcc1 is still active when this occurs, the receiver output (RXD) will go to a failsafe HIGH (recessive) value in about 6 microseconds.

Table 3. Undervoltage Lockout and Failsafe

$V_{CC}1$	$V_{CC}2$	DEVICE STATE	BUS OUTPUT	RXD
GOOD	GOOD	Functional	Per Device State and TXD	Mirrors Bus
BAD	GOOD	Protected	Recessive	High Impedance (3-state)
GOOD	BAD	Protected	High Impedance	Recessive (Failsafe High)

NOTE

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation in 300 µs

Floating Pins

Pull ups and pull downs should be used on critical pins to place the device into known states if the pins float. The TXD pin should be pulled up via a resistor to V_{CC1} to force a recessive input level if the microprocessor output to the pin floats.

CAN Bus Short Circuit Current Limiting

The device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include driver current limiting (dominant and recessive). The device has TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states with the data and control fields bits, thus the short circuit current may be viewed either as the instantaneous current during each bus state, or as a DC average current. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit stuffing
- Interframe space
- TXD dominant time out (fault case limiting)

These ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

NOTE

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

$I_{OS(AVG)}$ = %Transmit × [(%REC_Bits × $I_{OS(SS)\_REC}$) + (%DOM_Bits × $I_{OS(SS)\_DOM}$)] + [%Receive × $I_{OS(SS)\_REC}$]

Where

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

NOTE

Consider the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

ABSOLUTE MAXIMUM RATINGS(1) (2)

				VALUE / UNIT
V_{CC1}, V_{CC2}	Supply voltage (3)			–0.5 V to 6 V
V_I	Voltage input (TXD)			–0.5 V to 6 V
V_{CANH} or V_{CANH}	Voltage range at any bus terminal (CANH, CANL)			–27 V to 40 V
I_O	Receiver output current			±15 mA
ESD	Human Body Model	JEDEC Standard 22, Method A114-C.01	Bus pins and GND2(4)	±4 kV
			All pins	±4 kV
	Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1.5 kV
	Machine Model	ANSI/ESDS5.2-1996	All pins	±200 V
T_{stg}	Storage temperature			–65°C to 150°C
T_J	Junction temperature			–55°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This isolator is suitable for basic isolation within the safety limiting data. Maintenance of the safety data must be ensured by means of protective circuitry.
(3) All input and output logic voltage values are measured with respect to the GND1 logic side ground. Differential bus-side voltages are measured to the respective bus-side GND2 ground terminal.
(4) Tested while connected between Vcc2 and GND2.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage, controller side		3		5.5	V
V_{CC2}	Supply voltage, bus side		4.75	5	5.25	V
V_I or V_{IC}	Voltage at bus pins (separately or common mode)		–12(1)		12	V
V_{IH}	High-level input voltage	TXD	2		5.25	V
V_{IL}	Low-level input voltage	TXD	0		0.8	V
V_{ID}	Differential input voltage		–7		7	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–4			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			4	
T_A	Ambient Temperature		–55		105	°C
T_J	Junction temperature (see THERMAL CHARACTERISTICS)		–55		125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC1}	V_{CC1} Supply current		V_I = 0 V or V_{CC1} , V_{CC1} = 3.3V		1.8	2.8	mA
			V_I = 0 V or V_{CC1} , V_{CC1} = 5V		2.3	3.6	
I_{CC2}	V_{CC2} Supply current	Dominant	V_I = 0 V, 60-Ω Load		52	73	mA
		Recessive	V_I = V_{CC1}		8	12	

(1) All typical values are at 25°C with V_{CC1} = V_{CC2} = 5V.

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input to receiver output, Recessive to Dominant	See Figure 12	112	150	210	ns
t_{loop2}	Total loop delay, driver input to receiver output, Dominant to Recessive	See Figure 12	112	150	210	ns

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	See Figure 4 and Figure 5, V_I = 0 V, R_L = 60Ω	2.9	3.5	4.5	V
		CANL		0.8	1.2	1.5	
$V_{O(R)}$	Bus output voltage (Recessive)		See Figure 4 and Figure 5, V_I = 2 V, R_L= 60Ω	2	2.3	3	V
$V_{OD(D)}$	Differential output voltage (Dominant)		See Figure 4, Figure 5 and Figure 6, V_I = 0 V, R_L = 60Ω	1.5		3	V
			See Figure 4, Figure 5, and Figure 6 V_I = 0 V, R_L = 45Ω, Vcc > 4.8V	1.4		3	
$V_{OD(R)}$	Differential output voltage (Recessive)		See Figure 4 and Figure 5, V_I = 3 V, R_L = 60Ω	–0.12		0.012	V
			V_I = 3 V, No Load	–0.5		0.05	
$V_{OC(D)}$	Common-mode output voltage (Dominant)		See Figure 11	2	2.3	3	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage				0.3		
I_{IH}	High-level input current, TXD input		V_I at 2 V			5	µA
I_{IL}	Low-level input current, TXD input		V_I at 0.8 V	–5			µA
$I_{O(off)}$	Power-off TXD leakage current		V_{CC1}, V_{CC2} at 0 V, TXD at 5 V			10	µA
$I_{OS(ss)}$	Short-circuit steady-state output current		See Figure 14, V_{CANH} = –12 V, CANL Open	–105	–72		mA
			See Figure 14, V_{CANH} = 12 V, CANL Open		0.36	1	
			See Figure 14, V_{CANL} =–12 V, CANH Open	–1	–0.5		
			See Figure 14, V_{CANL} = 12 V, CANH Open		71	105	
C_O	Output capacitance		See receiver input capacitance				
CMTI	Common-mode transient immunity		See Figure 16, V_I = V_{CC} or 0 V	25	50		kV/µs

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, recessive-to-dominant output	See Figure 7	31	74	110	ns
t_{PHL}	Propagation delay time, dominant-to-recessive output		25	44	75	
t_r	Differential output signal rise time			20	50	
t_f	Differential output signal fall time			20	50	
t_{dom} (1)	Dominant time-out	↓ C_L=100 pF, See Figure 13	300	450	700	µs

(1) The TXD dominant time out (t_{dom}) disables the driver of the transceiver once the TXD has been dominant longer than (t_{dom}) which releases the bus lines to recessive preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults locking the bus dominant it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case where five successive dominant bits are followed immediately by an error frame. This along with the (t_{dom}) minimum limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ (t_{dom}) = 11 bits / 300 µs = 37 kbps.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going bus input threshold voltage	See Table 4		750	900	mV
V_{IT-}	Negative-going bus input threshold voltage		500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			150		mV
V_{OH}	High-level output voltage with Vcc = 5V	I_{OH} = –4 mA, See Figure 9	V_{CC} – 0.8	4.6		V
		I_{OH} = –20 µA, See Figure 9	V_{CC} – 0.1	5		
V_{OH}	High-level output voltage with Vcc1 = 3.3V	I_{OL} = 4 mA, See Figure 9	V_{CC} – 0.8	3.1		V
		I_{OL} = 20 µA, See Figure 9	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 9		0.2	0.4	V
		I_{OL} = 20 µA, See Figure 9		0	0.1	
C_I	Input capacitance to ground, (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5V		6		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		3		pF
R_{ID}	Differential input resistance	TXD at 3 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching $(1 - [R_{IN\ (CANH)} / R_{IN\ (CANL)}]) \times 100\%$	$V_{CANH} = V_{CANL}$	–3%	0%	3%	
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 16	25	50		kV/µs

(1) All typical values are at 25°C with $V_{CC1} = V_{CC2}$ = 5V.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	TXD at 3 V, See Figure 9	66	90	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		51	80	105	
t_r	Output signal rise time			3	6	
t_f	Output signal fall time			3	6	
t_{fs}	Failsafe output delay time from bus-side power loss	VCC1 at 5 V, See Figure 15		6		µs

PARAMETER MEASUREMENT INFORMATION

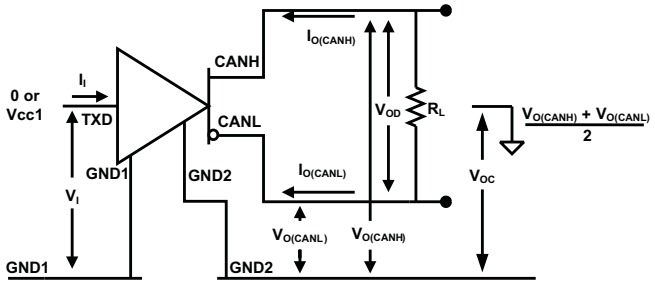


Figure 4. Driver Voltage, Current and Test Definitions

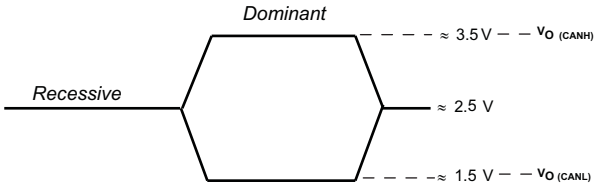


Figure 5. Bus Logic State Voltage Definitions

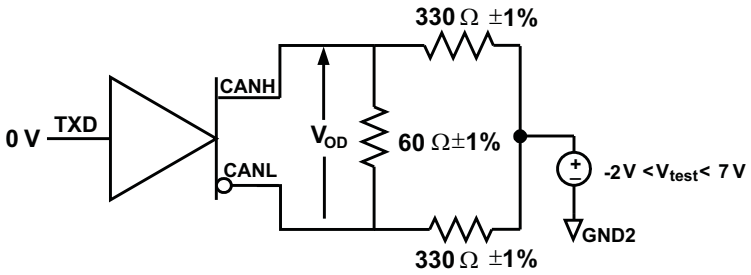
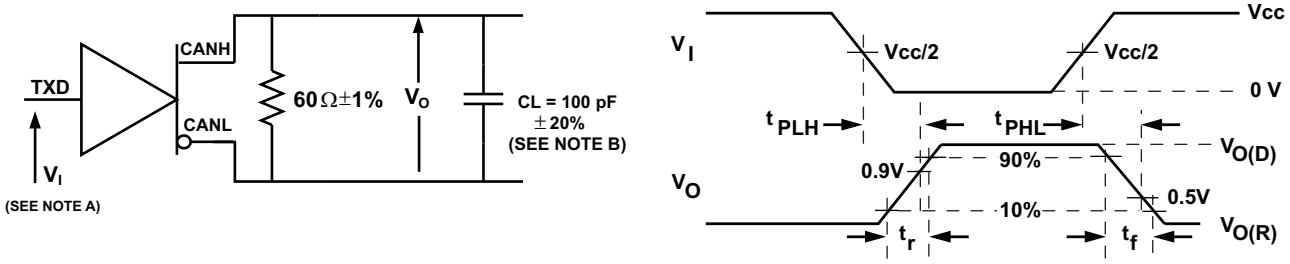


Figure 6. Driver V_{OD} with Common-mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7. Driver Test Circuit and Voltage Waveforms

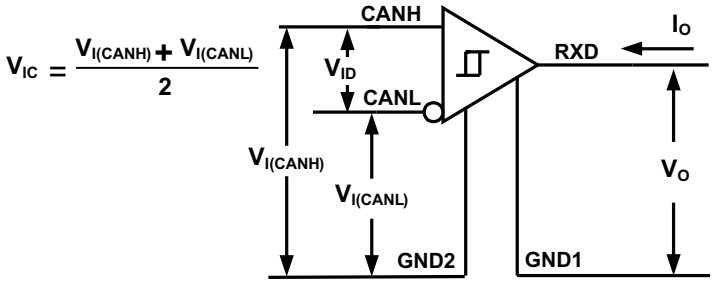
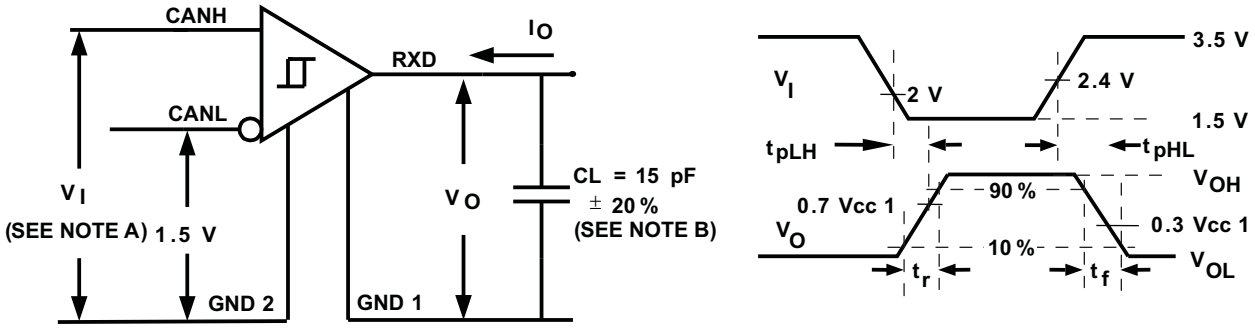


Figure 8. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



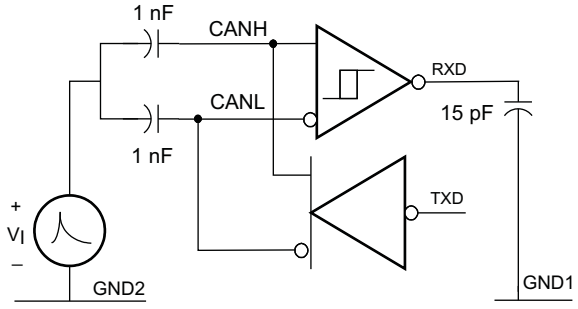
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 9. Receiver Test Circuit and Voltage Waveforms

Table 4. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	–6 V	H	
6 V	12 V	–6 V	H	
Open	Open	X	H	



The waveforms of the applied transients are in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b.

Figure 10. Transient Over-Voltage Test Circuit

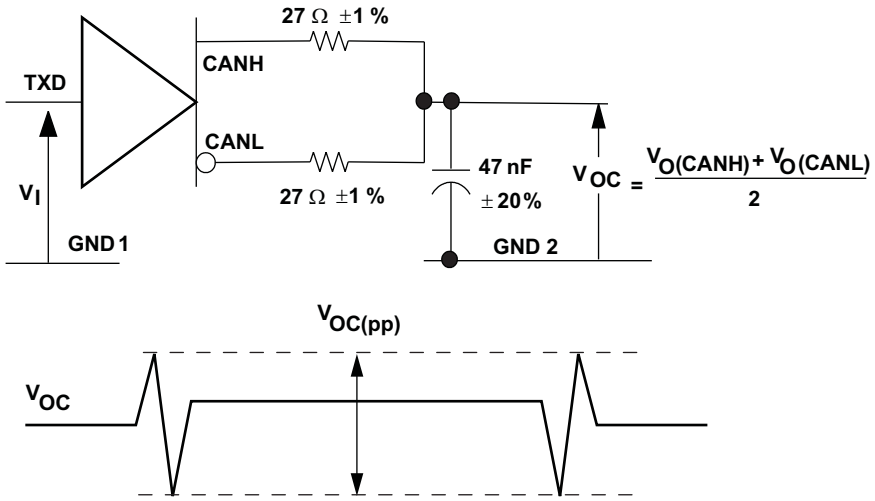


Figure 11. Peak-to-Peak Output Voltage Test Circuit and Waveform

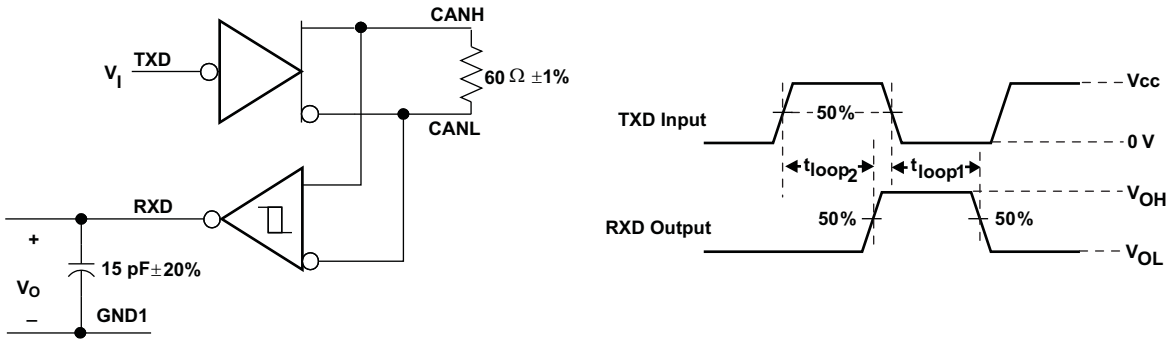
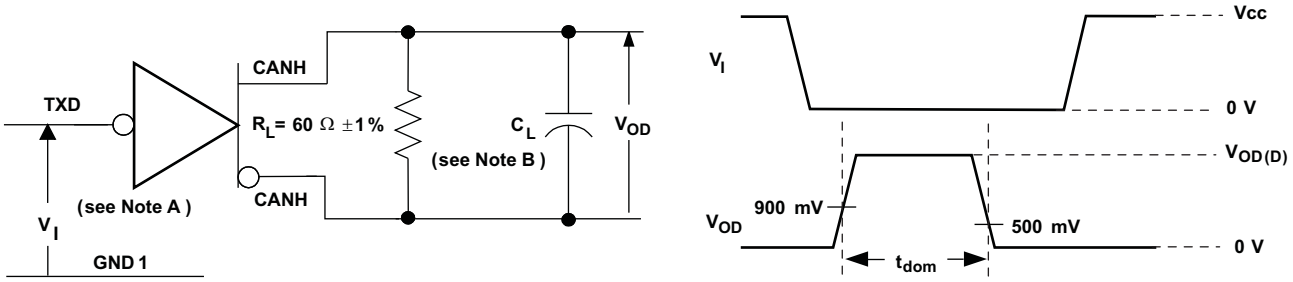


Figure 12. t_{LOOP} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 13. Dominant Timeout Test Circuit and Voltage Waveforms

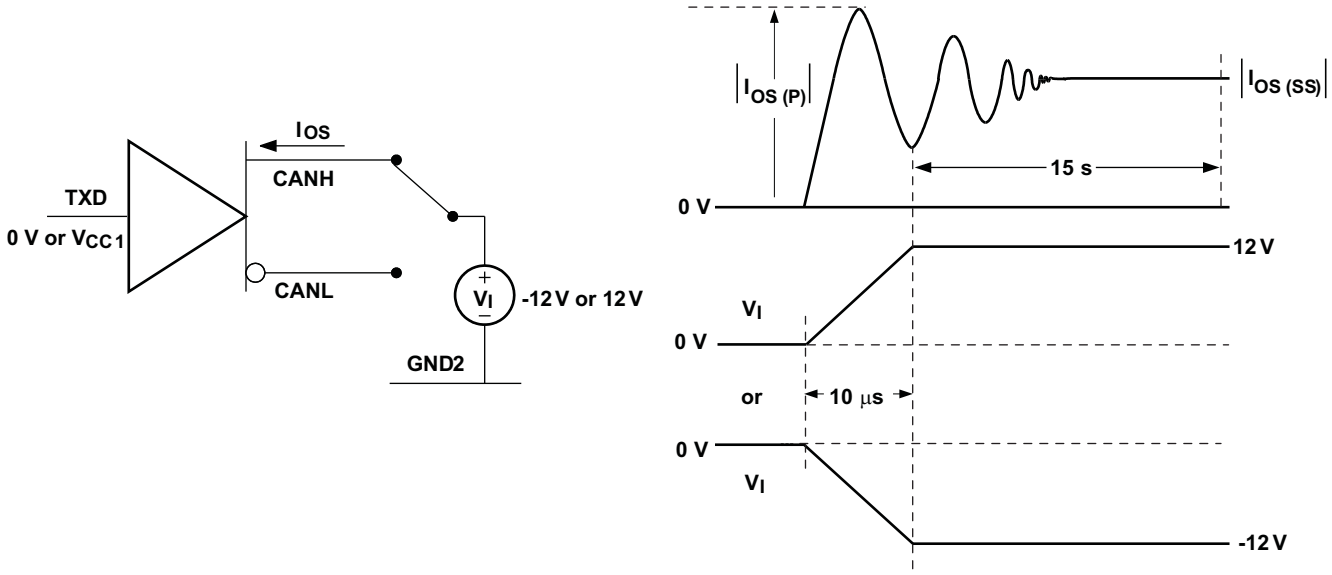


Figure 14. Driver Short-Circuit Current Test Circuit and Waveforms

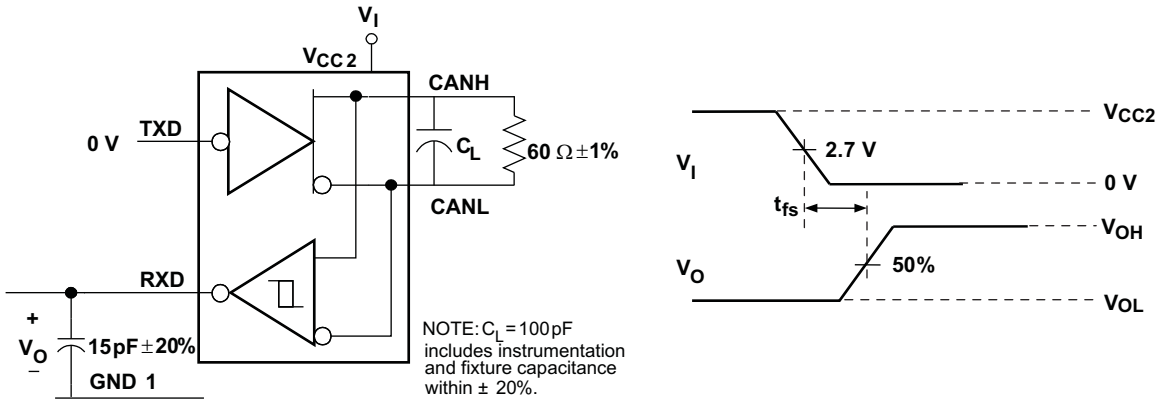


Figure 15. Failsafe Delay Time Test Circuit and Voltage Waveforms

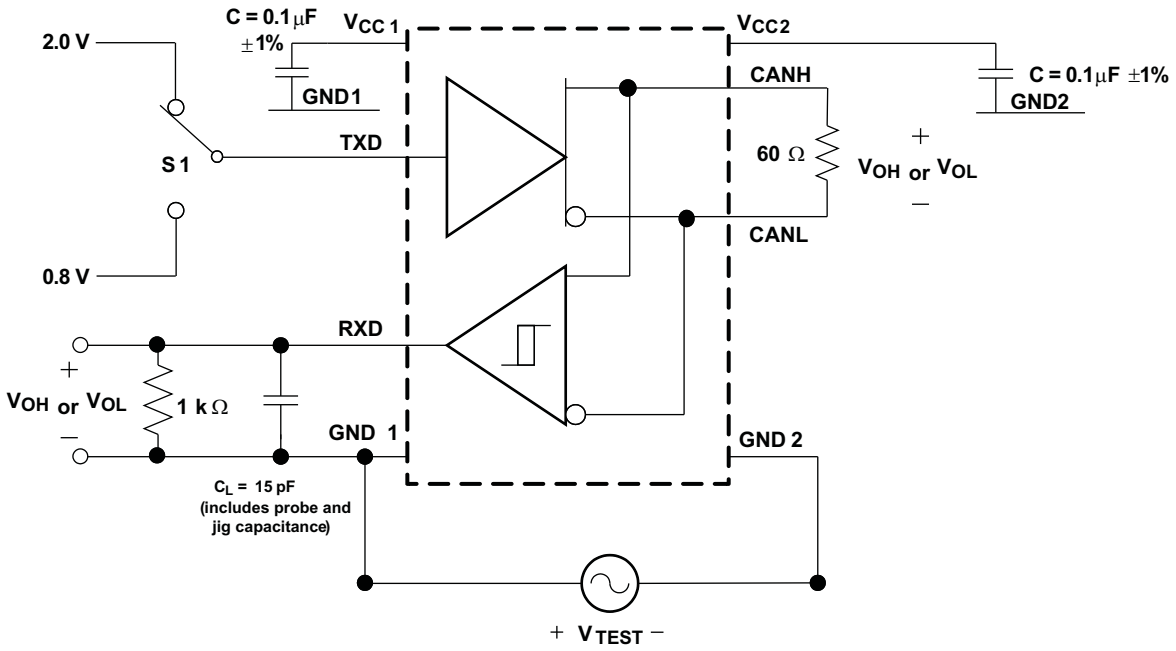


Figure 16. Common-Mode Transient Immunity Test Circuit

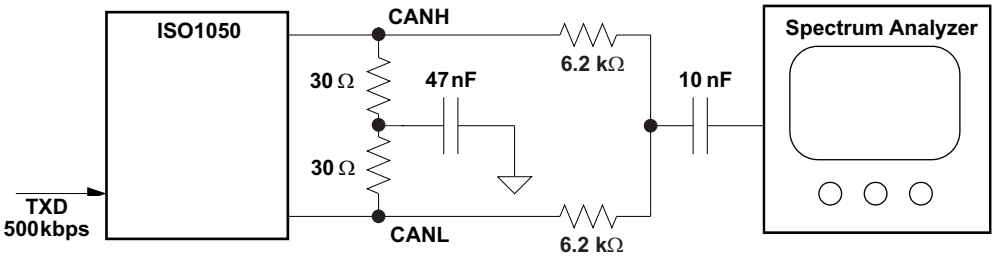


Figure 17. Electromagnetic Emissions Measurement Setup

DEVICE INFORMATION

FUNCTION TABLE(1)

DRIVER					RECEIVER		
INPUTS	OUTPUTS		BUS STATE		DIFFERENTIAL INPUTS V_{ID} = CANH–CANL	OUTPUT RXD	BUS STATE
TXD	CANH	CANL					
L(2)	H	L	DOMINANT		$V_{ID} \geq 0.9$ V	L	DOMINANT
H	Z	Z	RECESSIVE		0.5 V < V_{ID} < 0.9 V	?	?
Open	Z	Z	RECESSIVE		$V_{ID} \leq 0.5$ V	H	RECESSIVE
X	Z	Z	RECESSIVE		Open	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance
(2) Logic low pulses to prevent dominant time-out.

ISOLATOR CHARACTERISTICS (1) (2)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air, per JEDEC package dimensions	DUB-8	6.1			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface, per JEDEC package dimensions	DUB-8	6.8			mm
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air, per JEDEC package dimensions	DW-16	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface, per JEDEC package dimensions	DW-16	8.10			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation		0.014			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, Tamb < 100°C			$>10^{12}$		Ω
		Input to output V_{IO} = 500 V, 100°C ≤Tamb ≤Tamb max			$>10^{11}$		Ω
C_{IO}	Barrier capacitance	V_I = 0.4 sin (4E6πt)			1.9		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)			1.3		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.
(2) Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

INSULATION CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage per DIN EN 60747-5-2	ISO1050DUB		560	Vpeak
		ISO1050DW		1200	
V_{PR}	Input to output test voltage per DIN EN 60747-5-2	ISO1050DUB	$V_{P\ R}$ = 1.875 x V_{IORM}, t = 1 sec (100% production) Partial discharge < 5 pC	1050	Vpeak
		ISO1050DW		2250	
V_{IOTM}	Transient overvoltage per DIN EN 60747-5-2		t = 60 sec (qualification)	4000	Vpeak
			t = 1 sec (100% production)		
V_{ISO}	Isolation voltage per UL 1577	ISO1050DUB - Double Protection	t = 60 sec (qualification)	2500	Vrms
			t = 1 sec (100% production)	3000	
		ISO1050DW - Single Protection	t = 60 sec (qualification)	4243	Vrms
			t = 1 sec (100% production)	5092	
R_S	Isolation resistance		V_{IO} = 500 V at T_S	$> 10^9$	Ω
	Pollution Degree			2	

IEC 60664-1 RATINGS

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 Vrms	I–IV
	Rated mains voltage ≤ 300 Vrms	I–III
	Rated mains voltage ≤ 400 Vrms	I–II
	Rated mains voltage ≤ 600 Vrms (ISO1050DW only)	I-II
	Rated mains voltage ≤ 848 Vrms (ISO1050DW only)	I

IEC SAFETY LIMITING VALUES

safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DUB-8	θ_{JA} = 73.3 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			310	mA
			θ_{JA} = 73.3 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			474	
		DW-16	θ_{JA} = 76 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			299	mA
			θ_{JA} = 76 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			457	
T_S	Maximum case temperature					150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assured junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

REGULATORY INFORMATION

VDE	TUV	CSA	UL
Certified according to DIN EN 60747-5-2	Certified according to EN/UL/CSA 60950-1	Approved under CSA Component Acceptance Notice #5A	Recognized under 1577 (1)Component Recognition Program
Basic Insulation Transient Overvoltage, 4000 V_{PK} Surge Voltage, 4000 V_{PK} Maximum Working Voltage, 1200 V_{PK} (ISO1050DW) and 560 V_{PK} (ISO1050DUB)	**ISO1050DW:** 5000 V_{RMS} Reinforced Insulation, 400 V_{RMS} maximum working voltage 5000 V_{RMS} Basic Insulation, 600 V_{RMS} maximum working voltage **ISO1050DUB:** 2500 V_{RMS} Reinforced Insulation, 400 V_{RMS} maximum working voltage 2500 V_{RMS} Basic Insulation, 600 V_{RMS} maximum working voltage	5000 V_{RMS} Reinforced Insulation 2 Means of Patient Protection at 125 V_{RMS} per IEC 60601-1 (3rd Ed.)	ISO1050DUB: 2500 V_{RMS} Double Protection ISO1050DW: 3500 V_{RMS} Double Protection, 4243 V_{RMS} Single Protection
File Number: 40016131	Certificate Number: U8V 11 09 77311 008	File Number: 220991	File Number: E181974

(1) Production tested ≥ 3000 V_{RMS} (ISO1050DUB) and 5092 V_{RMS} (ISO1050DW) for 1 second in accordance with UL 1577.

THERMAL INFORMATION (DUB-8 PACKAGE)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance (1)		120		°C/W
		High-K Thermal Resistance		73.3		°C/W
θ_{JB}	Junction-to-board thermal resistance	Low-K Thermal Resistance		10.2		°C/W
θ_{JC}	Junction-to-case thermal resistance	Low-K Thermal Resistance		14.5		°C/W
P_D	Device power dissipation	V_{CC1}= 5.5V, V_{CC2}= 5.25V, T_A=105°C, R_L= 60Ω, TXD input is a 500kHz 50% duty-cycle square wave			200	mW
$T_{j\ shutdown}$	Thermal shutdown temperature (2)			190		°C

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.
(2) Extended operation in thermal shutdown may affect device reliability.

THERMAL INFORMATION (DW-16 PACKAGE)

THERMAL METRIC(1)		ISO1050 DW 16	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	76.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	41	
θ_{JB}	Junction-to-board thermal resistance	47.7	
ψ_{JT}	Junction-to-top characterization parameter	14.4	
ψ_{JB}	Junction-to-board characterization parameter	38.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

LIFE EXPECTANCY vs WORKING VOLTAGE (ISO1050DUB)

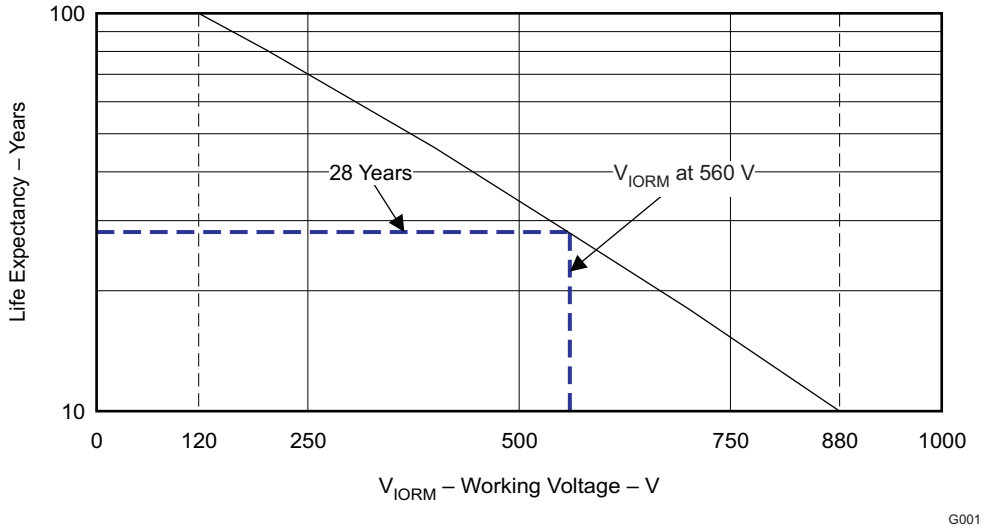
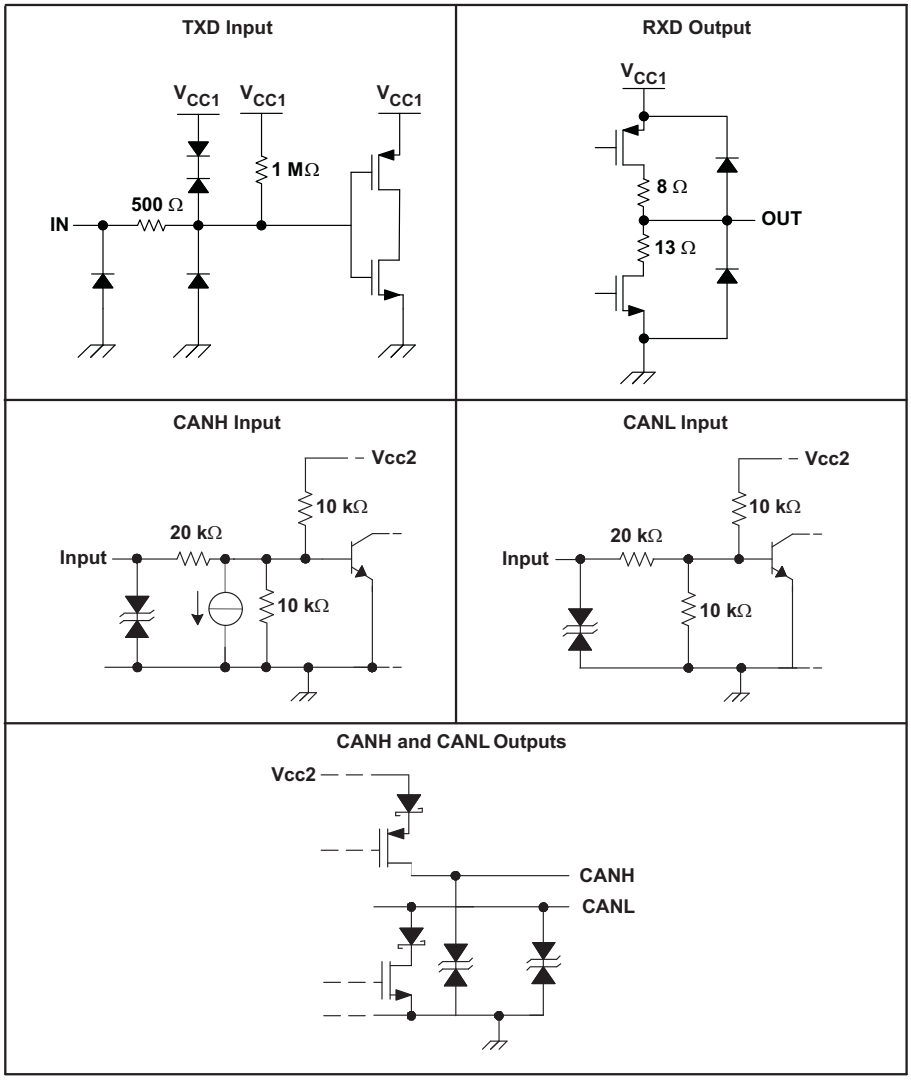


Figure 18. Life Expectancy vs Working Voltage

EQUIVALENT I/O SCHEMATICS



TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME
vs
FREE-AIR TEMPERATURE (across Vcc)

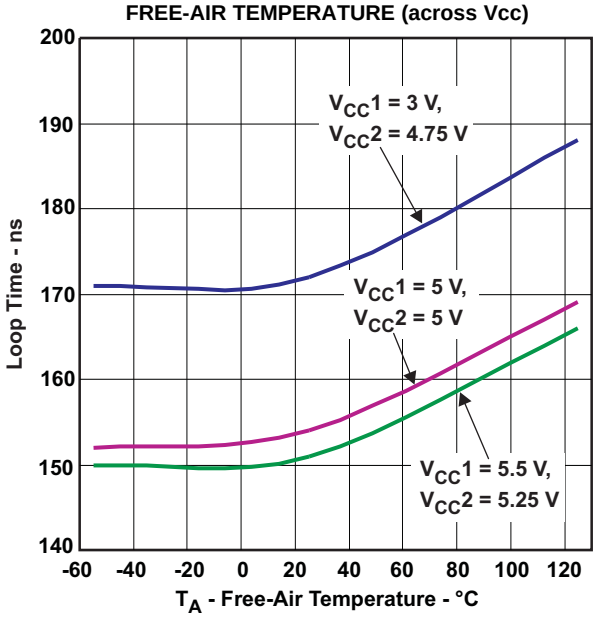


Figure 19.

DOMINANT-TO-RECESSIVE LOOP TIME
vs
FREE-AIR TEMPERATURE (across Vcc)

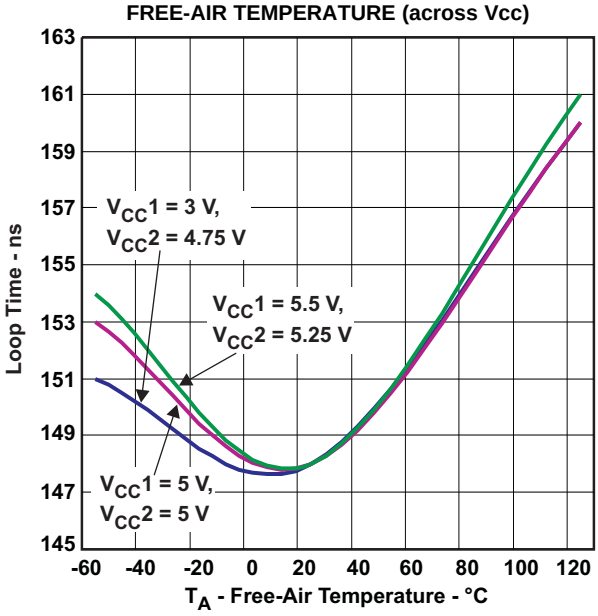


Figure 20.

SUPPLY CURRENT (RMS)
vs
SIGNALING RATE (kbps)

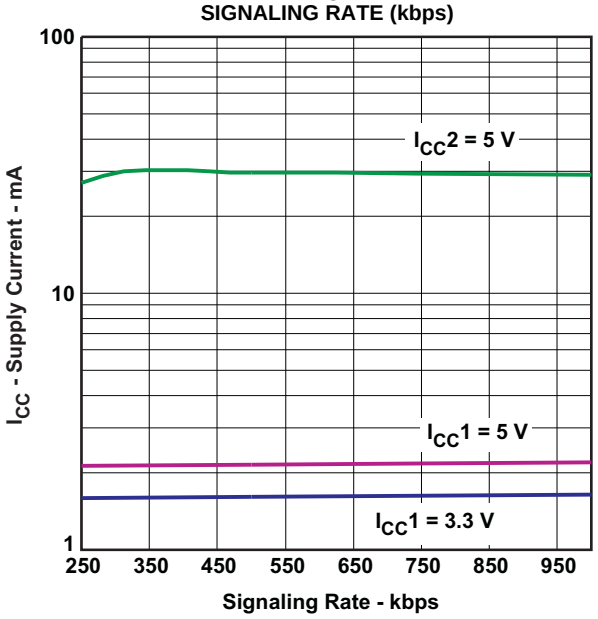


Figure 21.

DRIVER OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

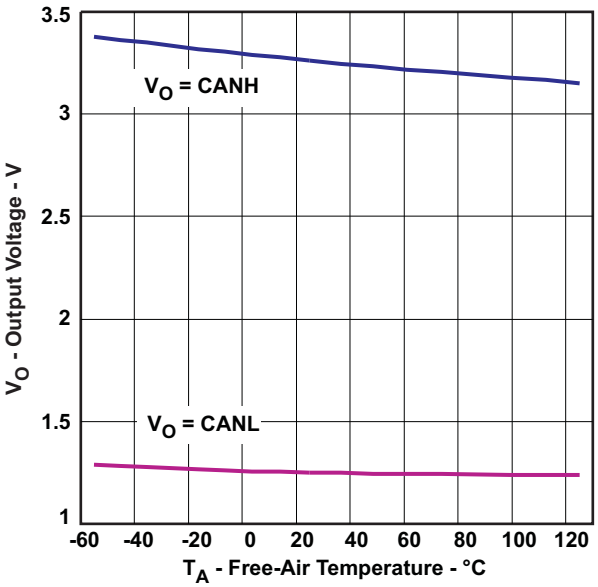


Figure 22.

TYPICAL CHARACTERISTICS (continued)

EMISSIONS SPECTRUM TO 10 MHz

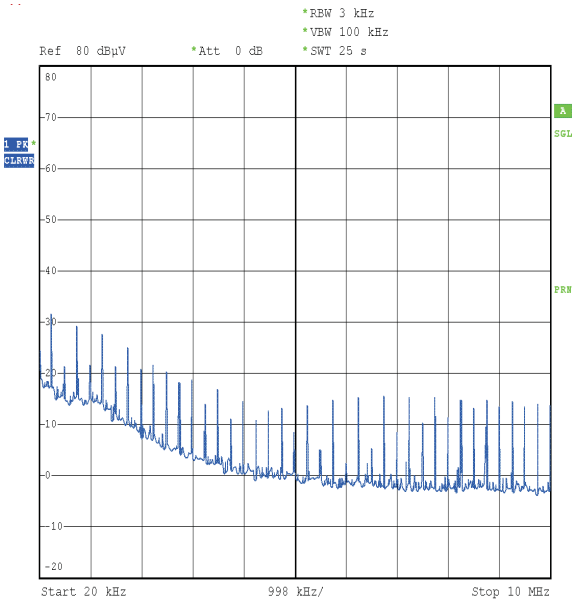


Figure 23.

EMISSIONS SPECTRUM TO 50 MHz

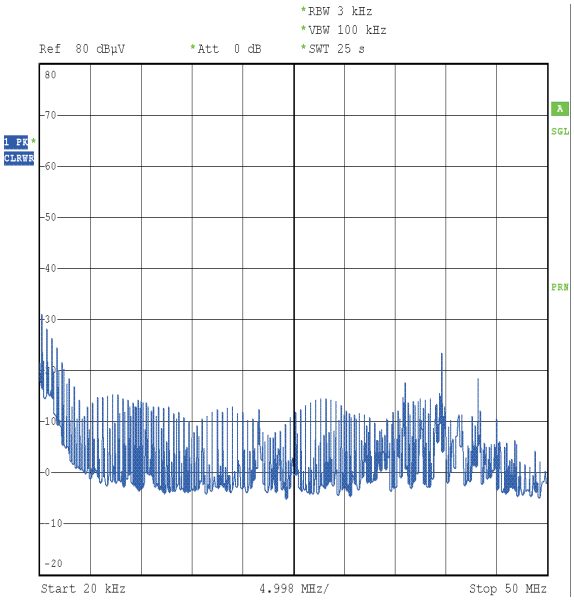


Figure 24.

APPLICATION INFORMATION

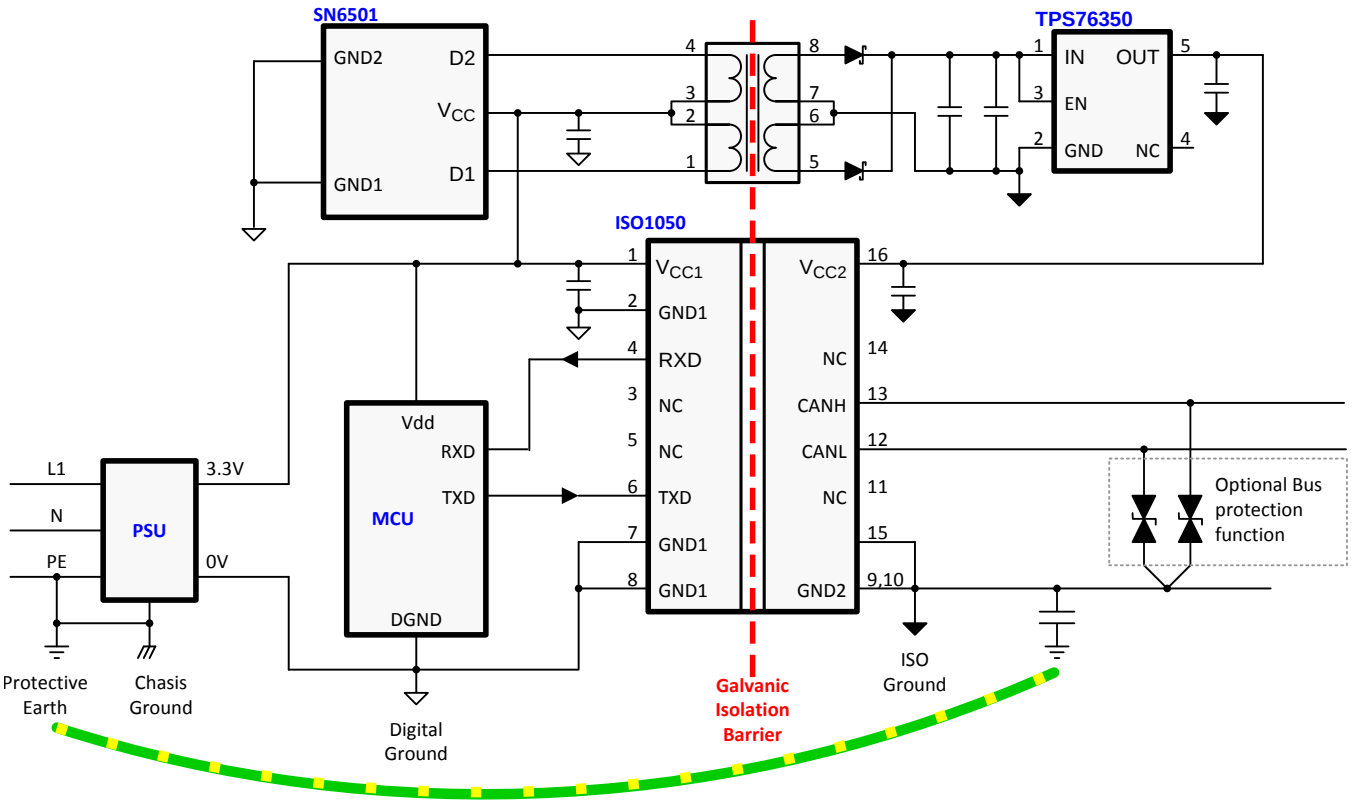


Figure 25. Application Circuit

BUS LOADING, LENGTH AND NUMBER OF NODES

The ISO11898 Standard specifies a maximum bus length of 40m and maximum stub length of 0.3m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the ISO1050.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They have made system level trade offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet and NMEA200.

A CAN network design is a series of tradeoffs, but these devices operate over wide –12-V to 12-V common-mode range. In ISO11898-2 the driver differential output is specified with a 60Ω load (the two 120Ω termination resistors in parallel) and the differential output must be greater than 1.5V. The ISO1050 is specified to meet the 1.5V requirement with a 60Ω load, and additionally specified with a differential output of 1.4V with a 45Ω load. The differential input resistance of the ISO1050 is a minimum of 30KΩ. If 167 ISO1050 transceivers are in parallel on a bus, this is equivalent to a 180Ω differential load. That transceiver load of 180Ω in parallel with the 60Ω gives a total 45Ω. Therefore, the ISO1050 theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2V minimum differential input at each node. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO11898 standard of 40m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO11898 CAN standard. In using this flexibility comes the responsibility of good network design.

CAN TERMINATION

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

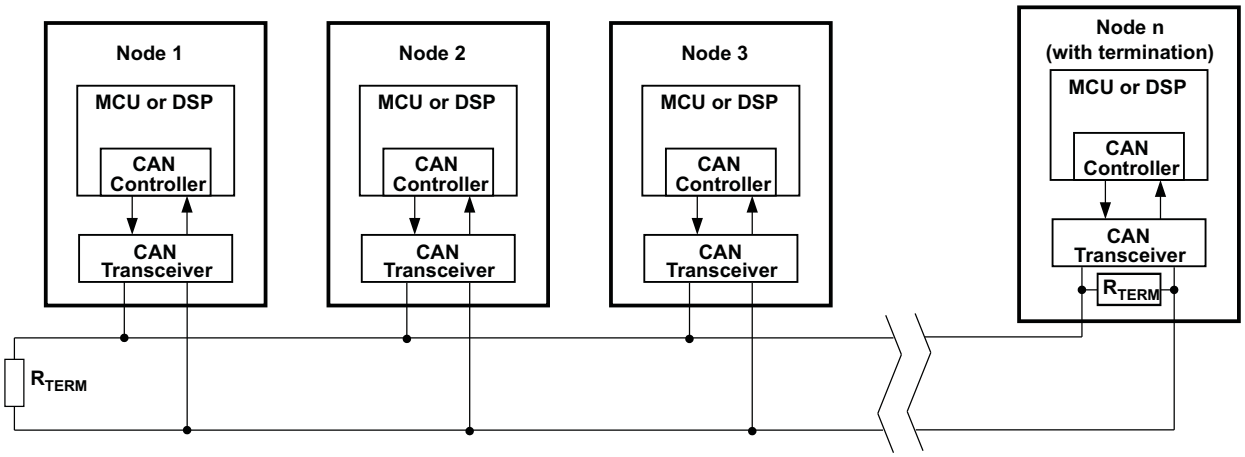


Figure 26. Typical CAN Bus

Termination may be a single 120 Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See Figure 27). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

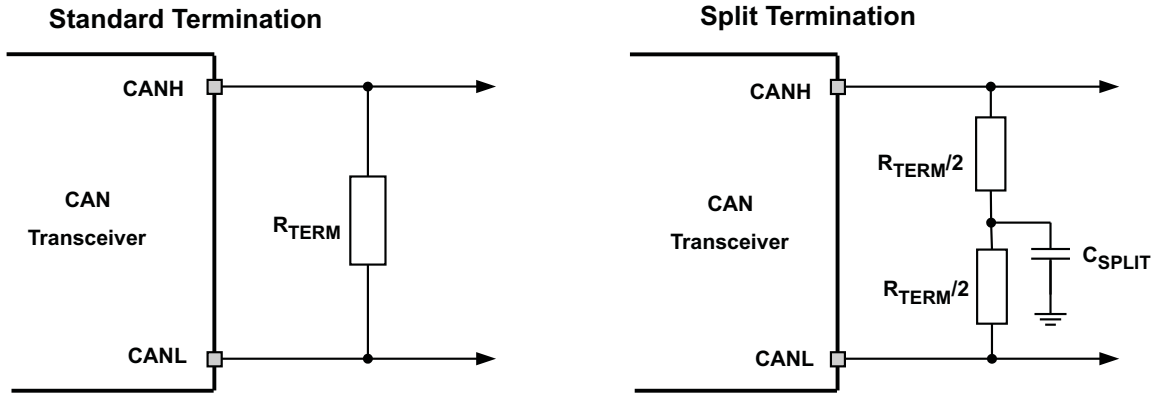


Figure 27. CAN Bus Termination Concepts

REVISION HISTORY

Changes from Original (June 2009) to Revision A **Page**

- Added IEC 60747-5-2 和 IEC61010-1 已批准的信息 1
- Added 额定工作电压下典型值为 25 年使用寿命到特性 1
- Added LIFE EXPECTANCY vs WORKING VOLTAGE section 17

Changes from Revision A (Sept 2009) to Revision B **Page**

- Changed DW 封装从预览到生产数据 1
- Added Insulation Characteristics and IEC 60664-1 Ratings tables 15
- Added IEC file number 16
- Added DW-16 thermal information table 17

Changes from Revision B (June 2009) to Revision C **Page**

- Changed IEC 60747-5-2 特性着重号从：对 DW 封装的批准未决到：VDE 通过检验可采用 DUB 和 DW 封装 1
- Changed the Minimum Internal Gap value from 0.008 to 0.014 in the Isolator Characteristics table 15
- Changed V_{IORM} Specification From: 1300 To: 1200 per VDE certification 15
- Changed V_{PR} Specification From 2438 To: 2250 15
- Added the Bus Loading paragraph to the Application Information section 21

Changes from Revision C (July 2010) to Revision D **Page**

- Changed the SUPPLY CURRENT table for I_{CC1} 1st row From: Typ = 1 To: 1.8 and MAX = 2 To: 2.8 7
- Changed the SUPPLY CURRENT table for I_{CC1} 2nd row From: Typ = 2 To: 2.8 and MAX = 3 To: 3.6 7
- Changed the REGULATORY INFORMATION table 16

Changes from Revision D (June 2011) to Revision E **Page**

- Added 器件 ISO1050L 1
- Changed 特性列表中的（DW 封装） 1
- Changed 特性列表中的（DUB 封装）在（ISO1050DUB和ISO1050LDW） 1
- 从 CSA 认可中删除了 IEC 60950-1 特性着重号 1
- 从：IEC 6060-1（医疗用）和 CSA 批准未决到：IEC 6060-1（医疗用）和 CSA 已批准 1
- 添加的特性 - 增强 5KVRMS。 1
- Added the AVAILABLE OPTIONS table 2
- Added Note 1 to the INSULATION CHARACTERISTICS table 15
- Changed V_{IORM} From: 8-DUB Package to ISO1050DUB and ISO1050LDW 15
- Changed V_{IORM} From: 16-DW to ISO1050DW 15
- Changed the V_{ISO} Isolation voltage per UL section of the INSULATION CHARACTERISTICS table. 15
- Changed the IEC 60664-1 Ratings Table 15
- Changed the REGULATORY INFORMATION table 16
- Changed From: File Number: 220991 (Approval Pending) To: File Number: 220991 16
- Changed in note (1) 3000 to 2500 and 6000 to 5000 16
- Changed in LIFE EXPECTANCY vs WORKING VOLTAGE (8-DUB PACKAGE TO: LIFE.....(ISO1050DW and ISO1050LDW) 17

Changes from Revision E (December 2011) to Revision F **Page**

- Deleted ISO1050L 器件 1
- Deleted （ISO1050DUB 和ISO1050LDW） 1
- Deleted 说明第一段中的 ISO1050LDW 1
- Deleted ISO1050LDW from AVAILABLE OPTIONS 2
- Added the PIN FUNCTIONS section 2
- Added the FUNCTIONAL DESCRIPTION section 3
- Added Note 1 to the DRIVER SWITCHING CHARACTERISTICS table 8
- Deleted ISO1050LDW from INSULATION CHARACTERISTICS 15
- Deleted ISO1050LDW from REGULATORY INFORMATION 16
- Deleted ISO1050LDW from LIFE EXPECTANCY vs WORKING VOLTAGE 17
- Deleted 40V from the CANH and CANL input diagrams and output diagrams in the EQUIVALENT I/O SCHEMATICS 18
- Changed the APPLICATION INFORMATION section 21

Changes from Revision F (January 2013) to Revision G **Page**

- Clarified clearance and creepage measurement method in ISOLATOR CHARACTERISTICS 15
- Clarified test methods for voltage ratings in INSULATION CHARACTERISTICS 15
- Changed UL Single Protection Certification pending to Single Protection in REGULATORY INFORMATION SECTION (certificate available) 16

Changes from Revision G (March 2013) to Revision H **Page**

- Changed title From: LIFE EXPECTANCY vs WORKING VOLTAGE (ISO1050DW To: LIFE EXPECTANCY vs WORKING VOLTAGE (ISO1050DUB) 17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1050DUB	ACTIVE	SOP	DUB	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-55 to 105	ISO1050	Samples
ISO1050DUBR	ACTIVE	SOP	DUB	8	350	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-55 to 105	ISO1050	Samples
ISO1050DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 105	ISO1050	Samples
ISO1050DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 105	ISO1050	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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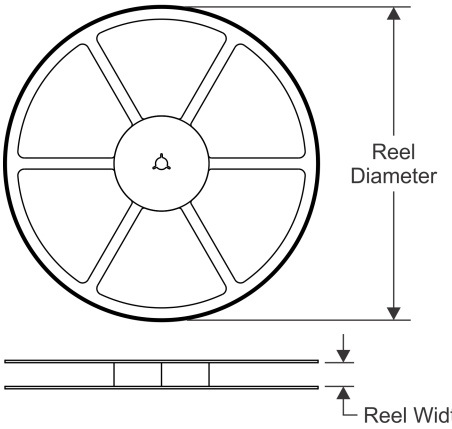
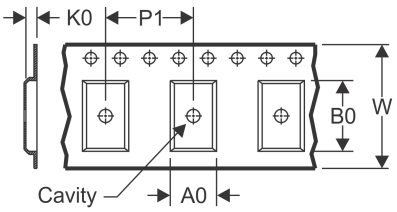
TAPE AND REEL INFORMATION

REEL DIMENSIONS

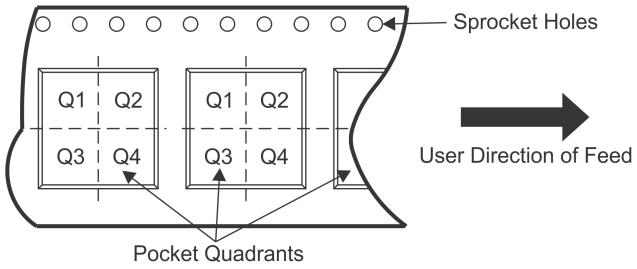


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

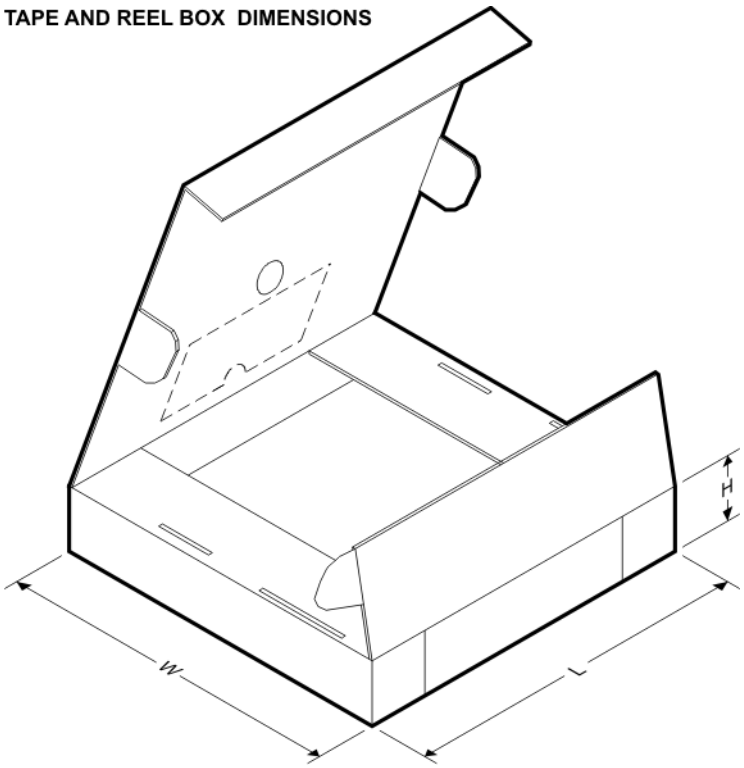
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1050DUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1
ISO1050DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

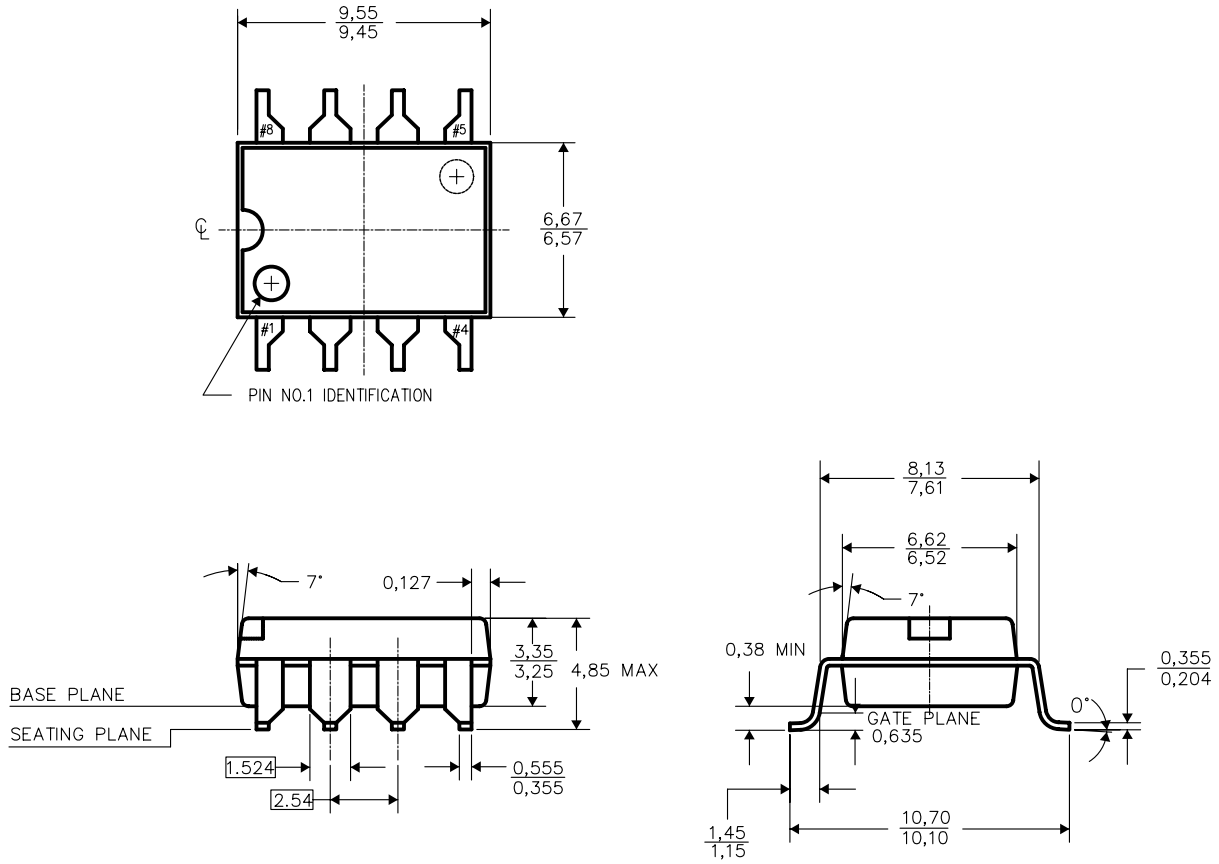
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

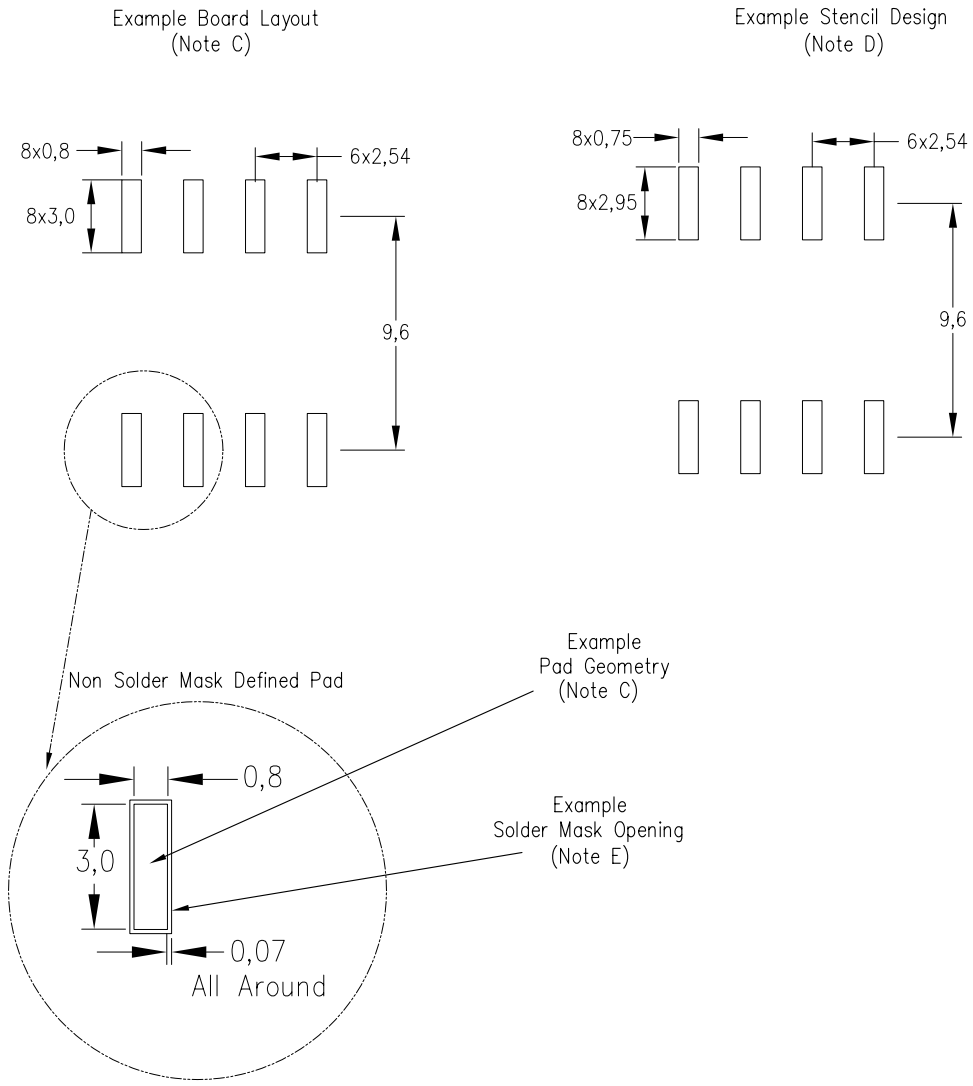
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1050DUBR	SOP	DUB	8	350	358.0	335.0	35.0
ISO1050DWR	SOIC	DW	16	2000	367.0	367.0	38.0

DUB (R–PDSO–G8) PLASTIC SMALL–OUTLINE



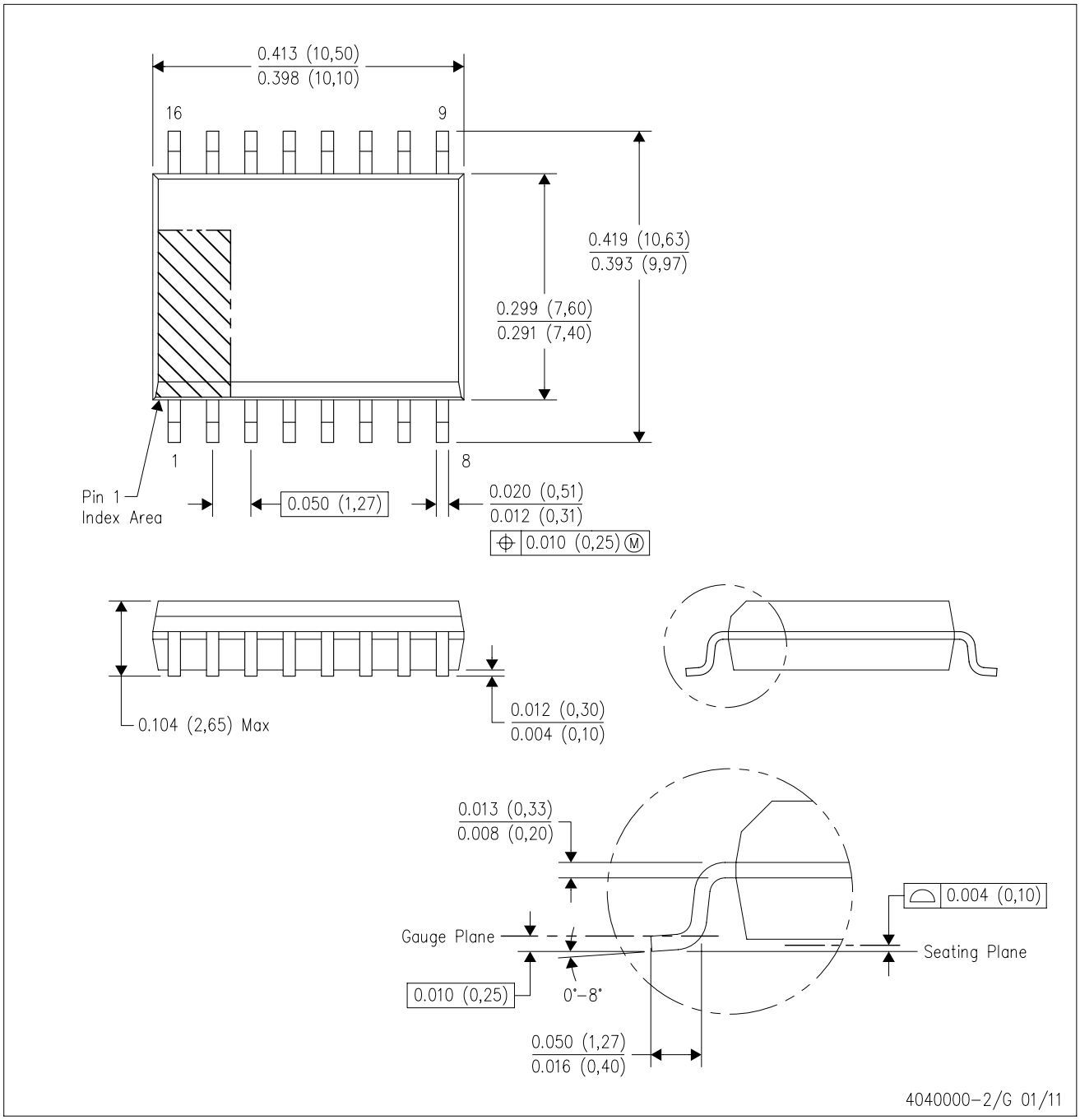
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ANSI Y14.5 M–1982.
B. This drawing is subject to change without notice.
C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.254mm.

DUB (R–PDSO–G8) PLASTIC SMALL OUTLINE



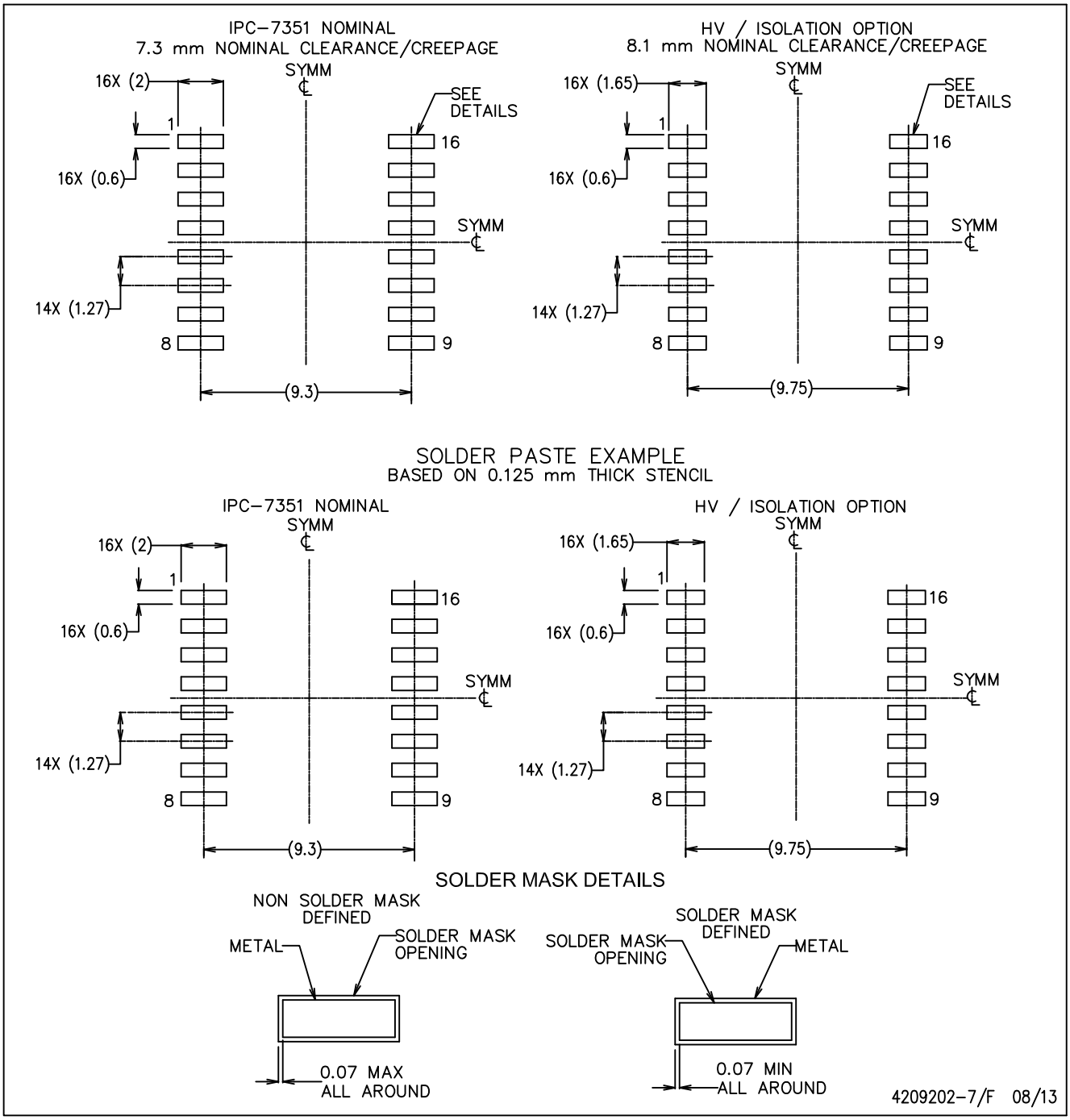
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
E. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
F. Board assembly site may have different recommendations for stencil design.

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