UNITRODE

UC1823
UC2823
UC3823

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V ±1%)

DESCRIPTION

The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance. The current limit reference (pin 11) is a DC input voltage to the current limit comparator. Consult specifications for details.

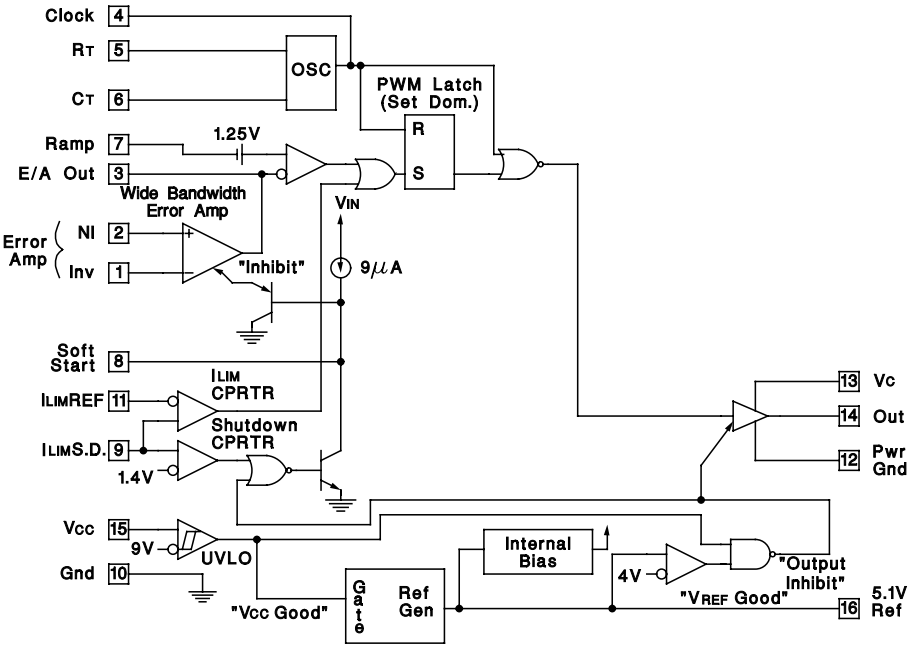
These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pin14)
DC 0.5A
Pulse (0.5µs) 2.0A
Analog Inputs (Pins 1, 2, 7, 8, 9, 11) . . . . . -0.3V to +6V
Clock Output Current (Pin 4) . . . . . -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) . . . . . -5mA
Power Dissipation at T_A = 60 °C 1W
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

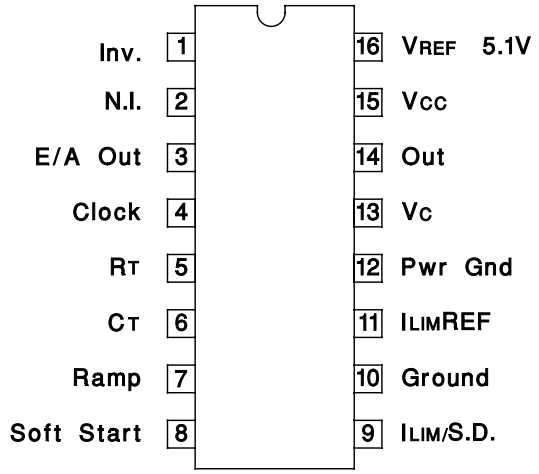
Note: All voltages are with respect to ground, Pin 10.
Currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

BLOCK DIAGRAM

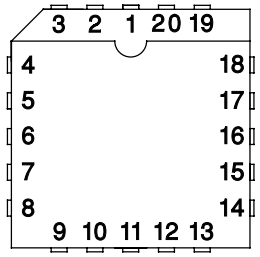


CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
Inv.	2
N.I.	3
E/A Out	4
Clock	5
N/C	6
R_T	7
C_T	8
Ramp	9
Soft start	10
N/C	11
I_{LIM}/S.D.	12
Ground	13
I_{LIM} REF	14
PWR Gnd	15
N/C	16
V_C	17
OUT	18
V_{CC}	19
V_{REF} 5.1V	20

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, 0°C < T_A < +70°C for the UC3823, -25°C < T_A < +85°C for the UC2823, and -55°C < T_A < +125°C for the UC1823, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10 < V_{CC} < 30V		2	20		2	20	mV
Load Regulation	1 < I_O < 10mA		5	20		5	20	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	T_J = 125°C, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF}=0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	T_J=25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10 < V_{CC} < 30V		0.2	2		0.2	2	%
Temperature Stability*	T_{MIN} <T_A < T_{MAX}		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	kHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

* These parameters are guaranteed by design but not 100% tested in production.

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, 0°C < T_A < +70°C for the UC3823, -25°C < T_A < +85°C for the UC2823, and -55°C < T_A < +125°C for the UC1823, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1 < V_O < 4V	60	95		60	95		dB
CMRR	1.5 < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10 < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ =1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µS
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			±10			±10	µA
Current Limit Offset	$V_{PIN\ 11}$ = 1.1V			15			15	mV
Current Limit Common Mode Range ($V_{PIN\ 11}$)		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = –20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = –200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		100	500	µA
Rise/Fall Time*	C_L = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ =0V, $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

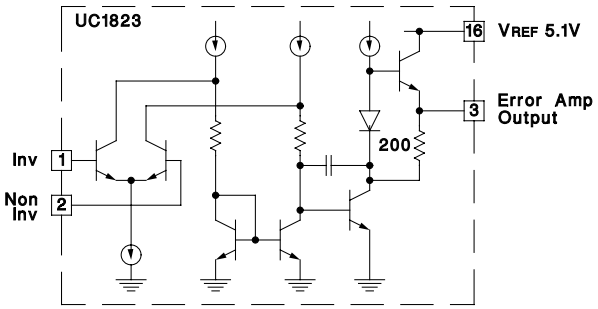
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UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

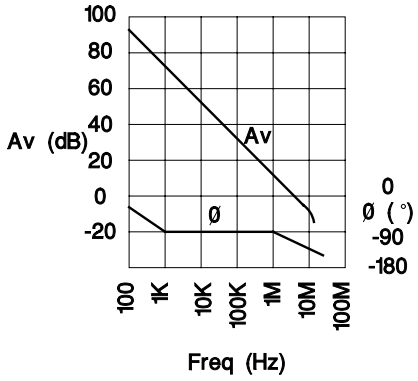
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

ERROR AMPLIFIER CIRCUIT

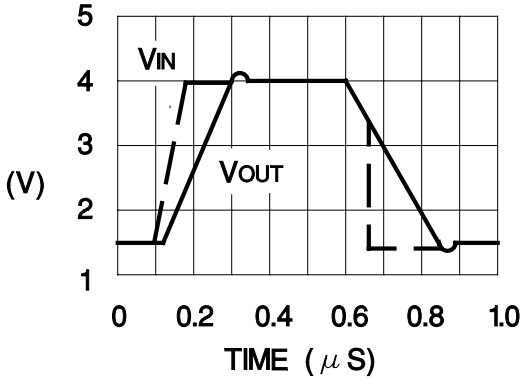
Simplified Schematic



Open Loop Frequency Response

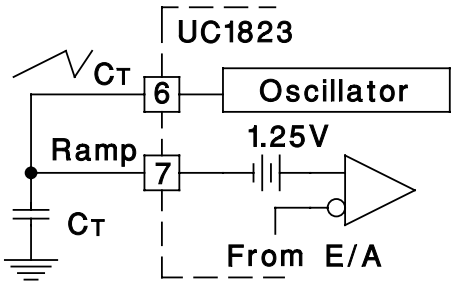


Unity Gain Slew Rate

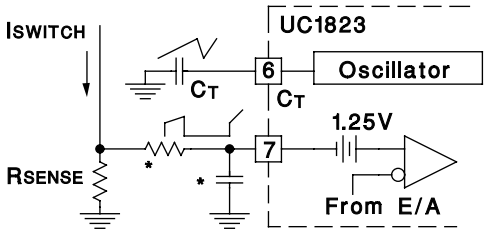


PWM APPLICATIONS

Conventional (Voltage Mode)

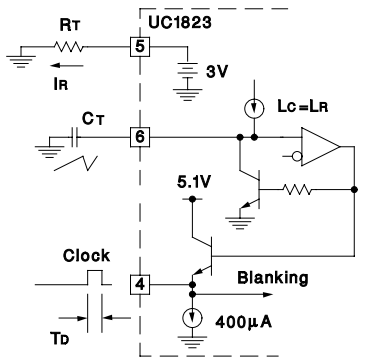


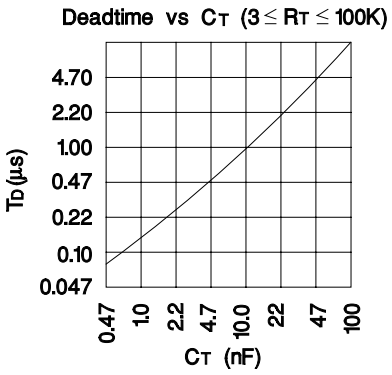
Current-Mode

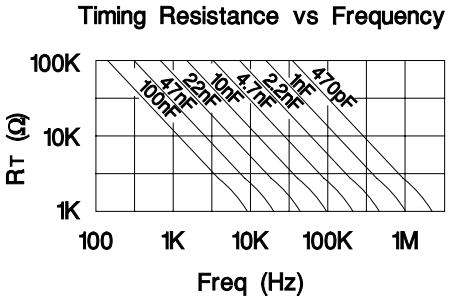


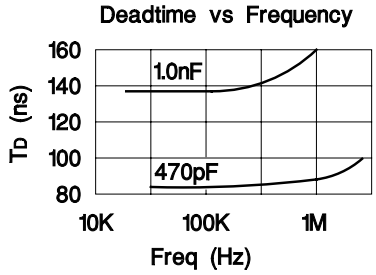
* A small filter may be required to suppress switch

OSCILLATOR CIRCUIT



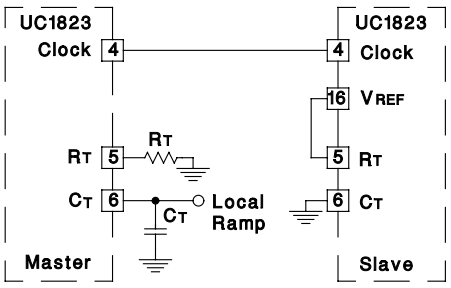




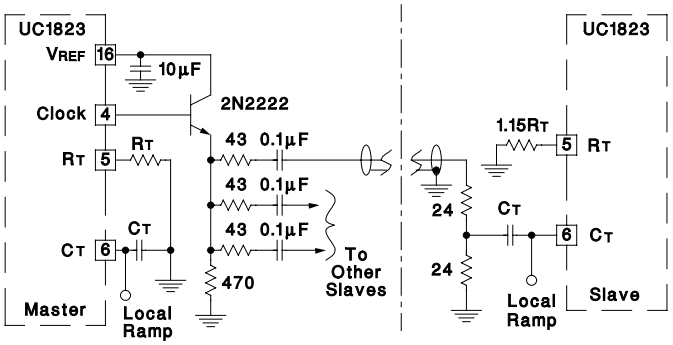


SYNCHRONIZED OPERATION

Two Units in Close Proximity

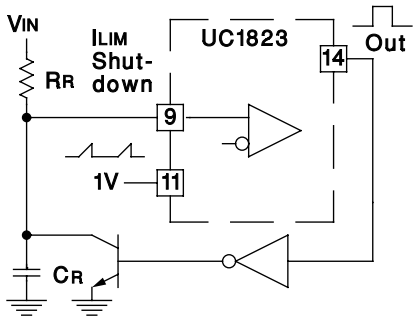


Generalized Synchronization

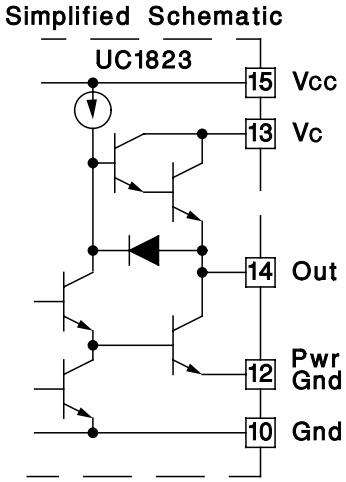


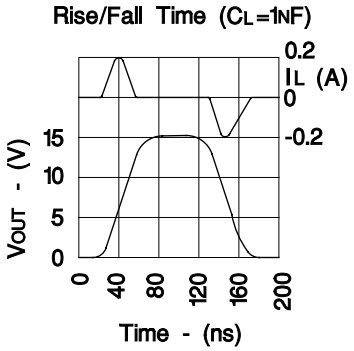
CONSTANT VOLT-SECOND CLAMP CIRCUIT

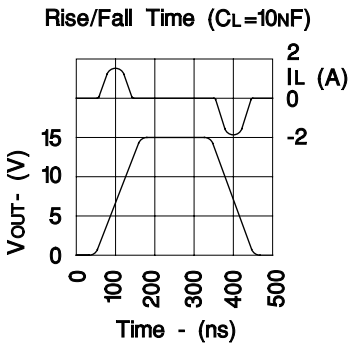
The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

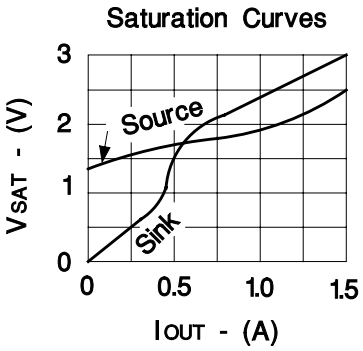


OUTPUT SECTION

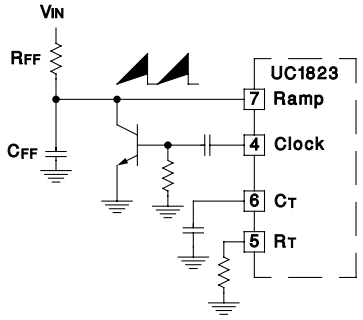








FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

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