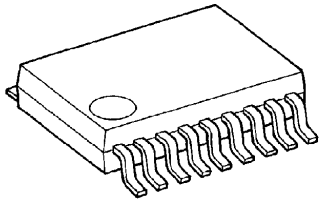
TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62445FN

LOW-SATURATION-TYPE SINK DRIVER WITH 4-CIRCUIT OVER-CURRENT DETECTION FUNCTION

The TD62445FN is a sink driver with over-current detector circuits. Each of four circuits can setting the limit current. Using an internal comparator, the TD62445FN detects over-current by comparing the current output through the external resistors as voltage. Over current detection is detected by the ERR terminal which is an open collector, comes on.
Construct a system so that the input signal turns off immediately the ERR pin comes on.



SSOP18-P-225-0.65

Weight : 0.08g (Typ.)

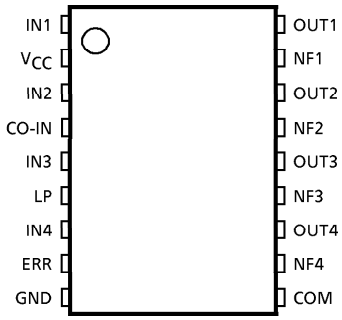
FEATURES

- Includes current limiter circuits:
  By connecting external resistors, each bit can be set to any limit current value.
- Includes an error detection signal filter pin:
  Connecting any capacitor between the LP pin and the GND filters the internal comparator detection signal and outputs this to the ERR pin.
- Over-current monitor detection output:
  Includes an ERR pin output to warn when current exceeds the limit. Construct a system so that the input signal turns off immediately the ERR pin comes on (open collector).
- Common input pin (CO-IN (pin 4)):
  Using this pin, the four over-current detector circuits can be forcibly turned off together.
- Low-saturation-type output (open collector):
  The voltage drop between the collector and emitter is $V_{OL1} = 0.4V$ (max.) @ $I_O = 100mA$.
- Supply voltage : $V_{CC} = 4.5$ to 5.5
- Input is TTL compatible.
- Ultra-compact package : VSOP 18 pins (0.65mm pitch)
- Output rating : $V_{CEO} = 30V$, $I_O = 150mA$ / ch
- Packing : Embossed taping only

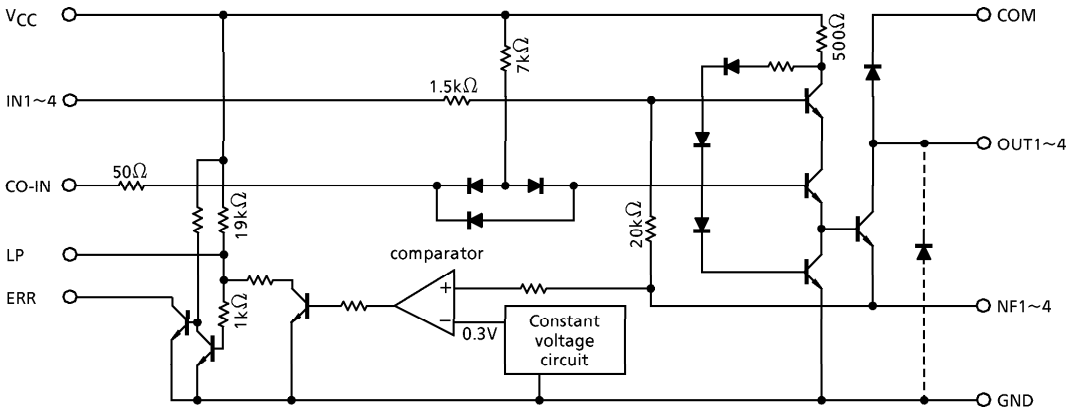
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PIN CONNECTION (Top View)



EQUIVALENT CIRCUIT DIAGRAM (Showing One Circuit)



- When the output pins of this IC are connected to the load power supply, over-current may flow to the outputs. While the device includes an over-current detection function, the device is not designed for applications where the output pins and load power supply are intentionally connected.
- Be sure to use the device with the NF1 to 4 and the GND pins connected via resistors or directly connected. Do not use with the NF1 to 4 pins open.
  This also applies to unused channels. If the pins are not connected, the operation of the over-current detection function is unstable.
  Note that if the NF1 to 4 and GND pins are directly connected, the over-current detection function does not operate.
- A parasitic diode is installed between the GND and output pins. While current is supplied to this diode, other circuit outputs may come on or be otherwise affected. If this phenomenon adversely affects the operation of the device, Toshiba recommends connecting an external diode.

TRUTH TABLE

IN1~4	CO-IN	OUT1~4	VOLTAGE BETWEEN NF1 TO 4 AND GND	ERR
L	H	OFF	0V	OFF
H	H	ON	0.3V max	OFF
H	H	ON	0.3V min	ON
X	L	OFF	0V	OFF

(Note) The above comparator circuit assumes some resistance connected between the NF1 to 4 and GND pins when the circuit operates.

PIN DESCRIPTION

PIN No.	PIN NAME	FUNCTION
1, 3, 5, 7	IN1 to 4	Driver input pins. TTL compatible input level. At high level the output is on; at low level the output is off.
2	V_{CC}	Power supply voltage pin.
4	CO-IN	Output control pin. When high the output operates in accordance with input logic; when low the output is forcibly turned off regardless of the input logic.
6	LP	CR filter circuit pin. Connecting a capacitor to the GND creates a filter for the over-current detection signal from the comparator. When not in use, leave open.
8	ERR	Over-current detection signal output pin. Comes on when excess current is detected. Normally, set to high impedance.
9	GND	GND pin.
10	COM	Clamp diode's common cathode pin.
17, 15, 13, 11	NF1 to 4	Resistor connecting pins for over-current detection setting. By connecting resistors between these pins and GND, the detection level can be set separately for each circuit.
18, 16, 14, 12	OUT1 to 4	Open collector output pins.

MAXIMUM RATINGS

CHARACTERISTIC	SIGNAL	RATING	UNIT
Power Supply Voltage	V_{CC}	7.0	V
COM Pin Voltage	V_{COM}	30.0	V
Output Voltage	V_{CEO}	30.0	V
ERR Pin Output Voltage	V_{ERR}	7.0	V
Output Sink Current	I_{OUT}	0~150	mA
ERR Pin Sink Current	I_{ERR}	10	mA
Input Voltage	V_{IN}	$-0.3 \sim V_{CC}+0.3$	V
NF Pin Voltage	$V_{IN\,(NF)}$	$-0.3 \sim 1.0$	V
LP Pin Voltage	$V_{IN\,(LP)}$	$-0.3 \sim V_{CC}+0.3$	V
Clamp Diode Reverse Voltage	V_{r1}	30	V
Clamp Diode Forward Current	I_{f1}	150	mA
Output Parasitic Diode Forward Current	I_{f2}	100	mA
Power Dissipation	P_D (*)	960	mW
Operating Temperature	T_{opr}	$-10 \sim 85$	°C
Storage Temperature	T_{stg}	$-55 \sim 150$	°C

(*) When the device is mounted on a PCB (with one surface 50 × 50 × 1.6mm Cu 40% glass epoxy) When operating at an ambient temperature of 25°C or higher, derate the power dissipation at 7.6mW / °C.

RECOMMENDED OPERATING CONDITIONS (Unless otherwise specified, V_{CC} = 5.0V, Ta = – 10 to 85°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{CC}	—	4.5	5.0	5.5	V
Output Voltage	V_{CEO}	OUT1~4	0	—	30.0	V
	V_{ERR}	ERR	0	—	V_{CC} + 0.3	V
Output Current	I_{OUT}	—	0	—	120	mA
	I_{ERR}	ERR	0	—	8	mA
Input Voltage	V_{IN}	V_{CC} = 5.0V : IN1~4, CO-IN, LP	0	—	V_{CC}	V
Power Dissipation	P_{D1}	Ta = 60°C	—	—	0.69	W / IC
	P_{D2}	Ta = 85°C	—	—	0.50	W / IC

ELECTRICAL CHARACTERISTICS
(Unless otherwise specified, V_{CC} = 5.0V ± 10%, Ta = – 10 to 85°C, $V_{IN\ (NF)}$ = GND)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Power Supply Voltage	V_{CC}	—	—	4.5	5.0	5.5	V
Output Leakage Current	I_{Oleak1}	1	V_{CE} = 30V, V_{IN} = 0V, Ta = 25°C : OUT1~4	0	—	100	μA
	I_{Oleak2}	1	V_{CE} = 7.0V, V_{NF} = 0V, Ta = 25°C : ERR	0	—	50	
Output Saturation Voltage	V_{OL1}	2	I_{OUT} = 100mA, R_{NF} = 0 : OUT1~4	0	0.15	0.40	V
	V_{OL2}	3	I_{OL} = 10mA : ERR	0	0.20	0.60	
Input Voltage	V_{I+}	3	V_{ERR} = "L", Ta = – 10~85°C : NF1~4	0.25	0.30	0.35	V
	V_{IH}	2	IN1~4, CO-IN	2.50	—	—	
	V_{IL}	1	NF1~4, CO-IN	—	—	0.70	
Input Current	I_{IH}	2	V_{IN} = 2.5V, Ta = 25°C : IN1~4	—	+ 0.5	+ 0.1	mA
	I_{IL1}	1	V_{IN} = 0.7V, Ta = 25°C : IN1~4	—	+ 0.1	+ 0.1	
	I_{IL2}	1	V_{IN} = 0.7V, Ta = 25°C : CO-IN	—	– 1.0	– 3.4	
Power Supply Current When Not Operating	I_{CC}	4	V_{IN} = 0.7V : CO-IN, IN1~4, Ta = 25°C All outputs off	—	8	10	mA / IC
Power Supply Current When Operating	I_{CCopr}	4	V_{IN} = 2.5V, I_{OUT} = 150mA, Ta = 25°C All outputs on	—	40	70	mA / IC
Clamp Diode Forward Voltage	V_{f1}	5	I_f = 100mA : OUT1~4 to COM	—	1.20	2.00	V
Clamp Diode Reverse Voltage	V_{r1}	1	I_r = 100μA : COM to OUT1~4	30	—	—	V
Input / Output Delay Time	t_{PDIO1} (t_{pLH})	6	Ta = 25°C, V_{CE} = 30V, I_{OUT} = 150mA, C_L = 10pF : IN1~4 to OUT1~4	—	(*) 0.25	(*) 1.25	μs
	t_{PDIO1} (t_{pHL})	6		—	(*) 0.40	(*) 2.00	

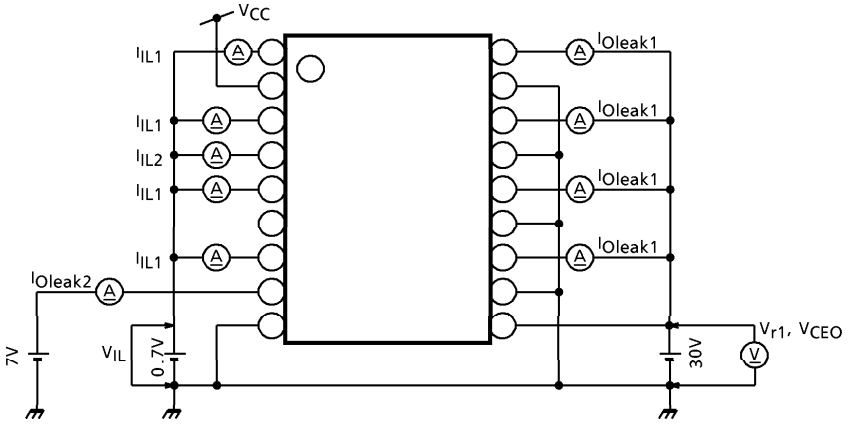
(*) The switching characteristic values indicate the guaranteed design limits.

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input / Output Delay Time	t_{PDIO2} (t_{pLH})	7	Ta = 25°C, V_{ERR} = 5.0V, I_{OL} = 10mA, C_L = 10pF, V_{NF} = 0 to 0.4V : NF1~4 to ERR	—	(*) 0.30	(*) 1.50	μs
	t_{PDIO2} (t_{pHL})	7		—	(*) 5.00	(*) 15.0	
	t_{PDIO3} (t_{pLH})	6	Ta = 25°C, V_{CE} = 30V, I_{OUT} = 150mA, C_L = 50pF : CO-IN to OUT1~4	—	(*) 0.25	(*) 1.25	
	t_{PDIO3} (t_{pHL})	6		—	(*) 0.40	(*) 2.00	
Output Rise Time	(t_{pLH})	6	Ta = 25°C, V_{CE} = 30V, I_{OUT} = 150mA, C_L = 50pF, 10%-90% : OUT1~4	—	(*) 0.40	(*) 1.00	μs
	t_{rERR}	7	Ta = 25°C, V_{ERR} = 5.0V, I_{OL} = 10mA, C_L = 10pF, 10%-90% : ERR	—	(*) 0.40	(*) 1.00	
Output Fall Time	t_{fOUT}	6	Ta = 25°C, V_{CE} = 30V, I_{OUT} = 150mA, C_L = 50pF, 90%-10% : OUT1~4	—	(*) 0.10	(*) 1.00	μs
	t_{fERR}	7	Ta = 25°C, V_{ERR} = 5.0V, I_{OL} = 10mA, C_L = 10pF, 90%-10% : ERR	—	(*) 0.02	(*) 1.00	

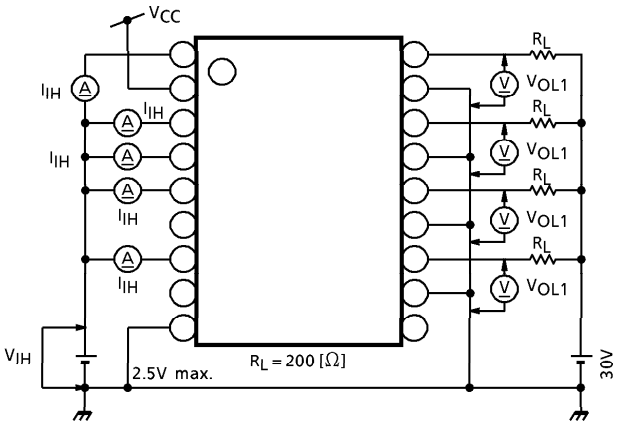
(*) The switching characteristic values indicate the guaranteed design limits.

TEST CIRCUIT

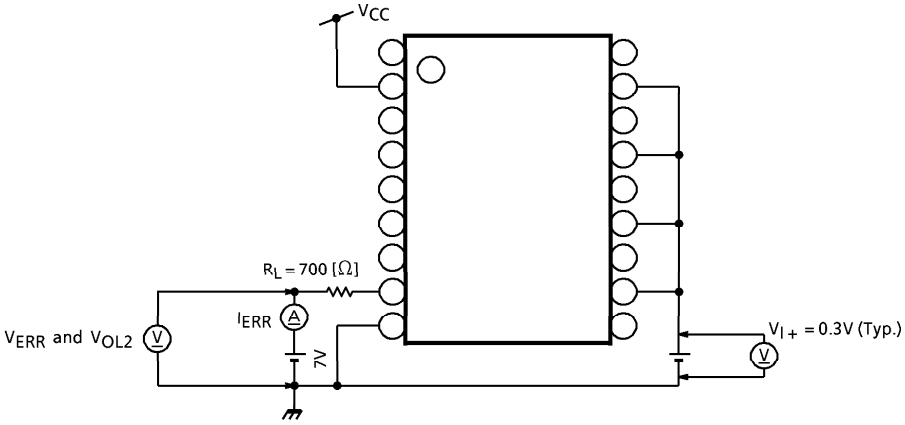
(1) V_{IL}, $I_{IL1\sim2}$, V_{r1}, V_{CEO}, I_{Oleak1}, I_{Oleak2}



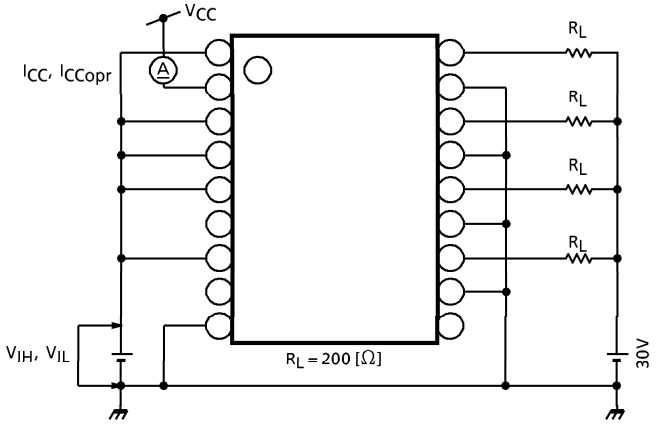
(2) V_{IH}, I_{IH}, V_{OL1}



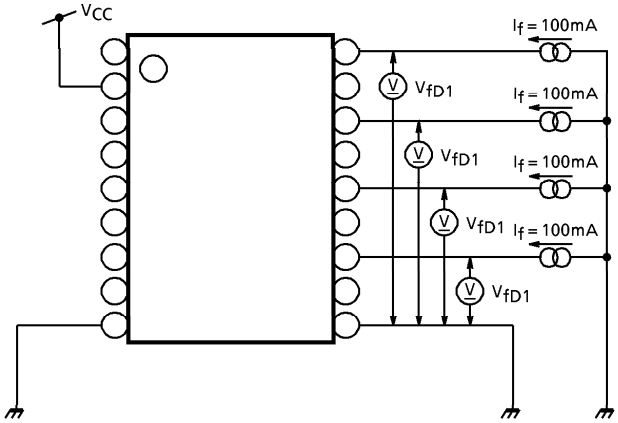
(3) V_{I+}, V_{ERR}, I_{ERR}, V_{OL2}



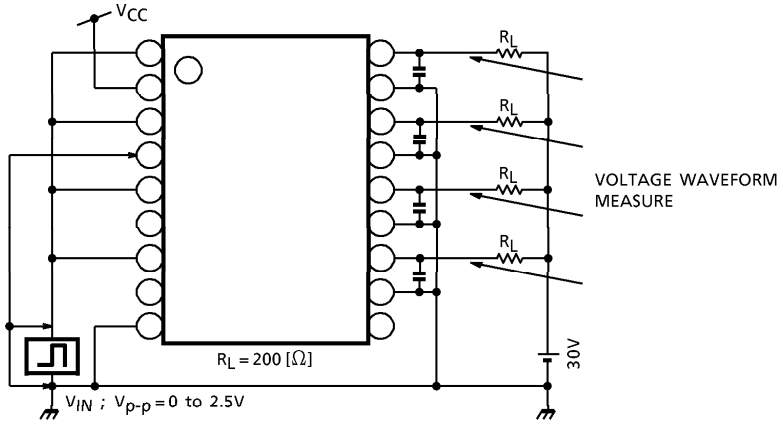
(4) I_{CC}, I_{CCopr}



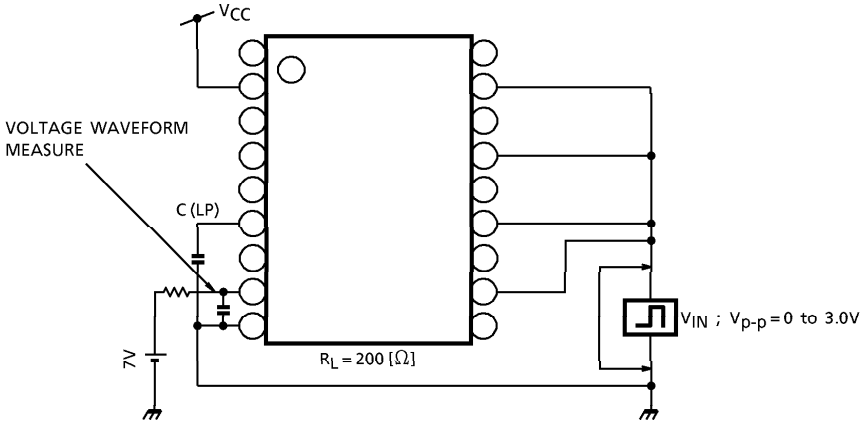
(5) V_{f1}



(6) t_{PDIO1}, t_{PDIO3}, t_{rOUT}, t_{fOUT}

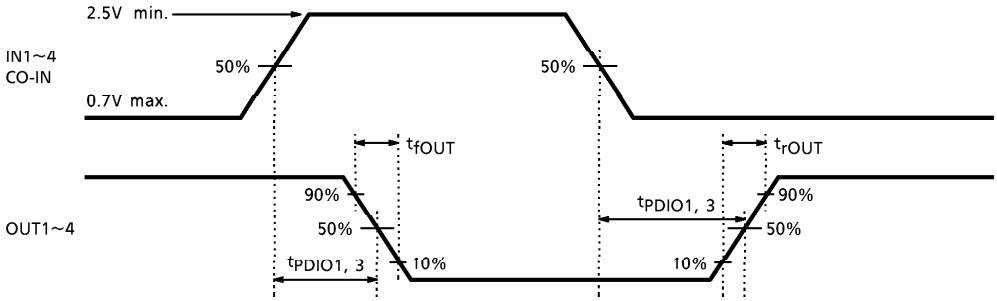


(7) t_{PDIO2}, t_{rERR}, t_{fERR}, C (LP)

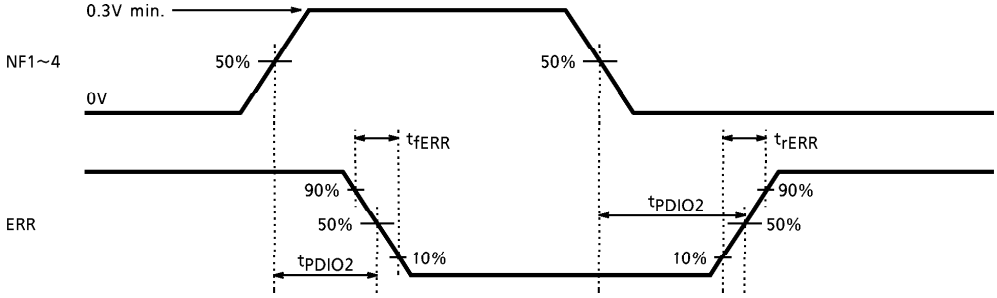


SWITCHING WAVEFORM

[$t_{PDIO1, 3}$, t_{rOUT}, t_{fOUT}]

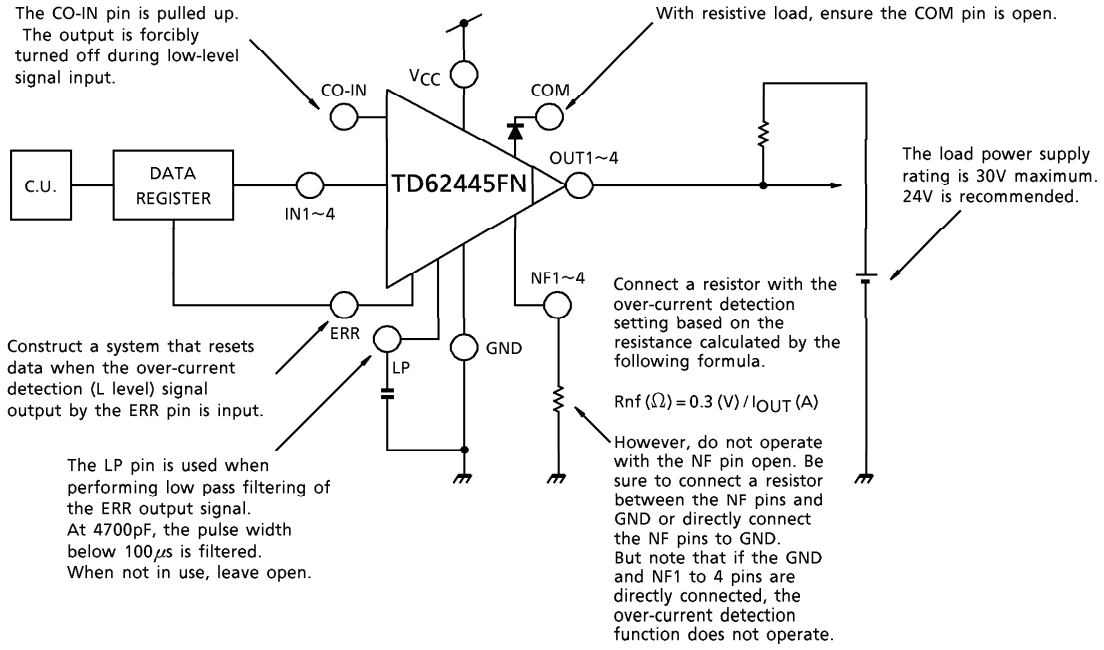


[t_{PDIO2}, t_{rERR}, t_{fERR}]

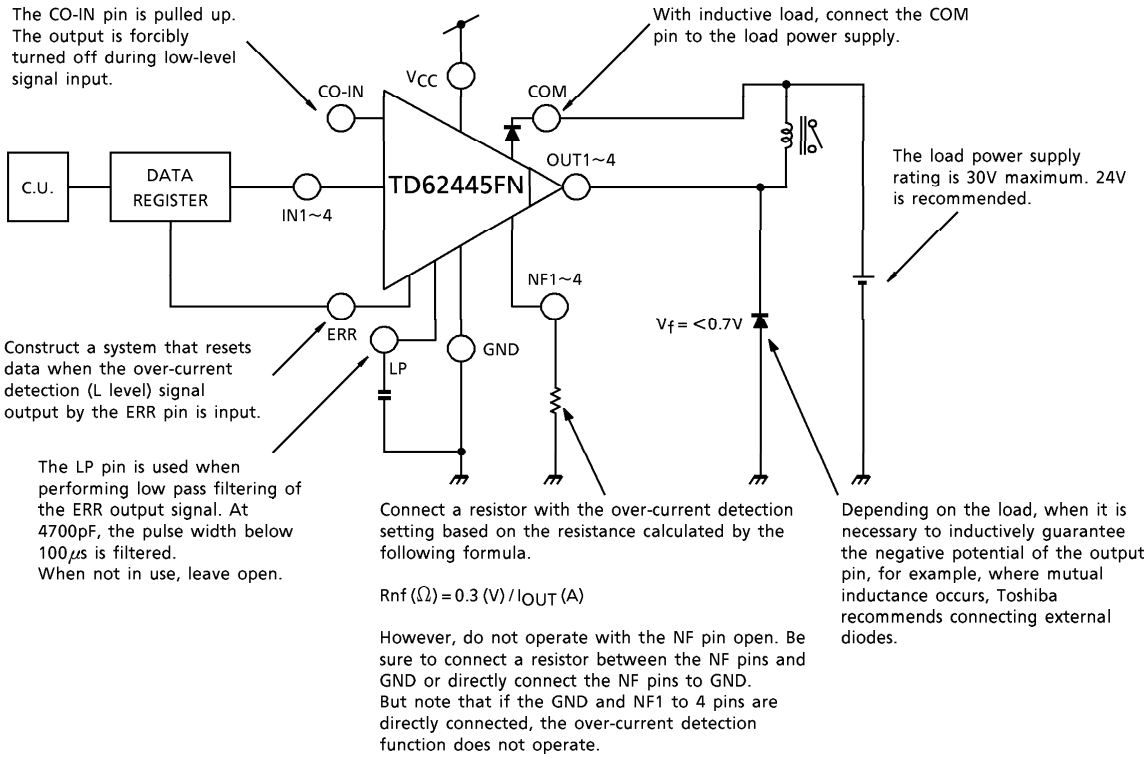


APPLICATION CIRCUIT

1. Using resistive load drive



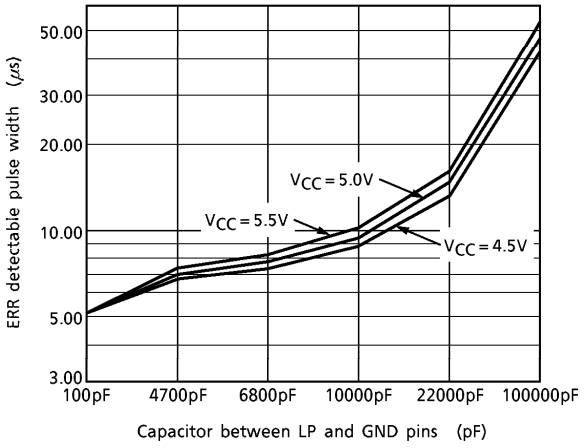
2. Using inductive load (eg, relay) drive



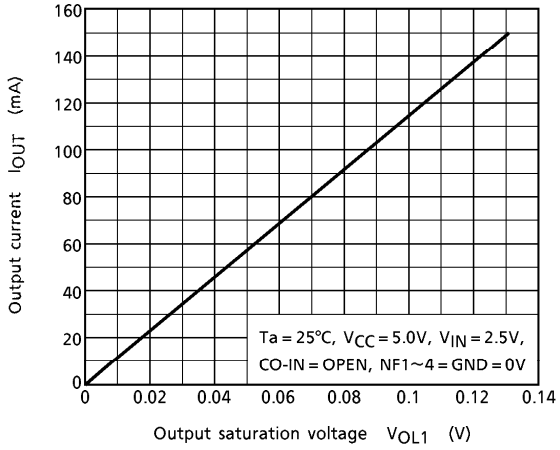
PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC}, COMMON and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

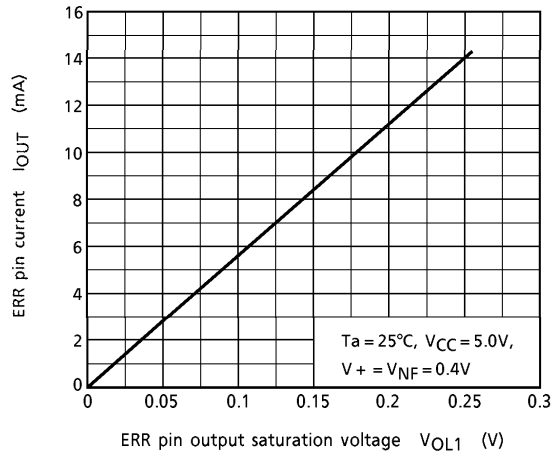
Capacitor between LP and GND pins vs ERR detectable pulse width
(At Ta = 25°C, ERR pin outputs a low-level pulse width of 1 μs.)



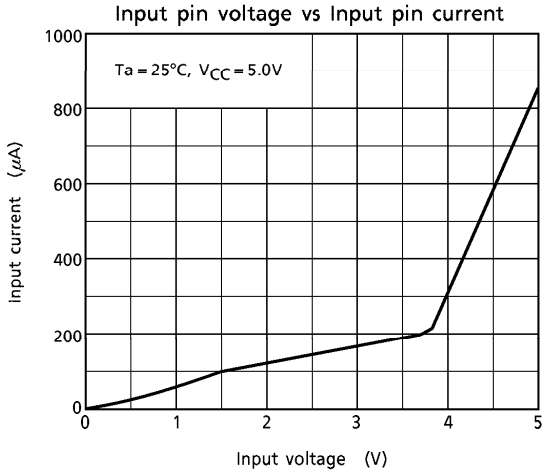
Output pin OUTn
Output saturation voltage vs Output pin current



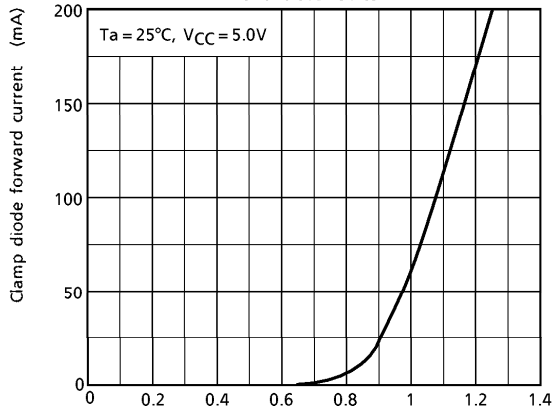
ERR pin
Output saturation voltage vs Output pin current



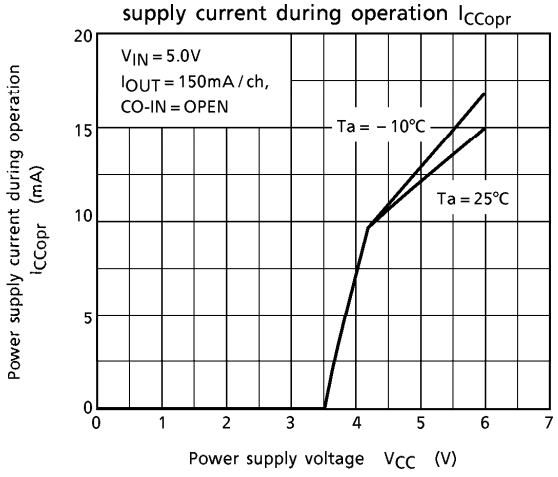
Input pin INn
Input pin voltage vs Input pin current



Clamp diode COM
Forward voltage V_f vs Forward current I_f characteristics

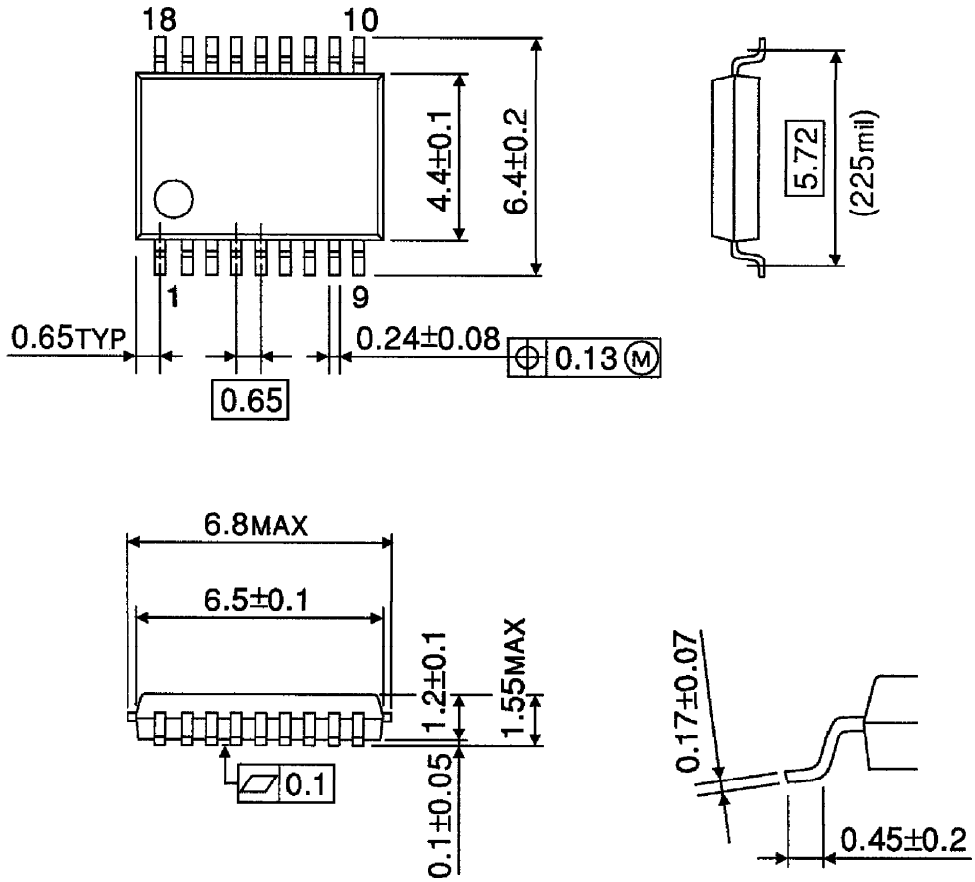


Power supply voltage V_{CC}
Applied power supply voltage V_{CC} vs Power supply current during operation I_{CCopr}



OUTLINE DRAWING

SSOP18-P-225-0.65 Unit : mm



Weight : 0.08g (Typ.)