GENERAL DESCRIPTION

The SX9510 and SX9511 are 8–button capacitive touch sensor controllers that include 8-channels of LED drivers, a buzzer, an IR detector and analog outputs designed ideally for TV applications. The SX9510 offers proximity sensing.

The SX9510 and SX9511 operate autonomously using a set of programmable button sensitivities & thresholds, plus LED intensities & breathing functions with no external I2C communication required.

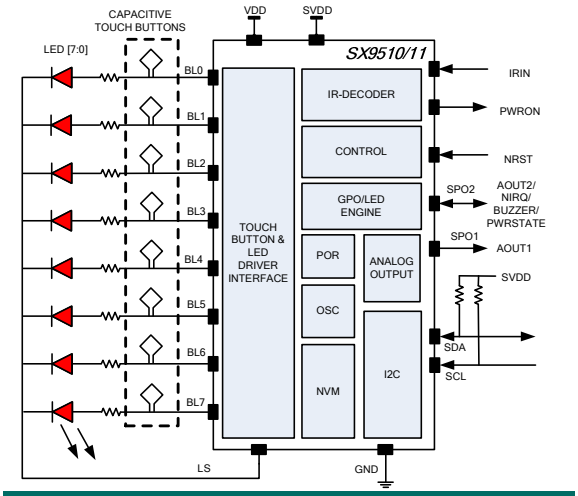
All devices feature three individual LED driver engines for advanced LED lighting control. On the SX9510, a proximity detection illuminates all LEDs to a pre-programmed intensity. Touching a button will enable the corresponding LED to a pre-programmed mode such as intensity, blinking or breathing.

Whenever the capacitive value changes from either a proximity detection or finger touch/release, the controller informs the host processor through the analog output(s) or an open drain interrupt and an I2C register read.

The SX9510 and SX9511 do not require additional external dynamic programming support or setting of parameters and will adapt to humidity and temperature changes to guarantee correct touch/no touch information.

The SX9510 and SX9511 are offered in 20-ld QFN and 24-ld TSSOP packages and operate over an ambient temperature range of -40°C to +85°C.

TYPICAL APPLICATION CIRCUIT



KEY PRODUCT FEATURES

- Separate Core and I/O Supplies
  - o 2.7V – 5.5V Core Supply Voltage
  - o 1.65V – 5.5V I/O Supply Voltage
- 8 - Button Capacitance Controller
  - o Capacitance Offset Compensation to 40pF
  - o Adaptive Measurements For Reliable Proximity And Button Detection
- Proximity Sensing (SX9510)
  - o High Sensitivity
  - o LEDs Activated During Proximity Sense
- 8-channel LED Controller & Driver
  - o Blink And Breathing Control
  - o High Current, 15 mA LED Outputs
- 2-Channel Analog Output, 6-bit DAC Programmable Control
- Support Metal Overlay UI Design (SX9510)
- Infra Red Detector for Power-On signaling and LED feedback
  - o programmable address with eight commands
  - o compatible with NEC, RC5, RC6, Toshiba, RCA, etc
- Simple (400kHz) I^2C Serial Interface
  - o Interrupt Driven Communication via NIRQ Output
- Power-On Reset, NRST Pin and Soft Reset
- Low Power
  - o Sleep, Proximity Sensing: 330uA
  - o Operating: 600uA
- -40°C to +85°C Operation
- 4.0 mm x 4.0 mm, 20-lead QFN package
- 4.4 mm x 7.8 mm, 24-lead TSSOP package
- Pb & Halogen free, RoHS/WEEE compliant

APPLICATIONS

- LCD TVs, Monitors
- White Goods
- Consumer Products, Instrumentation, Automotive
- Mechanical Button Replacement

ORDERING INFORMATION

Part Number	Package	Marking
SX9511EWLTRT[1]	QFN-20	ZK72
SX9511ETSTRT[2]	TSSOP-24	AC72T
SX9510EWLTRT[1]	QFN-20	ZL73
SX9510ETSTRT[2]	TSSOP-24	AC73X
SX9510EVK	Evaluation Kit	-

[1] 3000 Units/Reel
[2] 2500 Units/Reel

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1 GENERAL DESCRIPTION

1.1 Pin Diagram SX9510/11

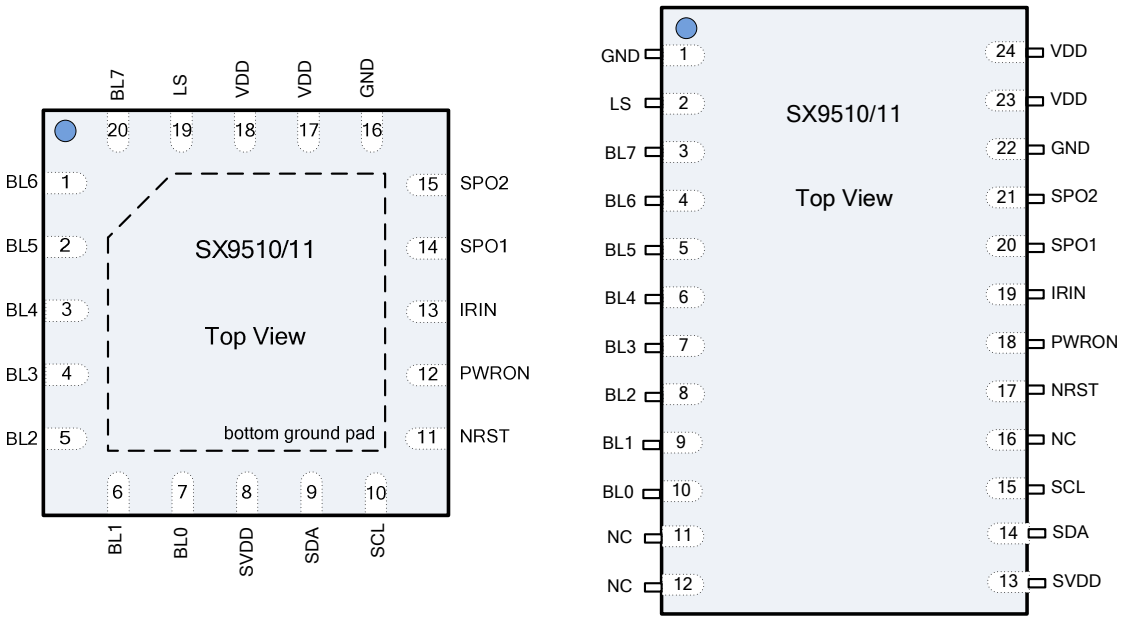


Figure 1 Pinout Diagram SX9510/11 (QFN, TSSOP)

1.2 Marking information SX9511

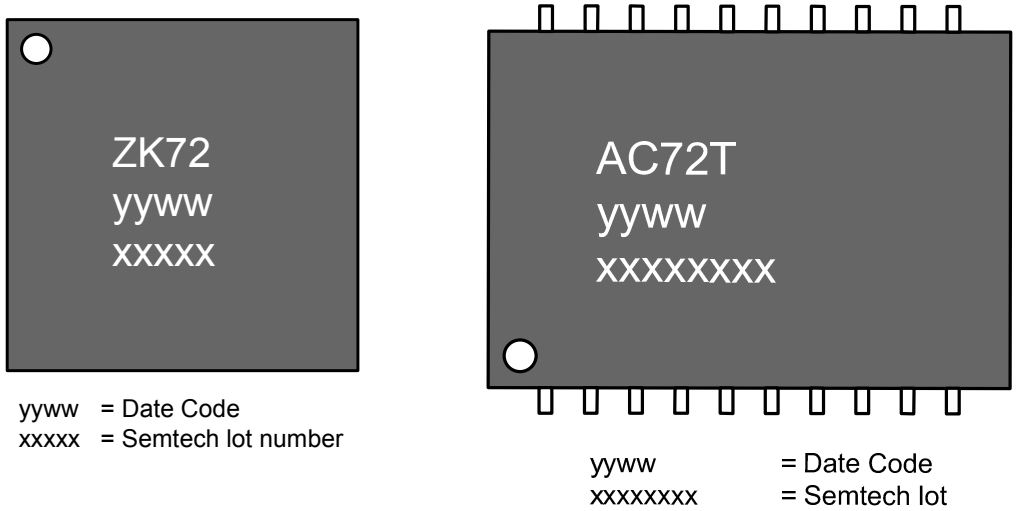


Figure 2 Marking Information SX9511 (QFN, TSSOP)

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1.3 Marking information SX9510

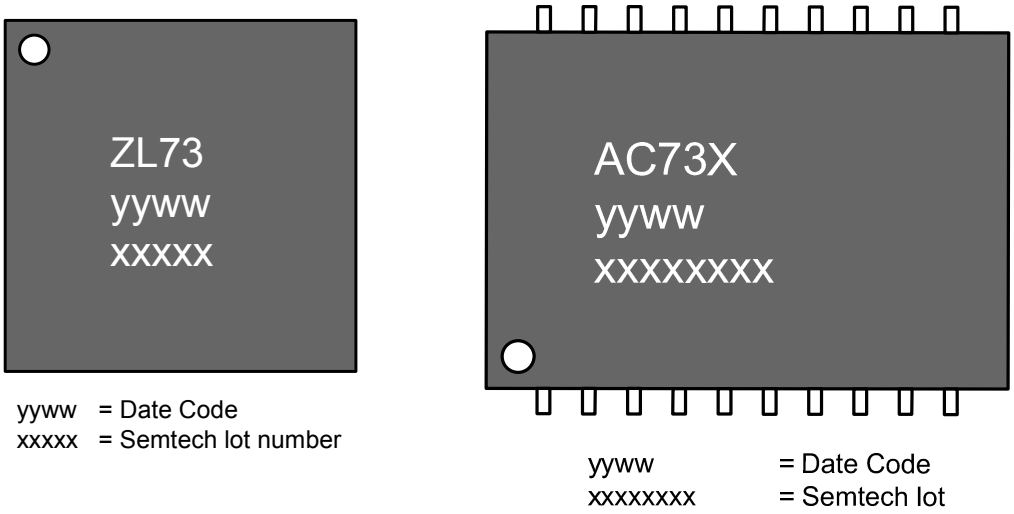


Figure 3 Marking Information SX9510 (QFN, TSSOP)

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1.4 Pin Description

Pin QFN	Pin TSSOP	Name	Type	Description
1	4	BL6	Analog	Button Sensor and Led Driver 6
2	5	BL5	Analog	Button Sensor and Led Driver 5
3	6	BL4	Analog	Button Sensor and Led Driver 4
4	7	BL3	Analog	Button Sensor and Led Driver 3
5	8	BL2	Analog	Button Sensor and Led Driver 2
6	9	BL1	Analog	Button Sensor and Led Driver 1
7	10	BL0	Analog	Button Sensor and Led Driver 0
8	13	SVDD	Power	IO Power Supply, SVDD must be ≤ VDD
9	14	SDA	Digital Input/Output	I2C Data, requires pull up resistor to SVDD (in host or external)
10	15	SCL	Digital Input	I2C Clock, requires pull up resistor to SVDD(in host or external)
11	17	NRST	Digital Input	Active Low Reset. Connect to SVDD if not used.
12	18	PWRON	Digital Output	Power On Signal (positive edge triggered, push pull)
13	19	IRIN	Digital Input	Input Signal from IR receiver.
14	20	SPO1	Analog	Special Purpose Output 1: - AOUT1: Analog Voltage indicating touched buttons (filtered digital)
15	21	SPO2	Analog/Digital	Special Purpose Output 2: - AOUT2: Analog Voltage indicating touched buttons (filtered digital) - BUZZER: Driver (digital push-pull output) - NIRQ: Interrupt Output, active low (digital open drain output) - PWRSTATE: Signal indicating system power state (digital input)
16	22	GND	Ground	Ground
17	23	VDD	Power	Power Supply
18	24	VDD	Power	Power Supply
19	2	LS	Analog	Led Sink/Shield
20	3	BL7	Analog	Button Sensor and Led Driver 7
bottom plate	1	GND	Ground	Connect to ground
	11, 12, 16	NC	No Connect	Leave Floating

Table 1 Pin description

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1.5 Simplified Block Diagram

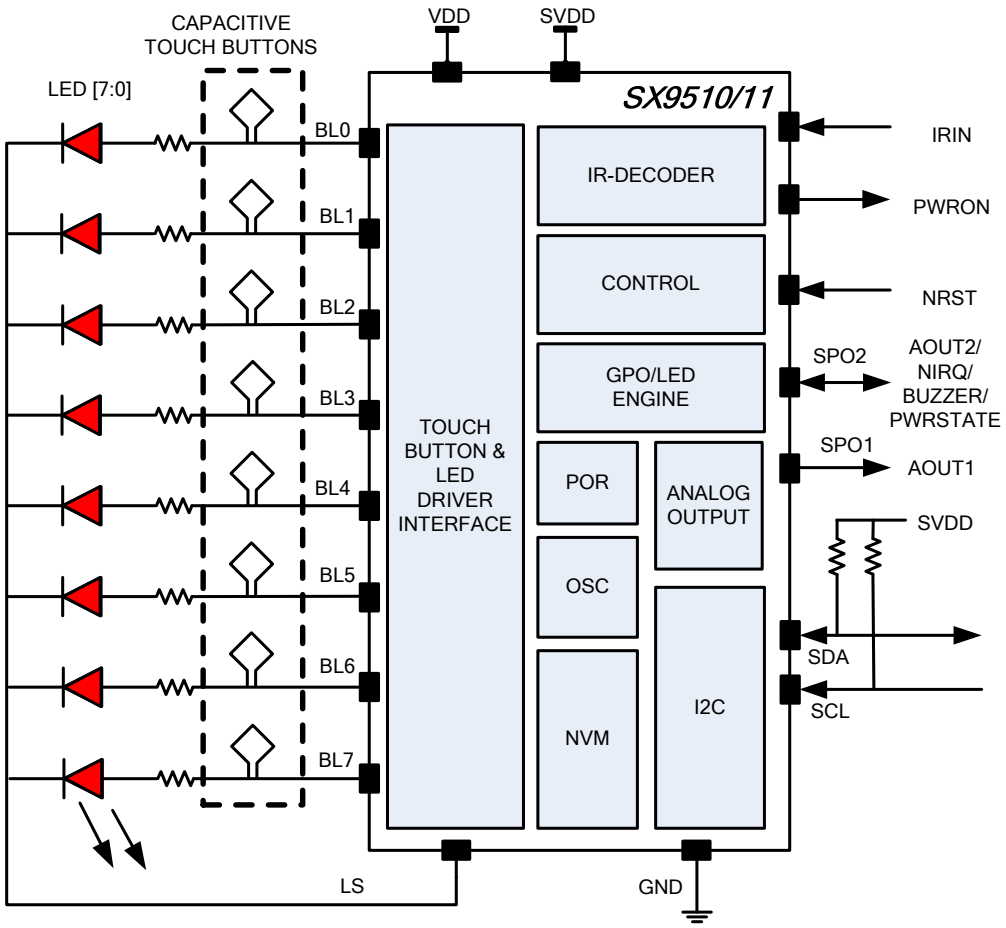


Figure 4 Simplified Block diagram of the SX9510/11

1.6 Acronyms

AOI	Analog Output Interface
ASI	Analog Sensor Interface
NVM	Non Volatile Memory
PWM	Pulse Width Modulation
SPO	Special Purpose Output

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2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Stresses above the values listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these, or any other conditions beyond the "Recommended Operating Conditions", is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	VDD, SVDD	-0.5	6.0	V
Input voltage (non-supply pins)	V_{IN}	-0.5	VDD + 0.3	V
Input current (non-supply pins)	I_{IN}	-10	10	mA
Operating Junction Temperature	T_{JCT}	-40	150	°C
Reflow temperature	T_{RE}		260	°C
Storage temperature	T_{STOR}	-50	150	°C
ESD HBM (Human Body model)(i)	ESD_{HBM}	3		kV
Latchup(ii)	I_{LU}	± 100		mA

Table 2 Absolute Maximum Ratings

(i) Tested to JEDEC standard JESD22-A114

(ii) Tested to JEDEC standard JESD78

2.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	2.7	5.5	V
Supply Voltage (SVDD must be ≤ VDD)	SVDD	1.65	5.5	V
Ambient Temperature Range	T_A	-40	85	°C

Table 3 Recommended Operating Conditions

2.3 Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance - Junction to Ambient (vi)	$\theta_{JA,QFN}$			25		°C/W
Thermal Resistance - Junction to Ambient (vi)	$\theta_{JA,SSOP}$			78		°C/W

Table 4 Thermal Characteristics

(vi) ThetaJA is calculated from a package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under exposed pad (if applicable) per JESD51 standards.

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2.4 Electrical Specifications

All values are valid within the operating conditions unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption						
Sleep	I_{sleep}	All buttons are scanned at a 200ms rate. (40ms scan with skip 4 frames)		330	350	uA
Operating	$I_{operating}$	All buttons are scanned at a 40 ms rate, excluding LED forward current.		600	650	uA
Input Levels NRST, IRIN, SCL, SDA, SPO2 (in PWRSTATE mode)						
Input logic high	V_{IH}		0.7*SVDD		SVDD + 0.3	V
Input logic low	V_{IL}	GND applied to GND pins	GND - 0.3		0.3*SVDD	V
Input leakage current	L_I	CMOS input			±1	uA
Output PWRON, SPO1, SPO2, SDA						
Output logic high (PWRON, SP01, & SP02 Only)	V_{OH}	I_{OH}<3mA	SVDD-0.4			V
Output logic low	V_{OL}	$I_{OL,}$<6mA			0.6	V
CapSense Interface						
Offset Compensation Range	C_{off}			40		pF
Power up time	t_{por}				10	ms
Reset						
Power on reset voltage	V_{por}			1.1		V
Reset time after power on	t_{por}			1		ms
Reset pulse width on NRST	t_{res}			20		ns
Recommended External components						
capacitor between SVDD, GND	C_{vreg}	tolerance +/-20%		0.1		uF
capacitor between VDD, GND	C_{vdd}	tolerance +/-20%		0.1		uF

Table 5 Electrical Specifications

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
I2C Timing Specifications (i)						
SCL clock frequency	f_{SCL}				400	KHz
SCL low period	t_{LOW}		1.3			us
SCL high period	t_{HIGH}		0.6			us
Data setup time	$t_{SU;DAT}$		100			ns
Data hold time	$t_{HD;DAT}$		0			ns
Data valid time	$t_{VD;DAT}$				0.9	us
Repeated start setup time	$t_{SU;STA}$		0.6			us
Start condition hold time	$t_{HD;STA}$		0.6			us
Stop condition setup time	$t_{SU;STO}$		0.6			us
Bus free time between stop and start	t_{BUF}		1.3			us
Input glitch suppression	t_{SP}	Up to 0.3xVDD from GND, down to 0.7xVDD from VDD			50	ns

Table 6 I2C Timing Specification

Notes:

(i) All timing specifications, Figure 5 and Figure 6, refer to voltage levels (V_{IL}, V_{IH}, V_{OL}) defined in Table 5.

(ii) $t_{VD;DAT}$ = Minimum time for SDA data out to be valid following SCL LOW.

The interface complies with slave F/S mode as described by NXP: “I2C-bus specification, Rev. 03 - 19 June 2007”

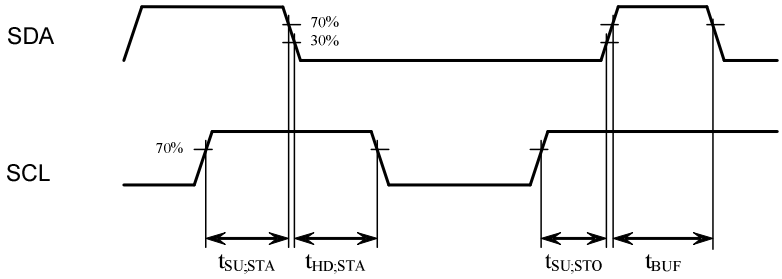


Figure 5 I2C Start and Stop timing

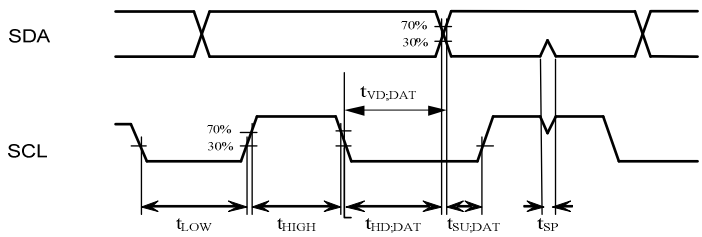


Figure 6 I2C Data timing

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3 FUNCTIONAL DESCRIPTION

3.1 Introduction

3.1.1 General

The SX9510/11 is intended to be used in applications which require capacitive sensors covered by isolating overlay material and which may need to detect the proximity of a finger/hand though the air. The SX9510/11 measures the change of charge and converts that into digital values. The larger the charge on the sensors, the larger the number of digital value will be. The charge to digital value conversion is done by the SX9510/11 Analog Sensor Interface (ASI).
The digital values are further processed by the SX9510/11 and converted in a high level, easy to use information for the user's host.
The information between SX9510/11 and the user's host is passed through the I2C interface with an additional interrupt signal indicating that the SX9510/11 has new information. For buttons this information is simply touched or released. The SX9510/11 can operate without the I2C and interrupt by using the analog output interface (SPO1, SPO2) with a changing voltage level to indicate the button touched.

3.1.2 Feedback

Visual feedback to the user is done by the button and LED pins BL[7...0]. The LED drivers will fade-in when a finger touches a button or proximity is detected and fade-out when the button is released or finger goes out of proximity. Fading intensity variations can be logarithmic or linear. Interval speed and initial and final light intensity can be selected by the user.

Audible feedback can be obtained through the Special Purpose Output (SPO2) pin connected to a buzzer.

3.1.3 Analog Output Interface SPO1 and SPO2

The Analog Output Interface (AOI) is a Digital signal driven from GND to SVDD and controlled by a PWM. When the digital signal on the SPO line is filtered with an RC low pass filter you produce a DC voltage, the level of which depends on the buttons that has been touched. A host controller can then measure the voltage delivered by the SPO output and determine which button is touched at any given time.
The AOI feature allows the SX9510/11 device to directly replace legacy mechanical button controllers in a quick and effortless manner. The SX9510/11 supports up to two Analog Output Interfaces, on SPO1 and SPO2 respectively. The SX9510/11 allows buttons to be mapped on either SPO1 or SPO2. The button mapping as well as the mean voltage level that each button produces on an SPO output can be configured by the user through a set of parameters described in later chapters.

3.1.4 Buzzer

The SX9510/11 can drive a buzzer (on SPO2) to provide audible feedback on button touches. The buzzer provides two phases, each of which can vary from 5ms to 30ms in length and can drive 1KHz, 2KHz, 4KHz or 8KHz tones.

3.1.5 Configuration

The control and configuration registers can be read from and written to an infinite number of times. During the development phase the parameters can be determined and fine tuned by the users and updated over the I2C.

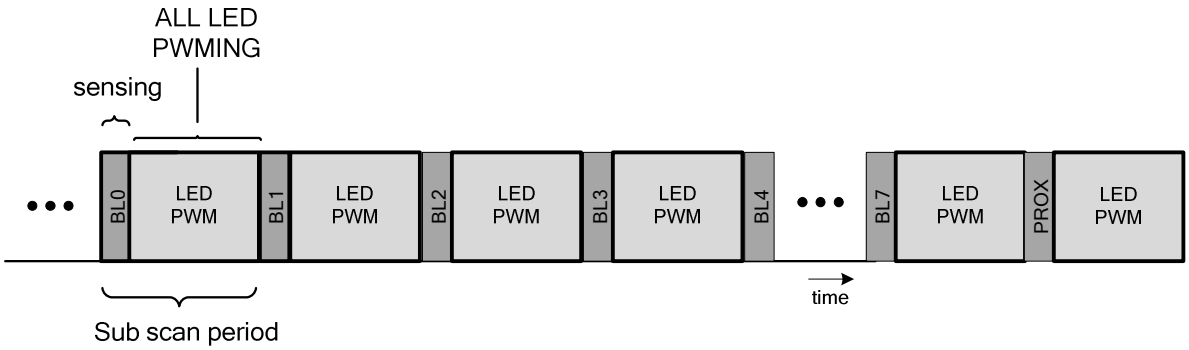
Once the parameter set has been determined, the settings can be downloaded over the I2C by the host each time the SX9510/11 boots up or they can be stored in the Multiple Time Programmable (MTP) Non Volatile Memory (NVM) on the SX9510/11. This allows the flexibility of dynamically setting the parameters at the expense of I2C traffic or autonomous operation without host intervention.

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After the parameters are written to the NVM, the registers can still be dynamically overwritten in whole or in part by the host when desired.

3.2 Scan Period

The SX9510/11 interleaves the sensing of the touch buttons with the driving of the LEDs. To keep the LED intensities constant and flicker free the BL sensing is done in a round robin fashion with an LED drive period between each of the BL sensing periods.



Nine (9) scan periods (1 frame) are required to scan all 8 buttons & Perform Combined Channel Proximity Sensing

Figure 7 CapSense Scan Frame SX9510/11

To keep timing consistency the scan frame always cycles through all channels (BL0 to BL7) and Combined Channel proximity even if a channel is disabled or a device does not have the proximity feature. This means that the frame time is always the sum of nine CapSense measurement times and nine LED PWM times.

The SX9510/11 can reduce it's average power consumption by inserting fames that skip the CapSense measurements but maintain the LED PWM timing.

The Scan period of the SX9510/11 is the time between the measurement of a particular channel and its next measurement. This period is the time for one CapSense frame plus the time for any skip frames and is the key factor in determining system touch response timing.

Figure 8 shows the different SX9510/11 periods over time.

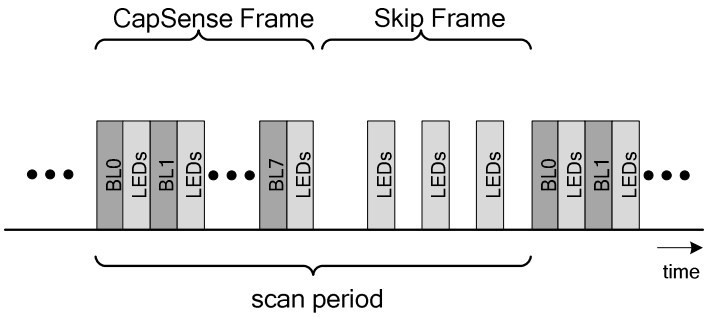


Figure 8 Scan Period SX9510/11

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3.3 Operation modes

The SX9510/11 has 2 operation modes, Active and Sleep. The main difference between the 2 modes is found in the reaction time (corresponding to the scan period) and power consumption.

Active mode offers fast scan periods. The typical reaction time is 40ms. All enabled sensors are scanned and information data is processed within this interval.

Sleep mode increases the scan period time which increases the reaction time to 200ms typical and at the same time reduces the operating current.

The user can specify other scan periods for the Active and Sleep mode and decide for other compromises between reaction time and power consumption.

In most applications the reaction time needs to be fast when fingers are present, but can be slow when no person uses the application. In case the SX9510/11 is not used during a scan frame it will go from Active mode into Sleep mode and power will be saved. (when sleep mode is enabled)

To leave Sleep mode and enter Active mode this can be done by a touch on any button or the detection of proximity.

The host can decide to force the operating mode by issuing commands over the I2C (using register 0x3A[3]) and take fully control of the SX9510/11. The diagram in Figure 9 shows the available operation modes and the possible transitions.

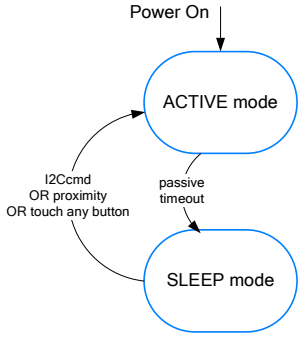


Figure 9 Operation modes

3.4 Sensors on the PCB

The capacitive sensors are relatively simple copper areas on the PCB connected to the eight SX9510/11 capacitive sensor input pins (BL0…BL7). The sensors are covered by isolating overlay material (typically 1mm...3mm). The area of a sensor is typically one square centimeter which corresponds to about the area of a finger touching the overlay material. The area of a proximity sensor is usually significantly larger than the smaller touch sensors.

The SX9510 and the SX9511 capacitive sensors can be setup as ON/OFF buttons for control applications (see example Figure 10).

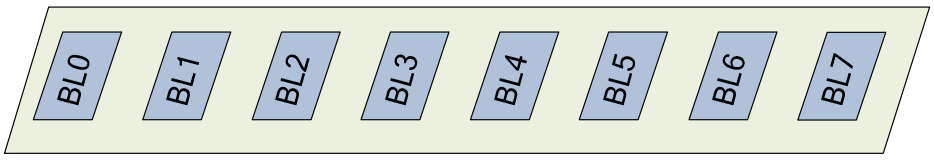


Figure 10 PCB top layer of touch buttons sensors surrounded by the shield, SX9510/11

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The SX9510 offers 2 options for proximity detection. Depending on the PCB area, the proximity detection distance can be optimized.

1) Individual Sensor Proximity

Single sensor proximity is done by replacing the shield area shown in Figure 10 with a connection to BL0 as shown in Figure 24.

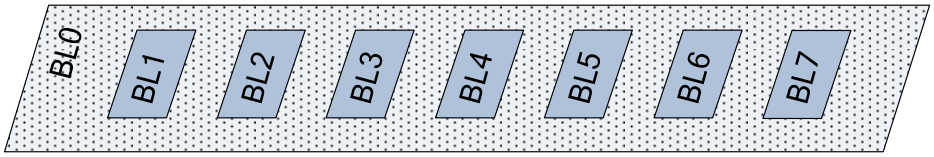


Figure 11 PCB top layer for proximity and touch buttons, SX9510

2) Combined Channel Proximity

In Combined Channel Proximity the SX9510 will put some or all of the sensors in parallel and execute one sensing cycle on this combined large sensor.

3.5 Button Information

The touch buttons have two simple states (see Figure 12): ON (touched by finger) and OFF (released and no finger press).

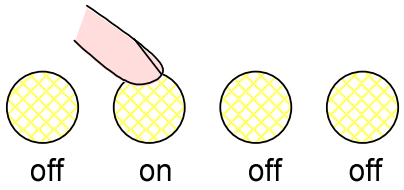


Figure 12 Buttons

A finger is detected as soon as the digital values from the ASI reach a user-defined threshold plus a hysteresis.

A release is detected if the digital values from the ASI go below the threshold minus a hysteresis. The hysteresis around the threshold avoids rapid touch and release signaling during transients.

Buttons can also be used to do proximity sensing. The principle of proximity sensing operation is exactly the same as for touch buttons except that proximity sensing is done several centimeters above the overlay through the air. ON state means that finger/hand is detected by the sensor and OFF state means the finger/hand is far from the sensor and not detected.

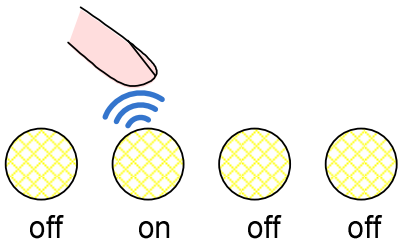


Figure 13 Proximity

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3.6 Buzzer

The SX9510/11 has the ability to drive a buzzer (on SPO2) to provide an audible indication that a button has been touched. The buzzer is driven by a square wave signal for approximately 10ms (default). During both the first phase (5ms) and the second phase (5ms) the signal's frequency is default 1KHz.
The buzzer is activated only once during any button touch and is not repeated for long touches. The user can choose to enable or disable the buzzer by configuration and define the idle level, frequencies and phase durations (see §4.6).

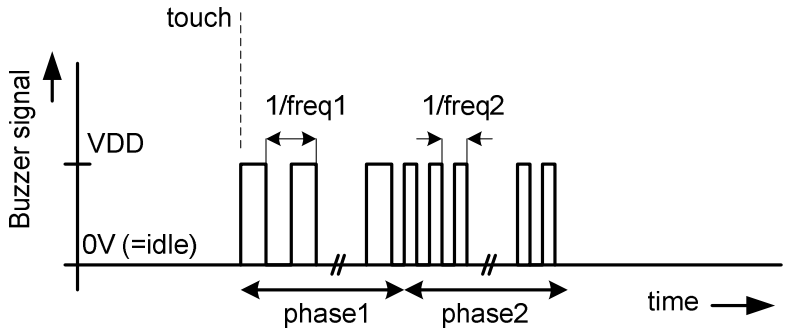


Figure 14 Buzzer behavior

3.7 Analog Output Interface

The Analog Output Interface outputs a PWM signal with a varying duty cycle depending on which button is touched. By filtering (with a simple RC filter) the PWM signal results in a DC voltage that is different for each button touch. The host controller measures the DC voltage level and determines which buttons has been touched.

In the case of single button touches, each button produces its own voltage level as configured by the user.

Figure 15 show how the AOI will behave when the user touches and releases different buttons.
The AOI will switch between the AOI idle level and the level for each button.

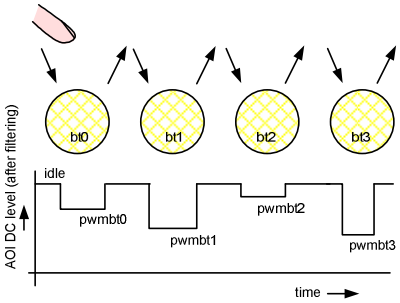


Figure 15 AOI behavior

The PWM Blocks used in AOI modes are 6-bits based and are typically clocked at 2MHz.

Figure 16 shows the PWM definition of the AOI.

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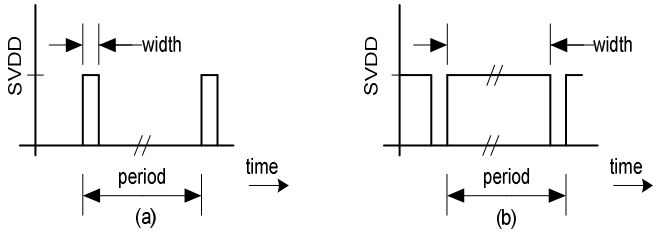


Figure 16 PWM definition, (a) small pulse width, (b) large pulse width

The AOI always reports one button per output channel. The AOI can be split over SPO1 and SPO2 (AOI-A, AOI-B. The user can map any button to either AOI-A or AOI-B or both.

In most applications only one AOI pin will be selected. The two AOI pins allow the user to use a more coarse detection circuit at the host. Assuming a 3.3V supply and 8 buttons on one single AOI then the AOI levels could be separated by around 0.3…0.4V. In the case of using the two AOI pins, 4 buttons could be mapped on AOI-A separated by around 0.8V (similar for 4 buttons on AOI-B) which is about double that of the case of a single AOI.

In the case of a single touch the button reporting is straight forward (as in Figure 15). If more than one button is touched the reported depends on the selected button reporting mode parameter (see yyy). Three reporting modes exist for the SX9510/11 (All, Single and Strongest).
The All reporting mode is applicable only for the I2C reporting (AOI is not available). In All-mode all buttons that are touched are reported in the I2C buttons status bits and on the LEDs. In the Single-mode a single touched button will be reported on the AOI and the I2C. All touches that occur afterwards will not be reported as long as the first touch sustains. Only when the first reported button is released will the SX9510/11 report another touch.

Figure 17 shows the Single-mode reporting in case of 2 touches occurring over time.

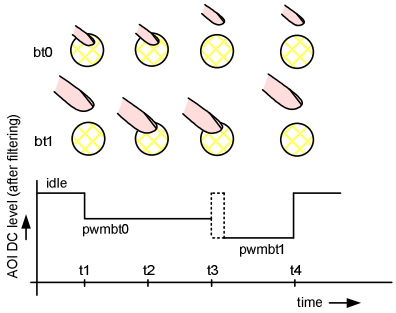


Figure 17 Single-mode reporting with 2 touches

At time t1 button0 is touched and reported on the AOI. At time t2 button1 is touched as well but not reported. At time t3 the button0 is released and button1 will be reported immediately (or after one scan period at idle level). At time t4 both buttons are released and the AOI reports the idle level.

The button with the lowest Cap pin index will be reported in case of a simultaneous touch (that means touches occurring within the same scan period).

In the Strongest-mode the strongest touched button will be reported on the AOI and the I2C. All touches that occur afterwards representing a weaker touch will not be reported. Only a touch which is stronger will be reported by the SX9510/11.
Figure 18 shows the Strongest-mode reporting in case of 2 touches (with bt1 the strongest touch).

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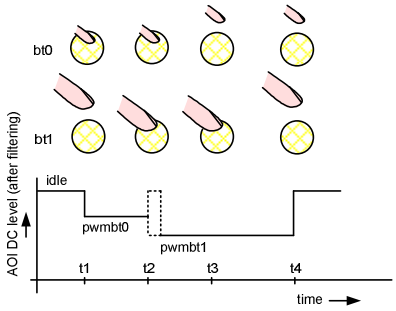


Figure 18 Strongest-mode reporting with 2 touches

At time t1 button0 is touched and reported on the AOI. At time t2 button1 is touched as well. As bt1 is the strongest touch it will be reported on the AOI immediately (or after one scan period at idle level). At time t3 the button0 is released while the AOI continues to report button1. At time t4 both buttons are released and the AOI reports the idle level.

3.8 Analog Sensing Interface

The Analog Sensing Interface (ASI) induces a charge on the sensors and then converts the charge into a digital value which is further digitally processed. The basic principle of the ASI will be explained in this section.

The ASI consists of a multiplexer selecting the sensor, analog switches, a reference voltage, a high-resolution ADC converter and an offset compensation DAC (see Figure 19).

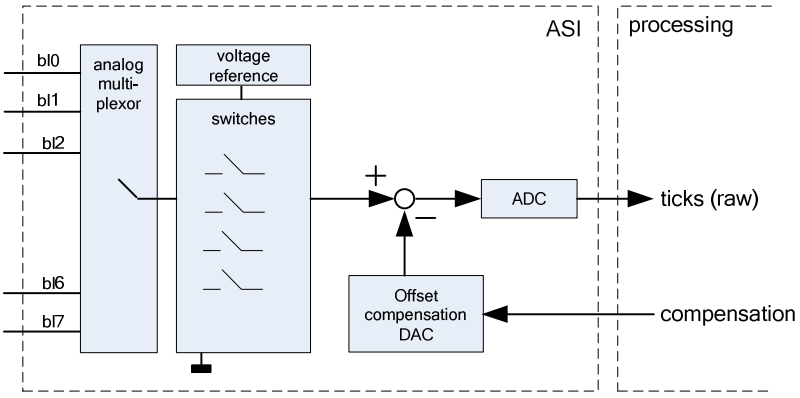


Figure 19 Analog Sensor Interface

The SX9510 offers the additional Combined Channel Proximity mode where all sensors are sensed in parallel.

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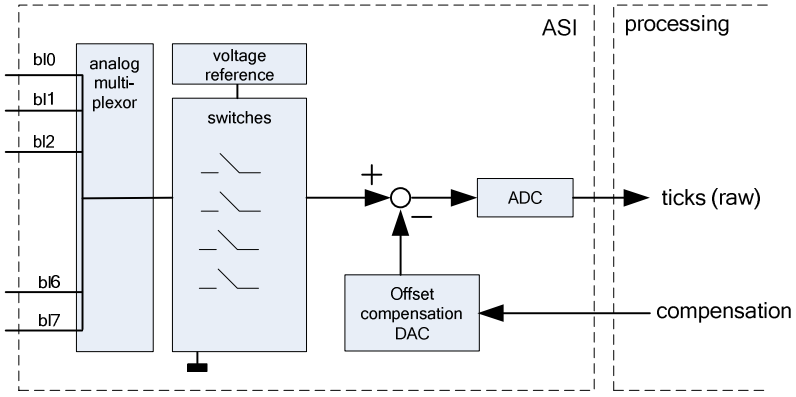


Figure 20 Analog Sensor Interface for SX9510, Combined Channel Prox Mode

To get the digital value representing the charge on a specific sensor the ASI will execute several steps. A voltage will be induced on the sensor developing a charge relative to the absolute capacitance of the sensor. The charge on a sensor cap (e.g BL0) will then be accumulated multiple times on the internal integration capacitor (Cint). This results in an increasing voltage on Cint proportional to the capacitance on BL0.

At this stage the offset compensation DAC is enabled. The compensation DAC generates a voltage proportional to an estimation of the external parasitic capacitance (the capacitance of the system without the calibration).

The difference between the DAC output and the charge on Cint is the desired signal. In the ideal case the difference of charge will be converted to a zero digital value if no finger is present and the digital value becomes high in case a finger is present.

The difference of charge on Cint and the DAC output will be transferred to the ADC.

After the charge transfer to the ADC the steps above will be repeated.

The SX9510/11 allows setting the sensitivity for each sensor individually for applications which have a variety of sensors sizes or different overlays or for fine-tuning performances. The optimal sensitivity depends heavily on the final application. If the sensitivity is too low the digital value will not pass the thresholds and touch/proximity detection will not be possible. In case the sensitivity is set too large, some power will be wasted and false touch/proximity information may be output (i.e. for touch buttons => finger not touching yet, for proximity sensors => finger/hand not close enough).

The digital values from the ASI will then be handled by the digital processing.

The ASI will shut down and wait until new sensing period will start.

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3.8.1 Processing

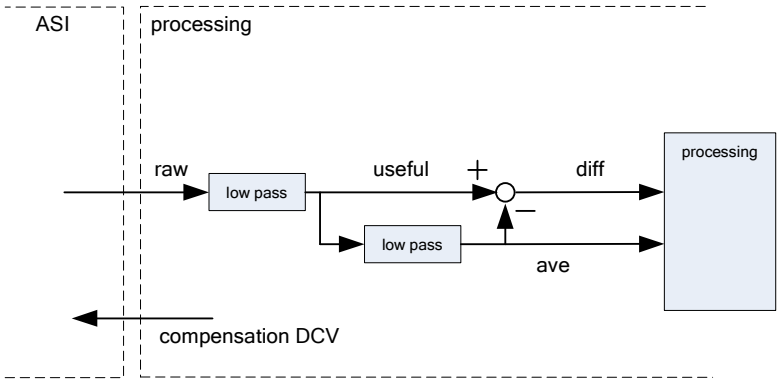


Figure 21 Processing

The raw data is processed through a programmable low pass filter to create useful data (data with fast environmental noise suppressed). The useful data is processed through a second programmable low pass filter (with a longer time constant) to create average data. The average data tracks along with the slow environmental changes and is subtracted from the useful data to create the diff data. The diff data represents any fast capacitance changes such as a touch or proximity event.

3.8.2 Offset Compensation

The parasitic capacitance at the BL pins is defined as the intrinsic capacitance of the integrated circuit, the PCB traces, ground coupling and the sensor planes. This parasitic capacitance is relatively large (tens of pF) and will also vary slowly over time due to environmental changes.

A finger touch is in the order of one pF and its effect typically occurs much faster than the environmental changes.

The ASI has the difficult task of detecting a small, fast changing capacitance that is riding on a large, slow varying capacitance. This would require a very precise, high resolution ADC and complicated, power consuming, digital processing.

The SX9510/11 features a 16 bit DAC which compensates for the large, slow varying capacitance already in front of the ADC. In other words the ADC converts only the desired small signal. In the ideal world the ADC will put out a zero digital value even if the external capacitance is as high as 40pF.

At each power-up of the SX9510/11 the Compensation Values are estimated by the digital processing algorithms. The algorithm will adjust the compensation values such that a near-zero value will be generated by the ADC. Once the correct compensation values are found these will be stored and used to compensate each BL pin.

If the SX9510/11 is shut down the compensation values will be lost. At a next power-up the procedure starts all over again. This assures that the SX9510/11 will operate under any condition.

However if temperature changes this will influence the external capacitance. The ADC digital values will drift then slowly around zero values basically because of the mismatch of the compensation circuitry and the external capacitance.

In case the average value of the digital values become higher than the positive calibration threshold (configurable by user) or lower than the negative threshold (configurable by user) then the SX9510/11 will initiate a compensation procedure and find a new set of compensation values.

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The host can initiate a compensation procedure by using the I2C interface. This is required after the host changes the sensitivity of sensors.

3.9 IR Interface

The IR interface for the SX9510/11 allows the user to save power by powering down their main processor. When a preprogrammed IR sequence is received the SX9510/11 generates a PWRON pulse to wake up the system.

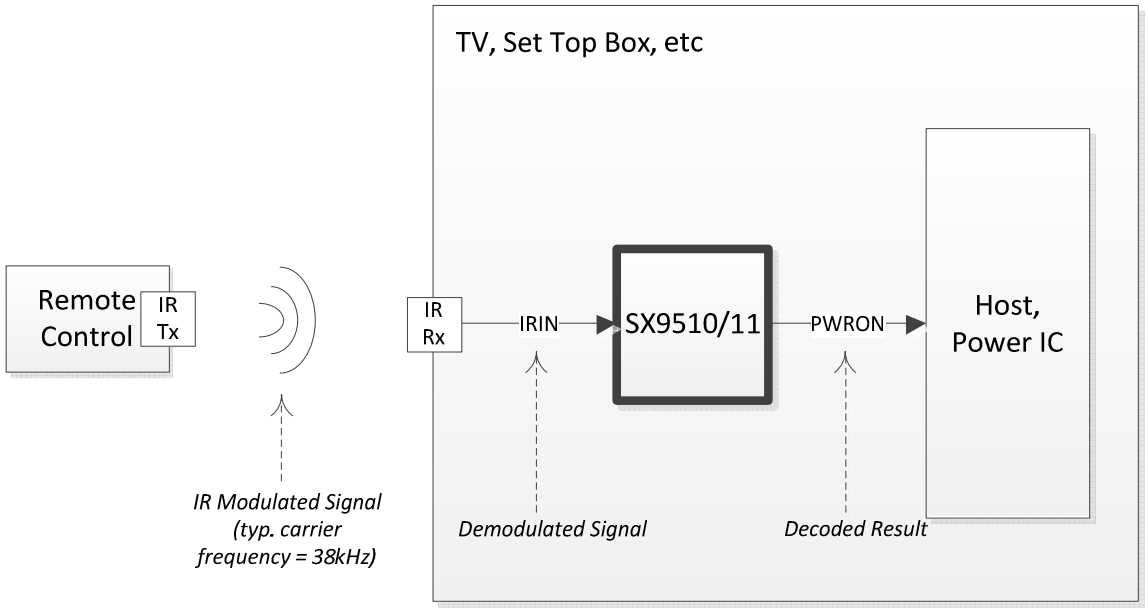


Figure 22 IR Interface Overview

The IR interface can be programmed to match one manufacturer code (address, 1 to 16 bits) and up to 8 button codes (commands, 1 to 8 bits each). The IR interface has been designed to be very flexible and can be programmed for phase coding (e.g. RC5/RC6) or space encoding (e.g. NEC, RCA, etc…), with or without header, etc, allowing it to be potentially usable with any type of IR remote control.

An added feature allows the user to blink the power LED (if power LED functions are enabled) when an IR sequence is received that matches either the specified manufacturer code (address) or match both the manufacturer code and one of the 8 button codes (commands). This gives a visual indication of incoming IR commands without main processor/host intervention.

3.9.1 Phase and Space Encoding

The IR signal sent over the IR is modulated and demodulated as follow:
- Mark = presence of carrier frequency
- Space = no presence of carrier frequency

In both encoding schemes, each logic bit is composed of a mark and a space.

Phase encoding (also called Manchester encoding) consists in having same duration/width for both space and mark and coding the logic level depending if mark or space comes first.
In other words, the edge of the transition defines the logical level. For example, with normal polarity, mark-to-space denotes logic 1 while space-to-mark denotes logic 0. For inverted polarity it is the opposite.

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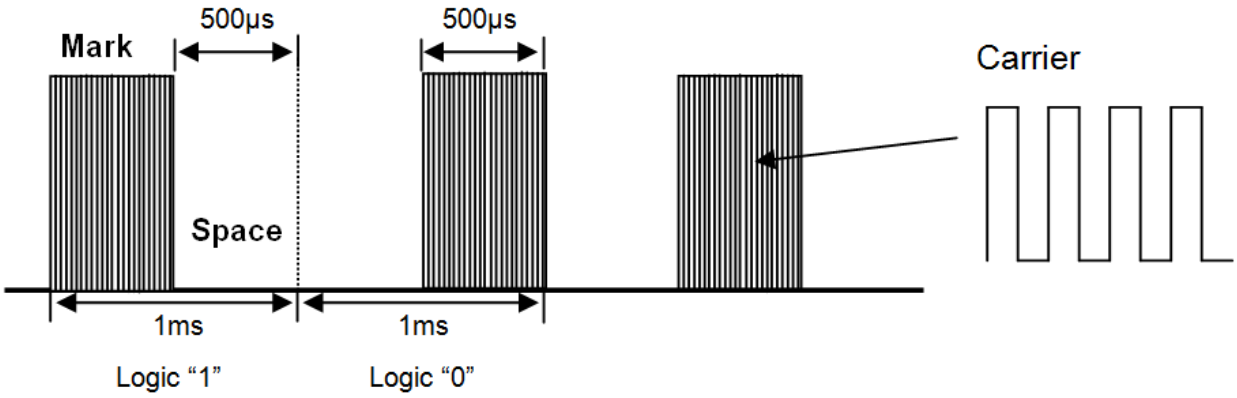


Figure 23 Phase Encoding Example (RC5) with Normal Polarity

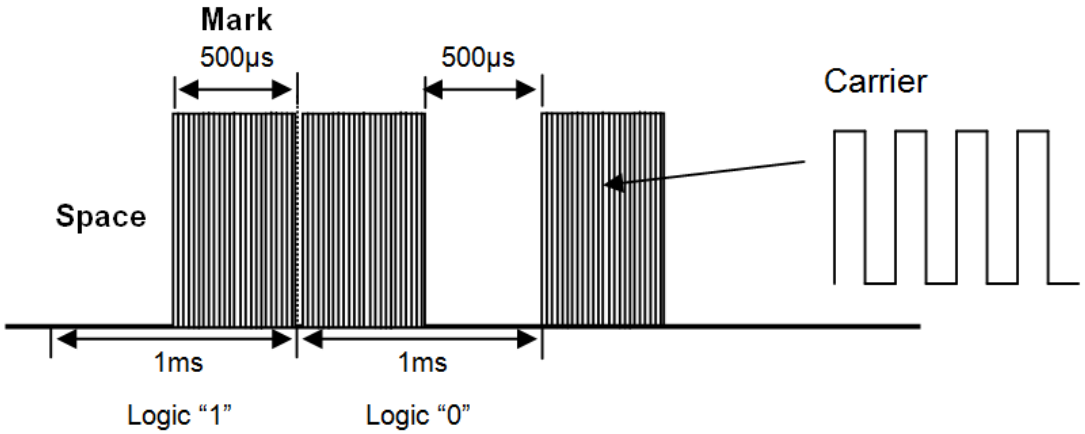


Figure 24 Phase Encoding Example (RC6) with Inverted Polarity

Space encoding consists in having same mark-space order and coding the logic level depending on the duration/width of the space.

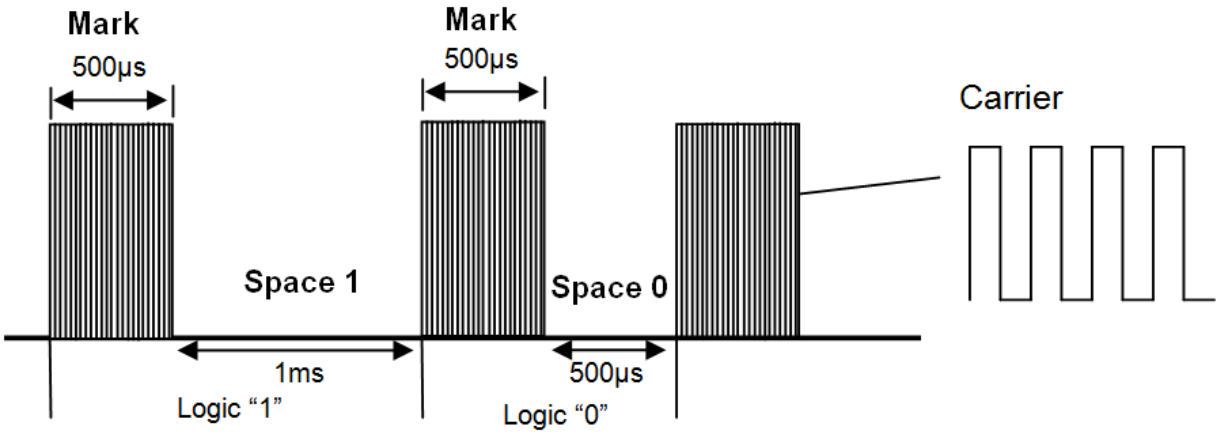


Figure 25 Space Encoding Example

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3.9.2 Header

The header, when used in the protocol, is the very first part of an IR frame and always consists in a mark followed by a space but usually with specific durations/widths different from the following data composing the frame.
Usually the header mark is quite long (several ms), and is used by the receiver to adjust its gain control for the strength of the signal.

3.9.3 Data (Address and Command)

After the header, comes the data section of the IR frame which for us consists in two fields:
- Address: manufacturer code
- Command: button code corresponding to the button pressed on the remote control (Power, Ch+, Ch-, etc)

Depending on the protocol, address or command field comes first.

If an IR frame which matches all pre-programmed timings (+/- IR margin), address, and command is received; then a pulse is generated on PWRON pin to wake up the system.

3.10 Configuration

Figure 26 shows the building Blocks used for configuring the SX9510/11.

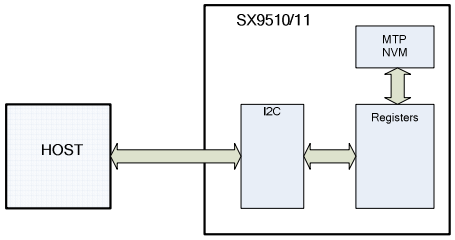


Figure 26 Configuration

During development of a touch system the register settings for the SX9510/11 are adjusted until the user is satisfied with the system operation. When the adjustments are finalized contents of the registers can be stored in the Multiple Time Programmable (MTP) Non Volatile Memory (NVM). The NVM contains all those parameters that are defined and stable for the application. Examples are the number of sensors enabled, sensitivity, active and Sleep scan period. The details of these parameters are described in the next chapters.

At power up or reset the SX9510/11 copies the settings from the NVM into the registers.

3.11 Clock Circuitry

The SX9510/11 has its own internal clock generation circuitry that does not require any external components. The clock circuitry is optimized for low power operation.

3.12 I2C interface

The host will interface with the SX9510/11 through the I2C bus and the analog output interface.
The I2C of the SX9510/11 consists of 95 registers. Some of these I2C registers are used to read the status and information of the buttons. Other I2C registers allow the host to take control of the SX9510/11.

The I2C slave implemented on the SX9510/11 is compliant with the standard (100kb/s) and fast mode (400kb/s)
The default SX9510/11 I2C address equals 0b010 1011.

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3.13 Interrupt

The NIRQ mode of SPO2 has two main functions, the power up sequence and maskable interrupts (detailed below).

3.13.1 Power up

During power up the NIRQ is kept low (if SPO2 is configured for NIRQ in the NVM). Once the power up sequence is terminated the NIRQ is cleared autonomously. The SX9510/11 is then ready for operation. The AOI levels are updated at the latest one scan period after the rising edge of NIRQ.

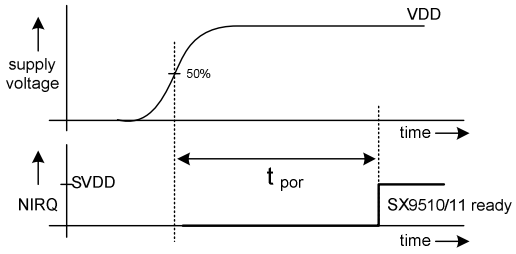


Figure 27 Power Up vs. NIRQ

During the power on period the SX9510/11 stabilizes the internal regulators, RC clocks and the firmware initializes all registers.

During the power up the SX9510/11 is not accessible and I2C communications are forbidden. The value of NIRQ before power up depends on the NIRQ pull up resistor to the SVDD supply voltage.

3.13.2 NIRQ Assertion

When the NIRQ function is enabled for SPO2 then NIRQ is updated in Active or Sleep mode once every scan period.

The NIRQ will be asserted at the following events:

- if a Button event occurred (touch or release if enabled)
- a proximity even occurred (prox or loss of prox (SX9510 only))
- once compensation procedure is completed either through automatic trigger or via host request
- during reset (power up, hardware NRST, software reset)

3.13.3 Clearing

The clearing of the NIRQ is done as soon as the host performs a read to any of the SX9510/11 I2C registers.

3.13.4 Example

A typical example of the assertion and clearing of the NIRQ and the I2C communication is shown in Figure 28.

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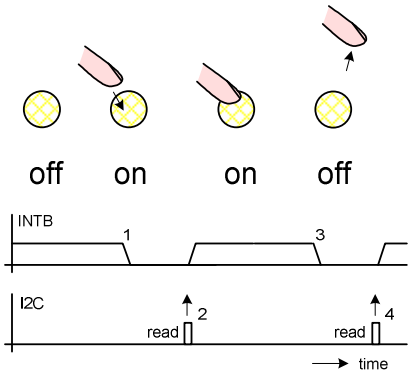


Figure 28 Interrupt and I2C

When a button is touched the SX9510/11 will assert the interrupt (1). The host will read the SX9510/11 status information over the I2C (2) and this clears the interrupt.

If the finger releases the button the interrupt will be asserted (3), the host reads the status (4) which clears the interrupt.

In case the host will not react to an interrupt then this will result in a missing touch.

3.14 Reset

The reset can be performed by 3 sources:

- power up,
- NRST pin,
- software reset.

3.14.1 Power up

During power up the NIRQ is kept low (if SPO2 is configured for NIRQ in the NVM). Once the power up sequence is terminated the NIRQ is cleared autonomously. The SX9510/11 is then ready for operation. The AOI levels are updated at the latest one scan period after the rising edge of NIRQ.

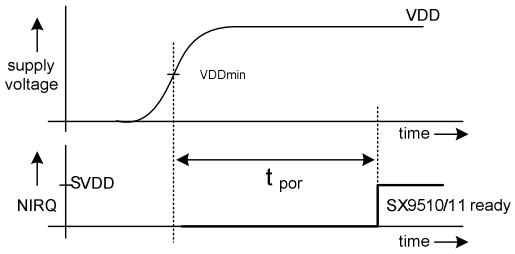


Figure 29 Power Up vs. NIRQ

During the power on period the SX9510/11 stabilizes the internal regulators, RC clocks and the firmware initializes all registers.

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During the power up the SX9510/11 is not accessible and I2C communications are forbidden.
As soon as the NIRQ rises the SX9510/11 will be ready for I2C communication.

3.14.2 NRST

When NRST is driven low the SX9510/11 will reset and start the power up sequence as soon as NRST is driven high or pulled high.

In case the user does not require a hardware reset control pin then the NRST pin can be connected to SVDD.

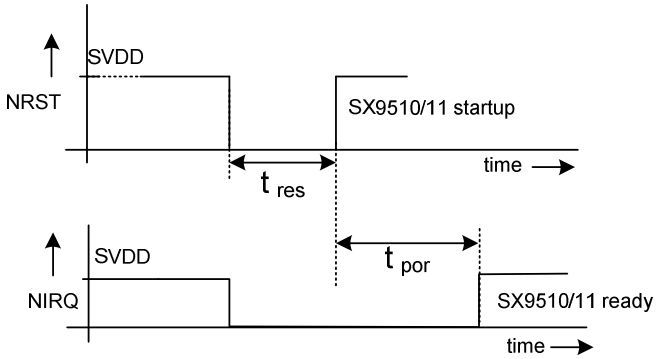


Figure 30 Hardware Reset

3.14.3 Software Reset

To perform a software reset the host needs to write 0xDE followed by 0x00 at the SoftReset register at address 0xFF.

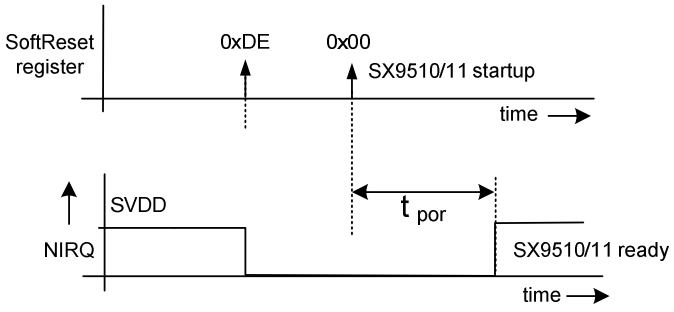


Figure 31 Software Reset

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3.15 LEDS on BL

The SX9510/11 offers eight BL pins that both detect the capacitance change on the touch/prox sensor and drive the associated LED.

The polarity of the BL pins is defined as in the figure below.

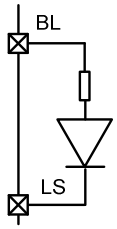


Figure 32 LED between BL and LS pins

The PWM Blocks used in BLP and LED modes are 8-bits based and clocked at 2MHz typ. hence offering 256 selectable pulse width values with a granularity of 0.5us typ.

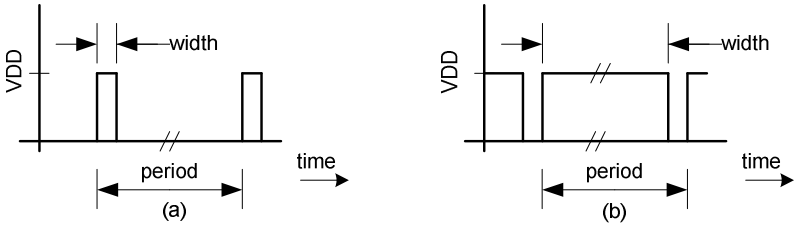


Figure 33 PWM definition, (a) small pulse width, (b) large pulse width

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3.15.1 LED Fading

The SX9510/11 supports two different fading modes, namely Single and Continuous. These fading modes can be configured for each GPIO individually. Please see “BL Parameters” for more information on how to configure this feature.

i) Single Fading Mode:

The LED pin fades in when the associated button is touched and it fades out when it is released. This is shown in Figure 34

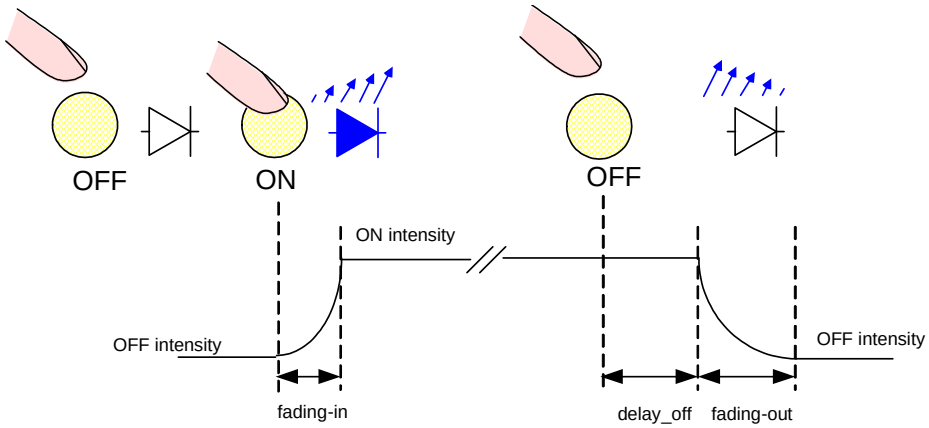


Figure 34 Single Fading Mode

ii) Continuous Fading Mode:

The LED in and fades out continuously when the associated button is touched. The fading in and out stops when the button is released. This is shown in Figure 35.

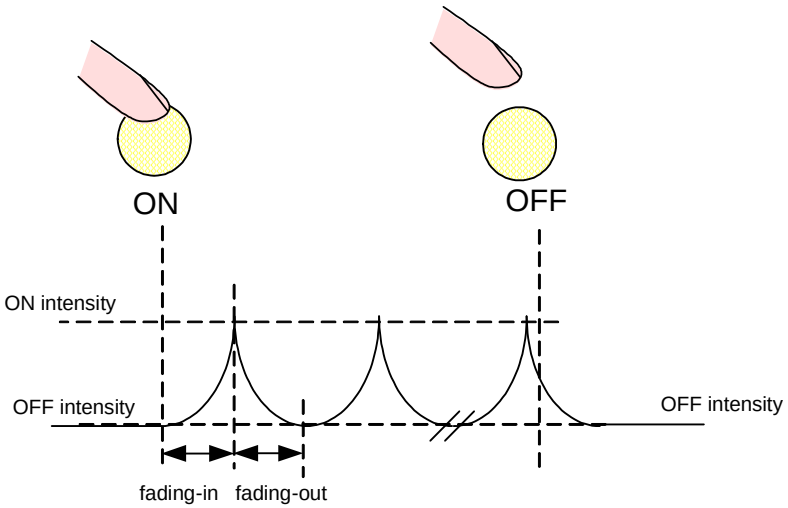


Figure 35 Continuous Fading Mode

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3.15.2 Intensity index vs. PWM pulse width

Tables below show the PWM pulse width for a given intensity (n) setting (for both linear and log modes).

n	Lin/ Log	n	Lin/ Log	n	Lin/ Log	n	Lin/ Log	n	Lin/ Log	n	Lin/ Log	n	Lin/ Log	n	Lin/ Log
0	0/0	**32**	33/5	**64**	65/12	**96**	97/26	**128**	129/48	**160**	161/81	**192**	193/125	**224**	225/184
1	2/0	**33**	34/5	**65**	66/13	**97**	98/27	**129**	130/49	**161**	162/82	**193**	194/127	**225**	226/186
2	3/0	**34**	35/5	**66**	67/13	**98**	99/27	**130**	131/50	**162**	163/83	**194**	195/129	**226**	227/188
3	4/0	**35**	36/5	**67**	68/13	**99**	100/28	**131**	132/51	**163**	164/84	**195**	196/130	**227**	228/190
4	5/0	**36**	37/5	**68**	69/14	**100**	101/29	**132**	133/52	**164**	165/86	**196**	197/132	**228**	229/192
5	6/2	**37**	38/6	**69**	70/14	**101**	102/29	**133**	134/53	**165**	166/87	**197**	198/133	**229**	230/194
6	7/2	**38**	39/6	**70**	71/14	**102**	103/30	**134**	135/54	**166**	167/88	**198**	199/135	**230**	231/197
7	8/2	**39**	40/6	**71**	72/15	**103**	104/30	**135**	136/55	**167**	168/89	**199**	200/137	**231**	232/199
8	9/2	**40**	41/6	**72**	73/15	**104**	105/31	**136**	137/55	**168**	169/91	**200**	201/139	**232**	233/201
9	10/2	**41**	42/6	**73**	74/15	**105**	106/32	**137**	138/56	**169**	170/92	**201**	202/140	**233**	234/203
10	11/2	**42**	43/7	**74**	75/16	**106**	107/32	**138**	139/57	**170**	171/93	**202**	203/142	**234**	235/205
11	12/2	**43**	44/7	**75**	76/16	**107**	108/33	**139**	140/58	**171**	172/95	**203**	204/144	**235**	236/208
12	13/2	**44**	45/7	**76**	77/16	**108**	109/33	**140**	141/59	**172**	173/96	**204**	205/146	**236**	237/210
13	14/2	**45**	46/7	**77**	78/17	**109**	110/34	**141**	142/60	**173**	174/97	**205**	206/147	**237**	238/212
14	15/3	**46**	47/7	**78**	79/17	**110**	111/35	**142**	143/61	**174**	175/99	**206**	207/149	**238**	239/215
15	16/3	**47**	48/8	**79**	80/18	**111**	112/35	**143**	144/62	**175**	176/100	**207**	208/151	**239**	240/217
16	17/3	**48**	49/8	**80**	81/18	**112**	113/36	**144**	145/63	**176**	177/101	**208**	209/153	**240**	241/219
17	18/3	**49**	50/8	**81**	82/19	**113**	114/37	**145**	146/64	**177**	178/103	**209**	210/155	**241**	242/221
18	19/3	**50**	51/8	**82**	83/19	**114**	115/38	**146**	147/65	**178**	179/104	**210**	211/156	**242**	243/224
19	20/3	**51**	52/9	**83**	84/20	**115**	116/38	**147**	148/66	**179**	180/106	**211**	212/158	**243**	244/226
20	21/3	**52**	53/9	**84**	85/20	**116**	117/39	**148**	149/67	**180**	181/107	**212**	213/160	**244**	245/229
21	22/3	**53**	54/9	**85**	86/21	**117**	118/40	**149**	150/68	**181**	182/109	**213**	214/162	**245**	246/231
22	23/3	**54**	55/9	**86**	87/21	**118**	119/40	**150**	151/69	**182**	183/110	**214**	215/164	**246**	247/233
23	24/4	**55**	56/10	**87**	88/22	**119**	120/41	**151**	152/71	**183**	184/111	**215**	216/166	**247**	248/236
24	25/4	**56**	57/10	**88**	89/22	**120**	121/42	**152**	153/72	**184**	185/113	**216**	217/168	**248**	249/238
25	26/4	**57**	58/10	**89**	90/23	**121**	122/43	**153**	154/73	**185**	186/114	**217**	218/170	**249**	250/241
26	27/4	**58**	59/10	**90**	91/23	**122**	123/44	**154**	155/74	**186**	187/116	**218**	219/172	**250**	251/243
27	28/4	**59**	60/11	**91**	92/24	**123**	124/44	**155**	156/75	**187**	188/117	**219**	220/174	**251**	252/246
28	29/4	**60**	61/11	**92**	93/24	**124**	125/45	**156**	157/76	**188**	189/119	**220**	221/176	**252**	253/248
29	30/4	**61**	62/11	**93**	94/25	**125**	126/46	**157**	158/77	**189**	190/121	**221**	222/178	**253**	254/251
30	31/4	**62**	63/12	**94**	95/25	**126**	127/47	**158**	159/78	**190**	191/122	**222**	223/180	**254**	255/253
31	32/5	**63**	64/12	**95**	96/26	**127**	128/48	**159**	160/80	**191**	192/124	**223**	224/182	**255**	256/256

Table 7 Intensity index vs. PWM pulse width (normal polarity)

Recommended/default settings are inverted polarity (to take advantage from high sink current capability) and logarithmic mode (due to the non-linear response of the human eye).

3.15.3 LED Triple Reporting

The button information touch and release can be reported on the LEDs in dual mode (ON and OFF).
The proximity information can be shown using the dual mode by attributing a dedicated LED to the proximity sensor. The LED will show then proximity detected or no proximity detected. The fading principles are equal to the fading of sensors defined as buttons as described in the previous sections.
In triple mode proximity is reported on all LEDs by an intermediate LED intensity.

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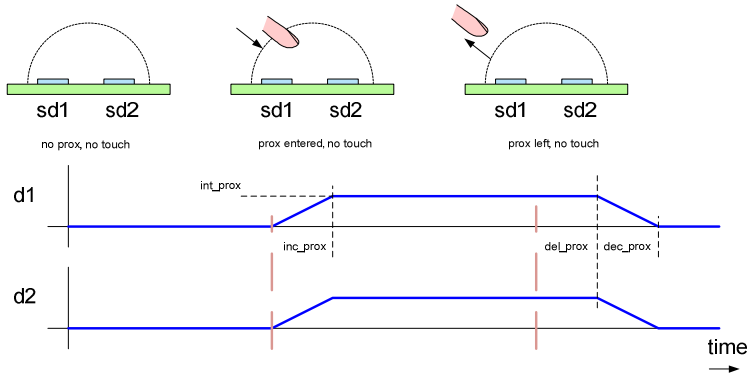


Figure 36 LEDs in triple reporting mode proximity

Figure 36 shows an example of proximity detection and the reporting on LEDs. As soon as proximity is detected all LEDs (2 LEDs are shown for simplicity) will fade in and stop at the proximity intensity level. In case proximity is not detected anymore then the LEDs remain at the proximity intensity for a configurable time and then the fading out will start.

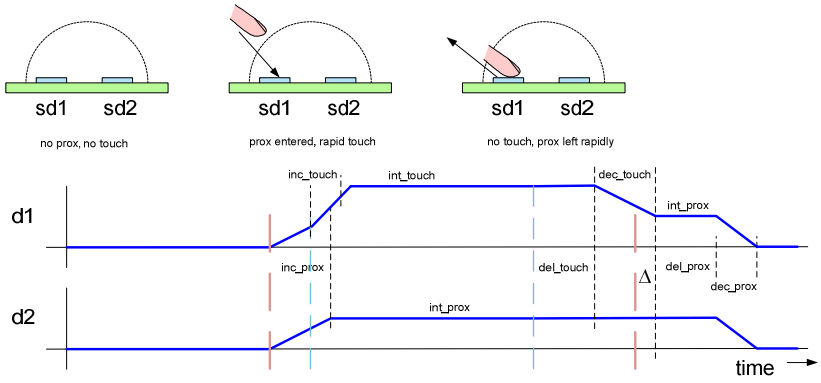


Figure 37 LEDs in triple reporting mode proximity and touch

Figure 37 shows an example of proximity detection followed by a rapid touch on the sensor sd1.
The LEDs d1 and d2 will fade in as soon as proximity is detected (using the Inc_Prox parameter).
As soon as the finger touches the sensor sd1 the fading in of d1 will go to the ON intensity (using the touch increment parameter).
The LED d2 remains at the proximity intensity level as sensors sd2 is not touched.

If the finger is removed rapidly the fading out of d1 will first use the touch decrement parameter to the proximity intensity level. If the finger leaves the proximity region d1 and 2 will fade out simultaneously using the proximity delay and decrement parameters.

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4 DETAILED CONFIGURATION DESCRIPTIONS

4.1 Introduction

The SX9510/11 configuration parameters are taken from the NVM and loaded into the registers at Power-Up or upon reset.

The registers are split by functionality into configuration sections:

- General section: operating modes,
- Capacitive Sensors section: related to lower level capacitive sensing,
- LED
- Special Purpose Outputs
- Buzzer
- Infrared (IR)
- System (Reserved)

The address space is divided up into areas that are (can be) stored in NVM and areas that are dynamic and not stored.

Within the register address space are values designated as 'Reserved'. These values can be disregarded when reading but bust be set to the specified values when writing.

	Address		Name
	0x00	General Control and Status	IrqSrc
	0x01		TouchStatus
	0x02		ProxStatus
	0x03		CompStatus
	0x04		NVMCtrl
	0x05		Reserved
	0x06		Reserved
"NVM" area	0x07		Spo2Mode
	0x08		PwrKey
	0x09		IrqMask
	0x0A		Reserved
	0x0B		Reserved
	0x0C	LED control	LEDMap1
	0x0D		LEDMap2
	0x0E		LEDPwmFreq
	0x0F		LEDMode
	0x10		LEDIdle
	0x11		LEDOffDelay
	0x12		LED1On
	0x13		LED1Fade
	0x14		LED2On
	0x15		LED2Fade
	0x16		LEDPwrIdle
	0x17		LEDPwrOn

	Address		Name
"NVM" area	0x38	Cap sensing	CapSenseStuck
	0x39		CapSenseFrameSkip
	0x3A		CapSenseMisc
	0x3B		ProxCombChanMask
	0x3C		Reserved
	0x3D		Reserved
	0x3E	Special output	SPOChanMap
	0x3F		SPOLevelBL0
	0x40		SPOLevelBL1
	0x41		SPOLevelBL2
	0x42		SPOLevelBL3
	0x43		SPOLevelBL4
	0x44		SPOLevelBL5
	0x45		SPOLevelBL6
	0x46		SPOLevelBL7
	0x47		SPOLevelIdle
	0x48		SPOLevelProx
	0x49		Reserved
	0x4A		Reserved
	0x4B	Buzzer	BuzzerTrigger
	0x4C		BuzzerFreq
	0x4D		Reserved
	0x4E	IR	IRAddressOffset
	0x4F		IRCommandOffset

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	0x18		LEDPwrOff
	0x19		LEDPwrFade
	0x1A		LEDPwrOnPw
	0x1B		LEDPwrMode
	0x1C		Reserved
	0x1D		Reserved
	0x1E	Cap sensing	CapSenseEnable
	0x1F		CapSensRange0
	0x20		CapSenseRange1
	0x21		CapSenseRange2
	0x22		CapSenseRange3
	0x23		CapSenseRange4
	0x24		CapSenseRange5
	0x25		CapSenseRange6
	0x26		CapSenseRange7
	0x27		CapSenseRangeAll
	0x28		CapSenseThresh0
	0x29		CapSenseThresh1
	0x2A		CapSenseThresh2
	0x2B		CapSenseThresh3
	0x2C		CapSenseThresh4
	0x2D		CapSenseThresh5
	0x2E		CapSenseThresh6
	0x2F		CapSenseThresh7
	0x30		CapSenseThreshComb
	0x31		CapSenseOp
	0x32		CapSenseMode
	0x33		CapSenseDebounce
	0x34		CapSenseNegCompThresh
	0x35		CapSensePosCompThresh
	0x36		CapSensePosFilt
	0x37		CapSenseNegFilt

	0x50		IRHeaderMarkWidth
	0x51		IRHeaderSpaceWidth
	0x52		IRMarkWidth
	0x53		IRSpaceWidth0
	0x54		IRSpaceWidth1
	0x55		IRSize
	0x56		IRAddressMsb
	0x57		IRAddressLsb
	0x58		IRCommand0
	0x59		IRCommand1
	0x5A		IRCommand2
	0x5B		IRCommand3
	0x5C		IRCommand4
	0x5D		IRCommand5
	0x5E		IRCommand6
	0x5F		IRCommand7
	0x60		IRMargin
	0x61		Reserved
	0x62		Reserved
	0x63	Sensor readback	CapSenseChanSelect
	0x64		CapSenseUsefulDataMsb
	0x65		CapSenseUsefulDataLsb
	0x66		CapSenseAverageDataMsb
	0x67		CapSenseAverageDataLsb
	0x68		CapSenseDiffDataMsb
	0x69		CapSenseDiffDataLsb
	0x6A		CapSenseCompMsb
	0x6B		CapSenseCompLsb
	0x6C		Reserved
…			
	0xFE		Reserved
	0xFF		I2CSoftReset

Table 8 Register Map

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4.2 General Control and Status

4.2.1 Interrupt Source

Address	Name	Acc	Bits	Field	Function
0x00	IrqSrc	R/W	7:0	Irq Source	Indicate active Irqs 0 : Irq inactive 1 : Irq active Bit map 7 : Reset 6 : Touch 5 : Release 4 : Near (Prox on) 3 : Far (Prox off) 2 : Compensation done (Write a 1 to this bit to trigger a compensation on all channels) 1 : Reserved, will read 0 0 : Reserved, will read 0

The Irq Source register will indicate that the specified event has occurred since the last read of this register. If the NIRQ function is selected for SPO2 then it will indicate the occurrence of any of these events that are not masked out in register 0x09.

The Irq mask in register 0x09 will prevent an Irq from being indicated by the NIRQ pin but it will not prevent the IRQ from being noted in this register.

4.2.2 Touch Status

Address	Name	Acc	Bits	Field	Function
0x01	TouchStatus	R	7:0	Touch Status	Indicates touch detected on indicated BL channel. Bit 7 = BL7 … Bit 0 = BL0 0 : No touch detected 1 : Touch detected

The Touch Status register will indicate when a touch occurs on one of the BL channels. A touch is indicated when a channels DiffData value goes at least the Hyst value above it's threshold level for debounce number of consecutive measurement cycles. A touch is lost when a channels DiffData value goes at least Hyst value below it's threshold for debounce number of measurement cycles. This is a dynamic read only regester that is not stored in NVM.

Example: BL2 is set to a threshold of 400 (0x21 = 0x19), a Hyst of 8 (0x37 [7:5] = 3'b001), a touch debounce of 0 (0x33 [3:2] = 2'b00) and a release debounce of 2 (0x33 [1:0] = 2'b01).

A touch will be indicated the first measurement cycle that the DiffData goes above 408 and the touch will be lost when the DiffData value goes below 392 on two successive measurement cycles.

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4.2.3 Proximity Status

Address	Name	Acc	Bits	Field	Function
0x02	ProxStatus	R	7	ProxBL0	Indicates proximity detected on BL0 0 : No Proximity detected 1 : Proximity detected (if Prox on BL0 enabled (0x31[6]))
		R	6	ProxMulti	Indicates proximity detected on combined channels 0 : No Proximity detected 1 : Proximity detected (if Prox on combined channels enabled (0x31[5]) and channels enabled for use (0x3B))
		R	5	ProxMulti Comp Pending	Indicates compensation pending for combined channel Prox sensing 0 : Compensation not pending 1 : Compensation pending (if Prox on combined channels enabled (0x31[5]) and channels enabled for use (0x3B))
		R	4:0	Reserved	Reserved, will read 00000

The ProxBL0 bit will indicate Proximity detected on the BL0 pin, The ProxMulti bit will indicate proximity on the Combined Channels and the ProxMulti Comp Pending bit will indicate that a compensation has been requested for the Combined Channels and is pending. (for SX9510 and if enabled),

4.2.4 Compensation Status

Address	Name	Acc	Bits	Field	Function
0x03	CompStatus	R	7:0	Comp Pending	Indicates compensation pending on indicated BL channel. Bit 7 = BL7 … Bit 0 = BL0 0 : Compensation not pending 1 : Compensation pending

The Comp Pending register indicates which pins from BL0 to BL7 have compensations requested and pending.

4.2.5 NVM Control

Address	Name	Acc	Bits	Field	Function
0x04	NVMCtrl	R/W	7:4	NVM Burn	Write 0x50 followed by 0xA0 to initiate transfer of reg 0x07 through 0x70 to NVM
		R/W	3	NVM Read	Trigger NVM read. 0 : Do nothing 1 : Read contents of current active NVM area into registers
		R	2:0	NVM Area	Indicates current active NVM area 000 : no areas are programmed. 001 : User1 area is programmed and in use. 011 : User2 area is programmed and in use. 111 : User3 area is Programmed and in use.

The NVM Area field indicates which of the user NVM areas are currently programmed and active (1, 2 or 3). The NVM Read bit gives the ability to manually request that the contents of the NVM be transferred to the registers and NVM Burn field gives the ability to burn the current registers to the next available NVM area.

Normally, the transfer of data from the NVM to the registers is done automatically on power up and upon a reset but occasionally a user might want to force a read manually.

Registers 0x07 through 0x60 are stored to NVM and loaded from NVM.

Caution, there are only three user areas and attempts to burn values beyond user area 3 will be ignored.

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4.2.6 SPO2 Mode Control

Address	Name	Acc	Bits	Field	Function
0x07	Spo2Mode	R/W	7	Reserved	Reserved, set to 0
		R/W	6:5	SPO2 Config	Set function of SPO2 pin 00 : Pin is open drain NIRQ 01 : Pin drives Buzzer (see registers 0x4B and 0x4C) 10 : Pin is Analog Output 2 11 : TV Power State input (see registers 0x07[4] and 0x1B[7])
		R/W	4	TV Power State	If SPO2 set to TV Power State input then TV power state indicated by this bit, if SPO2 set to other function then Host writes this bit to indicate current TV Power State. 0 : Off 1 : On
		R/W	3:0	Reserved	Reserved, set to 0000

The SPO2 Config field will specify the functionality of the SPO pin. When selected as NIRQ, the open drain output will go low whenever a non-masked Irq occurs and the NIRQ will go back high after a register 0x00 is read over the I2C. When selected as Buzzer, the SPO2 pin will drive a 2 phase 2 frequency signal onto an external buzzer for each specified event (see Buzzer section). When selected as SPO2, pin operates as an analog output similar to SPO1 (see SPO section). If selected as TV power state, the pin is driven from the system PMIC with a high (SPO2 = SVDD) indicating that the system power is on and a low (SPO2 = GND) when the system power is off.

The TV Power State bit reads back the current state of SPO2 if SPO2 is selected for TV power state, otherwise the system should write to this bit to indicate the current system power state. The SX9510/11 needs to know the current state in able to correctly process some of the LED modes for the Power Button (see LED modes).

4.2.7 Power Key Control (for generation of PWRON signal)

Address	Name	Acc	Bits	Field	Function
0x08	PwrKey	R/W	7:0	Power Keys	Set which BL sensors will trigger a PowerOn pulse when touched. Bit 7 = BL7 … Bit 0 = BL0 0 : Do not use channel 1 : Use channel If BL7 is enabled (0x1B[1]), it will be the main power button with respect to power button LED functions (see reg 0x16 through 0x1B)

The Power Keys field is a map that indicates which of the BL0 through BL7 channels should trigger a pulse on the PWRON pin when touched. This should not be confused with the BL7 Power Key enable bit as described in register 0x1B.

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4.2.8 Interrupt Request Mask

Address	Name	Acc	Bits	Field	Function
0x09	IrqMask	R/W	7:0	Irq Mask	Set which Irqs will be trigger an NIRQ (if enabled on SPO2) and report in reg 0x00 0 : Disable Irq 1 : Enable Irq Bit map 7 : Reset 6 : Touch 5 : Release 4 : Near (Prox on) 3 : Far (Prox off) 2 : Compensation done 1 : Reserved, set to 0 0 : Reserved, set to 0

The Irq Mask field determines which Irq events will trigger an NIRQ signal on SPO2 if SPO2 is set to the NIRQ function.

4.2.9 I2C Soft Reset

Address	Name	Acc	Bits	Field	Function
0xFF	I2CSoftReset	W	7:0	I2C Soft Reset	Write 0xDE followed by 0x00 to reset

Trigger a device reset and NVM re-load by writing 0xDE followed by 0x00 to this register.

4.3 LED Control

4.3.1 LED Map for Engine 1 and 2

Address	Name	Acc	Bits	Field	Function
0x0C	LEDMap1	R/W	7:0	LED Engine Map 1	Assign indicated BL channel to LED engine 1 Bit 7 = BL7 … Bit 0 = BL0 0 : Do not assign to LED engine 1 1 : Assign to LED engine 1
0x0D	LEDMap2	R/W	7:0	LED Engine Map 2	Assign indicated BL channel to LED engine 2 Bit 7 = BL7 … Bit 0 = BL0 0 : Do not assign to LED engine 2 1 : Assign to LED engine 2

Write a 1 for each bit (7 through 0) into the LED Engine Map 1 field for each channel (BL7 through BL0) that will be driven by LED Engine 1.
Write a 1 for each bit (7 through 0) into the LED Engine Map 2 field for each channel (BL7 through BL0) that will be driven by LED Engine 2.

In most cases each BL channel will only be assigned to one of the engines but there are some rare cases where a channel will be assigned to both.

4.3.2 LED PWM Frequency

Address	Name	Acc	Bits	Field	Function
0x0E	LEDPwmFreq	R/W	7:0	LED PWM Frequency	LEDPWMfreq = 2MHz / n

The LED PWM frequency is derived from the 2MHz oscillator and is the primary method for controlling the BL7 through BL0 frame scanning rate as well as impacting the maximum brightness achievable on each LED and impacting the smoothness of the LED illumination (flicker prevention).

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As displayed in Figure 6, the CapSense measurements and LED PWM drive is time multiplexed. The CapSense measurement time is nominally 648us and the LED PWM time is 255 LED clocks long. The LED refresh frequency must be above 50/60Hz to ensure that there is not a noticeable flicker on the LEDs. So we have:

LED max brightness = 255/(648us * LEDPwmFreq + 255)
LED refresh frequency = 1 / (648us + 255/LEDPwmFreq)

4.3.3 LED Mode

Address	Name	Acc	Bits	Field	Function
0x0F	LEDMode	R/W	7:4	LED Fade Repeat	Set number of fade in/out repeats when in LED Repeat X low and Repeat X high modes (see reg 0x0F[1:0])
		R/W	3	Reserved	Reserved, set to 0
		R/W	2	LED Fading	Set LED fade in and fade out type 0 : linear 1 : log
		R/W	1:0	LED Mode	Set LED mode of operation 00 : Single shot 01 : Repeat continuous 10 : Repeat X low 11 : Repeat X high

4.3.4 LED Idle Level

Address	Name	Acc	Bits	Field	Function
0x10	LEDIdle	R/W	7:0	LED Engine 1 & 2 Idle Level	Set LED engine 1 and LED engine 2 idle intensity level.

4.3.5 LED Off Delay

Address	Name	Acc	Bits	Field	Function
0x11	LEDOffDelay	R/W	7:4	LED Engine 1 Delay Off Time	Set time delay from loss of touch/prox to start of fade out. Delay = n * 256ms
		R/W	3:0	LED Engine 2 Delay Off Time	Set time delay from loss of touch/prox to start of fade out. Delay = n * 256ms

4.3.6 LED Engine 1 On Level

Address	Name	Acc	Bits	Field	Function
0x12	LED1On	R/W	7:0	LED Engine 1 on Level	Set LED engine 1 on intensity level.

4.3.7 LED Engine 1 Fade In/Out Timing

Address	Name	Acc	Bits	Field	Function
0x13	LED1Fade	R/W	7:4	LED engine 1 Fade In Time	Set time per intensity step when changing from idle to on, idle to prox or prox to on states. StepTime = (n + 1) * 500us The total time required to change from one level to another will be: ChangeTime = abs(CurrLevel - NewLevel) * StepTime

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		R/W	3:0	LED engine 1 Fade Out Time	Set time per intensity step when changing from on to idle, on to prox or prox to idle states. StepTime = (n + 1) * 500us The total time required to change from one level to another will be: ChangeTime = abs(CurrLevel - NewLevel) * StepTime

4.3.8 LED Engine 2 On Level

Address	Name	Acc	Bits	Field	Function
0x14	LED2On	R/W	7:0	LED Engine 2 on Level	Set LED engine 2 on intensity level.

4.3.9 LED Engine 2 Fade In/Out Timing

Address	Name	Acc	Bits	Field	Function
0x15	LED2Fade	R/W	7:4	LED engine 2 Fade In Time	Set time per intensity step when changing from idle to on, idle to prox or prox to on states. StepTime = (n + 1) * 500us The total time required to change from one level to another will be: ChangeTime = abs(CurrLevel - NewLevel) * StepTime
		R/W	3:0	LED engine 2 Fade Out Time	Set time per intensity step when changing from on to idle, on to prox or prox to idle states. StepTime = (n + 1) * 500us The total time required to change from one level to another will be: ChangeTime = abs(CurrLevel - NewLevel) * StepTime

4.3.10 LED Power Button Idle Level

Address	Name	Acc	Bits	Field	Function
0x16	LEDPwrIdle	R/W	7:0	Power Button LED Idle Level	Set Power button LED engine idle intensity level.

4.3.11 LED Power Button On Level

Address	Name	Acc	Bits	Field	Function
0x17	LEDPwrOn	R/W	7:0	Power Button LED On Level	Set Power button LED engine on intensity level.

4.3.12 LED Power Button Off Level

Address	Name	Acc	Bits	Field	Function
0x18	LEDPwrOff	R/W	7:0	Power Button LED Off Level	Set Power button LED engine off intensity level.

4.3.13 LED Power Button Fade In/Out Timing

Address	Name	Acc	Bits	Field	Function
0x19	LEDPwrFade	R/W	7:0	Power Button Fade In/Out Time	Set time per intensity step when changing from one level to another. StepTime = (n + 1) * 250us The total time required to change from one level to another will be: ChangeTime = abs(CurrLevel - NewLevel) * StepTime

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4.3.14 Power-On Pulse width

Address	Name	Acc	Bits	Field	Function
0x1A	LEDPwrOnPw	R/W	7:0	Power On Pulse Width	Set the duration of both the power on pulse driven on the PWRON pin and the power LED on time in breath idle power mode. PowerOnPw = (n + 1) * 1ms The power on pulse is triggered by either the power button (if power button enabled (0x1B[1])) or by an IR power event (if IR enabled (0x4E through 0x60))

4.3.15 LED Power Button Mode

Address	Name	Acc	Bits	Field	Function
0x1B	LEDPwrMode	R/W	7	Power LED Off Mode	Enable off sequence based on TV power state (0x07[4]) 0 : Switch from idle to breathing 1 : Switch from idle (0x16) to Power LED max (0x1B[5] and 0x17) for Power On PW time (0x1A) before switching to breathing if TV Power State = 1 (0x07[4])
		R/W	6	Power LED Max Level	Set Power LED max level to be used during power up and power down sequences 0 : Max set to Power Button LED On Level 1 : Max set to 255
		R/W	5	Power LED Breath Max	Set which level to use as high level while breathing 0 : Breathing swings between LED power button off level (0x18) and LED power button idle level (0x16) 1 : Breathing swings between LED power button off level (0x18) and LED power button on level (0x17)
		R/W	4	Power LED Waveform	Set Power LED waveform type 0 : Breath idle mode, power LED goes from idle to breathing, breathes for Power On Pw time and then goes back to idle 1 : Breath idle mode, power LED goes from breathing to Power LED max for Power On Pw time and then goes to idle
		R/W	3	Power LED IR Reporting PW	Set power LED pulse width when reporting valid IR signals 0 : 32ms 1 : 128ms
		R/W	2	Power LED IR Reporting EN	Enable the reporting of valid IR signals by flashing the power LED 0 : No IR reporting 1 : Report IR commands
		R/W	1	Power Button EN	Enable BL7 as power button 0 : BL7 is normal button 1 : BL7 is power button
		R/W	0	LED Touch Polarity Invert	Invert the polarity of the LED touch on level 0 : LED on level = programmed on level 1 : LED on level = 255 - programmed on level Effects touch on level only, not idle or prox levels.

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4.4 CapSense Control

4.4.1 CapSense Enable

Address	Name	Acc	Bits	Field	Function
0x1E	CapSenseEnable	R/W	7:0	Cap Sense EN	Set which BL sensors are enabled Bit 7 = BL7 … Bit 0 = BL0 0 : Disabled 1 : Enabled

4.4.2 CapSense 0 through 7 (and Combined Channel Mode) Delta Cin range and LS Control

Address	Name	Acc	Bits	Field	Function
0x1F	CapSensRange0	R/W	7:6	LS Control	LS usage during measurements for BL0 00 : LS high-Z (off) 01 : dynamically driven with measurement signal (preferred) 10 : LS tied to GND 11 : LS tied to an internal Vref
		R/W	5:2	Reserved	Reserved, set to 0000
		R/W	1:0	Delta Cin Range	For BL0 00 : +/-7pF 01 : +/-3.5pF 10 : +/-2.8pF 11: +/-2.3pF
0x20	CapSenseRange1	R/W	7:0		Same as CapSensRange0 but for BL1
0x21	CapSenseRange2	R/W	7:0		Same as CapSensRange0 but for BL2
0x22	CapSenseRange3	R/W	7:0		Same as CapSensRange0 but for BL3
0x23	CapSenseRange4	R/W	7:0		Same as CapSensRange0 but for BL4
0x24	CapSenseRange5	R/W	7:0		Same as CapSensRange0 but for BL5
0x25	CapSenseRange6	R/W	7:0		Same as CapSensRange0 but for BL6
0x26	CapSenseRange7	R/W	7:0		Same as CapSensRange0 but for BL7
0x27	CapSenseRangeAll	R/W	7:0		Same as CapSensRange0 but for combined channels used as a prox sensor

4.4.3 CapSense 0 through 7 (and Combined Channel Mode) Detection Threshold

Address	Name	Acc	Bits	Field	Function
0x28	CapSenseThresh0	R/W	7:0	Touch Detection Threshold BL0	Set the touch/prox detection threshold for BL0. Threshold = n * 16
0x29	CapSenseThresh1	R/W	7:0	Touch Detection Threshold BL1	Same as CapSenseThresh0 but for BL1
0x2A	CapSenseThresh2	R/W	7:0	Touch Detection Threshold BL2	Same as CapSenseThresh0 but for BL2
0x2B	CapSenseThresh3	R/W	7:0	Touch Detection Threshold BL3	Same as CapSenseThresh0 but for BL3
0x2C	CapSenseThresh4	R/W	7:0	Touch Detection Threshold BL4	Same as CapSenseThresh0 but for BL4
0x2D	CapSenseThresh5	R/W	7:0	Touch Detection Threshold BL5	Same as CapSenseThresh0 but for BL5
0x2E	CapSenseThresh6	R/W	7:0	Touch Detection Threshold BL6	Same as CapSenseThresh0 but for BL6
0x2F	CapSenseThresh7	R/W	7:0	Touch Detection Threshold BL7	Same as CapSenseThresh0 but for BL7
0x30	CapSenseThreshComb	R/W	7:0	Touch Detection Threshold Combined	Same as CapSenseThresh0 but for combined channels used as a prox sensor

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4.4.4 CapSense Auto Compensation, Proximity on BL0 and Combined Channels Proximity Enable

Address	Name	Acc	Bits	Field	Function
0x31	CapSenseOp	R/W	7	Auto Compensation	0 : Enable automatic compensation 1 : Disable automatic compensation
		R/W	6	Proximity BL0	0 : BL0 is normal button 1 : BL0 is proximity sensor
		R/W	5	Proximity Combined Channels	0 : Do not use combined channels for proximity sensing 1 : Use combined channels (0x3B) for proximity sensing
		R/W	4:0	Reserved	Reserved, set to 10100

4.4.5 CapSense Raw Data Filter Coef, Digital Gain, I2C touch reporting and CapSense reporting

Address	Name	Acc	Bits	Field	Function
0x32	CapSenseMode	R/W	7:5	Raw Filter	filter coefficient to turn raw data into useful data 000 : off 001 : 1-1/2 010 : 1-1/4 011 : 1-1/8 100 : 1-1/16 101 : 1-1/32 110 : 1-1/64 111 : 1-1/128
		R/W	4	Touch Reporting (I2C)	Set which touches will be reported in Touch Status (0x01) 0 : Report touches according to CapSense Report Mode (0x32[1:0]) 1 : Report all touches
		R/W	3:2	CapSense Digital Gain	Set digital gain factor 00 : No gain, Delta Cin Range = Delta Cin Range 01 : X2 gain, Delta Cin Range = Delta Cin Range / 2 10 : X4 gain, Delta Cin Range = Delta Cin Range / 4 11 : X8 gain, Delta Cin Range = Delta Cin Range / 8 Delta Cin outside of range will saturate.
		R/W	1:0	CapSense Report Mode	Set mode for Reporting touches on LEDs (and in reg 0x01 if 0x32[4] = 0) 00 : Single, only report the first touch 01 : Strongest, report the strongest touch 10 : Double, report the first touch for a BL assigned to LED engine 1 and the first touch for a BL assigned to LED engine 2 11 : Double LED, report the first two touches for each LED engine but the second touch goes directly from idle to on or on to idle with no fading Note: When prox detection is enabled, LED engine 1 is dedicated to the prox function and that limits these modes to LED engine 2.

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4.4.6 CapSense Debounce

Address	Name	Acc	Bits	Field	Function
0x33	CapSenseDebounce	R/W	7:6	CapSense Prox Near Debounce	Set number of consecutive samples that proximity detection must be true before proximity is indicated on LEDs and in register 0x02 00 : Debouncer off, proximity indicated on first sample 01 : 2 samples 10 : 4 samples 11 : 8 samples
		R/W	5:4	CapSense Prox Far Debounce	Set number of consecutive samples that proximity detection must be false before los of proximity is indicated on LEDs and in register 0x02 00 : Debouncer off, loss of proximity indicated on first sample 01 : 2 samples 10 : 4 samples 11 : 8 samples
		R/W	3:2	CapSense Touch Debounce	Set number of consecutive samples that touch detection must be true before touch is indicated on LEDs and in register 0x01 00 : Debouncer off, touch indicated on first sample 01 : 2 samples 10 : 4 samples 11 : 8 samples
		R/W	1:0	CapSense Release Debounce	Set number of consecutive samples that touch detection must be false before release is indicated on LEDs and in register 0x01 00 : Debouncer off, release indicated on first sample 01 : 2 samples 10 : 4 samples 11 : 8 samples

4.4.7 CapSense Negative Auto Compensation Threshold

Address	Name	Acc	Bits	Field	Function
0x34	CapSenseNegCompThresh	R/W	7:0	CapSense Neg Comp Thresh	Set negative level that average data must cross before triggering a negative drift auto compensation. Threshold = n * 128

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4.4.8 CapSense Positive Auto Compensation Threshold

Address	Name	Acc	Bits	Field	Function
0x35	CapSensePosCompThresh	R/W	7:0	CapSense Pos Comp Thresh	Set positive level that average data must cross before triggering a positive drift auto compensation. Threshold = n * 128

4.4.9 CapSense Positive Filter Coef, Positive Auto Compensation Debouce and Proximity Hyst

Address	Name	Acc	Bits	Field	Function
0x36	CapSensePosFilt	R/W	7:5	CapSense Prox Hyst	Set Proximity detection/loss hysteresis 000 : 2 001 : 8 010 : 16 011 : 32 100 : 64 101 : 128 110 : 256 111 : 512 Prox detection when Delta Data >= (Prox Thresh + Prox Hyst), Prox lost when Delta Data <= (Prox Thresh - Prox Hyst)
		R/W	4:3	CapSense Pos Comp Debounce	Set number of consecutive samples that average data is above the positive compensation threshold before a compensation is triggered 00 : Debouncer off, compensation triggered on first sample 01 : 2 samples 10 : 4 samples 11 : 8 samples
		R/W	2:0	CapSense Ave Pos Filt Coef	Set filter coefficient for turning positive useful data into average data 000 : Off, no averaging of positive data 001 : 1-1/2 010 : 1-1/4 011 : 1-1/8 100 : 1-1/16 101 : 1-1/32 (suggested) 110 : 1-1/64 111 : 1-1/128

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4.4.10 CapSense Negative Filter Coef, Negative Auto Compensation Debounce and Touch Hyst

Address	Name	Acc	Bits	Field	Function
0x37	CapSenseNegFilt	R/W	7:5	CapSense Touch Hyst	Set touch detection/loss hysteresis 000 : 2 001 : 8 010 : 16 011 : 32 100 : 64 101 : 128 110 : 256 111 : 512 Touch detection when Delta Data >= (Touch Thresh + Touch Hyst), Touch lost when Delta Data <= (Touch Thresh - Touch Hyst)
		R/W	4:3	CapSense Neg Comp Debounce	Set number of consecutive samples that average data is below the negative compensation threshold before a compensation is triggered 00 : Debouncer off, compensation triggered on first sample 01 : 2 samples 10 : 4 samples 11 : 8 samples
		R/W	2:0	CapSense Ave Neg Filt Coef	Set filter coefficient for turning negative useful data into average data 000 : Off, no averaging of positive data 001 : 1-1/2 010 : 1-1/4 (suggested) 011 : 1-1/8 100 : 1-1/16 101 : 1-1/32 110 : 1-1/64 111 : 1-1/128

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4.4.11 CapSense Stuck-at Timer and Periodic Compensation Timer

Address	Name	Acc	Bits	Field	Function
0x38	CapSenseStuck	R/W	7:4	CapSense Stuck at Timer	Set stuck at timeout timer. If touch lasts longer than timer, touch is disqualified and a compensation is triggered. 0000 : Off 00bb : Timeout = bb * FrameTime * 64 01bb : Timeout = bb * FrameTime * 128 1bbb : Timeout = bbb * FrameTime * 256 FrameTime = (CapSense time + LED Frame time) * 9 CapSense time = 648us LED Frame time = 255 / LED Frequency (0x0E)
		R/W	3:0	CapSense Periodic Comp	Set periodic compensation interval 0000 : Off, no periodic compensations bbbb : Periodic compensation triggered every bbbb * 128 frames FrameTime = (CapSense time + LED Frame time) * 9 CapSense time = 648us LED Frame time = 255 / LED Frequency (0x0E)

4.4.12 CapSense Frame Skip setting fro Active and Sleep

Address	Name	Acc	Bits	Field	Function
0x39	CapSenseFrameSkip	R/W	7:4	CapSense Active Frame Skip	Set number of frames to skip measuring BL pins between frames that do measure the BL pins in active mode. Timing and LED drive remains constant. Frames to skip = n
		R/W	3:0	CapSense Sleep Frame Skip	Set number of frames to skip measuring BL pins between frames that do measure the BL pins in sleep mode. Timing and LED drive remains constant. Frames to skip = n * 4

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4.4.13 CapSense Sleep Enable, Auto Compensation Channels Threshold, Inactive BL Control

Address	Name	Acc	Bits	Field	Function
0x3A	CapSenseMisc	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:4	Comp Chan Num Thresh	Set how many channels must request compensation before a compensation is done on all channels. 00 : Each channel is compensated individually when compensation is requested for that channel bb : Compensation for all channels is triggered when bb channels request compensation
		R/W	3	CapSense Sleep Mode Enable	0 : Disable sleep mode 1 : Enable sleep mode
		R/W	2	Reserved	Reserved, set to 0
		R/W	1:0	CapSense Inactive BL Mode	Set what is done with BL pins when other BL pins are being measured. 00 : Inactive BLs are driven to LS levels 01 : Inactive BLs are driven to LS levels 10 : Inactive BLs are HiZ 11 : Inactive BLs are connected to GND

4.4.14 Proximity Combined Channel Mode Channel Mapping

Address	Name	Acc	Bits	Field	Function
0x3B	ProxCombChanMask	R/W	7:0	Prox Combined Chan Mask	Assign indicated BL channel to be used in combined channel mode for proximity detection Bit 7 = BL7 … Bit 0 = BL0 0 : Do not use in combined channel mode 1 : Use in combined channel mode

4.5 SPO Control

4.5.1 SPO Channel Mapping

Address	Name	Acc	Bits	Field	Function
0x3E	SPOChanMap	R/W	7:0	SPO Channel Mapping	Assign each BL pin to report touches on either SPO1 or SPO2. Bit 7 = BL7 … Bit 0 = BL0 0 : Report touches on SPO1 1 : Report touches on SPO2

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4.5.2 SPO Analog Output Levels (BL0 through BL7 Touch, Idle and Proximity)

Address	Name	Acc	Bits	Field	Function
0x3F	SPOLevelBL0	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:0	SPO Level BL0	Specify analog output level for BL0 V = (n / 63) * SVDD
0x40	SPOLevelBL1	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:0	SPO Level BL1	Same as SPOLevelBL0 but for BL1
0x41	SPOLevelBL2	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:0	SPO Level BL2	Same as SPOLevelBL0 but for BL2
0x42	SPOLevelBL3	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:0	SPO Level BL3	Same as SPOLevelBL0 but for BL3
0x43	SPOLevelBL4	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:0	SPO Level BL4	Same as SPOLevelBL0 but for BL4
0x44	SPOLevelBL5	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:0	SPO Level BL5	Same as SPOLevelBL0 but for BL5
0x45	SPOLevelBL6	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:0	SPO Level BL6	Same as SPOLevelBL0 but for BL6
0x46	SPOLevelBL7	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:0	SPO Level BL7	Same as SPOLevelBL0 but for BL7
0x47	SPOLevelIdle	R/W	7:6	Reserved	Reserved, set to 00
		R/W	5:0	SPO Level Idle	Specify analog output level for idle V = (n / 63) * SVDD
0x48	SPOLevelProx	R/W	7	SPO Report Prox	Enable reporting of proximity on SPO 0 : Do not report proximity on SPO 1 : Report proximity on SPO
		R/W	6	SPO Prox Channel Mapping	0 : Report proximity on SPO1 1 : Report proximity on SPO2
		R/W	5:0	SPO Level Prox	Specify analog output level for proximity V = (n / 63) * SVDD

4.6 Buzzer Control

4.6.1 Buzzer Trigger Event Selection

Address	Name	Acc	Bits	Field	Function
0x4B	BuzzerTrigger	R/W	7:5	Reserved	Reserved, set to 000
		R/W	4	Buzzer Near	0 : Do not activate buzzer on proximity detection 1 : Activate buzzer on proximity detection
		R/W	3	Buzzer Far	0 : Do not activate buzzer on proximity loss 1 : Activate buzzer on proximity loss
		R/W	2	Buzzer Touch	0 : Do not activate buzzer on touch detection 1 : Activate buzzer on touch detection
		R/W	1	Buzzer Release	0 : Do not activate buzzer on touch release 1 : Activate buzzer on touch release
		R/W	0	Buzzer Idle Level	Set SPO2 pin drive level in buzzer mode when buzzer is not active. 0 : GND 1 : VDD

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4.6.2 Buzzer Duration and Frequency

Address	Name	Acc	Bits	Field	Function
0x4C	BuzzerFreq	R/W	7:6	Buzzer Phase 1 Duration	00 : 5ms 01 : 10ms 10 : 15ms 11 : 30ms
		R/W	5:4	Buzzer Phase 1 Frequency	00 : 1KHz 01 : 2KHz 10 : 4KHz 11 : 8KHz
		R/W	3:2	Buzzer Phase 2 Duration	00 : 5ms 01 : 10ms 10 : 15ms 11 : 30ms
		R/W	1:0	Buzzer Phase 2 Frequency	00 : 1KHz 01 : 2KHz 10 : 4KHz 11 : 8KHz

4.7 IR Control

4.7.1 IR Phase Polarity, Encoding Mode, Header Present and Address Field Offset

Address	Name	Acc	Bits	Field	Function
0x4E	IRAddressOffset	R/W	7	IR Phase Polarity	Defines the polarity of the protocol. 0 : Normal, 0 = [Space;Mark], 1 = [Mark;Space] 1 : Inverted, 0 = [Mark;Space], 1 = [Space;Mark]
		R/W	6	IR Encoding Mode	Defines the encoding method. 0 : Phase encoding 1 : Space encoding
		R/W	5	IR Header	Defines if the protocol contains a header. 0 : Yes 1 : No
		R/W	4:0	IR Address Offset	Defines the number of received bits to ignore before considering the start of the address field.

4.7.2 IR Speed, Command Field Offset and Power LED IR Reporting Mode

Address	Name	Acc	Bits	Field	Function
0x4F	IRCommandOffset	R/W	7	Reserved	Reserved, set to 0
		R/W	6	IR Activity Report Mode	Defines the match condition to flash the Power LED (Cf. 0x1B[3:2]) 0 : Address and Command 1 : Address only
		R/W	5	IR Speed	Defines the base clock period for all IR width definitions/calculations: 0 : Fast, 8us 1 : Slow, 128us
		R/W	4:0	IR Command Offset	Defines the number of received bits to ignore before considering the start of the command field.

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4.7.3 IR Header Mark Width

Address	Name	Acc	Bits	Field	Function
0x50	IRHeaderMarkWidth	R/W	7:0	IR Header Mark Width	Defines the width/duration of the header mark. Width = n * 16 * IR Speed

4.7.4 IR Header Space Width

Address	Name	Acc	Bits	Field	Function
0x51	IRHeaderSpaceWidth	R/W	7:0	IR Header Space Width	Defines the width/duration of the header space. Width = n * 16 * IR Speed

4.7.5 IR Data Mark Width

Address	Name	Acc	Bits	Field	Function
0x52	IRMarkWidth	R/W	7:0	IR Data Mark Width	Defines the width/duration of the data mark. Width = n * IR Speed

4.7.6 IR Data Space Width for Logic 0

Address	Name	Acc	Bits	Field	Function
0x53	IRSpaceWidth0	R/W	7:0	IR Data Space Width 0	Defines the width/duration of the data space for logic 0. Width = n * IR Speed

In phase encoding mode, must be set to same value as IR Data Mark Width.

4.7.7 IR Data Space Width for Logic 1

Address	Name	Acc	Bits	Field	Function
0x54	IRSpaceWidth1	R/W	7:0	IR Data Space Width 1	Defines the width/duration of the data space for logic 1. Width = n * IR Speed

In phase encoding mode, must be set to same value as IR Data Mark Width.

4.7.8 IR Word Order, Address Field Size and Command Field Size

Address	Name	Acc	Bits	Field	Function
0x55	IRSize	R/W	7	IR Word Order	Defines the order in which address and commands fields are expected: 0 : Address , Command 1 : Command , Address
		R/W	6:4	IR Command Size	Defines the size of the command in number of bits Size = n + 1
		R/W	3:0	IR Address Size	Defines the size of the address in number of bits Size = n + 1

4.7.9 IR Address MSB and LSB

Address	Name	Acc	Bits	Field	Function
0x56	IRAddressMsb	R/W	7:0	IR Address Msb	Defines the address expected from the matching remote control.
0x57	IRAddressLsb	R/W	7:0	IR Address Lsb	

Upper bits of the concatenated registers will be ignored if needed as defined in IR Address Size.

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4.7.10 IR Commands 0 through 7

Address	Name	Acc	Bits	Field	Function
0x58	IRCommand0	R/W	7:0	IR Command 0	Define the commands which will trigger PWRON pulse. If less than 8 commands are needed, the unused ones should be set to Command 0.
0x59	IRCommand1	R/W	7:0	IR Command 1	
0x5A	IRCommand2	R/W	7:0	IR Command 2	
0x5B	IRCommand3	R/W	7:0	IR Command 3	
0x5C	IRCommand4	R/W	7:0	IR Command 4	
0x5D	IRCommand5	R/W	7:0	IR Command 5	
0x5E	IRCommand6	R/W	7:0	IR Command 6	
0x5F	IRCommand7	R/W	7:0	IR Command 7	

Upper bits of the all registers will be ignored if needed as defined in IR Command Size.

4.7.11 IR Margin

Address	Name	Acc	Bits	Field	Function
0x60	IRMargin	R/W	7:4	Reserved	Reserved, set to 0000
		R/W	3:0	IR Margin	Defines the IR timing margin. All IR width timings are tested against specified values +/- IR Margin. Margin for header = n * 16 * IR Speed Margin for data= n * IR Speed Recommended value is 0x0F.

4.8 Real Time Sensor Data Readback

4.8.1 CapSense Channel Select for Readback

Address	Name	Acc	Bits	Field	Function
0x63	CapSenseChanSelect	R	7:4	Reserved	Reserved, will read 0000
		R	3:0	CapSense Chan Select	Set which BL channel data will be present in registers 0x64 through 0x6B 0000 : BL0 … 0111 : BL7 1000 : Combined channel proximity

4.8.2 CapSense Useful Data MSB and LSB

Address	Name	Acc	Bits	Field	Function
0x64	CapSenseUsefulDataMsb	R	7:0	CapSense Useful Data Msb	Selected channel useful data. Signed, 2's complement format
0x65	CapSenseUsefulDataLsb	R	7:0	CapSense Useful Data Lsb	

4.8.3 CapSense Average Data MSB and LSB

Address	Name	Acc	Bits	Field	Function
0x66	CapSenseAverageDataMsb	R	7:0	CapSense Average Data Msb	Selected channel average data. Signed, 2's complement format
0x67	CapSenseAverageDataLsb	R	7:0	CapSense Average Data Lsb	

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4.8.4 CapSense Diff Data MSB and LSB

Address	Name	Acc	Bits	Field	Function
0x68	CapSenseDiffDataMsb	R	7:0	CapSense Diff Data Msb	Selected channel diff data. Signed, 2's complement format
0x69	CapSenseDiffDataLsb	R	7:0	CapSense Diff Data Lsb	

4.8.5 CapSense Compensation DAC Value MSB and LSB

Address	Name	Acc	Bits	Field	Function
0x6A	CapSenseCompMsb	R/W	7:0	CapSense Comp Msb	Offset compensation DAC code. Read : Read the current value from the last compensation for the selected channel Write : Manually set the compensation DAC for the selected channel. When written, the internal DAC code is updated after the write of the LSB reg. MSB and LSB regs should be written in sequence.
0x6B	CapSenseCompLsb	R/W	7:0	CapSense Comp Lsb	

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5 I2C INTERFACE

The I2C implemented on the SX9510/11 is compliant with:
- standard (100kb/s), fast mode (400kb/s)
- slave mode
- 7 bit address (default 0x2B). The default address can be changed in the NVM at address 0x04.

The host can use the I2C to read and write data at any time.

Three types of registers are considered:

- status (read). These registers give information about the status of the capacitive buttons, GPIs, operation modes etc…

- control (read/write). These registers control the soft reset, operating modes, GPIOs and offset compensation.

- REGISTERS gateway (read/write). These registers are used for the communication between host and the REGISTERS. The REGISTERS gateway communication is done typically at power up and is not supposed to be changed when the application is running. The REGISTERS needs to be re-stored each time the SX9510/11 is powered down.
The REGISTERS can be stored permanently in the NVM memory of the SX9510/11. The REGISTERS gateway communication over the I2C at power up is then not required.

The I2C will be able to read and write from a start address and then perform read or writes sequentially, and the address increments automatically.

The supported I2C access formats are described in the next sections.

5.1 I2C Write

The format of the I2C write is given in Figure 38.
After the start condition [S], the slave address (SA) is sent, followed by an eighth bit (‘0’) indicating a Write. The SX9510/11 then acknowledges [A] that it is being addressed, and the master sends an 8 bit Data Byte consisting of the SX9510/11 Register Address (RA). The slave acknowledges [A] and the master sends the appropriate 8 bit Data Byte (WD0). Again the slave acknowledges [A]. In case the master needs to write more data, a succeeding 8 bit Data Byte will follow (WD1), acknowledged by the slave [A]. This sequence will be repeated until the master terminates the transfer with the Stop condition [P].

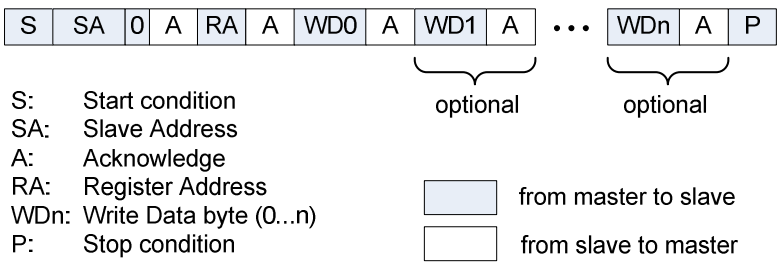


Figure 38 I2C write

The register address is incremented automatically when successive register data (WD1...WDn) is supplied by the master.

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5.2 I2C read

The format of the I2C read is given in Figure 39.
After the start condition [S], the slave address (SA) is sent, followed by an eighth bit ('0') indicating a Write. The SX9510/11 then acknowledges [A] that it is being addressed, and the master responds with an 8 bit data consisting of the Register Address (RA). The slave acknowledges [A] and the master sends the Repeated Start Condition [Sr]. Once again, the slave address (SA) is sent, followed by an eighth bit ('1') indicating a Read.
The SX9510/11 responds with acknowledge [A] and the Read Data byte (RD0). If the master needs to read more data it will acknowledge [A] and the SX9510/11 will send the next read byte (RD1). This sequence can be repeated until the master terminates with a NACK [N] followed by a stop [P].

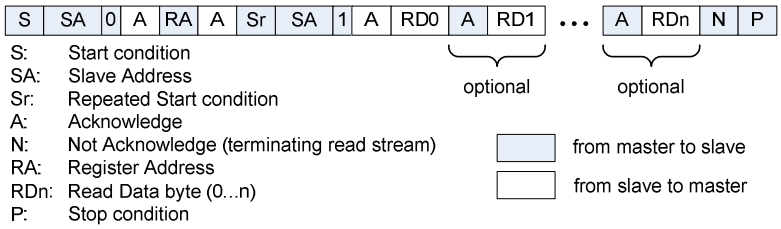


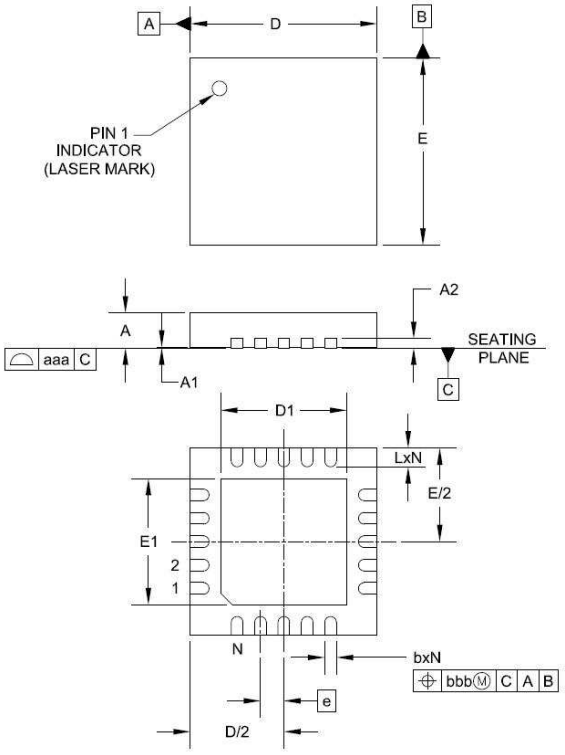
Figure 39 I2C read

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6 PACKAGING INFORMATION

6.1 Package Outline Drawing

SX9510 and SX9511 are assembled in a QFN-20 package as shown in Figure 40 and TSSOP-24 as show in Figure 41.

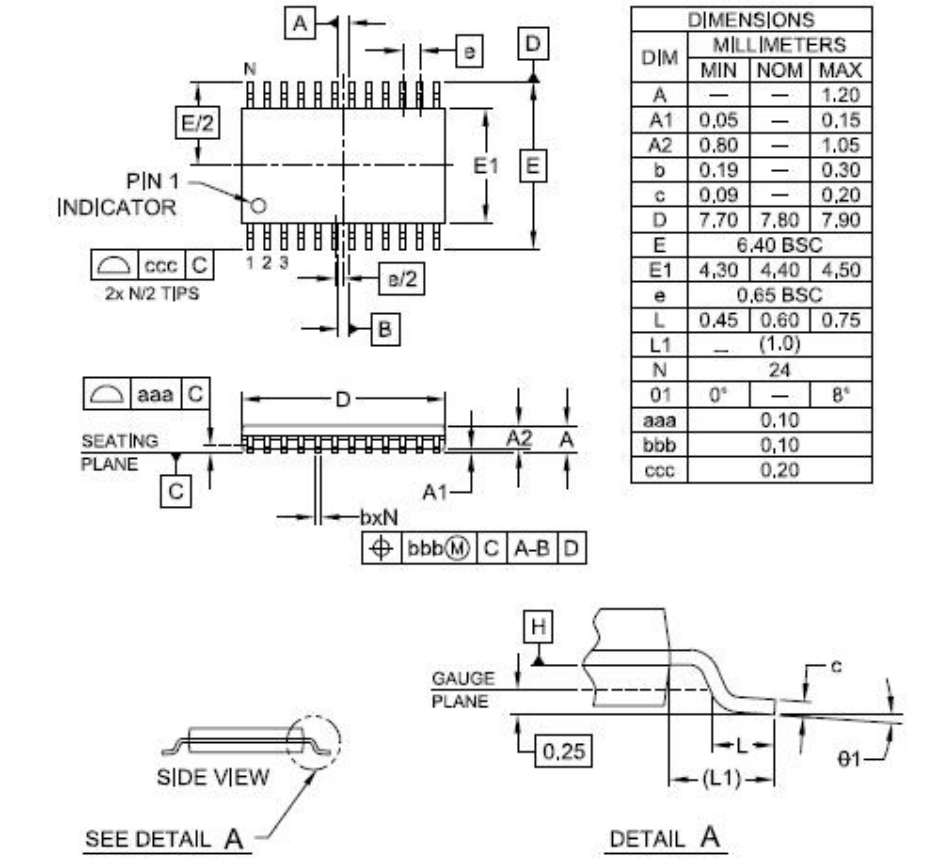


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	-	0.80
A1	0.00	-	0.05
A2	-	(0.20)	-
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D1	2.55	2.70	2.80
E	3.90	4.00	4.10
E1	2.55	2.70	2.80
e	0.50 BSC		
L	0.30	0.40	0.50
N	20		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 40 QFN Package outline drawing

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DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	—	—	1.20
A1	0,05	—	0,15
A2	0,80	—	1,05
b	0,19	—	0,30
c	0,09	—	0,20
D	7,70	7,80	7,90
E		6,40 BSC	
E1	4,30	4,40	4,50
e		0,65 BSC	
L	0,45	0,60	0,75
L1	—	(1,0)	
N		24	
θ1	0°	—	8°
aaa		0,10	
bbb		0,10	
ccc		0,20	

NOTES:

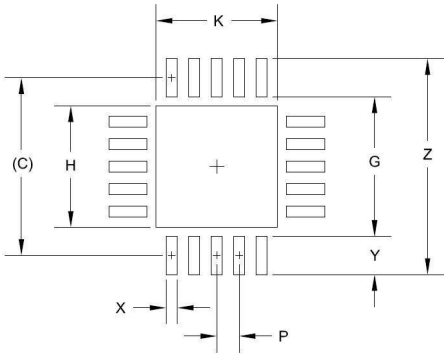
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Figure 41 TSSOP Package outline drawing

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6.2 Land Pattern

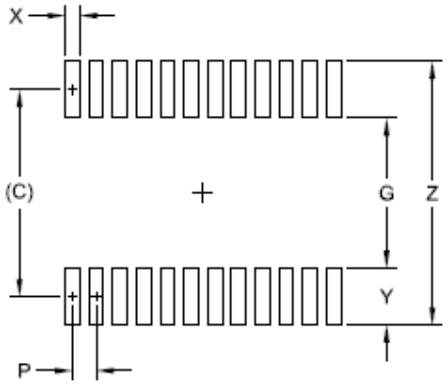
The land pattern of QFN-20 package is shown in Figure 42.
The land pattern of TSSOP-24 package is shown in Figure 43.



DIMENSIONS	
DIM	MILLIMETERS
C	(3.95)
G	3.10
H	2.70
K	2.70
P	0.50
X	0.25
Y	0.85
Z	4.80

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Figure 42 QFN-20 Land Pattern



DIMENSIONS	
DIM	MILLIMETERS
C	(5.65)
G	4.10
P	0.65
X	0.40
Y	1.55
Z	7.20

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSE ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Figure 43 TSSOP-24 Land Pattern

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