# 3-Ω, High Bandwidth, Dual SPDT Analog Switch

## DESCRIPTION

The DG2517, DG2518 are low-voltage dual single-pole/ double-throw monolithic CMOS analog switches. Designed to operate from 1.8 V to 5.5 V power supply, the DG2517, DG2518 achieves a bandwidth of 242 MHz while providing low on-resistance (3 Ω), excellent on-resistance matching (0.2 Ω) and flatness (1 Ω) over the entire signal range.

The DG2517, DG2518 offers the advantage of high linearity that reduces signal distortion, making ideal for audio, video, and USB signal routing applications. Additionally, the DG2517, DG2518 are 1.6 V logic compatible within the full operation voltage range.

Built on Vishay Siliconix's proprietary sub-micron high-density process, the DG2517, DG2518 brings low power consumption at the same time as reduces PCB spacing with the MSOP10 and DFN10 packages.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. The DFN package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix. The MSOP package uses 100 % matte Tin device termination and is represented by the lead (Pb)- free "-E3" suffix. Both the matte Tin and nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL ratings.

## FEATURES

- 1.8 V to 5.5 V single supply operation
- Low $R_{ON}$: 3 Ω at 4.2 V
- 242 MHz, - 3 dB bandwidth
- Low off-isolation, - 51 dB at 10 MHz
- + 1.6 V logic compatible

Pb-free
RoHS COMPLIANT

## BENEFITS

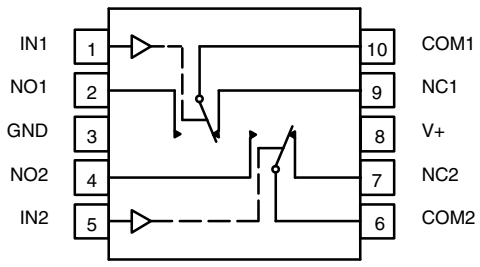
- High linearity
- Low power consumption
- High bandwidth
- Full rail signal swing range

## APPLICATIONS

- USB/UART signal switching
- Audio/video switching
- Cellular phone
- Media players
- Modems
- Hard drives
- PCMCIA

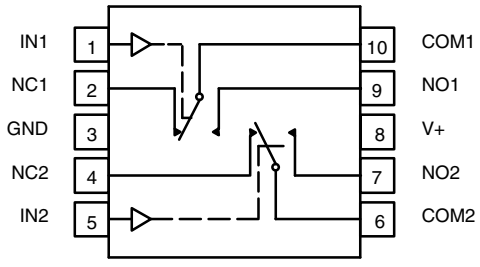
## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG2517**




Top View

**DG2518**




Top View

| TRUTH TABLE | | |
|---|---|---|
| **Logic** | **NC1 and NC2** | **NO1 and NO2** |
| 0 | ON | OFF |
| 1 | OFF | ON |

| ORDERING INFORMATION | | |
|---|---|---|
| **Temp. Range** | **Package** | **Part Number** |
| - 40 °C to 85 °C | MSOP-10 | DG2517DQ-T1-E3 |
| | | DG2518DQ-T1-E3 |
| | DFN-10 | DG2517DN-T1-E4 |
| | | DG2518DN-T1-E4 |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Limit | Unit |
|---|---|---|---|
| **Reference to GND** | | | |
| V+ | | - 0.3 to + 6 | V |
| IN, COM, NC, NO[a] | | - 0.3 to (V+ + 0.3) | |
| Continuous Current (Any terminal) | | ± 50 | mA |
| Peak Current (Pulsed at 1 ms, 10 % duty cycle) | | ± 200 | |
| Storage Temperature (D Suffix) | | - 65 to 150 | °C |
| Power Dissipation (Packages)[b] | MSOP-10[c] | 320 | mW |
| | DFN-10[d] | 1191 | |

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 4.0 mW/°C above 70 °C.
d. Derate 14.9 mW/°C above 70 °C.

## SPECIFICATIONS (V+ = 3 V)

| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, $V_{IN}$ = 0.5 or 1.4 V[e] | | Temp.[a] | Limits - 40 °C to 85 °C Min.[b] | Typ.[c] | Max.[b] | Unit |
|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | |
| Analog Signal Range[d] | $V_{NO}$, $V_{NC}$, $V_{COM}$ | | | Full | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 2.7 V, $V_{COM}$ = 1.5 V, $I_{NO/NC}$ = 10 mA | | Room<br>Full | | 3.2 | 4.5<br>5.0 | Ω |
| $R_{ON}$ Flatness | $R_{ON}$ Flatness | V+ = 2.7 V, $V_{COM}$ = 1.5, 2 V, $I_{NO/NC}$ = 10 mA | | Room<br>Full | | 1.0 | 1.4<br>16 | |
| $R_{ON}$ Match Between Channels | $\Delta R_{ON}$ | V+ = 2.7 V, $V_{COM}$ = 1.5 V, $I_{NO/NC}$ = 10 mA | | Room<br>Full | | 0.1 | 0.3<br>0.4 | |
| Switch Off Leakage Current[f] | $I_{NO(off)}$, $I_{NC(off)}$ | V+ = 3.6 V, $V_{NO}$, $V_{NC}$ = 0.3 V/ 3 V, $V_{COM}$ = 3 V/0.3 V | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | nA |
| | $I_{COM(off)}$ | | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| Channel-On Leakage Current[f] | $I_{COM(on)}$ | V+ = 3.6 V, $V_{NO}$, $V_{NC}$ = $V_{COM}$ = 0.3 V/3 V | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| **Digital Control** | | | | | | | | |
| Input High Voltage[d] | $V_{INH}$ | | | Full | 1.4 | | | V |
| Input Low Voltage | $V_{INL}$ | | | Full | | | 0.5 | |
| Input Capacitance | $C_{in}$ | | | Full | | 4 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | | | Full | 1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | | |
| Turn-On Time | $t_{ON}$ | V+ = 2.7 V, $V_{NO}$ or $V_{NC}$ = 1.5 V, $R_L$ = 300 Ω, $C_L$ = 35 pF | | Room<br>Full | | 15 | 30<br>50 | ns |
| Turn-Off Time | $t_{OFF}$ | | | Room<br>Full | | 10 | 25<br>35 | |
| Break-Before-Make Time | $t_d$ | $V_{NO}$ or $V_{NC}$ = 1.5 V, $R_L$ = 300 Ω, $C_L$ = 35 pF | | Full | 1 | | | |
| Charge Injection[d] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{GEN}$ = 1.5 V, $R_{GEN}$ = 0 Ω | | Room | | 1 | | pC |
| - 3 dB Bandwidth | BW | 0 dBm, $C_L$ = 5 pF, $R_L$ = 50 Ω | | Room | | 242 | | MHz |
| Off-Isolation[d] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF | f = 1 MHz | Room | | - 71 | | dB |
| | | | f = 10 MHz | Room | | - 51 | | |
| Crosstalk[d] | $X_{TALK}$ | $R_L$ = 50 Ω, $C_L$ = 5 pF | f = 1 MHz | Room | | - 73 | | |
| | | | f = 10 MHz | Room | | - 55 | | |
| $N_O$, $N_C$ Off Capacitance[d] | $C_{NO(off)}$ | $V_{IN}$ = 0 or V+, f = 1 MHz | | Room | | 8 | | pF |
| | $C_{NC(off)}$ | | | Room | | 8 | | |
| Channel-On Capacitance[d] | $C_{NO(on)}$ | | | Room | | 35 | | |
| | $C_{NC(on)}$ | | | Room | | 35 | | |
| **Power Supply** | | | | | | | | |
| Power Supply Current | I+ | $V_{IN}$ = 0 or V+ | | Full | | 0.01 | 1.0 | µA |

Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. $V_{IN}$ = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

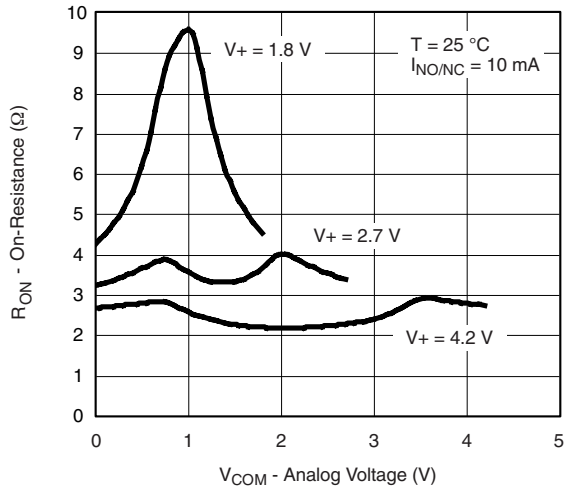
**SPECIFICATIONS** (V+ = 5 V)

| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, $V_{IN}$ = 0.8 or 2.0 V[e] | | Temp.[a] | Limits - 40 °C to 85 °C Min.[b] | Typ.[c] | Max.[b] | Unit |
|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | |
| Analog Signal Range[d] | $V_{NO}$, $V_{NC}$, $V_{COM}$ | | | Full | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 4.2 V, $V_{COM}$ = 3.5 V, $I_{NO/NC}$ = 10 mA | | Room<br>Full | | 3 | 4.0<br>4.3 | Ω |
| $R_{ON}$ Flatness | $R_{ON}$ Flatness | V+ = 4.2 V, $V_{COM}$ = 1, 2, 3.5 V<br>$I_{NO/NC}$ = 10 mA | | Room<br>Full | | 1.1 | 1.4<br>1.6 | |
| $R_{ON}$ Match Between Channels | $\Delta R_{ON}$ | V+ = 4.2 V, $V_{COM}$ = 3.5 V, $I_{NO/NC}$ = 10 mA | | Room<br>Full | | 0.1 | 0.3<br>0.4 | |
| Switch Off Leakage Current | $I_{NO(off)}$, $I_{NC(off)}$ | V+ = 5.5 V<br>$V_{NO}$, $V_{NC}$ = 1 V/4.5 V, $V_{COM}$ = 4.5 V/1 V | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | nA |
| | $I_{COM(off)}$ | | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| Channel-On Leakage Current | $I_{COM(on)}$ | V+ = 5.5 V, $V_{COM}$ = $V_{NO}$, $V_{NC}$ = 1 V/4.5 V | | Room<br>Full | - 1<br>- 10 | | 1<br>10 | |
| **Digital Control** | | | | | | | | |
| Input High Voltage[d] | $V_{INH}$ | | | Full | 2.0 | | | V |
| Input Low Voltage | $V_{INL}$ | | | Full | | | 0.8 | |
| Input Capacitance | $C_{in}$ | | | Full | | 4 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 V or V+ | | Full | 1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | | |
| Turn-On Time | $t_{ON}$ | V+ = 4.2 V, $V_{NO}$ or $V_{NC}$ = 3 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF | | Room<br>Full | | 12 | 25<br>45 | ns |
| Turn-Off Time | $t_{OFF}$ | | | Room<br>Full | | 8 | 20<br>30 | |
| Break-Before-Make Time | $t_d$ | $V_{NO}$ or $V_{NC}$ = 3 V, $R_L$ = 300 Ω, $C_L$ = 35 pF | | Full | 1 | | | |
| Charge Injection[d] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{GEN}$ = 2.5 V, $R_{GEN}$ = 0 Ω | | Room | | 2 | | pC |
| - 3 dB Bandwidth | BW | 0 dBm, $C_L$ = 5 pF, $R_L$ = 50 Ω | | Room | | 242 | | MHz |
| Off-Isolation[d] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF | f = 1 MHz | Room | | - 71 | | dB |
| | | | f = 10 MHz | Room | | - 51 | | |
| Crosstalk[d] | $X_{TALK}$ | $R_L$ = 50 Ω, $C_L$ = 5 pF | f = 1 MHz | Room | | - 73 | | |
| | | | f = 10 MHz | Room | | - 55 | | |
| Source-Off Capacitance[d] | $C_{NO(off)}$ | $V_{IN}$ = 0 or V+, f = 1 MHz | | Room | | 8 | | pF |
| | $C_{NC(off)}$ | | | Room | | 8 | | |
| Channel-On Capacitance[d] | $C_{NO(on)}$ | | | Room | | 35 | | |
| | $C_{NC(on)}$ | | | Room | | 35 | | |
| **Power Supply** | | | | | | | | |
| Power Supply Range | V+ | | | | 1.8 | | 5.5 | V |
| Power Supply Current | I+ | $V_{IN}$ = 0 or V+ | | Full | | 0.01 | 1.0 | µA |

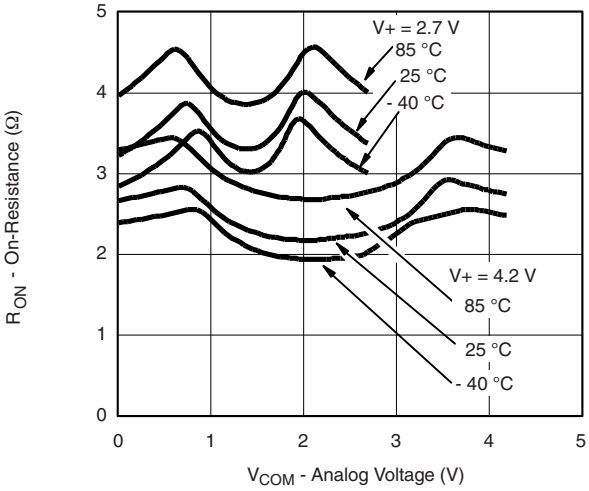
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. $V_{IN}$ = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

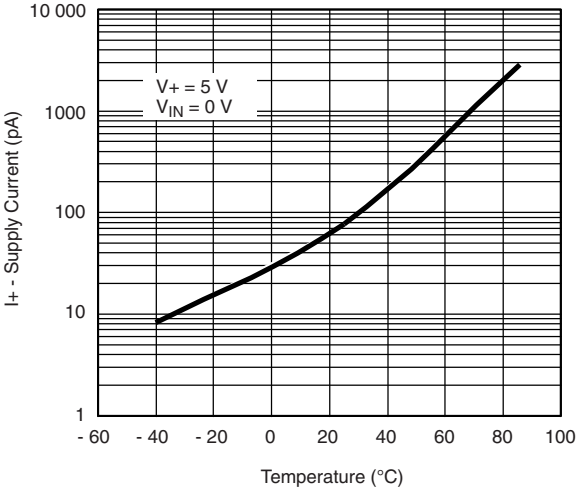
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



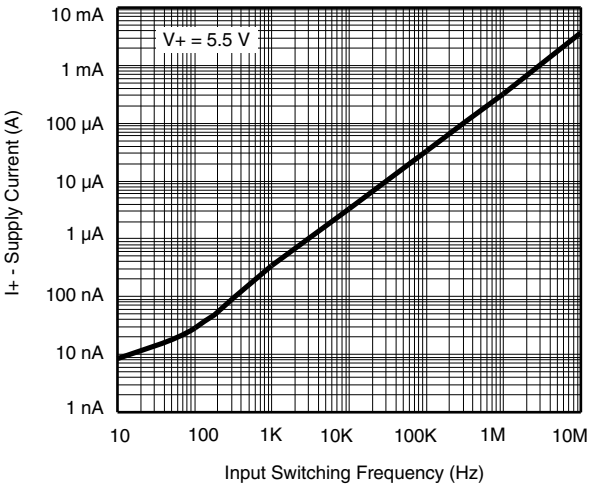

**$R_{ON}$ vs. $V_{COM}$ and Supply Voltage**



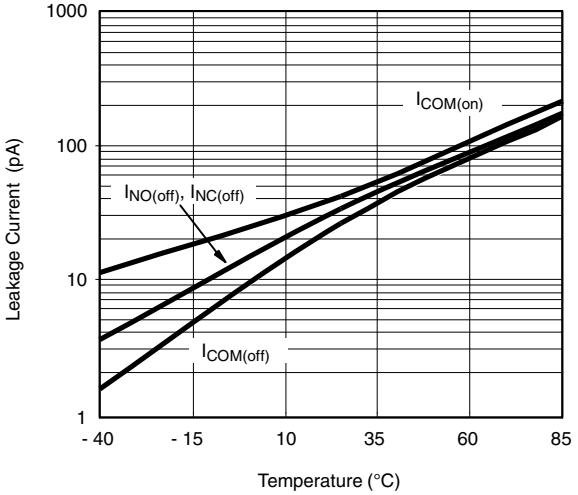

**$R_{ON}$ vs. Analog Voltage and Temperature**



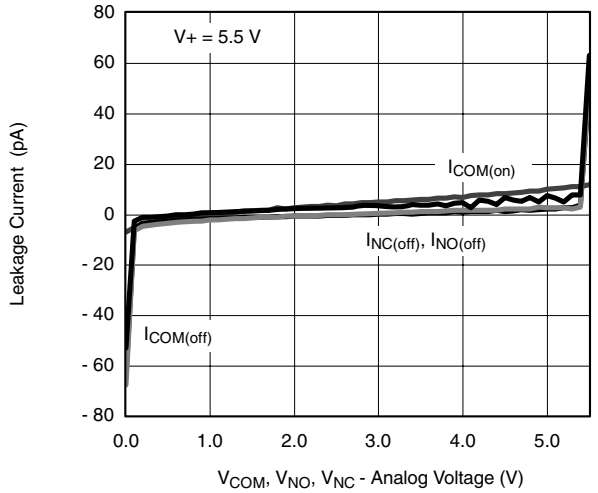

**Supply Current vs. Temperature**




**Supply Current vs. Input Switching Frequency**

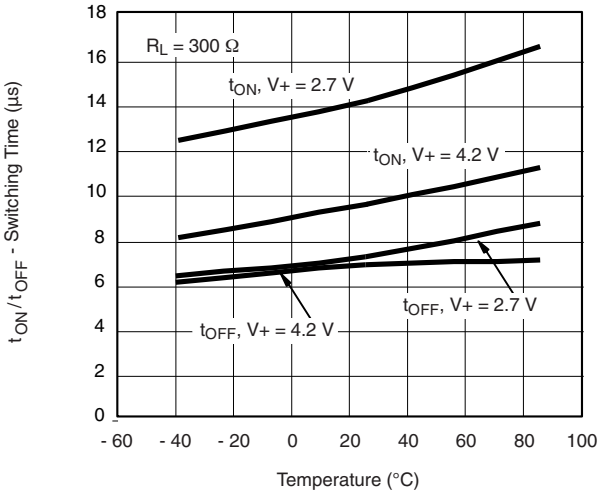



**Leakage Current vs. Temperature**

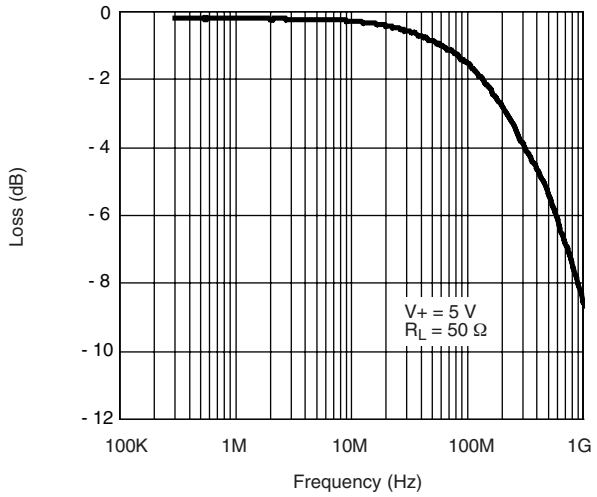



**Leakage vs. Analog Voltage**

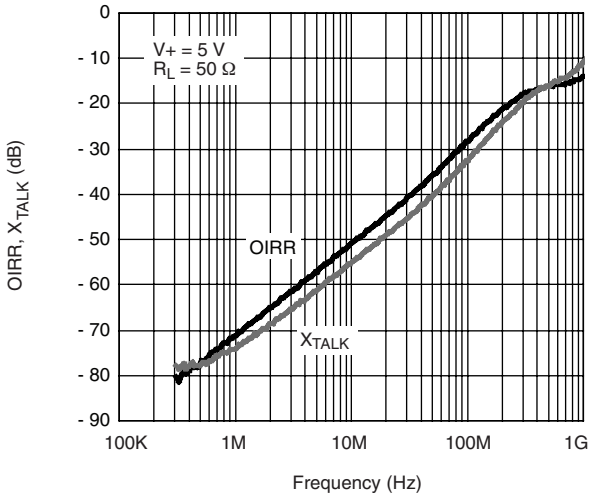
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



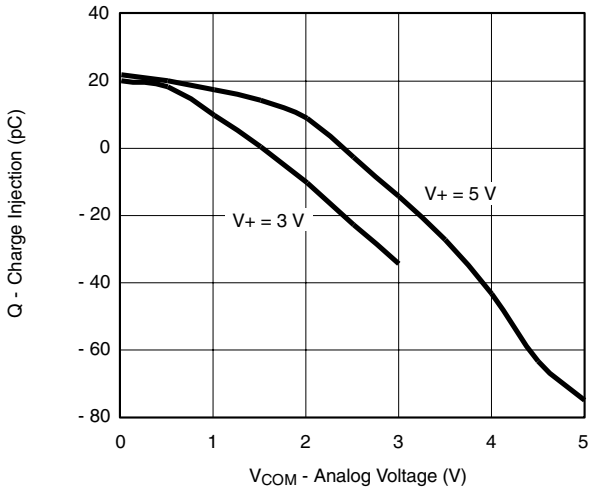

**Switching Time vs. Temperature**



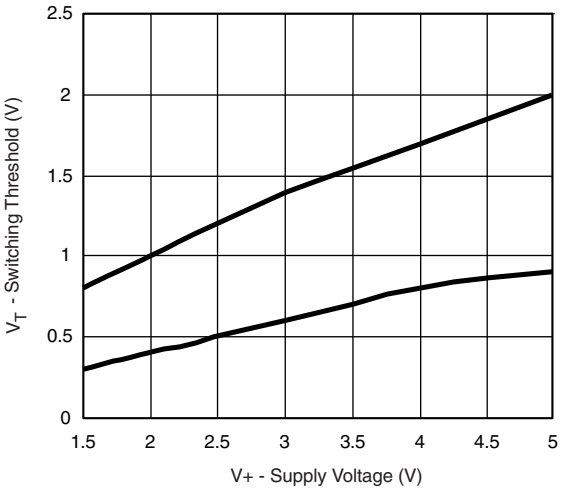

**Insertion Loss vs. Frequency**




**Off-Isolation and Crosstalk vs. Frequency**

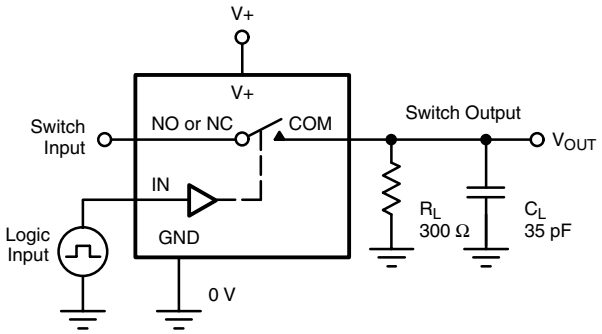



**Charge Injection vs. Analog Voltage**



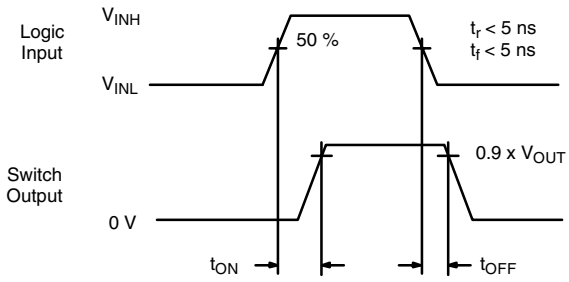

**Switching Threshold vs. Supply Voltage**

## TEST CIRCUITS



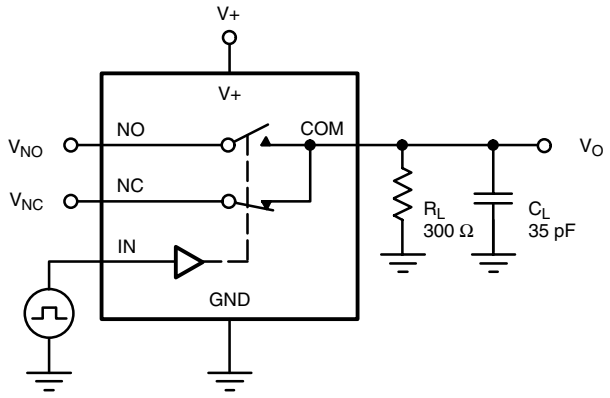

$C_L$ (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$




Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

**Figure 1. Switching Time**




$C_L$ (includes fixture and stray capacitance)

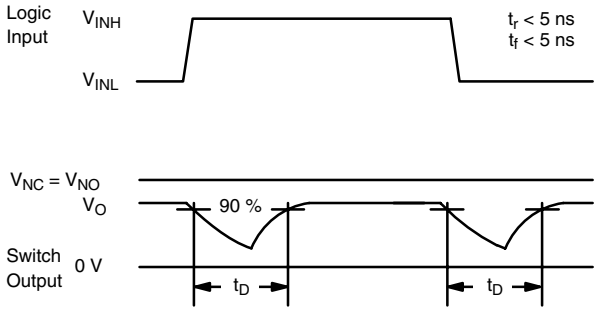
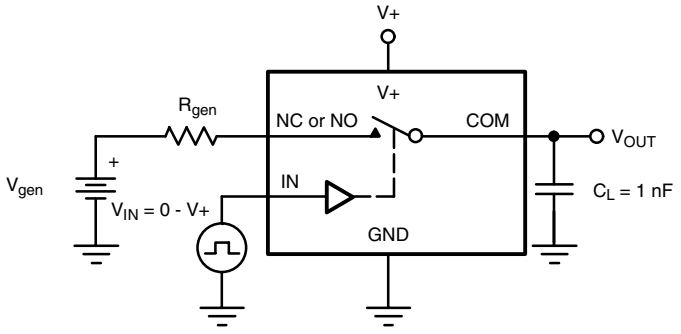
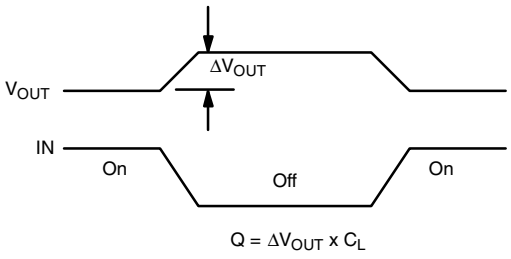



**Figure 2. Break-Before-Make Interval**




$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

**Figure 3. Charge Injection**

## TEST CIRCUITS

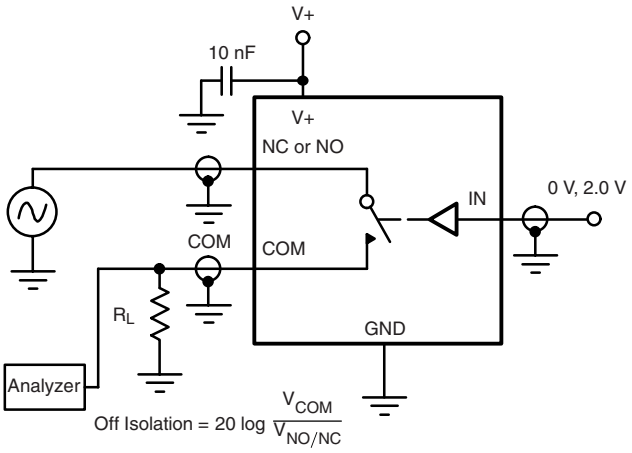



**Figure 4. Off-Isolation**

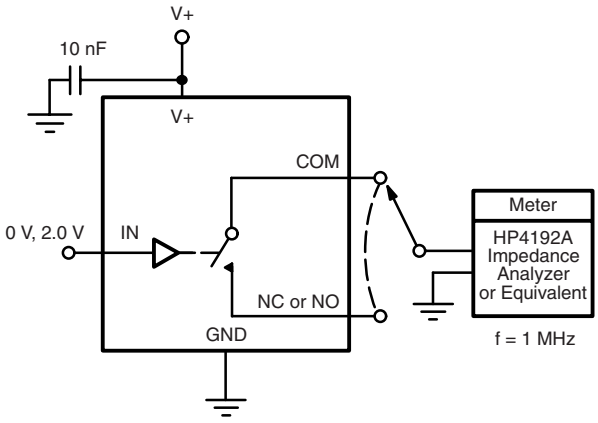



**Figure 5. Channel Off/On Capacitance**

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