HIGH-SPEED 2.5V 512/256K x 18 ASYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V 0R 2.5V INTERFACE

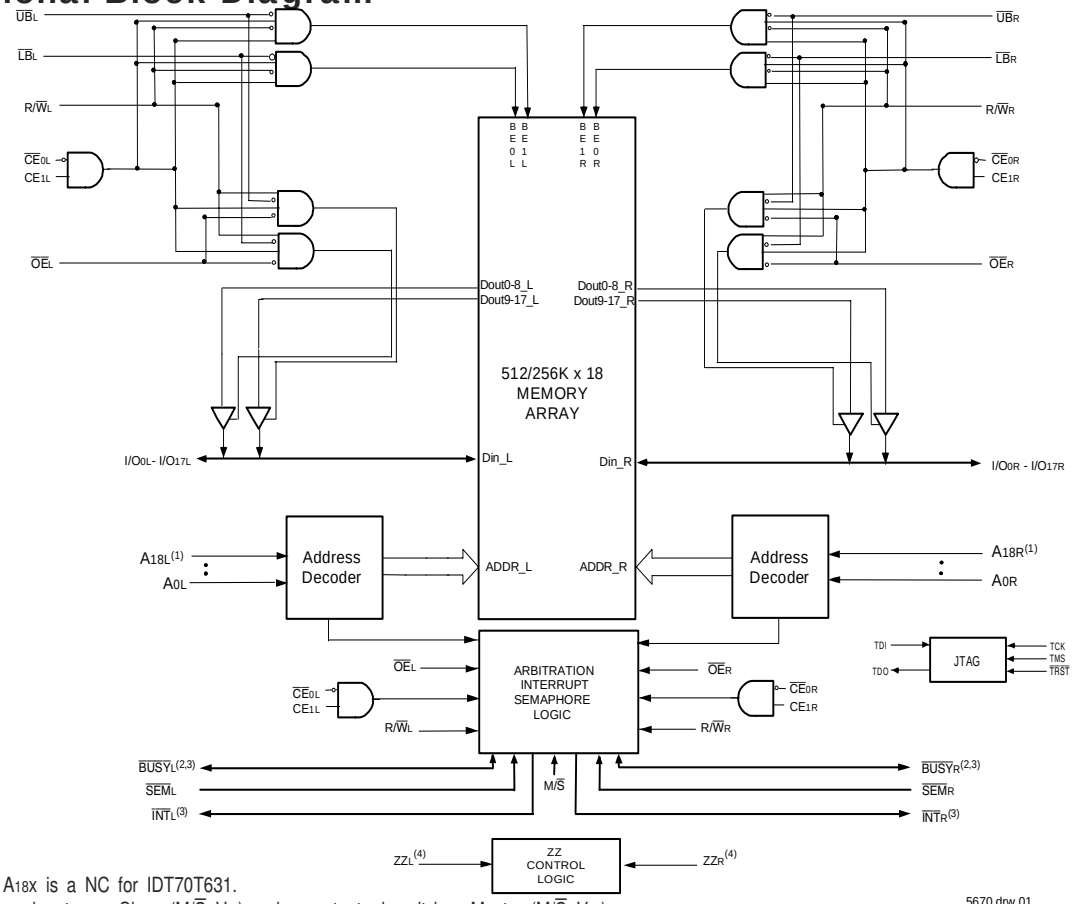
IDT70T633/1S

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- True Dual-Port memory cells which allow simultaneous access of the same memory location
- High-speed access
  - *Commercial: 10/12/15ns (max.)*
  - *Industrial: 10/12ns (max.)*
- RapidWrite Mode simplifies high-speed consecutive write cycles
- Dual chip enables allow for depth expansion without external logic
- IDT70T633/1 easily expands data bus width to 36 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = VIH for $\overline{BUSY}$ output flag on Master, M/$\overline{S}$ = VIL for $\overline{BUSY}$ input on Slave
- Busy and Interrupt Flags
- On-chip port arbitration logic
- Full hardware support of semaphore signaling between ports on-chip
- Fully asynchronous operation from either port
- Separate byte controls for multiplexed bus and bus matching compatibility
- Sleep Mode Inputs on both ports
- Supports JTAG features compliant to IEEE 1149.1 in BGA-208 and BGA-256 packages
- Single 2.5V (±100mV) power supply for core
- LVTTL-compatible, selectable 3.3V (±150mV)/2.5V (±100mV) power supply for I/Os and control signals on each port
- Available in a 256-ball Ball Grid Array and 208-ball fine pitch Ball Grid Array
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



5670 drw 01

NOTES:

1. Address A18X is a NC for IDT70T631.
2. $\overline{BUSY}$ is an input as a Slave (M/$\overline{S}$=VIL) and an output when it is a Master (M/$\overline{S}$=VIH).
3. $\overline{BUSY}$ and $\overline{INT}$ are non-tri-state totem-pole outputs (push-pull).
4. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. OPTx, $\overline{INT}$x, M/$\overline{S}$ and the sleep mode pins themselves (ZZx) are not affected during sleep mode.

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Description

The IDT70T633/1 is a high-speed 512/256K x 18 Asynchronous Dual-Port Static RAM. The IDT70T633/1 is designed to be used as a stand-alone 9216/4608K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 36-bit-or-more word system. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 36-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by the chip enables (either $\overline{CE}_0$ or CE_1) permit the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70T633/1 has a RapidWrite Mode which allows the designer to perform back-to-back write operations without pulsing the R/$\overline{W}$ input each cycle. This is especially significant at the 10ns cycle times of the IDT70T633/1, easing design considerations at these high performance levels.

The 70T633/1 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controlled by the OPT pins. The power supply for the core of the device (V_{DD}) remains at 2.5V.

Pin Configuration[1,2,3]

70T633/1BC
BC-256[5,6]

256-Pin BGA
Top View

03/13/03

A1 NC	A2 TDI	A3 NC	A4 A_{17L}	A5 A_{14L}	A6 A_{11L}	A7 A_{8L}	A8 NC	A9 CE_{1L}	A10 $\overline{OE}_L$	A11 $\overline{INT}_L$	A12 A_{5L}	A13 A_{2L}	A14 A_{0L}	A15 NC	A16 NC
B1 NC	B2 NC	B3 TDO	B4 A_{18L}[4]	B5 A_{15L}	B6 A_{12L}	B7 A_{9L}	B8 $\overline{UB}_L$	B9 $\overline{CE}_{0L}$	B10 $R/\overline{W}_L$	B11 NC	B12 A_{4L}	B13 A_{1L}	B14 NC	B15 NC	B16 NC
C1 NC	C2 I/O_{9L}	C3 V_{SS}	C4 A_{16L}	C5 A_{13L}	C6 A_{10L}	C7 A_{7L}	C8 NC	C9 $\overline{LB}_L$	C10 $\overline{SEM}_L$	C11 $\overline{BUSY}_L$	C12 A_{6L}	C13 A_{3L}	C14 OPT_L	C15 NC	C16 I/O_{8L}
D1 NC	D2 I/O_{9R}	D3 NC	D4 V_{DD}	D5 V_{DDQL}	D6 V_{DDQL}	D7 V_{DDQR}	D8 V_{DDQR}	D9 V_{DDQL}	D10 V_{DDQL}	D11 V_{DDQR}	D12 V_{DDQR}	D13 V_{DD}	D14 NC	D15 NC	D16 I/O_{8R}
E1 I/O_{10R}	E2 I/O_{10L}	E3 NC	E4 V_{DDQL}	E5 V_{DD}	E6 V_{DD}	E7 V_{SS}	E8 V_{SS}	E9 V_{SS}	E10 V_{SS}	E11 V_{DD}	E12 V_{DD}	E13 V_{DDQR}	E14 NC	E15 I/O_{7L}	E16 I/O_{7R}
F1 I/O_{11L}	F2 NC	F3 I/O_{11R}	F4 V_{DDQL}	F5 V_{DD}	F6 NC	F7 V_{SS}	F8 V_{SS}	F9 V_{SS}	F10 V_{SS}	F11 V_{SS}	F12 V_{DD}	F13 V_{DDQR}	F14 I/O_{6R}	F15 NC	F16 I/O_{6L}
G1 NC	G2 NC	G3 I/O_{12L}	G4 V_{DDQR}	G5 V_{SS}	G6 V_{SS}	G7 V_{SS}	G8 V_{SS}	G9 V_{SS}	G10 V_{SS}	G11 V_{SS}	G12 V_{SS}	G13 V_{DDQL}	G14 I/O_{5L}	G15 NC	G16 NC
H1 NC	H2 I/O_{12R}	H3 NC	H4 V_{DDQR}	H5 V_{SS}	H6 V_{SS}	H7 V_{SS}	H8 V_{SS}	H9 V_{SS}	H10 V_{SS}	H11 V_{SS}	H12 V_{SS}	H13 V_{DDQL}	H14 NC	H15 NC	H16 I/O_{5R}
J1 I/O_{13L}	J2 I/O_{14R}	J3 I/O_{13R}	J4 V_{DDQL}	J5 ZZ_R	J6 V_{SS}	J7 V_{SS}	J8 V_{SS}	J9 V_{SS}	J10 V_{SS}	J11 V_{SS}	J12 ZZ_L	J13 V_{DDQR}	J14 I/O_{4R}	J15 I/O_{3R}	J16 I/O_{4L}
K1 NC	K2 NC	K3 I/O_{14L}	K4 V_{DDQL}	K5 V_{SS}	K6 V_{SS}	K7 V_{SS}	K8 V_{SS}	K9 V_{SS}	K10 V_{SS}	K11 V_{SS}	K12 V_{SS}	K13 V_{DDQR}	K14 NC	K15 NC	K16 I/O_{3L}
L1 I/O_{15L}	L2 NC	L3 I/O_{15R}	L4 V_{DDQR}	L5 V_{DD}	L6 NC	L7 V_{SS}	L8 V_{SS}	L9 V_{SS}	L10 V_{SS}	L11 V_{SS}	L12 V_{DD}	L13 V_{DDQL}	L14 I/O_{2L}	L15 NC	L16 I/O_{2R}
M1 I/O_{16R}	M2 I/O_{16L}	M3 NC	M4 V_{DDQR}	M5 V_{DD}	M6 V_{DD}	M7 V_{SS}	M8 V_{SS}	M9 V_{SS}	M10 V_{SS}	M11 V_{DD}	M12 V_{DD}	M13 V_{DDQL}	M14 I/O_{1R}	M15 I/O_{1L}	M16 NC
N1 NC	N2 I/O_{17R}	N3 NC	N4 V_{DD}	N5 V_{DDQR}	N6 V_{DDQR}	N7 V_{DDQL}	N8 V_{DDQL}	N9 V_{DDQR}	N10 V_{DDQR}	N11 V_{DDQL}	N12 V_{DDQL}	N13 V_{DD}	N14 NC	N15 I/O_{0R}	N16 NC
P1 NC	P2 I/O_{17L}	P3 TMS	P4 A_{16R}	P5 A_{13R}	P6 A_{10R}	P7 A_{7R}	P8 NC	P9 $\overline{LB}_R$	P10 $\overline{SEM}_R$	P11 $\overline{BUSY}_R$	P12 A_{6R}	P13 A_{3R}	P14 NC	P15 NC	P16 I/O_{0L}
R1 NC	R2 NC	R3 $\overline{TRST}$	R4 A_{18R}[4]	R5 A_{15R}	R6 A_{12R}	R7 A_{9R}	R8 $\overline{UB}_R$	R9 $\overline{CE}_{0R}$	R10 $R/\overline{W}_R$	R11 $M/\overline{S}$	R12 A_{4R}	R13 A_{1R}	R14 OPT_R	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 A_{17R}	T5 A_{14R}	T6 A_{11R}	T7 A_{8R}	T8 NC	T9 CE_{1R}	T10 $\overline{OE}_R$	T11 $\overline{INT}_R$	T12 A_{5R}	T13 A_{2R}	T14 A_{0R}	T15 NC	T16 NC

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NOTES:
1. All V_{DD} pins must be connected to 2.5V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{DD} (2.5V), and 2.5V if OPT pin for that port is set to V_{SS} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. A_{18X} is a NC for IDT70T631.
5. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
6. This package code is used to reference the package diagram.

Pin Configurations[1,2,3](con't.)

03/12/03

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	I/O_{9L}	NC	V_{SS}	TDO	NC	A_{16L}	A_{12L}	A_{8L}	NC	V_{DD}	$\overline{SEM}_L$	$\overline{INT}_L$	A_{4L}	A_{0L}	OPT_L	NC	V_{SS}	A
B	NC	V_{SS}	NC	TDI	A_{17L}	A_{13L}	A_{9L}	NC	$\overline{CE}_{0L}$	V_{SS}	$\overline{BUSY}_L$	A_{5L}	A_{1L}	V_{SS}	V_{DDQR}	I/O_{8L}	NC	B
C	V_{DDQL}	I/O_{9R}	V_{DDQR}	V_{DD}	A_{18L}[4]	A_{14L}	A_{10L}	$\overline{UB}_L$	CE_{1L}	V_{SS}	$R/\overline{W}_L$	A_{6L}	A_{2L}	V_{DD}	I/O_{8R}	NC	V_{SS}	C
D	NC	V_{SS}	I/O_{10L}	NC	A_{15L}	A_{11L}	A_{7L}	$\overline{LB}_L$	V_{DD}	$\overline{OE}_L$	NC	A_{3L}	V_{DD}	NC	V_{DDQL}	I/O_{7L}	I/O_{7R}	D
E	I/O_{11L}	NC	V_{DDQR}	I/O_{10R}										I/O_{6L}	NC	V_{SS}	NC	E
F	V_{DDQL}	I/O_{11R}	NC	V_{SS}										V_{SS}	I/O_{6R}	NC	V_{DDQR}	F
G	NC	V_{SS}	I/O_{12L}	NC										NC	V_{DDQL}	I/O_{5L}	NC	G
H	V_{DD}	NC	V_{DDQR}	I/O_{12R}										V_{DD}	NC	V_{SS}	I/O_{5R}	H
J	V_{DDQL}	V_{DD}	V_{SS}	ZZ_R										ZZ_L	V_{DD}	V_{SS}	V_{DDQR}	J
K	I/O_{14R}	V_{SS}	I/O_{13R}	V_{SS}										I/O_{3R}	V_{DDQL}	I/O_{4R}	V_{SS}	K
L	NC	I/O_{14L}	V_{DDQR}	I/O_{13L}										NC	I/O_{3L}	V_{SS}	I/O_{4L}	L
M	V_{DDQL}	NC	I/O_{15R}	V_{SS}										V_{SS}	NC	I/O_{2R}	V_{DDQR}	M
N	NC	V_{SS}	NC	I/O_{15L}										I/O_{1R}	V_{DDQL}	NC	I/O_{2L}	N
P	I/O_{16R}	I/O_{16L}	V_{DDQR}	NC	$\overline{TRST}$	A_{16R}	A_{12R}	A_{8R}	NC	V_{DD}	$\overline{SEM}_R$	$\overline{INT}_R$	A_{4R}	NC	I/O_{1L}	V_{SS}	NC	P
R	V_{SS}	NC	I/O_{17R}	TCK	A_{17R}	A_{13R}	A_{9R}	NC	$\overline{CE}_{0R}$	V_{SS}	$\overline{BUSY}_R$	A_{5R}	A_{1R}	V_{SS}	V_{DDQL}	I/O_{0R}	V_{DDQR}	R
T	NC	I/O_{17L}	V_{DDQL}	TMS	A_{18R}[4]	A_{14R}	A_{10R}	$\overline{UB}_R$	CE_{1R}	V_{SS}	$R/\overline{W}_R$	A_{6R}	A_{2R}	V_{SS}	NC	V_{SS}	NC	T
U	V_{SS}	NC	V_{DD}	NC	A_{15R}	A_{11R}	A_{7R}	$\overline{LB}_R$	V_{DD}	$\overline{OE}_R$	M/$\overline{S}$	A_{3R}	A_{0R}	V_{DD}	OPT_R	NC	I/O_{0L}	U

70T633/1BF
BF-208[5,6]

208-Ball BGA
Top View[7]

5670 drw 02b

NOTES:
1. All V_{DD} pins must be connected to 2.5V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{DD} (2.5V), and 2.5V if OPT pin for that port is set to V_{SS} (0V).
3. All V_{SS} pins must be connected to ground.
4. A_{18X} is a NC for IDT70T631.
5. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
6. This package code is used to reference the package diagram.
7. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables (Input)
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable (Input)
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable (Input)
A_{0L} - A_{18L}[1]	A_{0R} - A_{18R}[1]	Address (Input)
I/O_{0L} - I/O_{17L}	I/O_{0R} - I/O_{17R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable (Input)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag (Output)
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag (Output)
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select (Input)
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select (Input)
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V)[2] (Input)
OPT_L	OPT_R	Option for selecting V_{DDQX}[2,3] (Input)
ZZ_L	ZZ_R	Sleep Mode Pin[4] (Input)
M/$\overline{S}$		Master or Slave Select (Input)[5]
V_{DD}		Power (2.5V)[2] (Input)
V_{SS}		Ground (0V) (Input)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz) (Input)
TMS		Test Mode Select (Input)
$\overline{TRST}$		Reset (Initialize TAP Controller) (Input)

5670 tbl 01

NOTES:
1. Address A_{18X} is a NC for IDT70T631.
2. V_{DD}, OPT_X, and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on I/O_X.
3. OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to V_{DD} (2.5V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to V_{SS} (0V), then that port's I/Os and controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
4. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. OPT_X, $\overline{INT}_X$, M/$\overline{S}$ and the sleep mode pins themselves (ZZ_X) are not affected during sleep mode. It is recommended that boundry scan not be operated during sleep mode.
5. $\overline{BUSY}$ is an input as a Slave (M/$\overline{S}$=V_{IL}) and an output when it is a Master (M/$\overline{S}$=V_{IH}).

Truth Table I—Read/Write and Enable Control(1)

$\overline{OE}$	$\overline{SEM}$	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	R/$\overline{W}$	ZZ	Upper Byte I/O9-17	Lower Byte I/O0-8	MODE
X	H	H	X	X	X	X	L	High-Z	High-Z	Deselected–Power Down
X	H	X	L	X	X	X	L	High-Z	High-Z	Deselected–Power Down
X	H	L	H	H	H	X	L	High-Z	High-Z	Both Bytes Deselected
X	H	L	H	H	L	L	L	High-Z	DIN	Write to Lower Byte
X	H	L	H	L	H	L	L	DIN	High-Z	Write to Upper Byte
X	H	L	H	L	L	L	L	DIN	DIN	Write to Both Bytes
L	H	L	H	H	L	H	L	High-Z	DOUT	Read Lower Byte
L	H	L	H	L	H	H	L	DOUT	High-Z	Read Upper Byte
L	H	L	H	L	L	H	L	DOUT	DOUT	Read Both Bytes
H	H	L	H	L	L	X	L	High-Z	High-Z	Outputs Disabled
X	X	X	X	X	X	X	H	High-Z	High-Z	High-Z Sleep Mode

5670 tbl 02

NOTE:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.

Truth Table II – Semaphore Read/Write Control(1)

Inputs(1)						Outputs		
$\overline{CE}$(2)	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O1-17	I/O0	Mode
H	H	L	L	L	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag(3)
H	↑	X	X	L	L	X	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	X	X	L	——	——	Not Allowed

5670 tbl 03

NOTES:
1. There are eight semaphore flags written to I/O0 and read from all the I/Os (I/O0-I/O17). These eight semaphore flags are addressed by A0-A2.
2. $\overline{CE}$ = L occurs when $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}. $\overline{CE}$ = H when $\overline{CE}_0$ = V_{IH} and/or CE_1 = V_{IL}.
3. Each byte is controlled by the respective $\overline{UB}$ and $\overline{LB}$. To read data $\overline{UB}$ and/or $\overline{LB}$ = V_{IL}.

Recommended Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	VDD
Commercial	0°C to +70°C	0V	2.5V ± 100mV
Industrial	-40°C to +85°C	0V	2.5V ± 100mV

5670 tbl 04

NOTE:
1. This is the parameter TA. This is the "instant on" case temperature.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
VTERM (VDD)	VDD Terminal Voltage with Respect to GND	-0.5 to 3.6	V
VTERM(2) (VDDQ)	VDDQ Terminal Voltage with Respect to GND	-0.3 to VDDQ + 0.3	V
VTERM(2) (INPUTS and I/O's)	Input and I/O Terminal Voltage with Respect to GND	-0.3 to VDDQ + 0.3	V
TBIAS(3)	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-65 to +150	°C
TJN	Junction Temperature	+150	°C
IOUT(For VDDQ = 3.3V)	DC Output Current	50	mA
IOUT(For VDDQ = 2.5V)	DC Output Current	40	mA

5670 tbl 07

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed VDDQ during power supply ramp up.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.

Capacitance(1)

(TA = +25°C, F = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions(2)	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	8	pF
COUT(3)	Output Capacitance	VOUT = 3dV	10.5	pF

5670 tbl 08

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. COUT also references CI/O.

Recommended DC Operating Conditions with VDDQ at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	2.4	2.5	2.6	V
VDDQ	I/O Supply Voltage(3)	2.4	2.5	2.6	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage (Address, Control & Data I/O Inputs)(3)	1.7	—	VDDQ + 100mV(2)	V
VIH	Input High Voltage – JTAG	1.7	—	VDD + 100mV(2)	V
VIH	Input High Voltage - ZZ, OPT, M/$\overline{S}$	VDD - 0.2V	—	VDD + 100mV(2)	V
VIL	Input Low Voltage	-0.3(1)	—	0.7	V
VIL	Input Low Voltage - ZZ, OPT, M/$\overline{S}$	-0.3(1)	—	0.2	V

5670 tbl 05

NOTES:
1. VIL (min.) = -1.0V for pulse width less than tRC/2 or 5ns, whichever is less.
2. VIH (max.) = VDDQ + 1.0V for pulse width less than tRC/2 or 5ns, whichever is less.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to VSS (0V), and VDDQX for that port must be supplied as indicated above.

Recommended DC Operating Conditions with VDDQ at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	2.4	2.5	2.6	V
VDDQ	I/O Supply Voltage(3)	3.15	3.3	3.45	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage (Address, Control &Data I/O Inputs)(3)	2.0	—	VDDQ + 150mV(2)	V
VIH	Input High Voltage – JTAG	1.7	—	VDD + 100mV(2)	V
VIH	Input High Voltage - ZZ, OPT, M/$\overline{S}$	VDD - 0.2V	—	VDD + 100mV(2)	V
VIL	Input Low Voltage	-0.3(1)	—	0.8	V
VIL	Input Low Voltage - ZZ, OPT, M/$\overline{S}$	-0.3(1)	—	0.2	V

5670 tbl 06

NOTES:
1. VIL (min.) = -1.0V for pulse width less than tRC/2 or 5ns, whichever is less.
2. VIH (max.) = VDDQ + 1.0V for pulse width less than tRC/2 or 5ns, whichever is less.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to VDD (2.5V), and VDDQX for that port must be supplied as indicated above.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 2.5V ± 100mV)

Symbol	Parameter	Test Conditions	70T633/1S Min.	70T633/1S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[1]	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\|I_{LI}\|$	JTAG & ZZ Input Leakage Current[1,2]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	±30	µA
$\|I_{LO}\|$	Output Leakage Current[1,3]	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage[1]	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage[1]	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage[1]	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage[1]	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

5670 tbl 09

NOTES:
1. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to page 5 for details.
2. Applicable only for TMS, TDI and $\overline{TRST}$ inputs.
3. Outputs tested in tri-state mode.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 2.5V ± 100mV)

Symbol	Parameter	Test Condition	Version		70T633/1S10 Com'l & Ind[6] Typ.[4]	70T633/1S10 Com'l & Ind[6] Max.	70T633/1S12 Com'l & Ind Typ.[4]	70T633/1S12 Com'l & Ind Max.	70T633/1S15 Com'l Only Typ.[4]	70T633/1S15 Com'l Only Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	300	405	300	355	225	305	mA
			IND	S	300	445	300	395	—	—	
I_{SB1}[6]	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}, f = f_{MAX}[1]	COM'L	S	90	120	75	105	60	85	mA
			IND	S	90	145	75	130	—	—	
I_{SB2}[6]	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5], Active Port Outputs Disabled, f = f_{MAX}[1]	COM'L	S	200	265	180	230	150	200	mA
			IND	S	200	290	180	255	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DDQ}$ - 0.2V, $V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[2]	COM'L	S	2	10	2	10	2	10	mA
			IND	S	2	20	2	20	—	—	
I_{SB4}[6]	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{DDQ}$ - 0.2V[5], $V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Port, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	200	265	180	230	150	200	mA
			IND	S	200	290	180	255	—	—	
I_{ZZ}	Sleep Mode Current (Both Ports - TTL Level Inputs)	ZZ_L = ZZ_R = V_{IH}, f = f_{MAX}[1]	COM'L	S	2	10	2	10	2	10	mA
			IND	S	2	20	2	20	—	—	

5670 tbl 10

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, using "AC TEST CONDITIONS".
2. f = 0 means no address or control lines change. Applies only to input at CMOS level standby.
3. V_{DD} = 2.5V, T_A = 25°C for Typ. values, and are not production tested. $I_{DD\,DC}$(f=0) = 100mA (Typ).
4. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X \leq$ 0.2V means $\overline{CE}_{0X} \leq$ 0.2V and $CE_{1X} \geq V_{DDQX}$ - 0.2V
   $\overline{CE}_X \geq V_{DDQX}$ - 0.2V means $\overline{CE}_{0X} \geq V_{DDQX}$ - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.
5. I_{SB1}, I_{SB2} and I_{SB4} will all reach full standby levels (I_{SB3}) on the appropriate port(s) if ZZ_L and /or ZZ_R = V_{IH}.

AC Test Conditions (V_{DDQ} = 3.3V/2.5V)

Input Pulse Levels	GND to 3.0V / GND to 2.5V
Input Rise/Fall Times	2ns Max.
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figure 1

5670 tbl 11

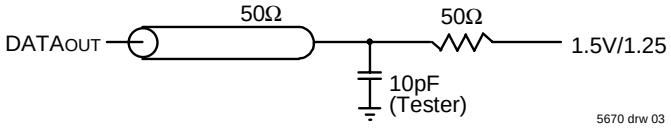


Figure 1. AC Output Test load.

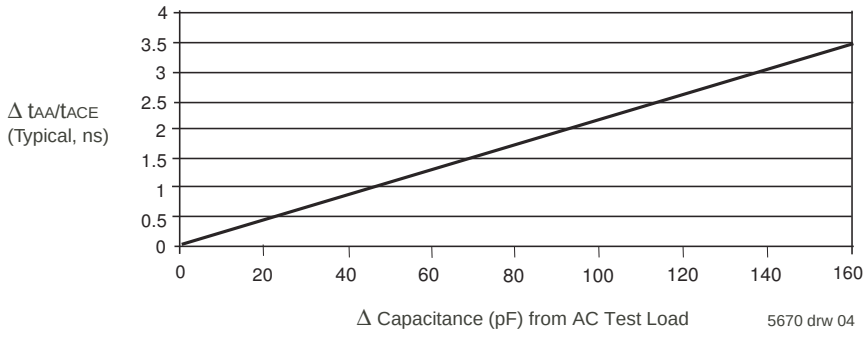


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[4]

Symbol	Parameter	70T633/1S10 Com'l & Ind[5]		70T633/1S12 Com'l & Ind		70T633/1S15 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACE}	Chip Enable Access Time[3]	—	10	—	12	—	15	ns
t_{ABE}	Byte Enable Access Time[3]	—	5	—	6	—	7	ns
t_{AOE}	Output Enable Access Time	—	5	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time Chip Enable and Semaphore[1,2]	3	—	3	—	3	—	ns
t_{LZOB}	Output Low-Z Time Output Enable and Byte Enable[1,2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	0	4	0	6	0	8	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	8	—	8	—	12	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	—	4	—	6	—	8	ns
t_{SAA}	Semaphore Address Access Time	2	10	2	12	2	15	ns
t_{SOE}	Semaphore Output Enable Access Time	—	5	—	6	—	7	ns

5670 tbl 12

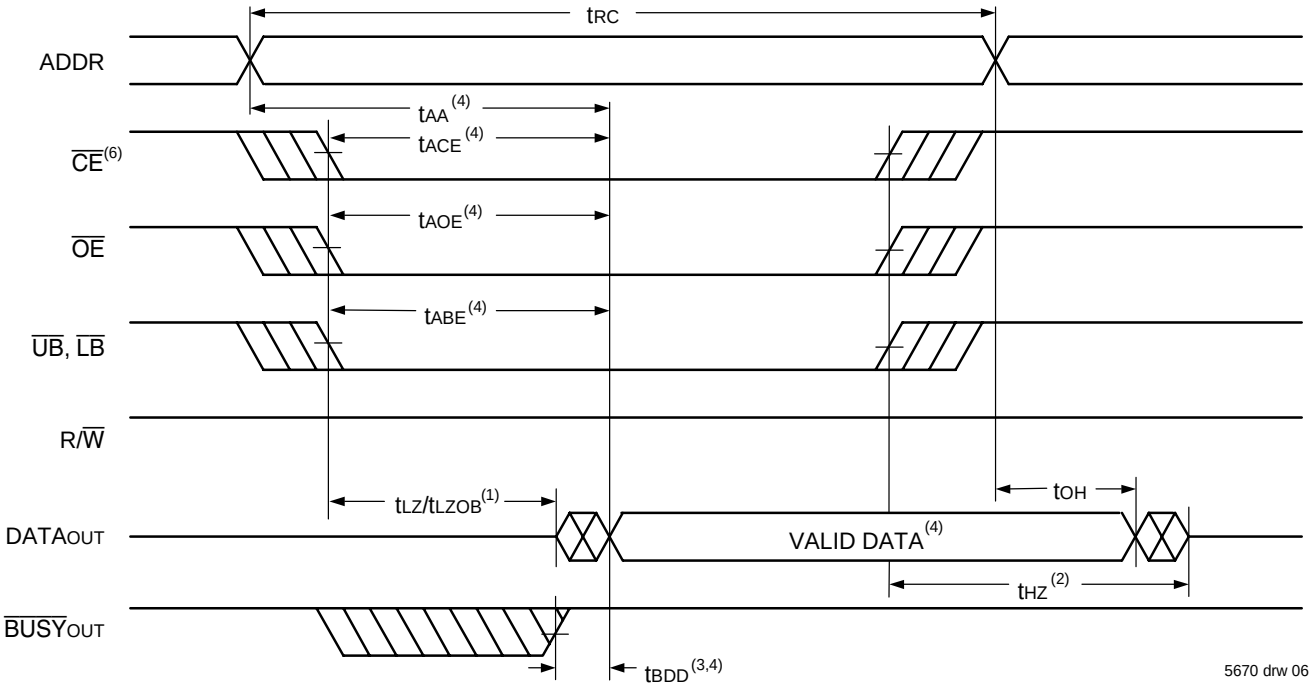
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[4]

Symbol	Parameter	70T633/1S10 Com'l & Ind[5]		70T633/1S12 Com'l & Ind		70T633/1S15 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	7	—	9	—	12	—	ns
t_{AW}	Address Valid to End-of-Write	7	—	9	—	12	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	7	—	9	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	5	—	7	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	4	—	6	—	8	ns
t_{OW}	Output Active from End-of-Write[1,2]	3	—	3	—	3	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

5670 tbl 13

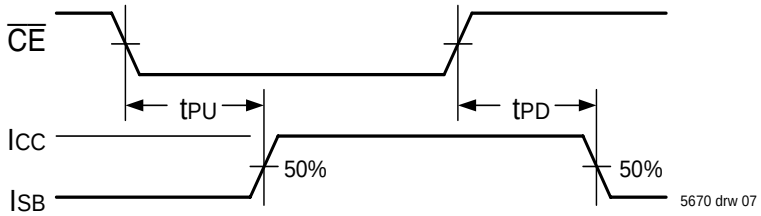
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 1).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$= V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time. $\overline{CE}$ = V_{IL} when $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}. $\overline{CE}$ = V_{IH} when $\overline{CE}_0$ = V_{IH} and/or CE_1 = V_{IL}.
4. These values are valid regardless of the power supply level selected for I/O and control signals (3.3V/2.5V). See page 6 for details.

Waveform of Read Cycles(5)

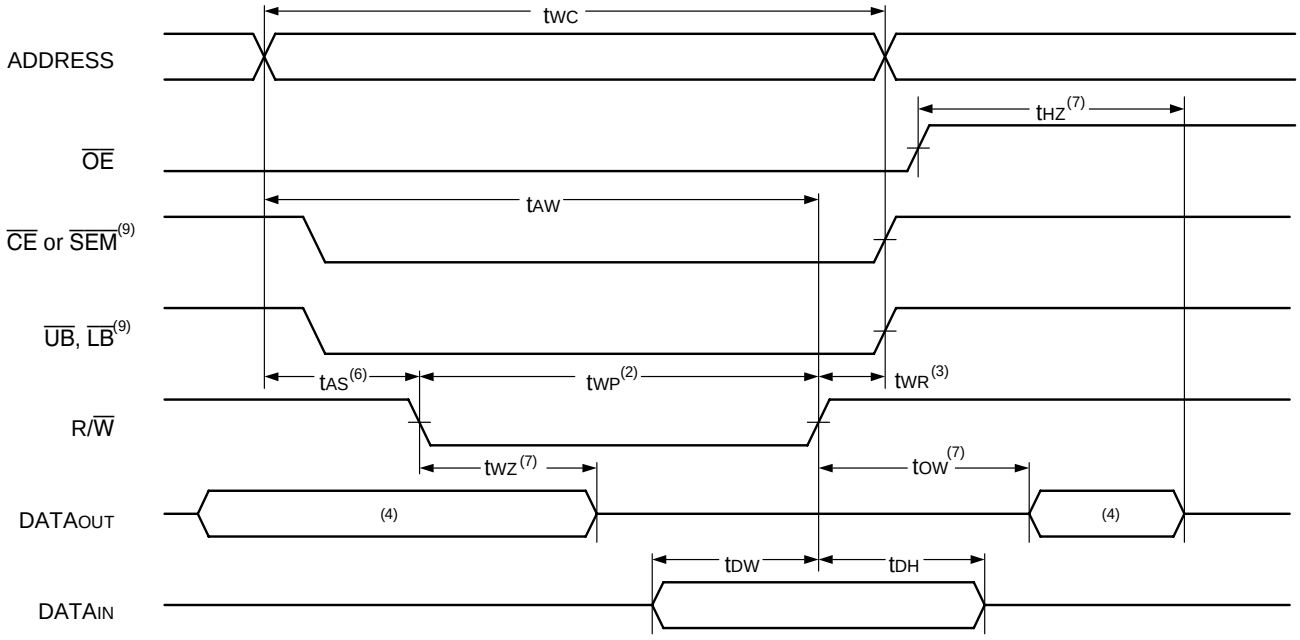


NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$ or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$ or $\overline{UB}$.
3. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last: t_{AOE}, t_{ACE}, t_{AA}, t_{ABE}, or t_{BDD}.
5. $\overline{SEM}$ = V_{IH}.
6. $\overline{CE}$ = L occurs when $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}. $\overline{CE}$ = H when $\overline{CE}_0$ = V_{IH} and/or CE_1 = V_{IL}.

Timing of Power-Up Power-Down

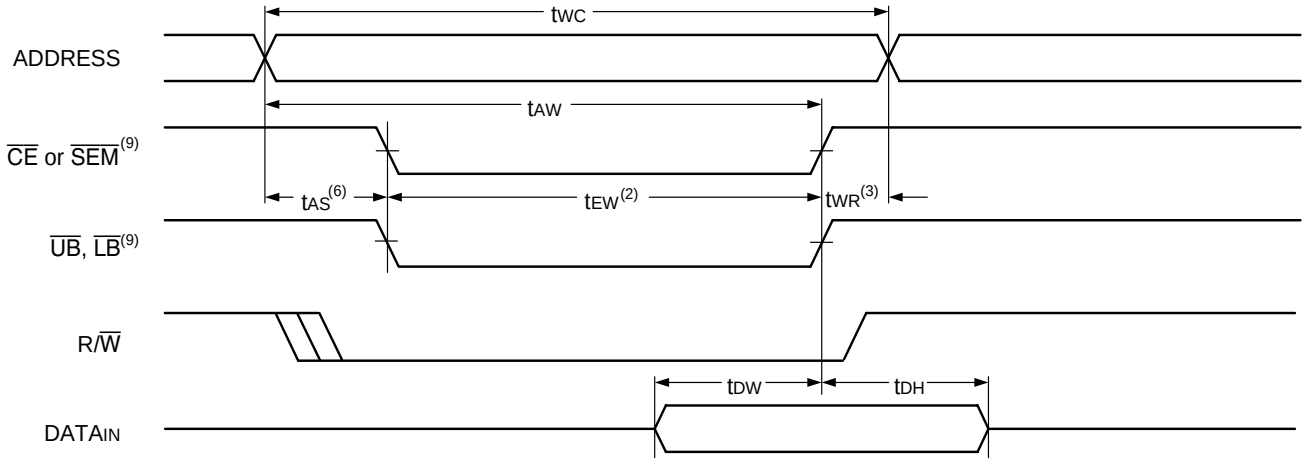


Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



5670 drw 10

Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing(1,5,8)



5670 drw 11

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ or $\overline{LB}$ = V_{IH} during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ = V_{IL} and a R/$\overline{W}$ = V_{IL} for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ = V_{IL} transition occurs simultaneously with or after the R/$\overline{W}$ = V_{IL} transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 1).
8. If $\overline{OE}$ = V_{IL} during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ = V_{IH} during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. t_{EW} must be met for either condition. $\overline{CE}$ = V_{IL} when $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}. $\overline{CE}$ = V_{IH} when $\overline{CE}_0$ = V_{IH} and/or CE_1 = V_{IL}.

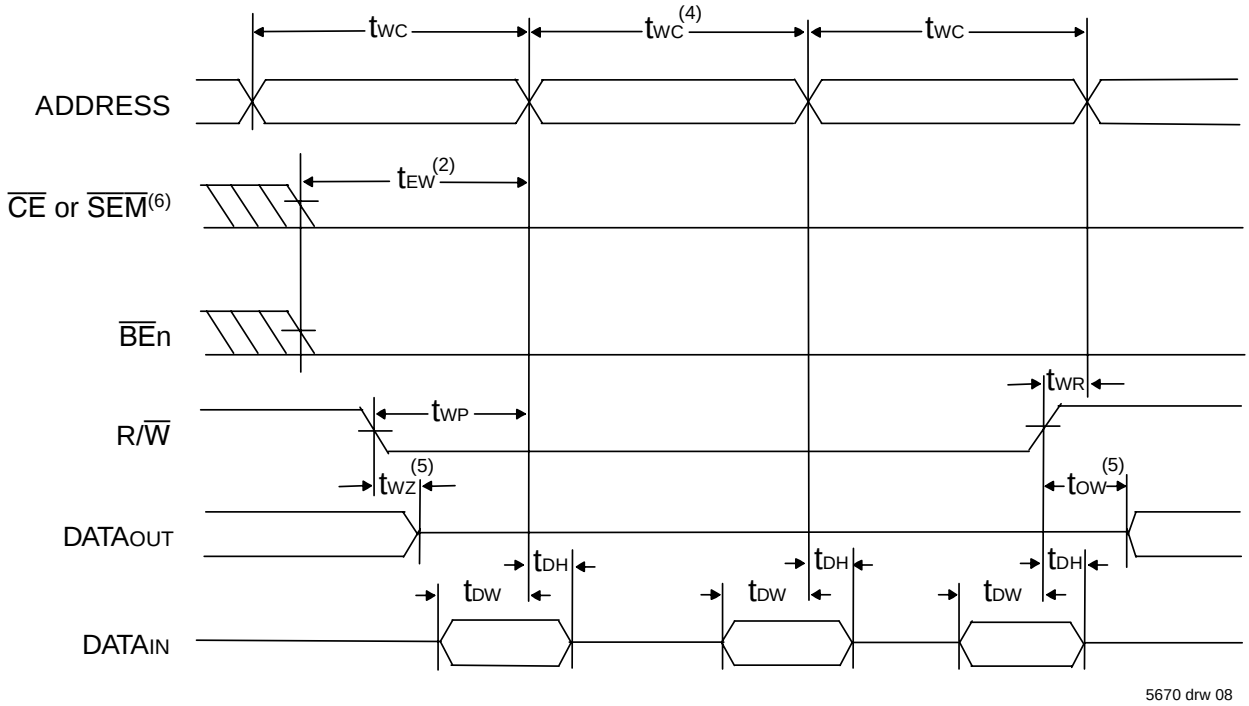
RapidWrite Mode Write Cycle

Unlike other vendors' Asynchronous Random Access Memories, the IDT70T633/1 is capable of performing multiple back-to-back write operations without having to pulse the R/$\overline{W}$, $\overline{CE}$, or $\overline{BE}$n signals high during address transitions. This RapidWrite Mode functionality allows the system designer to achieve optimum back-to-back write cycle performance without the difficult task of generating narrow reset pulses every cycle, simplifying system design and reducing time to market.

During this new RapidWrite Mode, the end of the write cycle is now defined by the ending address transition, instead of the R/$\overline{W}$ or $\overline{CE}$ or $\overline{BE}$n transition to the inactive state. R/$\overline{W}$, $\overline{CE}$, and $\overline{BE}$n can be held active throughout the address transition between write cycles.

Care must be taken to still meet the Write Cycle time (t_{WC}), the time in which the Address inputs must be stable. Input data setup and hold times (t_{DW} and t_{DH}) will now be referenced to the ending address transition. In this RapidWrite Mode the I/O will remain in the Input mode for the duration of the operations due to R/$\overline{W}$ being held low. All standard Write Cycle specifications must be adhered to. However, t_{AS} and t_{WR} are only applicable when switching between read and write operations. Also, there are two additional conditions on the Address Inputs that must also be met to ensure correct address controlled writes. These specifications, the Allowable Address Skew (t_{AAS}) and the Address Rise/Fall time (t_{ARF}), must be met to use the RapidWrite Mode. If these conditions are not met there is the potential for inadvertent write operations at random intermediate locations as the device transitions between the desired write addresses.

Timing Waveform of Write Cycle No. 3, RapidWrite Mode Write Cycle(1,3)



NOTES:

1. $\overline{OE}$ = V_{IL} for this timing waveform as shown. $\overline{OE}$ may equal V_{IH} with same write functionality; I/O would then always be in High-Z state.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ = V_{IL}, $\overline{BE}$n = V_{IL}, and a R/$\overline{W}$ = V_{IL} for memory array writing cycle. The last transition LOW of $\overline{CE}$, $\overline{BE}$n, and R/$\overline{W}$ initiates the write sequence. The first transition HIGH of $\overline{CE}$, $\overline{BE}$n, and R/$\overline{W}$ terminates the write sequence.
3. If the $\overline{CE}$ or $\overline{SEM}$ = V_{IL} transition occurs simultaneously with or after the R/$\overline{W}$ = V_{IL} transition, the outputs remain in the High-impedance state.
4. The timing represented in this cycle can be repeated multiple times to execute sequential RapidWrite Mode writes.
5. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 1).
6. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. t_{EW} must be met for either condition. $\overline{CE}$ = V_{IL} when $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}. $\overline{CE}$ = V_{IH} when $\overline{CE}_0$ = V_{IH} and/or CE_1 = V_{IL}.

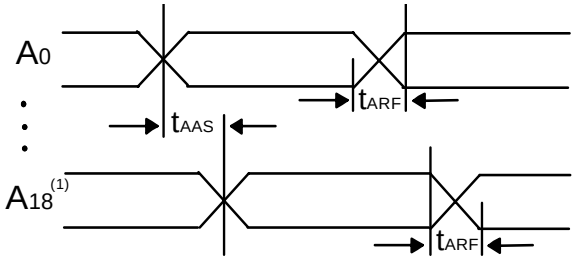
AC Electrical Characteristics over the Operating Temperature Range and Supply Voltage Range for RapidWrite Mode Write Cycle(1)

Symbol	Parameter	Min	Max	Unit
t_{AAS}	Allowable Address Skew for RapidWrite Mode	—	1	ns
t_{ARF}	Address Rise/Fall Time for RapidWrite Mode	1.5	—	V/ns

5670 tbl 14

NOTE:
1. Timing applies to all speed grades when utilizing the RapidWrite Mode Write Cycle.

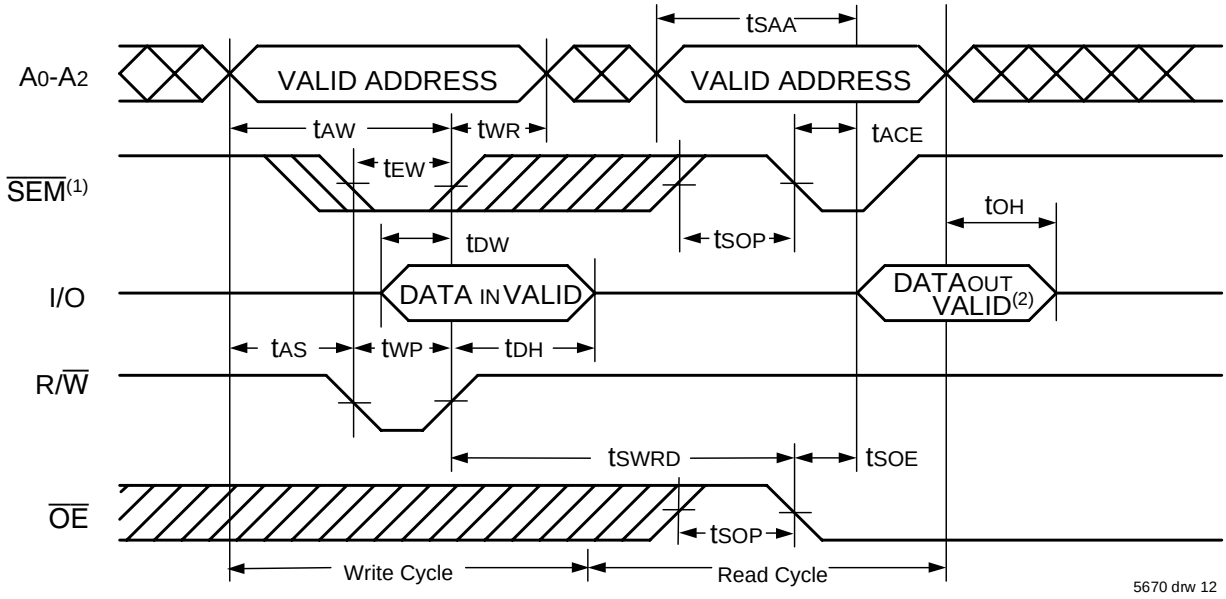
Timing Waveform of Address Inputs for RapidWrite Mode Write Cycle



5670 drw 09

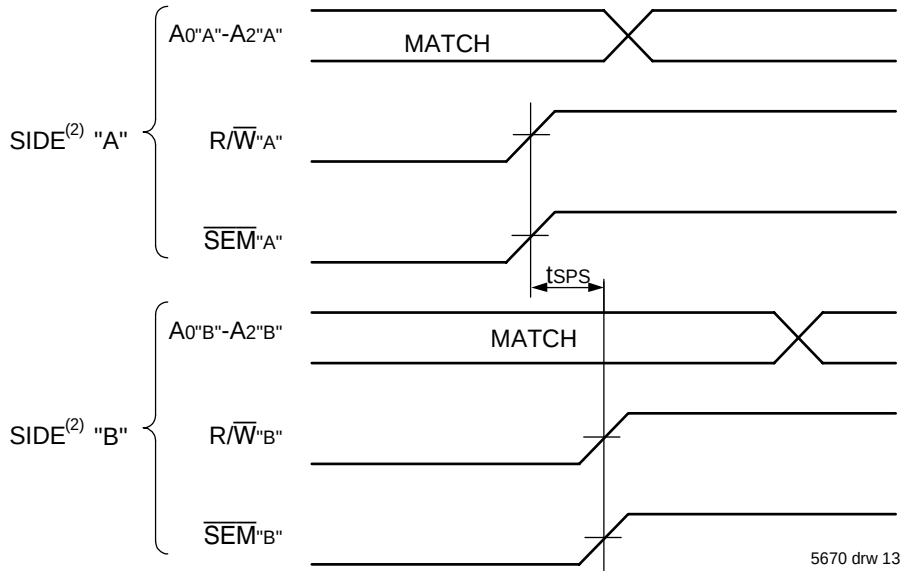
NOTE:
1. A_{17} for IDT70T631.

Timing Waveform of Semaphore Read after Write Timing, Either Side(1)



NOTES:
1. $\overline{CE}_0$ = V_{IH} and CE_1 = V_{IL} are required for the duration of both the write cycle and the read cycle waveforms shown above. Refer to Truth Table II for details and for appropriate $\overline{UB}/\overline{LB}$ controls.
2. "$DATA_{OUT}$ VALID" represents all I/O's (I/O_0 - I/O_{17}) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention(1,3,4)



NOTES:
1. D_{OR} = D_{OL} = V_{IL}, $\overline{CE}_{0L}$ = $\overline{CE}_{0R}$ = V_{IH}; CE_{1L} = CE_{1R} = V_{IL}. Refer also to Truth Table II for appropriate $\overline{UB}/\overline{LB}$ controls.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going HIGH to R/$\overline{W}$"B" or $\overline{SEM}$"B" going HIGH.
4. If t_{SPS} is not satisfied,the semaphore will fall positively to one side or the other, but there is no guarantee which side will be granted the semaphore flag.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

Symbol	Parameter	70T633/1S10 Com'l & Ind(6)		70T633/1S12 Com'l & Ind		70T633/1S15 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING (M/$\overline{S}$=VIH)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	10	—	12	—	15	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	10	—	12	—	15	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable Low	—	10	—	12	—	15	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable High	—	10	—	12	—	15	ns
tAPS	Arbitration Priority Set-up Time(2)	2.5	—	2.5	—	2.5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data(3)	—	10	—	12	—	15	ns
tWH	Write Hold After $\overline{BUSY}$(5)	7	—	9	—	12	—	ns
$\overline{BUSY}$ TIMING (M/$\overline{S}$=VIL)								
tWB	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(5)	7	—	9	—	12	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay(1)	—	14	—	16	—	20	ns
tDDD	Write Data Valid to Read Data Delay(1)	—	14	—	16	—	20	ns

5670 tbl 15

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of the Max. spec, tWDD – tWP (actual), or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".

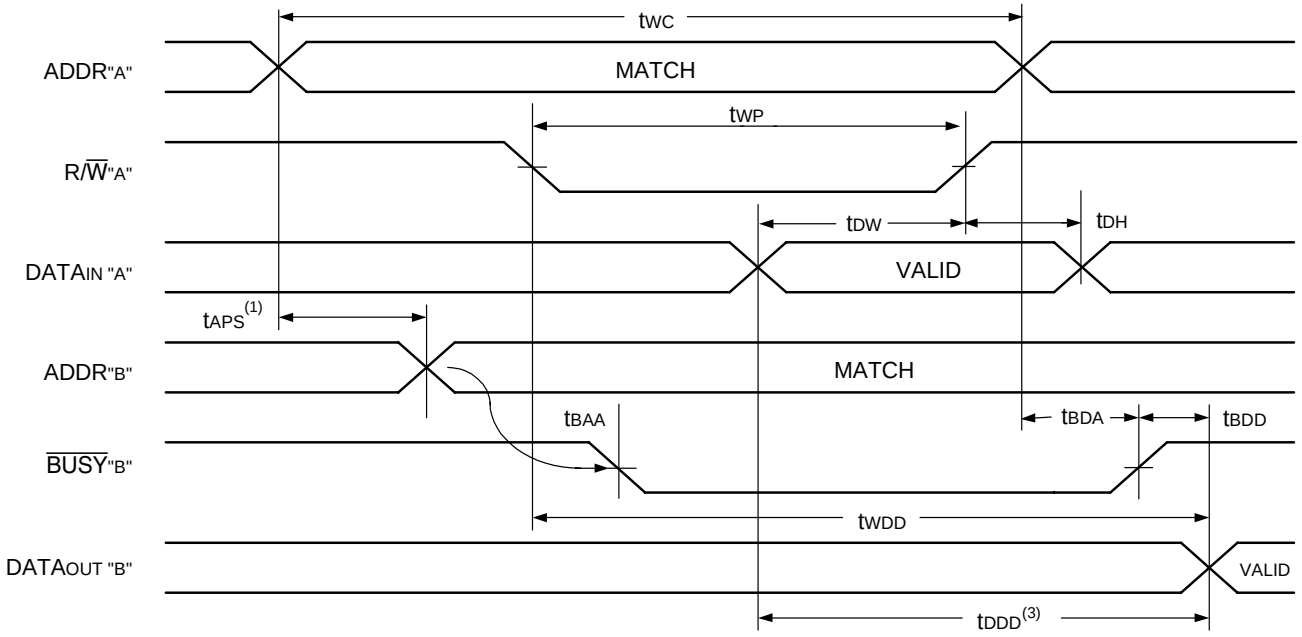
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1,2,3)

Symbol	Parameter	70T633/1S10 Com'l & Ind		70T6331S12 Com'l & Ind		70T633/1S15 Com'l Only	
		Min.	Max.	Min.	Max.	Min.	Max.
SLEEP MODE TIMING (ZZx=VIH)							
tZZS	Sleep Mode Set Time	10	—	12	—	15	—
tZZR	Sleep Mode Reset Time	10	—	12	—	15	—
tZZPD	Sleep Mode Power Down Time(4)	10	—	12	—	15	—
tZZPU	Sleep Mode Power Up Time(4)	—	0	—	0	—	0

5670 tbl 15a

NOTES:
1. Timing is the same for both ports.
2. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. OPTx, $\overline{INT}$x, M/$\overline{S}$ and the sleep mode pins themselves (ZZx) are not affected during sleep mode. It is recommended that boundary scan not be operated during sleep mode.
3. These values are valid regardless of the power supply level selected for I/O and control signals (3.3V/2.5V). See page 5 for details.
4. This parameter is guaranteed by device characterization, but is not production tested.

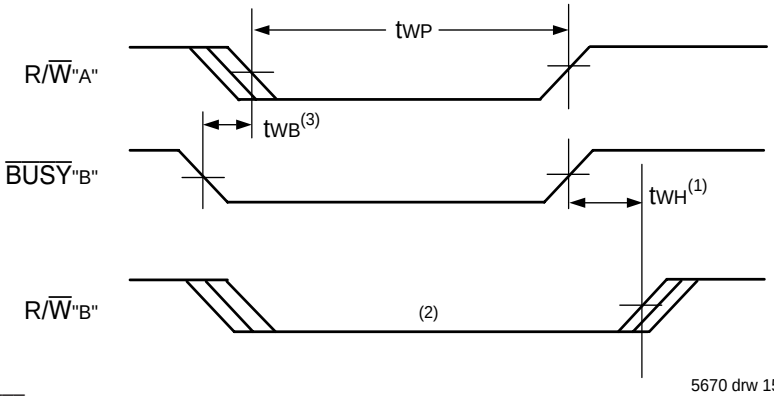
Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)(2,4,5)



5670 drw 14

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}_{0L}$ = $\overline{CE}_{0R}$ = VIL; CE_{1L} = CE_{1R} = VIH.
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL (slave), $\overline{BUSY}$ is an input. Then for this example $\overline{BUSY}$"A" = VIH and $\overline{BUSY}$"B" input is shown above.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

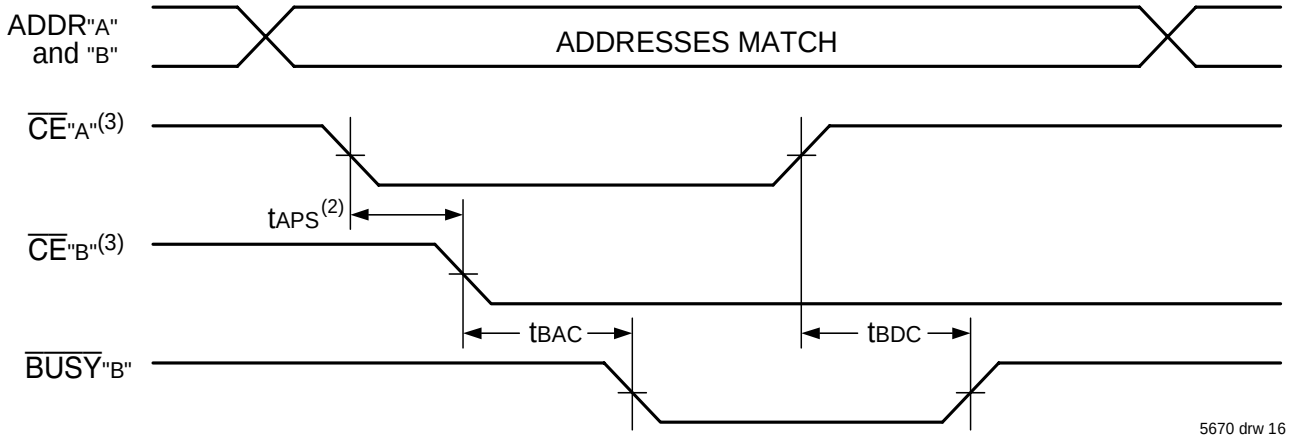
Timing Waveform of Write with $\overline{BUSY}$ (M/$\overline{S}$ = VIL)



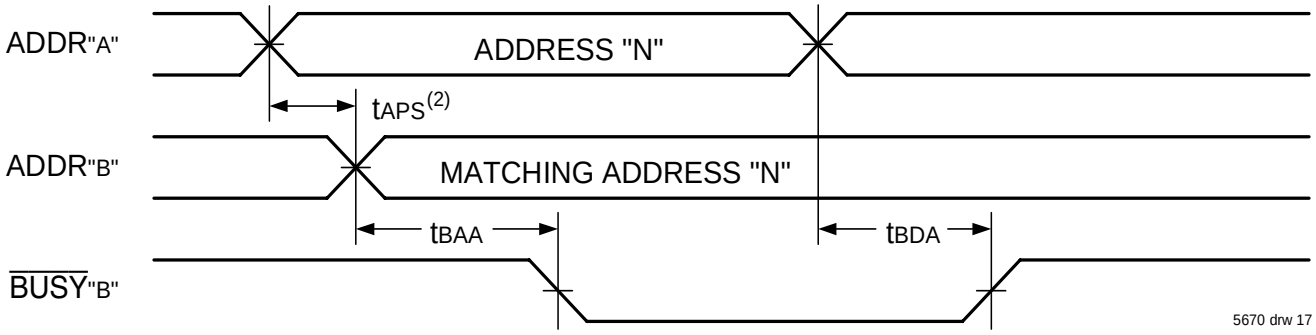
5670 drw 15

NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes HIGH.
3. tWB only applies to the slave mode.

Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing (M/$\overline{S}$ = V_{IH})(1)



Waveform of $\overline{BUSY}$ Arbitration Cycle Controlled by Address Match Timing (M/$\overline{S}$ = V_{IH})(1,3,4)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If t_{APS} is not satisfied, the $\overline{BUSY}$ signal will be asserted on one side or another but there is no guarantee on which side $\overline{BUSY}$ will be asserted.
3. $\overline{CE}_X$ = V_{IL} when $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}. $\overline{CE}_X$ = V_{IH} when $\overline{CE}_{0X}$ = V_{IH} and/or CE_{1X} = V_{IL}.
4. $\overline{CE}_{0X}$ = $\overline{OE}_X$ = $\overline{LB}_X$ = $\overline{UB}_X$ = V_{IL}. CE_{1X} = V_{IH}.

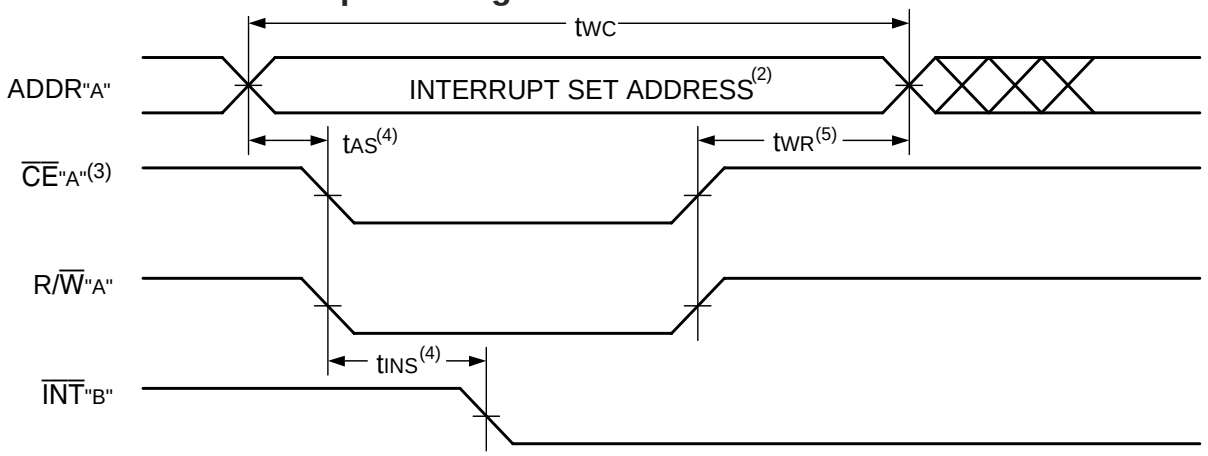
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1,2)

		70T633/1S10 Com'l & Ind		70T633/1S12 Com'l & Ind		70T633/1S15 Com'l Only		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	10	—	12	—	15	ns
t_{INR}	Interrupt Reset Time	—	10	—	12	—	15	ns

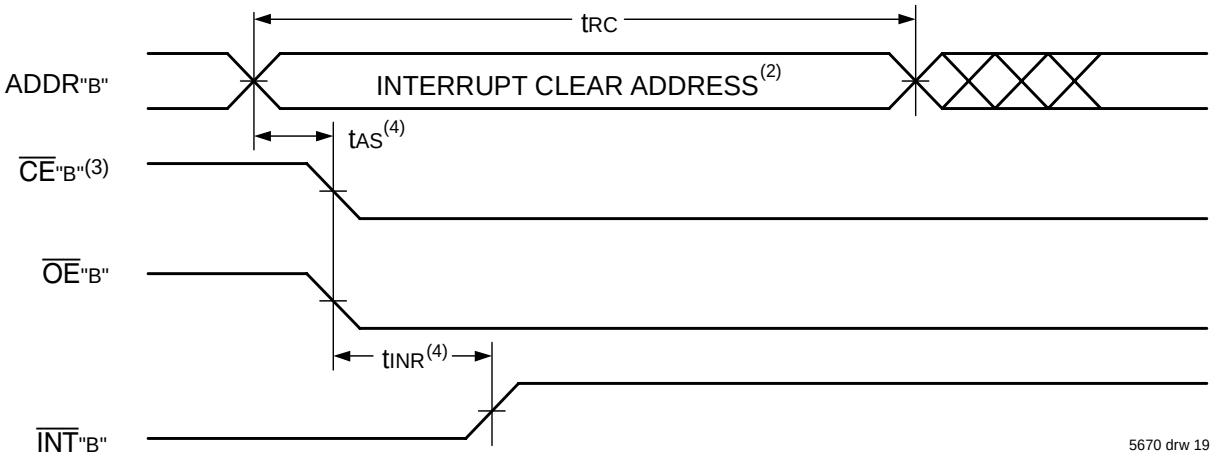
5670 tbl 16

NOTES:
1. Timing is the same for both ports.
2. These values are valid regardless of the power supply level selected for I/O and control signals (3.3V/2.5V). See page 5 for details.

Waveform of Interrupt Timing(1)



5670 drw 18



5670 drw 19

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. Refer to Interrupt Truth Table.
3. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}. $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} and/or CE_{1X} = V_{IL}.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
5. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

Truth Table III — Interrupt Flag(1,4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{18L}-A_{0L}(5)	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{18R}-A_{0R}(5)	$\overline{INT}_R$	Function
L	L	X	7FFFF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FFFF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FFFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FFFE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

5670 tbl 17

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ =V_{IH}. $\overline{CE}_X$ = L means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}.
2. If $\overline{BUSY}_L$ = V_{IL}, then no change.
3. If $\overline{BUSY}_R$ = V_{IL}, then no change.
4. $\overline{INT}_L$ and $\overline{INT}_R$ must be initialized at power-up.
5. A_{18X} is a NC for IDT70T631. Therefore, Interrupt Addresses are 3FFFF and 3FFFE.

Truth Table IV — Address BUSY Arbitration

Inputs			Outputs		
$\overline{CE}_L$(5)	$\overline{CE}_R$(5)	A_{0L}-A_{18L}(4) A_{0R}-A_{18R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

5670 tbl 18

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT70T633/1 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.
4. A_{18} is a NC for IDT70T631. Address comparison will be for A_0 - A_{17}.
5. $\overline{CE}_X$ = L means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}. $\overline{CE}_X$ = H means $\overline{CE}_{0X}$ = V_{IH} and/or CE_{1X} = V_{IL}.

Truth Table V — Example of Semaphore Procurement Sequence(1,2,3)

Functions	D_0 - D_{17} Left	D_0 - D_{17} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

5670 tbl 19

NOTES:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70T633/1.
2. There are eight semaphore flags written to via I/O_0 and read from all I/O's (I/O_0-I/O_{17}). These eight semaphores are addressed by A_0 - A_2.
3. $\overline{CE}_0$ = V_{IH}, CE_1 = $\overline{SEM}$ = V_{IL} to access the semaphores. Refer to the Semaphore Read/Write Control Truth Table.

Functional Description

The IDT70T633/1 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70T633/1 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}_0$ and CE_1 control the on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FFFE (HEX), where a write is defined as $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 7FFFE when $\overline{CE}_L$ = $\overline{OE}_L$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FFFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FFFF. The message (18 bits) at 7FFFE or 7FFFF (3FFFF or 3FFFE for IDT70T631) is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFFE and 7FFFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of $\overline{BUSY}$ logic is not desirable, the $\overline{BUSY}$ logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW.

The $\overline{BUSY}$ outputs on the IDT70T633/1 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the $\overline{BUSY}$ indication for the resulting array requires the use of an external AND gate.

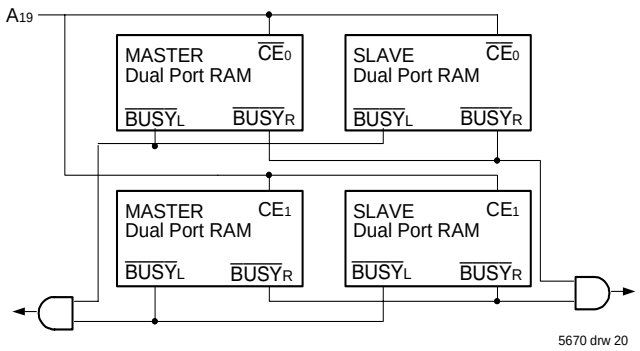


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70T633/1 Dual-Port RAMs.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT70T633/1 RAM array in width while using $\overline{BUSY}$ logic, one master part is used to decide which side of the RAMs array will receive a $\overline{BUSY}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the $\overline{BUSY}$ signal as a write inhibit signal. Thus on the IDT70T633/1 RAM the $\overline{BUSY}$ pin is an output if the part is used as a master (M/$\overline{S}$ pin = V_{IH}), and the $\overline{BUSY}$ pin is an input if the part used as a slave (M/$\overline{S}$ pin = V_{IL}) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating $\overline{BUSY}$ on one side of the array and another master indicating $\overline{BUSY}$ on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{BUSY}$ arbitration on a master is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{BUSY}$ flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT70T633/1 is an extremely fast Dual-Port 512/256K x 18 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, with both ports being completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from or written to at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}_0$ and CE_1, the Dual-Port RAM chip enables, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}_0$, CE_1, and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected.

Systems which can best use the IDT70T633/1 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the hardware semaphores of the IDT70T633/1, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70T633/1 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then

verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70T633/1 in a separate memory space from the Dual-Port RAM array. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{CE}_0$, CE_1, R/$\overline{W}$ and $\overline{LB}$/$\overline{UB}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins $A_0 – A_2$. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table V). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros for a semaphore read, the $\overline{SEM}$, $\overline{BE}$n, and $\overline{OE}$ signals need to be active. (Please refer to Truth Table II). Furthermore, the read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$, $\overline{BE}$n) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table V). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the opposite side HIGH. This condition will continue until a one is written to the same semaphore request latch.

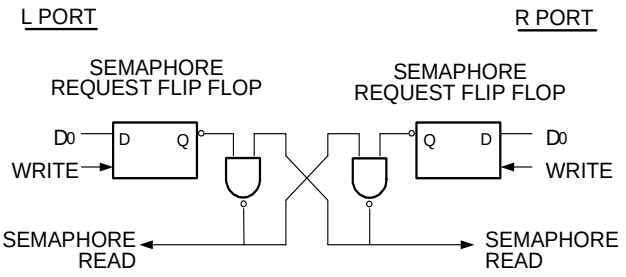


Figure 4. IDT70T633/1 Semaphore Logic 5670 drw 21

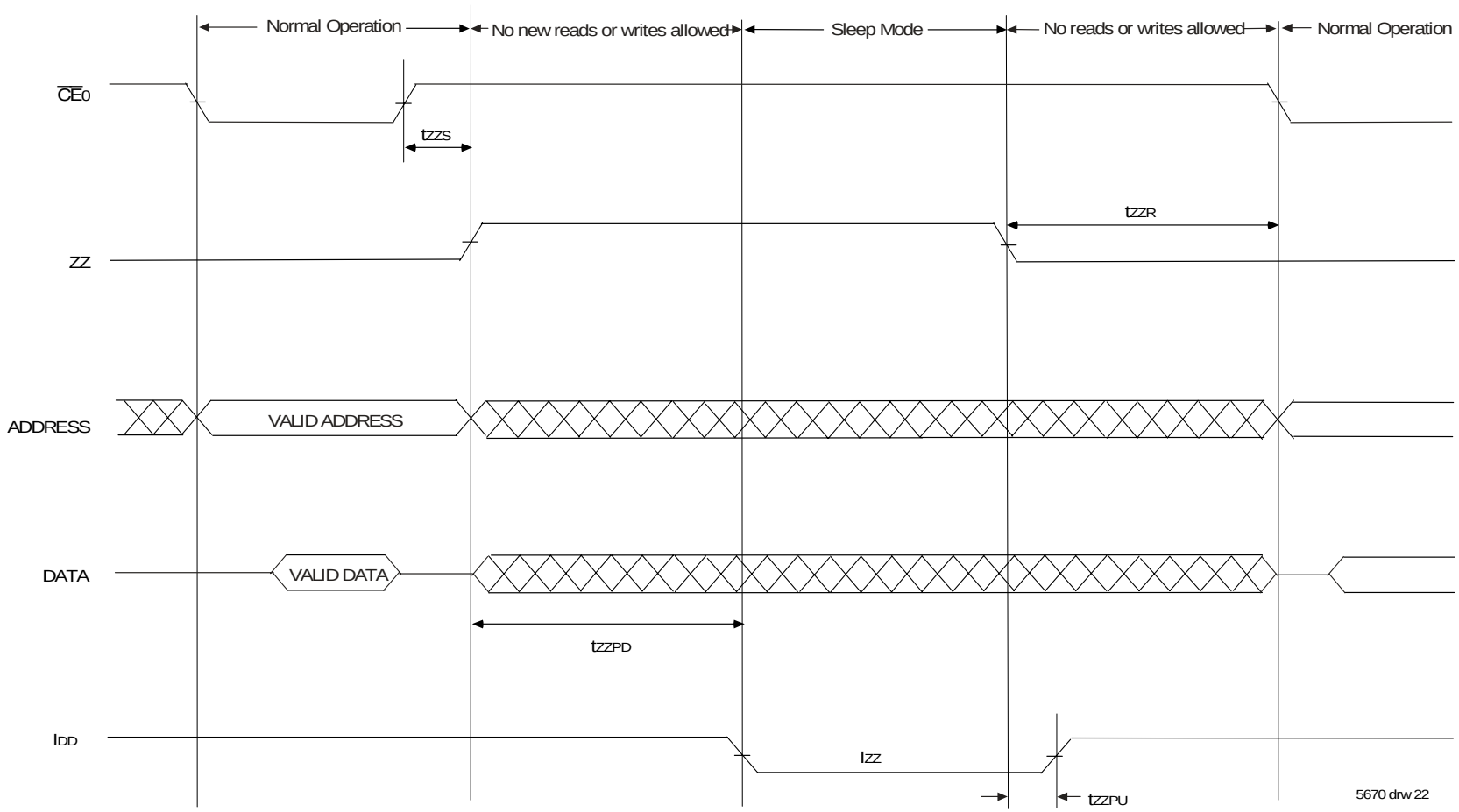
If the opposite side semaphore request latch has been written to zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first request latch. The opposite side flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Timing Waveform of Sleep Mode(1,2)



NOTES:
1. $CE_1 = V_{IH}$.
2. All timing is same for Left and Right ports.

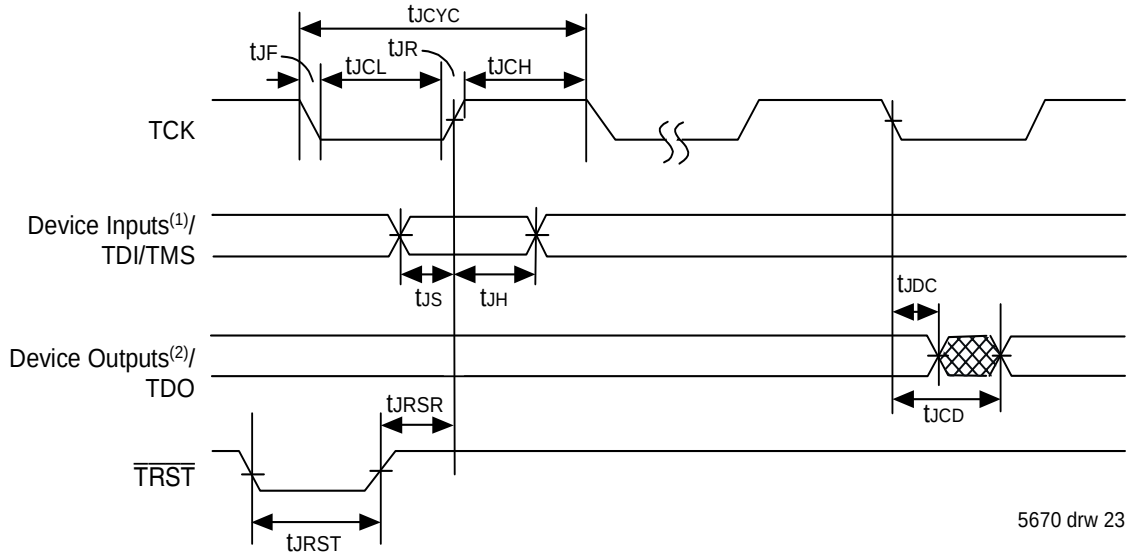
Sleep Mode

The IDT70T633/1 is equipped with an optional sleep or low power mode on both ports. The sleep mode pin on both ports is active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will have the lowest possible power consumption. The sleep mode timing diagram demonstrates the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

For a period of time prior to sleep mode and after recovering from sleep mode (t_{ZZS} and t_{ZZR}), new reads or writes are not allowed. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep).

During sleep mode the RAM automatically deselects itself and disconnects its internal buffer. All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle, but the RAM will not be selected and will not perform any reads or writes.

JTAG Timing Specifications



NOTES:
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics(1,2,3,4,5)

Symbol	Parameter	70T633/1		
		Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	3(1)	ns
t_{JF}	JTAG Clock Fall Time	—	3(1)	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	25	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	15	—	ns
t_{JH}	JTAG Hold	15	—	ns

5670 tbl 20

NOTES:
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.
5. JTAG cannot be tested in sleep mode.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x33B(1)	Defines IDT part number 70T633
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5670 tbl 21

NOTE:
1. Device ID for IDT70T631 is 0x33C.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5670 tbl 22

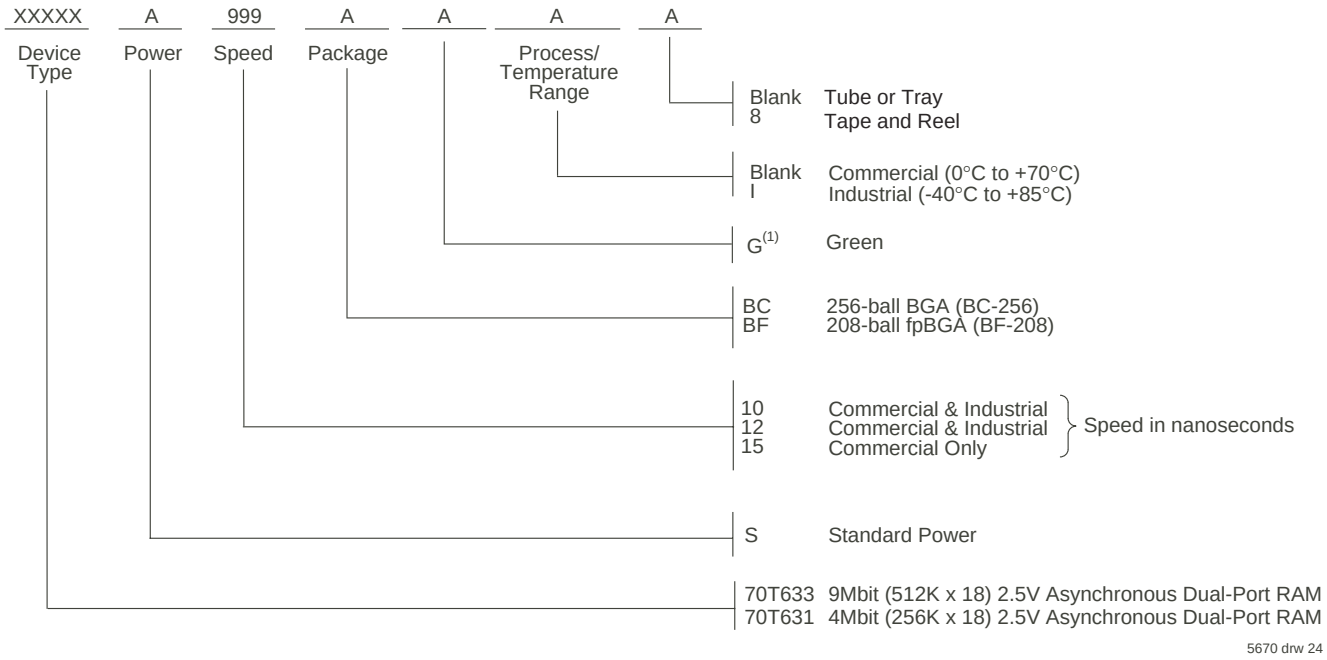
System Interface Parameters

Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(2) and outputs(1) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

5670 tbl 23

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information



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NOTES:
1. Green parts available. For specific speeds and packages contact your local sales office.
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History:

04/25/03:		Initial Datasheet
10/01/03:	Page 9	Added 8ns speed DC power numbers to DC Electrical Characteristics Table
	Page 9	Updated DC power numbers for 10, 12 & 15ns speeds in the DC Electrical Characteristics Table
	Page 9,11,15, 17&25	Added footnote that indicates that 8ns speed is available in BF-208 and BC-256 packages only
	Page 10	Added Capacitance Derating Drawing
	Page 11,15 & 17	Added 8ns AC timing numbers to the AC Electrical Characteristics Tables
	Page 11	Added t_{SOE} and t_{LZOB} to the AC Read Cycle Electrical Characteristics Table
	Page 12	Added t_{LZOB} to the Waveform of Read Cycles Drawing
	Page 14	Added t_{SOE} to Timing Waveform of Semaphore Read after Write Timing, Either Side Drawing
	Page 1& 25	Added 8ns speed grade and 10ns I-temp to features and to ordering information
	Page 1, 14 & 15	Added RapidWrite Mode Write Cycle text and waveforms
10/20/03:	Page 15	Corrected t_{ARF} to 1.5V/ns Min.
04/21/04:		Removed Preliminary status from entire datasheet
01/05/06:	Page 1	Added green availability to features
	Page 27	Added green indicator to ordering information
07/25/08:	Page 9	Corrected a typo in the DC Chars table
01/19/09:	Page 27	Removed "IDT" from orderable part number
04/20/10:		Removed the DD 144-pin TQFP (DD-144) Thin Quad Flatpack per PDN: F-08-01
10/15/11:	Page 2,13	Corrected 70T651/9 to 70T633/1
	Page 26	Updated ordering information to include tube or tray and tape & reel.
06/18/12:	Page 1,2,8,10, 16,18,26	Removed 8ns from datasheet to match pricebook.
11/27/17:		Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018

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