SI2302

PUOLOP 迪浦

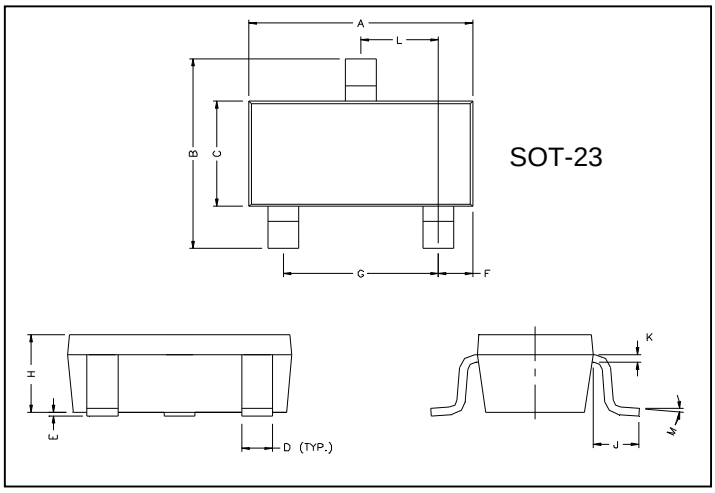
20V N-Channel Enhancement Mode MOSFET

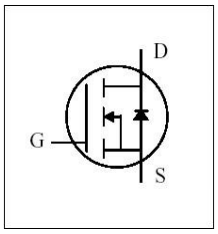
VDS= 20V
RDS(ON), Vgs@ 4.5V, Ids@ 3A ＜45mΩ
RDS(ON), Vgs@ 2.5V, Ids@ 2.5A ＜59mΩ

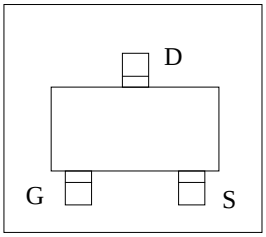
Features

Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance

Package Dimensions







REF.	Millimeter		REF.	Millimete	
	Min.	Max.		Min.	Max.
A	2.80	3.00	G	1.80	2.00
B	2.30	2.50	H	0.90	1.1
C	1.20	1.40	K	0.10	0.20
D	0.30	0.50	J	0.35	0.70
E	0	0.10	L	0.92	0.98
F	0.45	0.55	M	0°	10°

Maximum Ratings and Thermal Characteristics (TA = 25oC unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±10	
Continuous Drain Current		I_D	3	A
Pulsed Drain Current [1]		I_{DM}	12	
Maximum Power Dissipation [2]	TA = 25°C	P_D	1.25	W
	TA = 75°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) [2]		R_{thJA}	100	°C/W
Junction-to-Ambient Thermal Resistance (PCB mounted) [3]			166	

Notes
1) Pulse width limited by maximum junction temperature.
2) Surface Mounted on FR4 Board, t ≤ 5 sec.
3) Surface Mounted on FR4 Board.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Miax.	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250uA	20			V
Drain-Source On-State Resistance[1)]	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 3A		30	45	mΩ
		V_{GS} = 2.5V, I_D = 2.5A		37	59	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = 250uA	0.45		1.5	V
Zero Gate Voltage Drain Current 0	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V		1		uA
		V_{DS} = 16V, V_{GS} = 0V TJ=55°C			10	
Gate Body Leakage	I_{GSS}	V_{GS} = ± 10V, V_{DS} = 0V			±100	nA
Forward Transconductance[1)]	g_{fs}	V_{DS} = 5V, I_D = 3A		10	—	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 3A V_{GS} = 4.5V		5.4		nC
Gate-Source Charge	Q_{gs}			0.65		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, RL=5.5Ω I_D ≅ 3A,V_{GEN} = 4.5V R_G = 6Ω		12		ns
Turn-On Rise Time	t_r			36		
Turn-Off Delay Time	$t_{d(off)}$			34		
Turn-Off Fall Time	t_f			10		
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V f = 1.0 MHz		340		pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			33		
Source-Drain Diode						
Max. Diode Forward Current	I_S				1.6	A
Diode Forward Voltage	V_{SD}	I_S = 1.0A, V_{GS} = 0V			1.2	V

1) Pulse test: pulse width <= 300us, duty cycle<= 2%

Typical ElectricalL and Thermal Characteristics

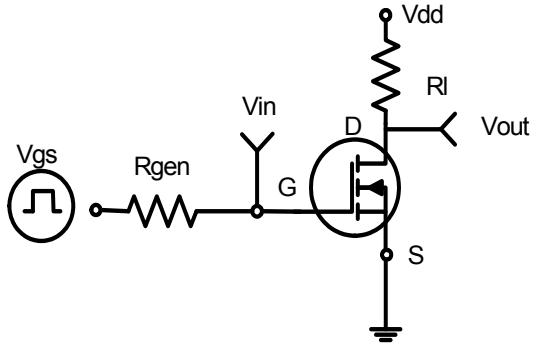


Figure 1:Switching Test Circuit

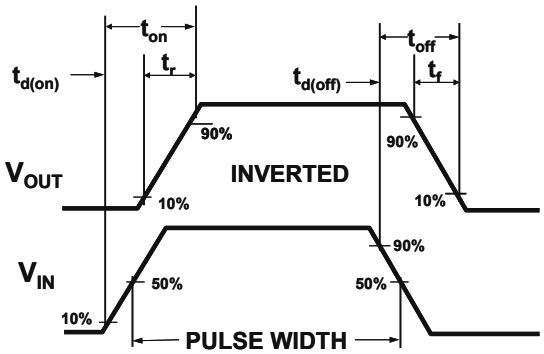


Figure 2:Switching Waveforms

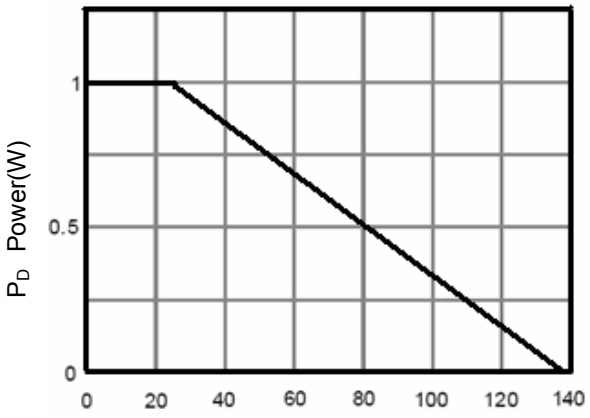


Figure 3 Power Dissipation

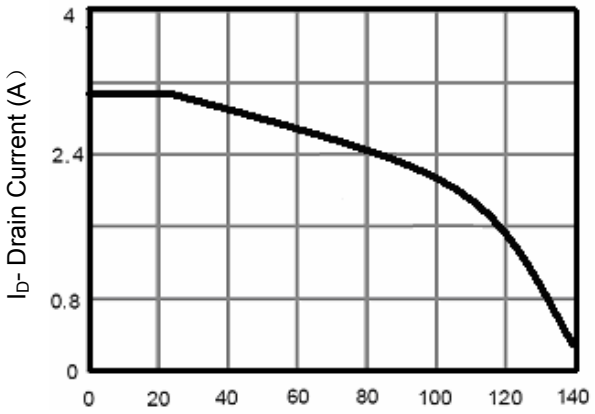


Figure 4 Drain Current

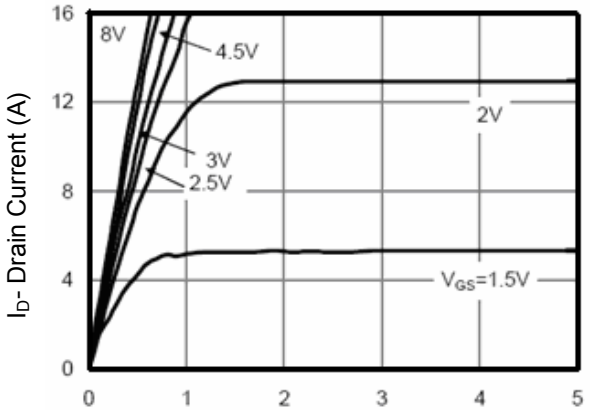


Figure 5 Output Characteristics

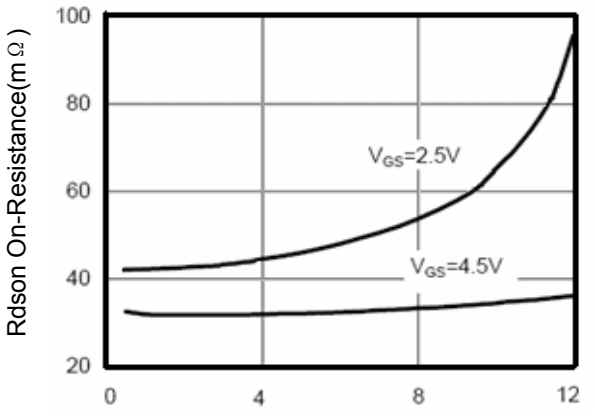


Figure 6 Drain-Source On-Resistance

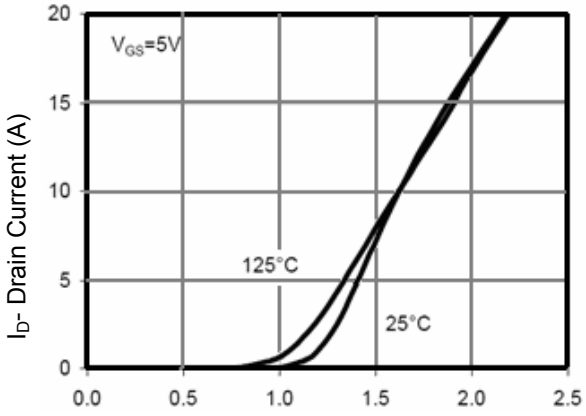


Figure 7 Transfer Characteristics

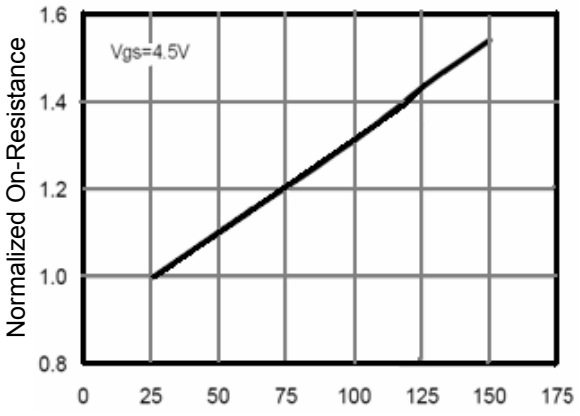


Figure 8 Drain-Source On-Resistance

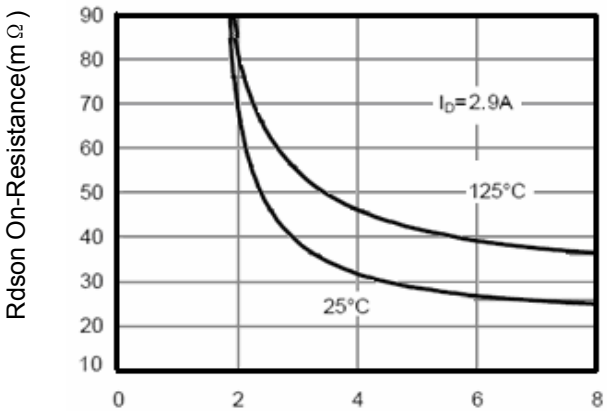


Figure 9 Rdson vs Vgs

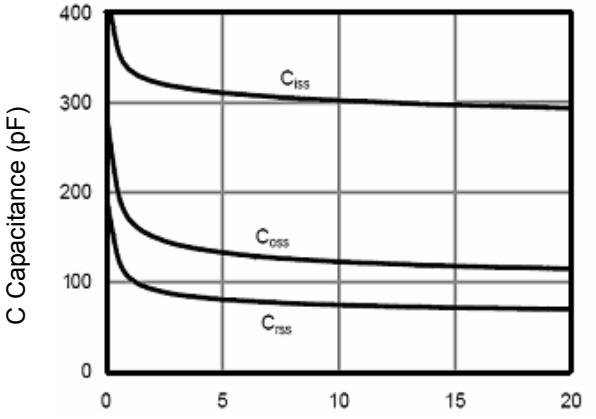


Figure 10 Capacitance vs Vds

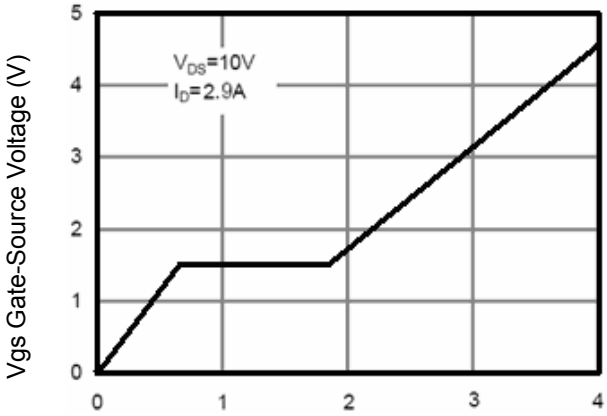


Figure 11 Gate Charge

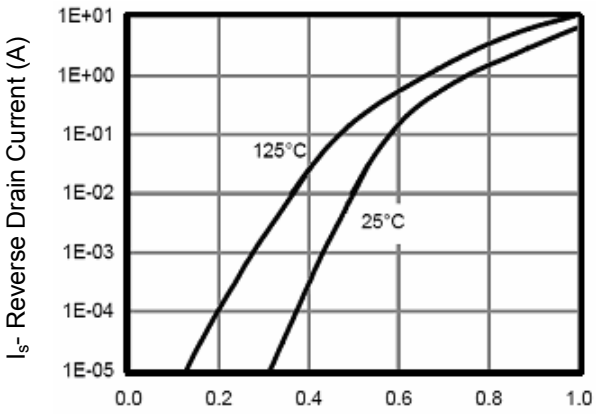


Figure 12 Source- Drain Diode Forward

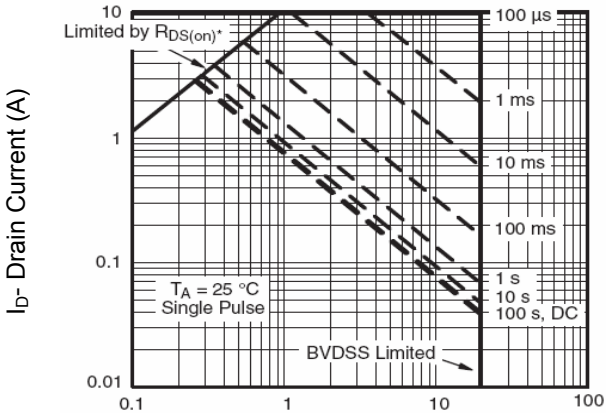


Figure 13 Safe Operation Area

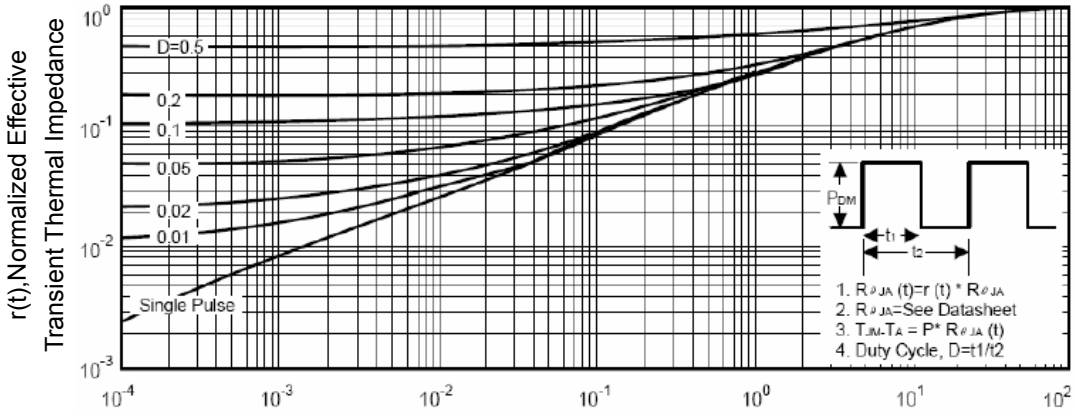


Figure 14 Normalized Maximum Transient Thermal Impedance