Ordering number : EN*5420

CMOS LSI

LC89962, LC89962M

NTSC Format Delay Line

Overview

The LC89962 and LC89962M are delay line circuits that provide a delayed signal by a 1H period of NTSC format with an external low-pass filter.

Features

- Requires only the input of a 3.58-MHz clock to produce a 1H delayed signal and the external low-pass filter.
- Uses a 5-V single-voltage power supply.
- Requires a minimal number of external components due to the peripheral components provided on chip.
- Output signal has the same phase as the input signal.
- Operation has a 4fsc clock synchronized with the input clock allows these products to be used as wide bandwidth delay lines.
- A 4fsc clock can be output from the 4FSC pin (pin 7).

Functions

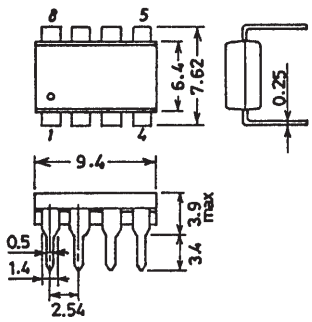
- 906-bit CCD shift register
- Timing generator and CCD driver circuits
- Auto-bias circuit
- Sync-tip clamp circuit
- Sample-and-hold and output amplifier circuits
- 4 × PLL circuit
- 4fsc output circuit

Package Dimensions

unit: mm

3001B-DIP8

[LC89962]

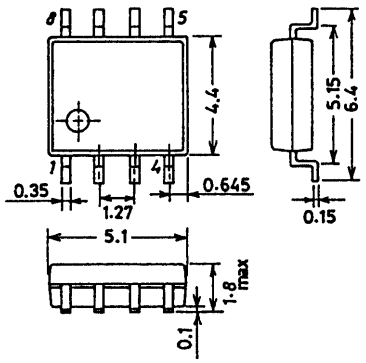


SANYO: DIP8

unit: mm

3032B-MFP8

[LC89962M]



SANYO: MFP8

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.0	V
Allowable power dissipation	Pd max	LC89962	400	mW
		LC89962M	140	mW
Operating temperature	Topr		–10 to +60	°C
Storage temperature	Tstg		–55 to +125	°C

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Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Clock input amplitude	V_{CLK}	Sine wave	200	300	500	mVp–p
Clock frequency	F_{CLK}			3.579545		MHz
Signal input amplitude	V_{IN}	(*1)		500	572	mVp–p

Note 1. The input signal must be input with low impedance for correct operation of sync-tip clamping.

Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0 V, CLK = 3.579545 MHz; 300 mV p-p

Parameter	Symbol	Switch states				min	typ	max	Unit
		SW1	SW2	SW3	Test conditions				
Supply current	I_{DD}	a	a	a	*1	5	15	25	mA
Voltage gain	G_V	a	b	a	*2	–2	0	+2	dB
Frequency characteristics	G_f	b	b	a	*3	–2	–1	0	dB
Differential gain	DG	a	a	a	*4	0	5		%
Differential phase	DP	a	a	a	*4	0	5		deg
Linearity	LS	a	a	a	*5	37	40	43	%
Clock leakage	Lck	a	b	a	*6		5	50	mVrms
Noise	N_O	a	b	a	*7		1	2	mVrms
Output impedance	Z_O	a	b	a↔b	*8	220	370	520	Ω
Delay time	TD	a	b	a	*9		63.33		µs

Test Conditions

1. The supply current with no input signal

2. The following formula is used to calculate the voltage gain (G_V).

$$G_V = 20\log \frac{V_{OUT}\ [\text{mVp-p}]}{500\ [\text{mVp-p}]}\ [\text{dB}]$$

Output signal symbol	Input signal
V_{OUT}	Sine wave: 200 kHz, 500 mV p-p

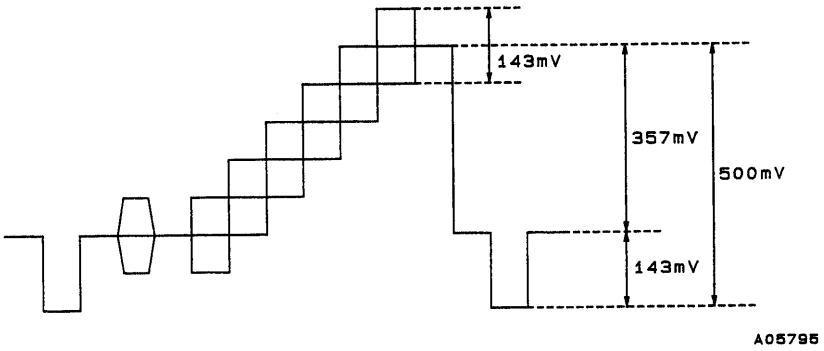
3. The following formula is used to calculate the frequency characteristics (Gf).

$$G_f = 20\log \frac{V2\ [\text{mVp-p}]}{V1\ [\text{mVp-p}]}\ [\text{dB}]$$

Output signal symbol	Input signal
V1	Sine wave: 200 kHz, 200 mV p-p
V2	Sine wave: 3.58 MHz, 200 mV p-p

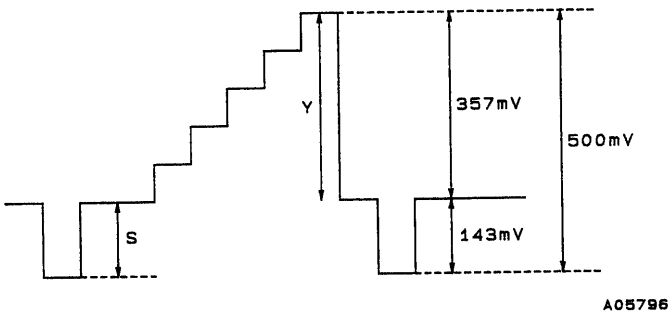
During this test, adjust Vbias so that the input signal DC level is 250 mV higher than the clamp level.

4. Measure the differential gain (DG) and differential phase (DP) using a vector scope with a 5-step function wave input. (See the following figure.)



5. To measure LS, input a 5-step function wave and measure the ratio of the sync level (S) to the luminance level (Y).

$$LS = \frac{S\ [mV]}{Y\ [mV]} \times 100\ [\%]$$



6. To measure clock leakage (Lck), measure the 4fsc (14.3 MHz) component in the output signal with a spectrum analyzer when no input signal is presented.

7. To measure the noise level (N_O), measure the noise output in the OUT pin output when no input signal is present with a video noise meter. Set up the noise meter with a 200-kHz high-pass filter, a 4.2-MHz low-pass filter, and 3.58-MHz trap filter.

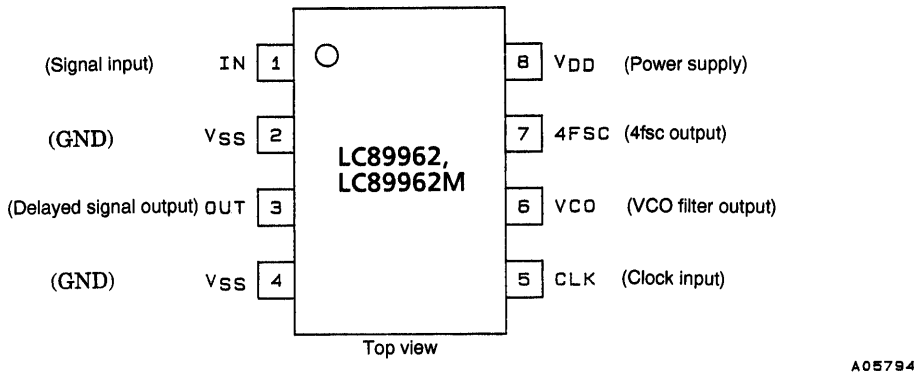
8. The following formula is used to calculate the output impedance (Z_O).

$$Z_O = \frac{V1\ [mVp\text{-}p] - V2\ [mVp\text{-}p]}{V2\ [mVp\text{-}p]} \times 500\ [\Omega]$$

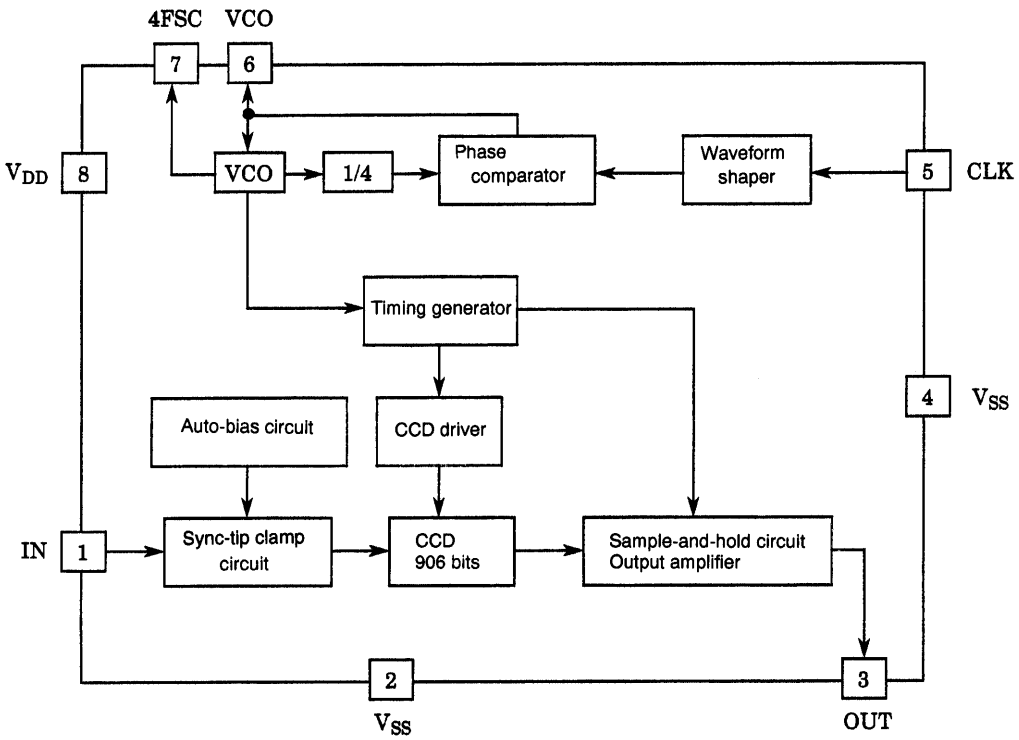
Output signal symbol	SW3	Input signal
V1	a	Sine wave: 200 kHz, 500 mV p-p
V2	b	

9. To measure the delay time (TD), measure the delay time of the output signal to the input signal. In this measurement, the delay time associated with the low-pass filter must be excluded.

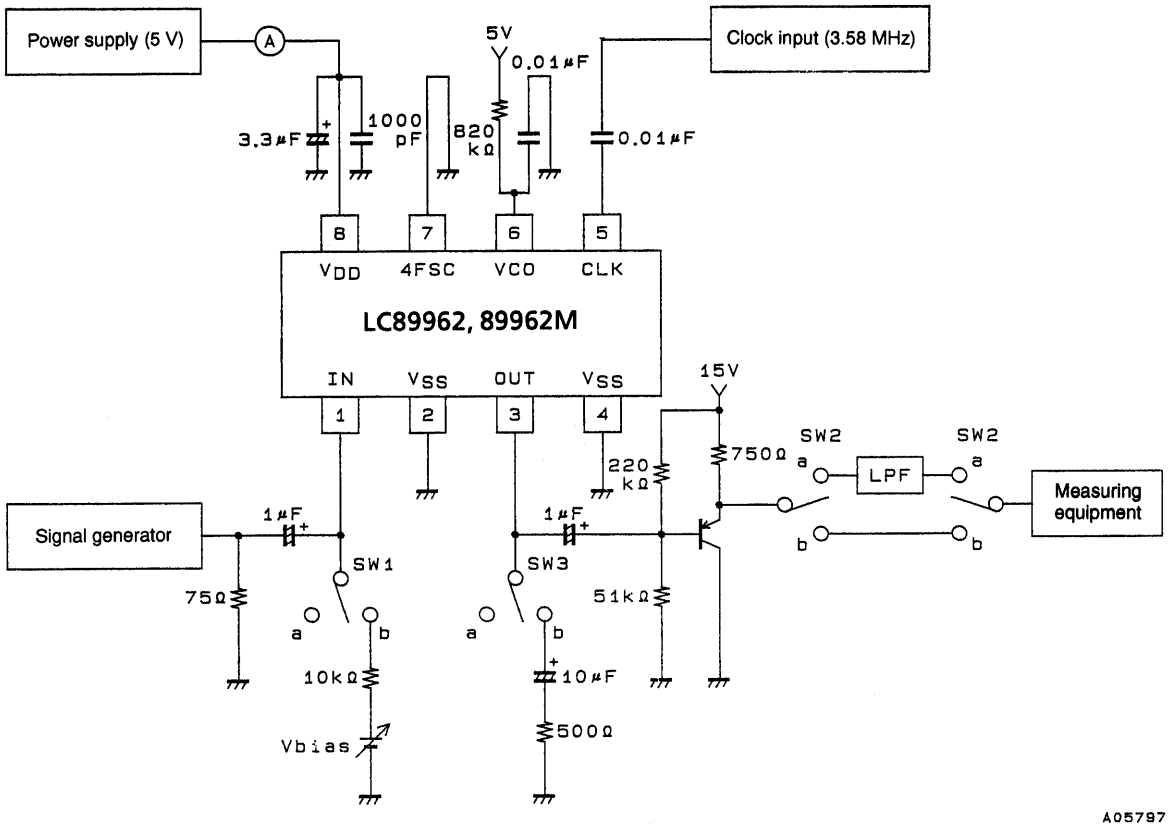
Pin Assignment



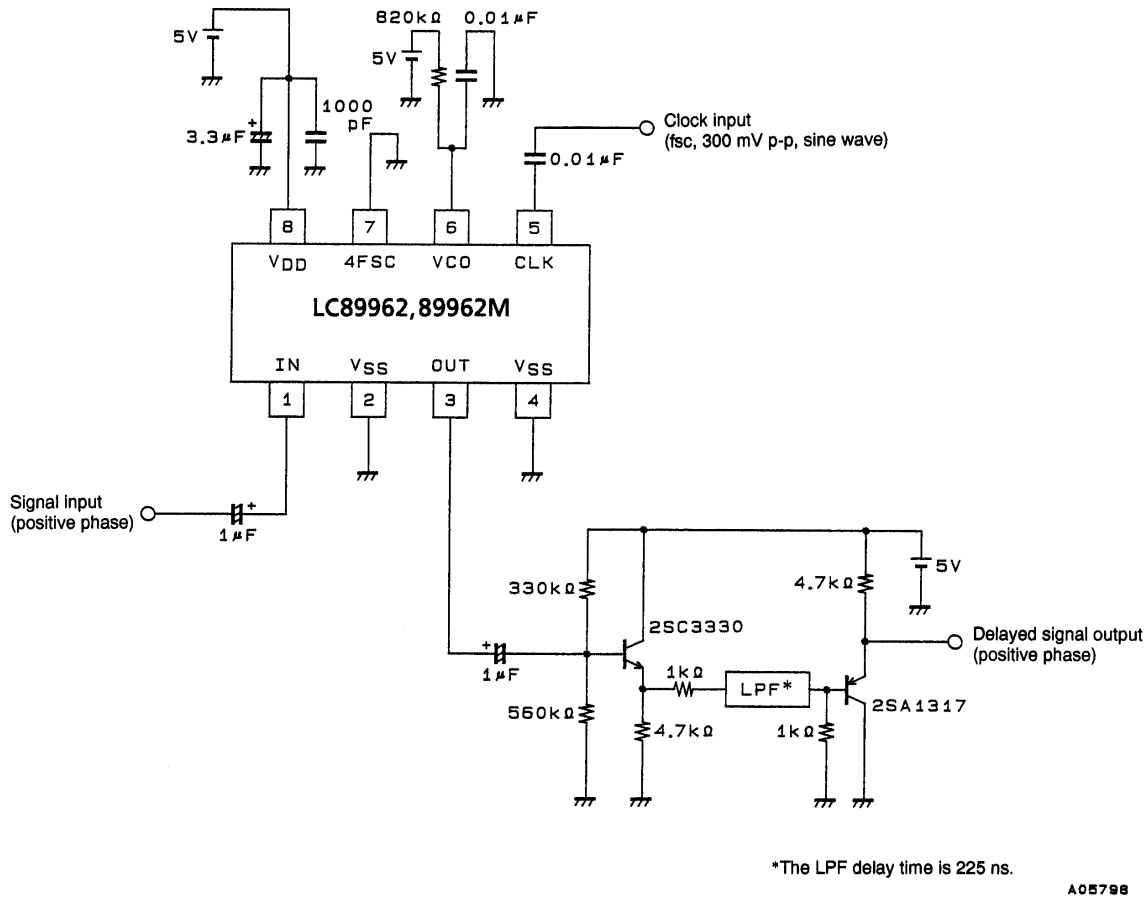
Block Diagram



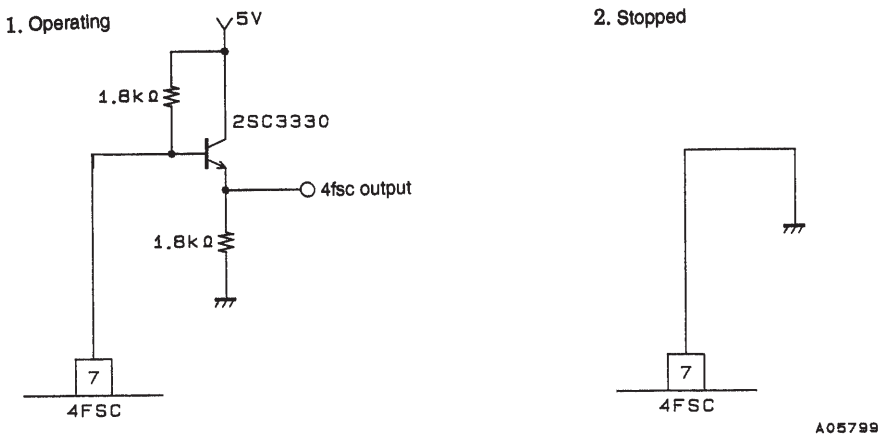
Test Circuit



Sample Application Circuit



4FSC (pin 7) Sample Application Circuit



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