

MUX50x

36V 低电容、低电荷注入、精密模拟多路复用器

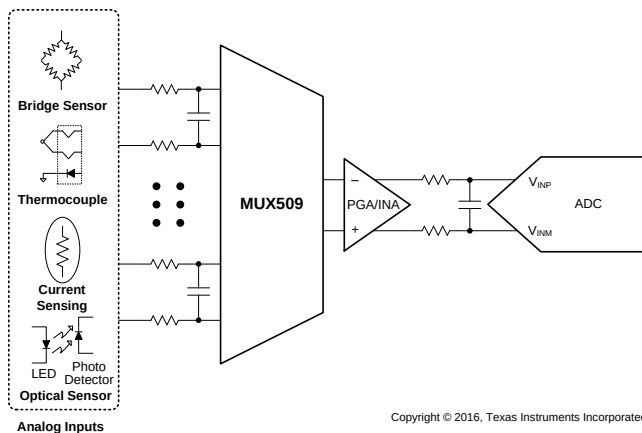
1 特性

- 低导通电容
 - MUX508: 9.4pF
 - MUX509: 6.7pF
- 低输入泄漏电流: 10pA
- 低电荷注入: 0.3pC
- 轨到轨运行
- 宽电源电压范围: $\pm 5\text{V}$ 至 $\pm 18\text{V}$ 或 10V 至 36V
- 低导通电阻: 125 Ω
- 转换时间: 92ns
- 先断后合开关操作
- EN 引脚与 V_{DD} 相连
- 逻辑电平: 2V 至 V_{DD}
- 低电源电流: 45 μA
- 人体放电模式 (HBM) 静电放电 (ESD) 保护 > 2000V
- 行业标准的薄型小外形尺寸 (TSSOP) 封装和小外形尺寸集成电路 (SOIC) 封装

2 应用

- 工厂自动化和工业过程控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- 自动测试设备 (ATE)
- 数字万用表
- 电池监控系统

简化电路原理图



3 说明

MUX508 和 MUX509 (MUX50x) 是现代互补金属氧化物半导体 (CMOS) 模拟多路复用器 (mux)。MUX508 提供 8:1 单端通道, 而 MUX509 提供 4:1 差分通道或双 4:1 单端通道。MUX508 和 MUX509 在双电源 ($\pm 5\text{V}$ 至 $\pm 18\text{V}$) 或单电源 (10V 至 36V) 供电时均能正常运行。两种器件在由对称电源 (如 $V_{DD} = 12\text{V}$, $V_{SS} = -12\text{V}$) 和非对称电源 (如 $V_{DD} = 12\text{V}$, $V_{SS} = -5\text{V}$) 供电时也能保证优异性能。所有数字输入具有兼容晶体管-晶体管逻辑电路 (TTL) 的阈值。当器件在有效电源电压范围内运行时, 该阈值可确保 TTL 和 CMOS 逻辑电路的兼容性。

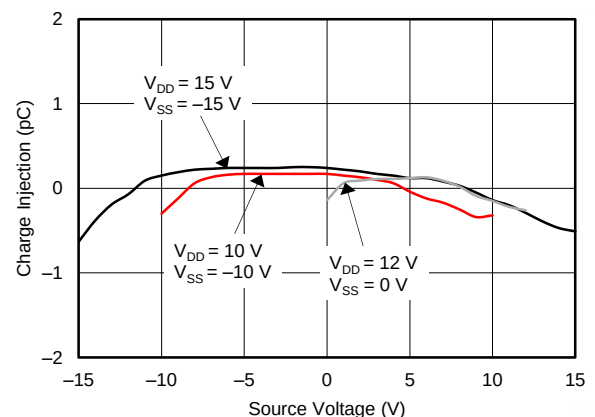
MUX508 和 MUX509 这两款多路复用器的导通和关断泄漏电流都非常低, 因此能够以最小误差切换高输入阻抗源信号。该器件的电源电流低至 45 μA , 因此适用于便携式进行 VTT 放电。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
MUX50x	TSSOP (16)	5.00mm x 4.40mm
	SOIC (16)	9.90mm x 3.91mm

(1) 要了解所有可用封装, 请参见数据表末尾的封装选项附录。

电荷注入与源电压间的关系



目录

1	特性	1	8.10	Channel-to-Channel Crosstalk	21
2	应用	1	8.11	Bandwidth	22
3	说明	1	8.12	THD + Noise	22
4	修订历史记录	2	9	Detailed Description	23
5	Device Comparison Table	4	9.1	Overview	23
6	Pin Configuration and Functions	4	9.2	Functional Block Diagram	23
7	Specifications	6	9.3	Feature Description	24
7.1	Absolute Maximum Ratings	6	9.4	Device Functional Modes	26
7.2	ESD Ratings	6	10	Applications and Implementation	27
7.3	Recommended Operating Conditions	6	10.1	Application Information	27
7.4	Thermal Information	7	10.2	Typical Application	27
7.5	Electrical Characteristics: Dual Supply	7	11	Power-Supply Recommendations	29
7.6	Electrical Characteristics: Single Supply	9	12	Layout	30
7.7	Typical Characteristics	11	12.1	Layout Guidelines	30
8	Parameter Measurement Information	15	12.2	Layout Example	30
8.1	Truth Tables	15	13	器件和文档支持	31
8.2	On-Resistance	16	13.1	文档支持	31
8.3	Off-Leakage Current	16	13.2	相关链接	31
8.4	On-Leakage Current	17	13.3	接收文档更新通知	31
8.5	Transition Time	17	13.4	社区资源	31
8.6	Break-Before-Make Delay	18	13.5	商标	31
8.7	Turn-On and Turn-Off Time	19	13.6	静电放电警告	31
8.8	Charge Injection	20	13.7	Glossary	31
8.9	Off Isolation	21	14	机械、封装和可订购信息	31

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (July 2016) to Revision C	Page
• 已将 D (SOIC) 封装添加至文档	1
• 已更改最后的 特性 分项以包括 SOIC 封装	1
• 已更改“描述”部分的第 部分	1
• 已将 SOIC 封装添加至 器件信息表	1
• Changed MUX509 description in <i>Device Comparison Table</i>	4
• Added D package to <i>Pin Configuration and Functions</i> section	4
• Added D package to <i>Thermal Information</i> table	7
• Changed Analog Switch, I_D parameter in <i>Electrical Characteristics: Dual Supply</i> table: split parameter into $I_{D(ON)}$ and $I_{D(OFF)}$ parameters, changed symbols, parameter names, and test conditions	7
• Changed <i>On-resistance drift</i> parameter in <i>Electrical Characteristics: Single Supply</i> table: changed V_S value in test conditions	9
• Changed Analog Switch, I_D parameter in <i>Electrical Characteristics: Single Supply</i> table: split parameter into $I_{D(ON)}$ and $I_{D(OFF)}$ parameters, changed symbols, parameter names, and $I_{D(ON)}$ test conditions	9
• Changed Figure 26 : changed switch symbol to a closed switch symbol	16
• Changed Figure 32 : added 0 V line, flipped V_S supply symbol	20
• Changed description of MUX509 in <i>Overview</i> section	23
• Changed Figure 42 : changed OPA140 amplifier and charge kickback filter box	27
• Added D package description to <i>Layout Guidelines</i> section	30

Changes from Revision A (March 2016) to Revision B**Page**

-
- 已增加 TI 设计 [1](#)
 - Changed Analog Switch, $I_{S(OFF)}$ and I_D parameter specifications in *Electrical Characteristics: Single Supply* table..... [9](#)
-

Changes from Original (January 2016) to Revision A**Page**

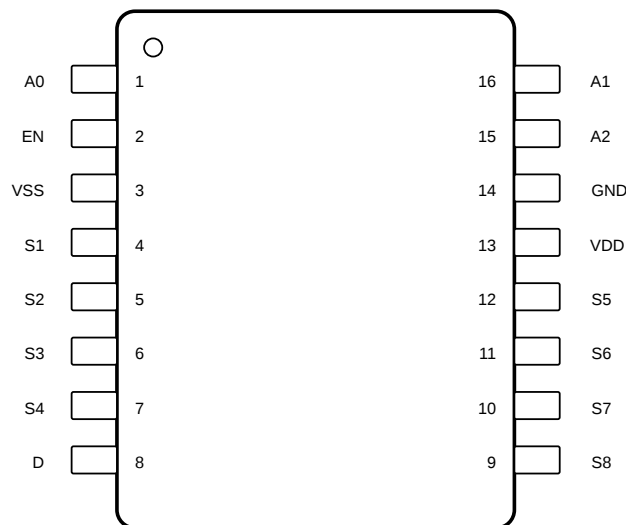
-
- 已将“产品预览”更改为“量产数据” [1](#)
-

5 Device Comparison Table

PRODUCT	DESCRIPTION
MUX508	8-channel, single-ended analog multiplexer (8:1 mux)
MUX509	4-channel differential or dual 4:1 single-ended analog multiplexer (8:2 mux)

6 Pin Configuration and Functions

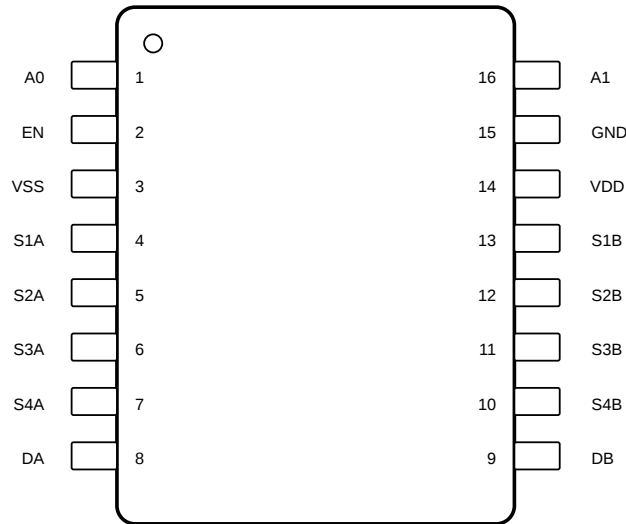
**MUX508: PW and D Packages
16-Pin TSSOP and SOIC
Top View**



Pin Functions: MUX508

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	1	Digital input	Address line 0
A1	16	Digital input	Address line 1
A2	15	Digital input	Address line 2
D	8	Analog input or output	Drain pin. Can be an input or output.
EN	2	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[2:0] logic inputs determine which switch is turned on.
GND	14	Power supply	Ground (0 V) reference
S1	4	Analog input or output	Source pin 1. Can be an input or output.
S2	5	Analog input or output	Source pin 2. Can be an input or output.
S3	6	Analog input or output	Source pin 3. Can be an input or output.
S4	7	Analog input or output	Source pin 4. Can be an input or output.
S5	12	Analog input or output	Source pin 5. Can be an input or output.
S6	11	Analog input or output	Source pin 6. Can be an input or output.
S7	10	Analog input or output	Source pin 7. Can be an input or output.
S8	9	Analog input or output	Source pin 8. Can be an input or output.
VDD	13	Power supply	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between VDD and GND.
VSS	3	Power supply	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between VSS and GND.

**MUX509: PW and D Packages
16-Pin TSSOP and SOIC
Top View**



Pin Functions: MUX509

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	1	Digital input	Address line 0
A1	16	Digital input	Address line 1
DA	8	Analog input or output	Drain pin A. Can be an input or output.
DB	9	Analog input or output	Drain pin B. Can be an input or output.
EN	2	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[1:0] logic inputs determine which pair of switches is turned on.
GND	15	Power supply	Ground (0 V) reference
S1A	4	Analog input or output	Source pin 1A. Can be an input or output.
S2A	5	Analog input or output	Source pin 2A. Can be an input or output.
S3A	6	Analog input or output	Source pin 3A. Can be an input or output.
S4A	7	Analog input or output	Source pin 4A. Can be an input or output.
S1B	13	Analog input or output	Source pin 1B. Can be an input or output.
S2B	12	Analog input or output	Source pin 2B. Can be an input or output.
S3B	11	Analog input or output	Source pin 3B. Can be an input or output.
S4B	10	Analog input or output	Source pin 4B. Can be an input or output.
VDD	14	Power supply	Positive power supply. This pin is the most positive power supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between VDD and GND.
VSS	3	Power supply	Negative power supply. This pin is the most negative power supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between VSS and GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage	V_{DD}		–0.3	40	V
	V_{SS}		–40	0.3	
	$V_{DD} - V_{SS}$			40	
Digital input pins ⁽²⁾	EN, A0, A1, A2 pins	Voltage	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
		Current	–30	30	mA
Analog input pins ⁽²⁾	Sx, SxA, SxB pins	Voltage	$V_{SS} - 2$	$V_{DD} + 2$	V
		Current	–30	30	mA
Analog output pins ⁽²⁾	D, DA, DB pins	Voltage	$V_{SS} - 2$	$V_{DD} + 2$	V
		Current	–30	30	mA
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Only one pin at a time

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD} ⁽¹⁾	Positive power-supply voltage	Dual supply	5		18	V
		Single supply	10		36	
V_{SS} ⁽²⁾	Negative power-supply voltage (dual supply)		–5		–18	V
$V_{DD} - V_{SS}$	Supply voltage		10		36	V
V_S	Source pins voltage ⁽³⁾		V_{SS}		V_{DD}	V
V_D	Drain pins voltage		V_{SS}		V_{DD}	V
V_{EN}	Enable pin voltage		V_{SS}		V_{DD}	V
V_A	Address pins voltage		V_{SS}		V_{DD}	V
I_{CH}	Channel current ($T_A = 25^\circ\text{C}$)		–25		25	mA
T_A	Operating temperature		–40		125	°C

(1) When $V_{SS} = 0$ V, V_{DD} can range from 10 V to 36 V.

(2) V_{DD} and V_{SS} can be any value as long as $10\text{ V} \leq (V_{DD} - V_{SS}) \leq 36\text{ V}$, and $V_{DD} \geq 5\text{ V}$.

(3) V_S is the voltage on all the S pins.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		MUX50x		UNIT
		PW (TSSOP)	D (SOIC)	
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	103.8	78.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	36.8	37.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	49.8	35.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2.7	8.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	49.1	35.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#).

7.5 Electrical Characteristics: Dual Supply

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
Analog signal range		T _A = −40°C to +125°C		V _{SS}		V _{DD}	V
R _{ON}	On-resistance	V _S = 0 V, I _{CH} = 1 mA		125		170	Ω
				145		200	
		V _S = ±10 V, I _{CH} = 1 mA	T _A = −40°C to +85°C			230	
			T _A = −40°C to +125°C			250	
ΔR _{ON}	On-resistance mismatch between channels	V _S = ±10 V, I _{CH} = 1 mA		2.4		6	Ω
			T _A = −40°C to +85°C			9	
			T _A = −40°C to +125°C			11	
R _{FLAT}	On-resistance flatness	V _S = 10 V, 0 V, −10 V		22		45	Ω
			T _A = −40°C to +85°C			53	
			T _A = −40°C to +125°C			58	
On-resistance drift		V _S = 0 V		0.52			%/°C
I _{S(OFF)}	Input leakage current	Switch state is off, V _S = ±10 V, V _D = ±10 V ⁽¹⁾		−1	0.01	1	nA
			T _A = −40°C to +85°C	−10		10	
			T _A = −40°C to +125°C	−25		25	
I _{D(OFF)}	Output off leakage current	Switch state is off, V _S = ±10 V, V _D = ±10 V ⁽¹⁾		−1	0.01	1	nA
			T _A = −40°C to +85°C	−10		10	
			T _A = −40°C to +125°C	−50		50	
I _{D(ON)}	Output on leakage current	Switch state is on, V _D = ±10 V, V _S = floating		−1	0.01	1	nA
			T _A = −40°C to +85°C	−10		10	
			T _A = −40°C to +125°C	−50		50	
LOGIC INPUT							
V _{IH}	High-level input voltage			2.0			V
V _{IL}	Low-level input voltage					0.8	V
I _D	Input current					0.15	μA

(1) When V_S is positive, V_D is negative, and vice versa.

MUX508, MUX509

ZHCSEV2C – JANUARY 2016 – REVISED SEPTEMBER 2016

www.ti.com.cn

Electrical Characteristics: Dual Supply (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SWITCH DYNAMICS ⁽²⁾							
t _{ON}	Enable turn-on time	V _S = ±10 V, R _L = 300 Ω, C _L = 35 pF		88	136	ns	
			T _A = −40°C to +85°C		144		
			T _A = −40°C to +125°C		151		
t _{OFF}	Enable turn-off time	V _S = ±10 V, R _L = 300 Ω, C _L = 35 pF		63	75	ns	
			T _A = −40°C to +85°C		83		
			T _A = −40°C to +125°C		90		
t _t	Transition time	V _S = 10 V, R _L = 300 Ω, C _L = 35 pF,		92	143	ns	
			T _A = −40°C to +85°C		151		
			T _A = −40°C to +125°C		157		
t _{BBM}	Break-before-make time delay	V _S = 10 V, R _L = 300 Ω, C _L = 35 pF, T _A = −40°C to +125°C		30	54	ns	
Q _J	Charge injection	C _L = 1 nF, R _S = 0 Ω	V _S = 0 V	0.3	pC		
			V _S = −15 V to +15 V	±0.6			
	Off-isolation	R _L = 50 Ω, V _S = 1 V _{RMS} , f = 1 MHz	Nonadjacent channel to D, DA, DB	−96	dB		
			Adjacent channel to D, DA, DB	−85			
	Channel-to-channel crosstalk	R _L = 50 Ω, V _S = 1 V _{RMS} , f = 1 MHz	Nonadjacent channels	−96	dB		
			Adjacent channels	−88			
C _{S(OFF)}	Input off-capacitance	f = 1 MHz, V _S = 0 V		2.4	2.9	pF	
C _{D(OFF)}	Output off-capacitance	f = 1 MHz, V _S = 0 V	MUX508	7.5	8.4	pF	
			MUX509	4.3	5		
C _{D(ON)}	Input/Output on-capacitance	f = 1 MHz, V _S = 0 V	MUX508	9.4	10.6	pF	
			MUX509	6.7	7.7		
POWER SUPPLY							
V _{DD}	supply current	All V _A = 0 V or 3.3 V, V _S = 0 V, V _{EN} = 3.3 V,		45	59	μA	
			T _A = −40°C to +85°C		62		
			T _A = −40°C to +125°C		83		
V _{SS}	supply current	All V _A = 0 V or 3.3 V, V _S = 0 V, V _{EN} = 3.3 V,		25	34	μA	
			T _A = −40°C to +85°C		37		
			T _A = −40°C to +125°C		57		

(2) Specified by design, not production tested.

7.6 Electrical Characteristics: Single Supply

at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
Analog signal range		T _A = −40°C to +125°C		V _{SS}		V _{DD}	V
R _{ON}	On-resistance	V _S = 10 V, I _{CH} = 1 mA		235		340	Ω
			T _A = −40°C to +85°C			390	
			T _A = −40°C to +125°C			430	
ΔR _{ON}	On-resistance match	V _S = 10 V, I _{CH} = 1 mA		3.1		12	Ω
			T _A = −40°C to +85°C			19	
			T _A = −40°C to +125°C			23	
On-resistance drift		V _S = 10 V		0.47			%/°C
I _{S(OFF)}	Input leakage current	Switch state is off, V _S = 1 V and V _D = 10 V, or V _S = 10 V and V _D = 1 V ⁽²⁾		−1	0.01	1	nA
			T _A = −40°C to +85°C	−10		10	
			T _A = −40°C to +125°C	−25		25	
I _{D(OFF)}	Output off leakage current	Switch state is off, V _S = 1 V and V _D = 10 V, or V _S = 10 V and V _D = 1 V ⁽²⁾		−1	0.01	1	nA
			T _A = −40°C to +85°C	−10		10	
			T _A = −40°C to +125°C	−50		50	
I _{D(ON)}	Output on leakage current	Switch state is on, V _D = 1 V and 10 V, V _S = floating		−1	0.01	1	nA
			T _A = −40°C to +85°C	−10		10	
			T _A = −40°C to +125°C	−50		50	
LOGIC INPUT							
V _{IH}	High-level input voltage			2.0			V
V _{IL}	Low-level input voltage					0.8	V
I _D	Input current					0.15	μA
SWITCH DYNAMIC CHARACTERISTICS							
t _{ON}	Enable turn-on time	V _S = 8 V, R _L = 300 Ω, C _L = 35 pF		85		140	ns
			T _A = −40°C to +85°C			145	
			T _A = −40°C to +125°C			149	
t _{OFF}	Enable turn-off time	V _S = 8 V, R _L = 300 Ω, C _L = 35 pF		48		83	ns
			T _A = −40°C to +85°C			94	
			T _A = −40°C to +125°C			102	
t _t	Transition time	V _S = 8 V, C _L = 35 pF		87		147	ns
		V _S = 8 V, R _L = 300 Ω, C _L = 35 pF,	T _A = −40°C to +85°C			153	
		V _S = 8 V, R _L = 300 Ω, C _L = 35 pF,	T _A = −40°C to +125°C			155	
t _{BBM}	Break-before-make time delay	V _S = 8 V, R _L = 300 Ω, C _L = 35 pF, T _A = −40°C to +125°C		30	54		ns
Q _J	Charge injection	C _L = 1 nF, R _S = 0 Ω	V _S = 6 V	0.15			pC
			V _S = 0 V to 12 V,	±0.4			
	Off-isolation	R _L = 50 Ω, V _S = 1 V _{RMS} , f = 1 MHz	Nonadjacent channel to D, DA, DB	-96			dB
			Adjacent channel to D, DA, DB	-85			
	Channel-to-channel crosstalk	R _L = 50 Ω, V _S = 1 V _{RMS} , f = 1 MHz	Nonadjacent channels	−96			dB
			Adjacent channels	-88			
C _{S(OFF)}	Input off-capacitance	f = 1 MHz, V _S = 6 V		2.7	3.2		pF
C _{D(OFF)}	Output off-capacitance	f = 1 MHz, V _S = 6 V	MUX508	9.1	10		pF
			MUX509	5	5.7		
C _{D(ON)}	Input/Output on-capacitance	f = 1 MHz, V _S = 6 V	MUX508	10.8	12		pF
			MUX509	6.9	8		

(1) Specified by design, not production tested.

(2) When V_S is 1 V, V_D is 10 V, and vice versa.

MUX508, MUX509

ZHCSEV2C – JANUARY 2016 – REVISED SEPTEMBER 2016

www.ti.com.cn
Electrical Characteristics: Single Supply (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY					
V_{DD} supply current	All $V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$, $V_{EN} = 3.3\text{ V}$		42	53	μA
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		56	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		77	
V_{SS} supply current	All $V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$, $V_{EN} = 3.3\text{ V}$		23	38	μA
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		31	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		51	

7.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

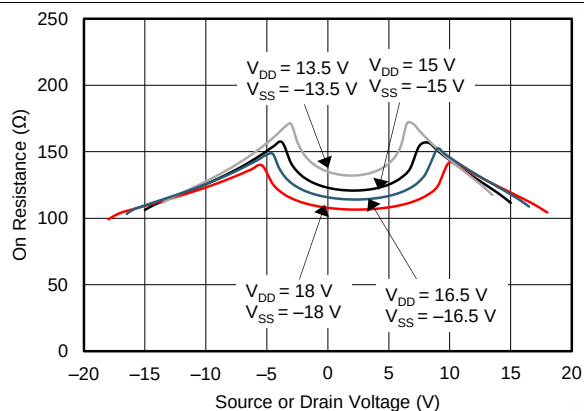
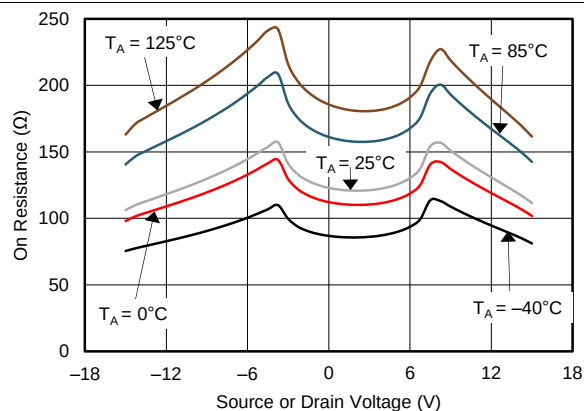


Figure 1. On-Resistance vs Source or Drain Voltage



$V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$

Figure 2. On-Resistance vs Source or Drain Voltage

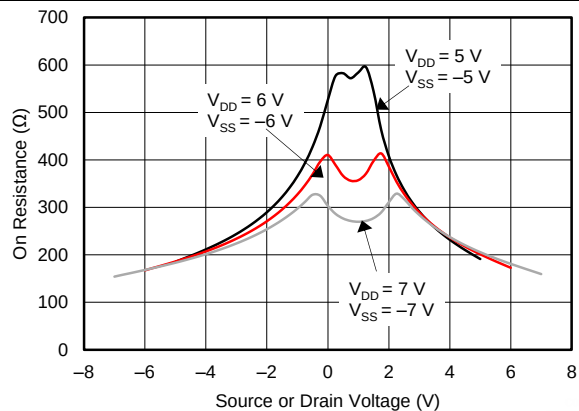
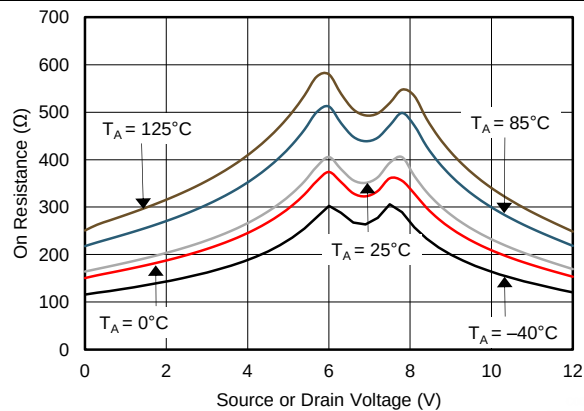


Figure 3. On-Resistance vs Source or Drain Voltage



$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 4. On-Resistance vs Source or Drain Voltage

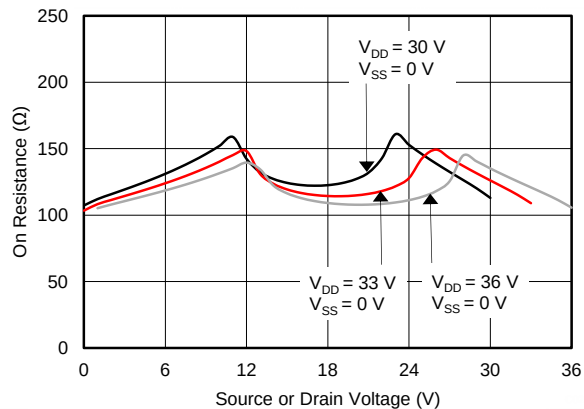


Figure 5. On-Resistance vs Source or Drain Voltage

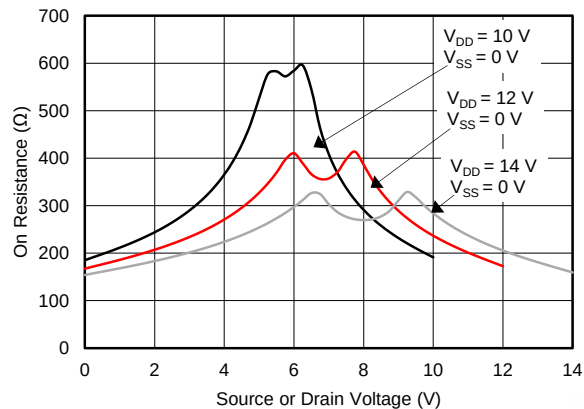


Figure 6. On-Resistance vs Source or Drain Voltage

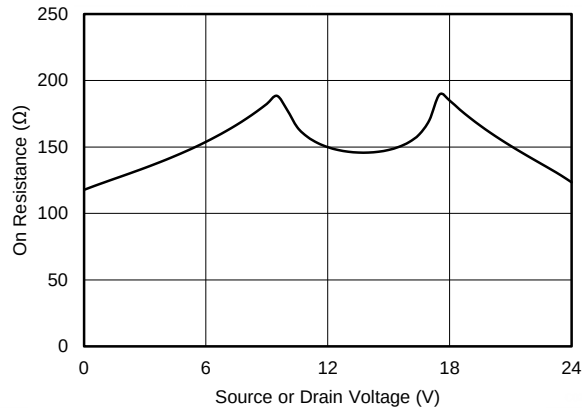
MUX508, MUX509

ZHCSEV2C – JANUARY 2016 – REVISED SEPTEMBER 2016

www.ti.com.cn

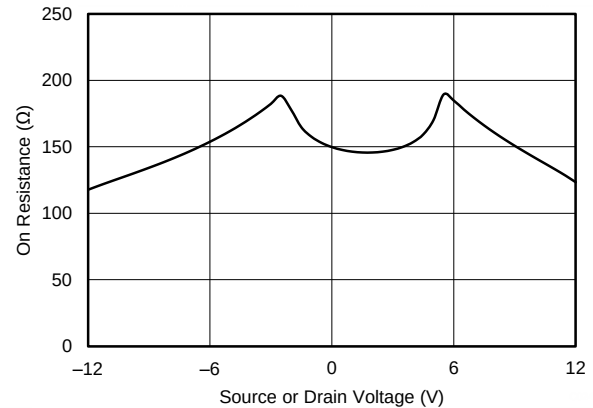
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)



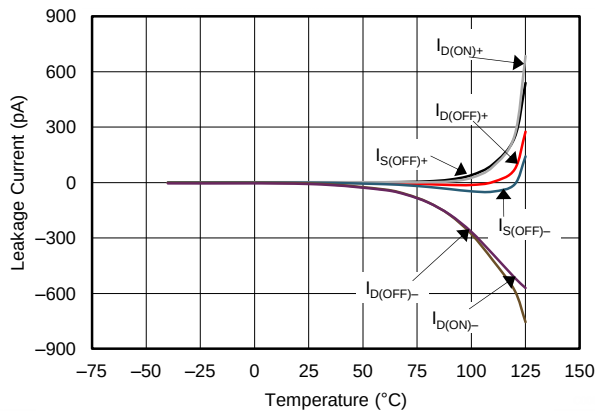
$V_{DD} = 24\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 7. On-Resistance vs Source or Drain Voltage



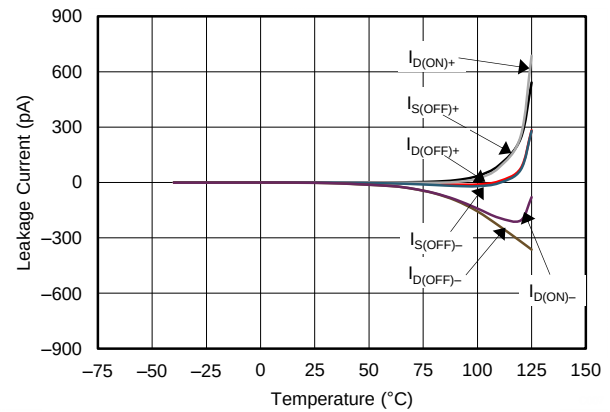
$V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$

Figure 8. On-Resistance vs Source or Drain Voltage



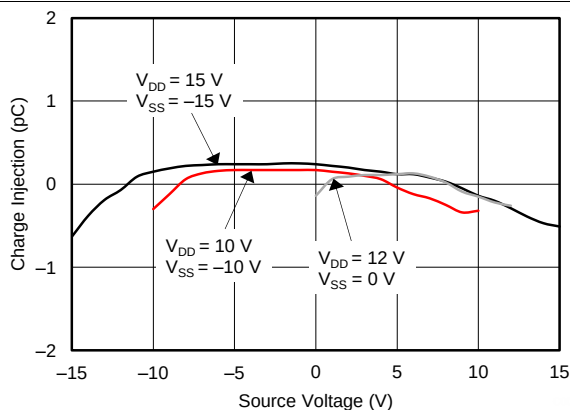
$V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$

Figure 9. Leakage Current vs Temperature



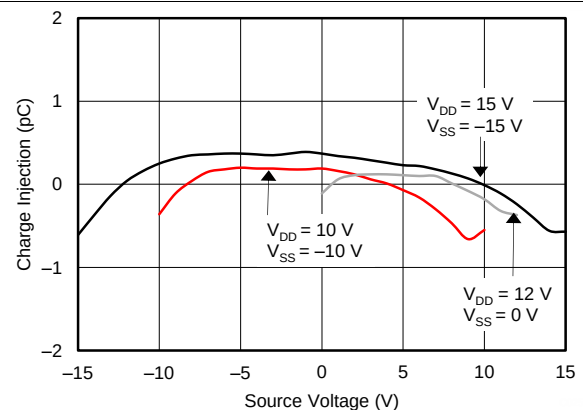
$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 10. Leakage Current vs Temperature



MUX508, source-to-drain

Figure 11. Charge Injection vs Source Voltage

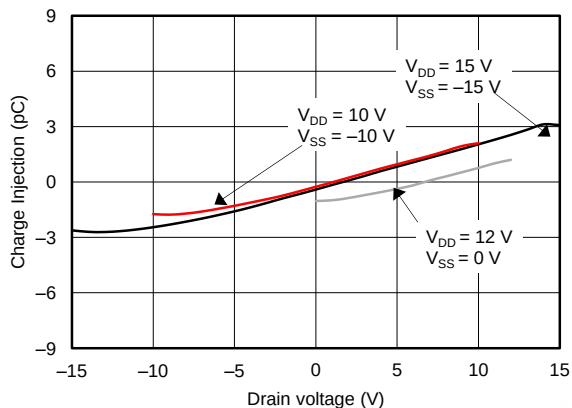


MUX509, source-to-drain

Figure 12. Charge Injection vs Source Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)



Drain-to-source

Figure 13. Charge Injection vs Source or Drain Voltage

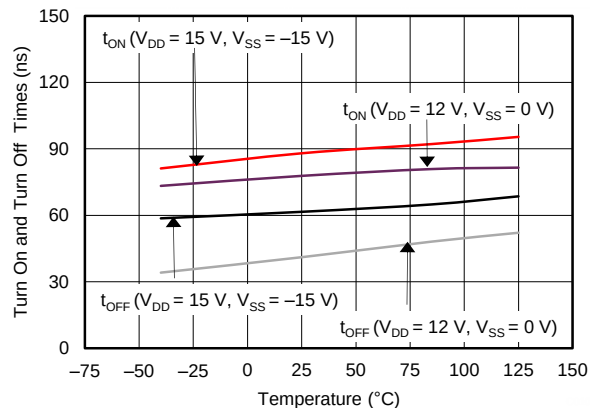


Figure 14. Turn-On and Turn-Off Times vs Temperature

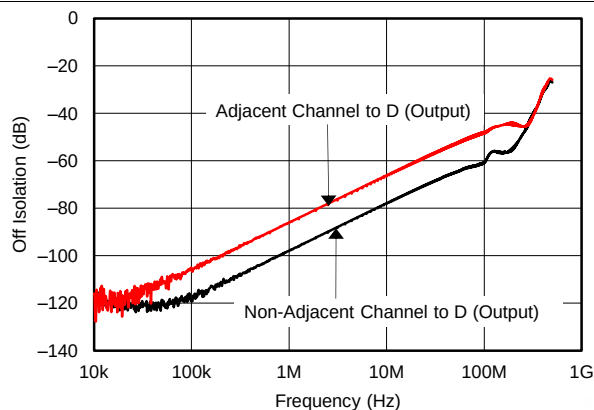


Figure 15. Off Isolation vs Frequency

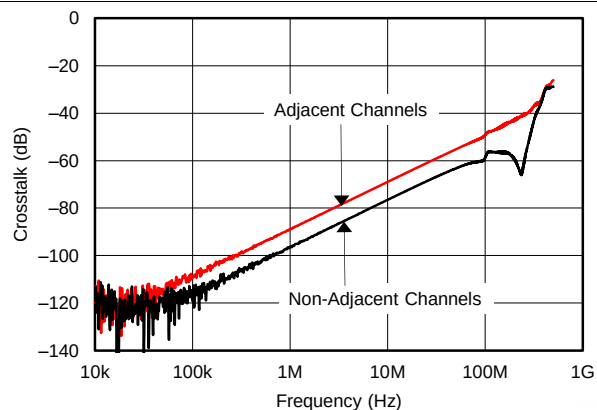


Figure 16. Crosstalk vs Frequency

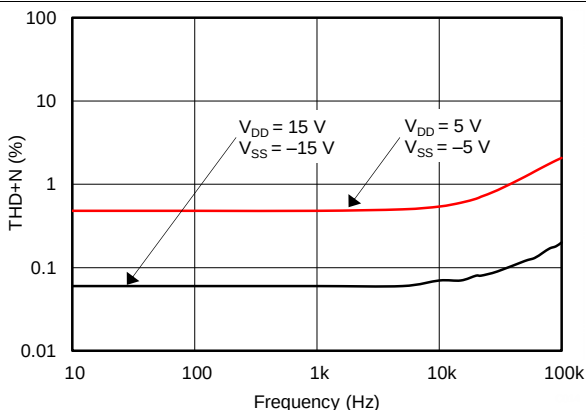


Figure 17. THD+N vs Frequency

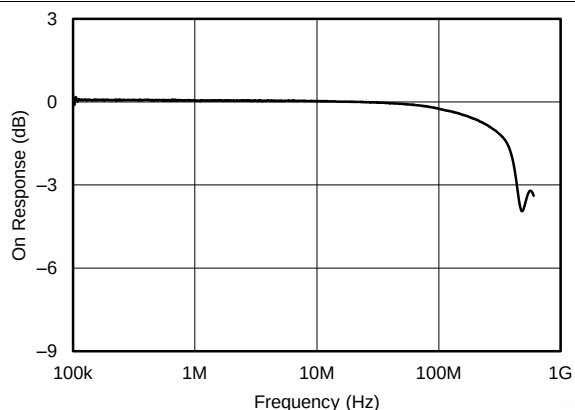


Figure 18. On Response vs Frequency

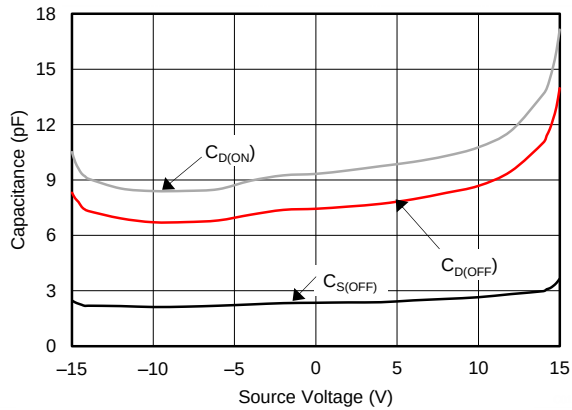
MUX508, MUX509

ZHCSEV2C – JANUARY 2016 – REVISED SEPTEMBER 2016

www.ti.com.cn

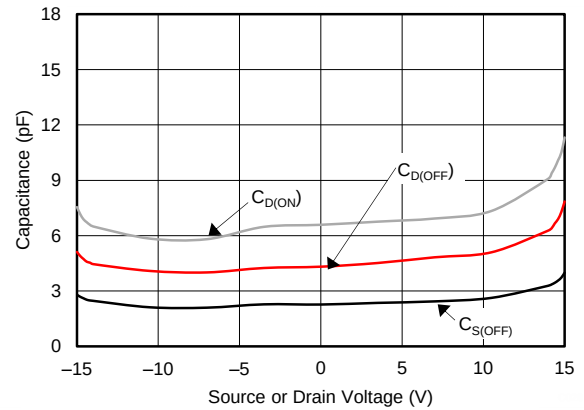
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)



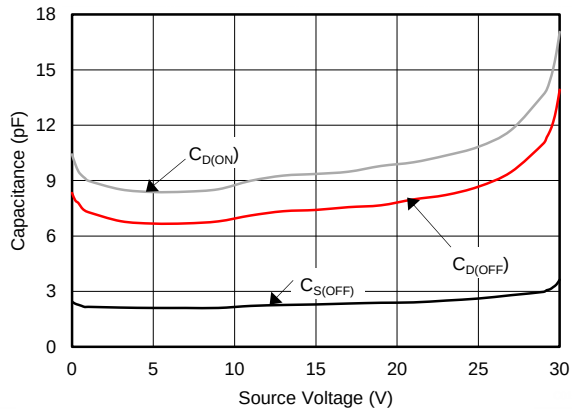
MUX508, $V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$

Figure 19. Capacitance vs Source Voltage



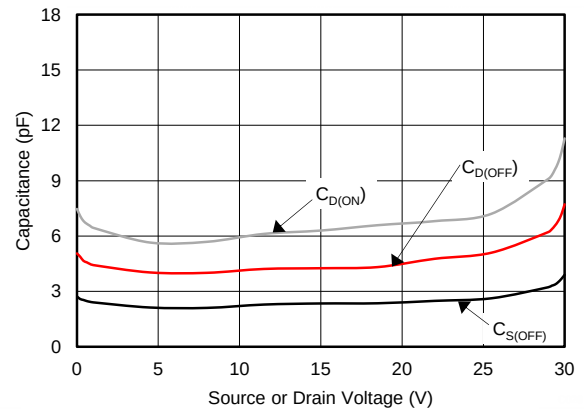
MUX509, $V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$

Figure 20. Capacitance vs Source Voltage



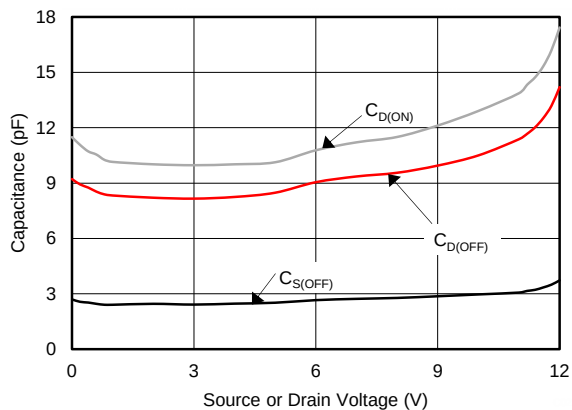
MUX508, $V_{DD} = 30\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 21. Capacitance vs Source Voltage



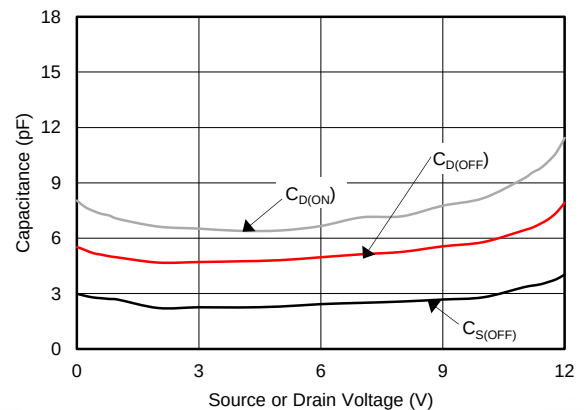
MUX509, $V_{DD} = 30\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 22. Capacitance vs Source Voltage



MUX508, $V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 23. Capacitance vs Source Voltage



MUX509, $V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 24. Capacitance vs Source Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

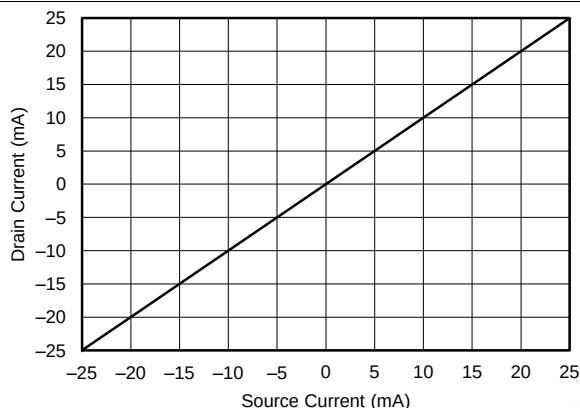


Figure 25. Source Current vs Drain Current

8 Parameter Measurement Information

8.1 Truth Tables

Table 1 and Table 2 show the truth tables for the MUX508 and MUX509, respectively.

Table 1. MUX508 Truth Table

EN	A2	A1	A0	STATE
0	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	All channels are off
1	0	0	0	Channel 1 on
1	0	0	1	Channel 2 on
1	0	1	0	Channel 3 on
1	0	1	1	Channel 4 on
1	1	0	0	Channel 5 on
1	1	0	1	Channel 6 on
1	1	1	0	Channel 7 on
1	1	1	1	Channel 8 on

(1) X denotes *don't care*..

Table 2. MUX509 Truth Table

EN	A1	A0	STATE
0	X ⁽¹⁾	X ⁽¹⁾	All channels are off
1	0	0	Channels 1A and 1B on
1	0	1	Channels 2A and 2B on
1	1	0	Channels 3A and 3B on
1	1	1	Channels 4A and 4B on

(1) X denotes *don't care*.

8.2 On-Resistance

The on-resistance of the MUX50x is the ohmic resistance across the source (Sx, SxA, or SxB) and drain (D, DA, or DB) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 26. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in Equation 1.

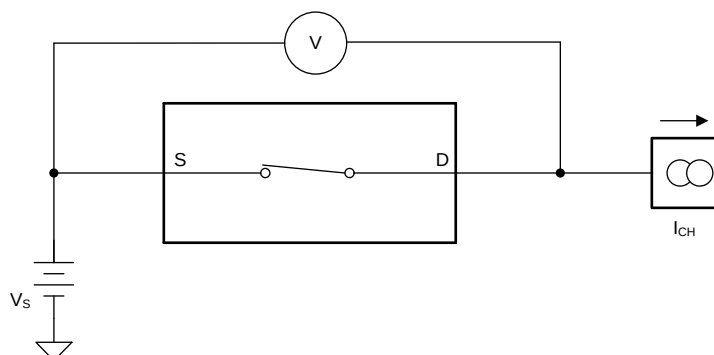


Figure 26. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

8.3 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source off-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain off-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both types of off-leakage currents is shown in Figure 27.

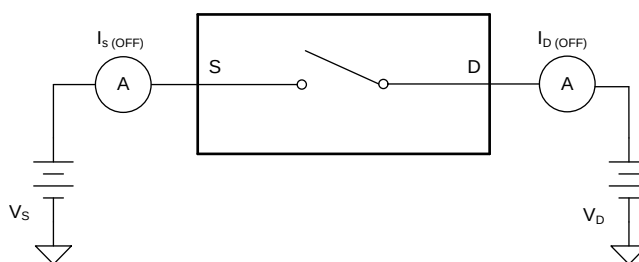


Figure 27. Off-Leakage Measurement Setup

8.4 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. Figure 28 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

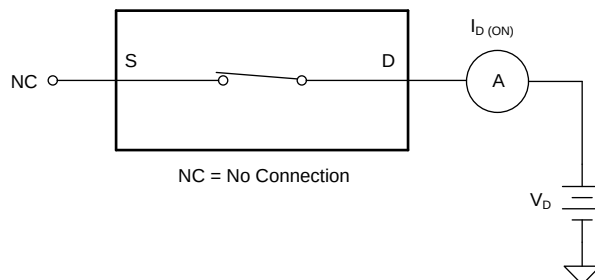
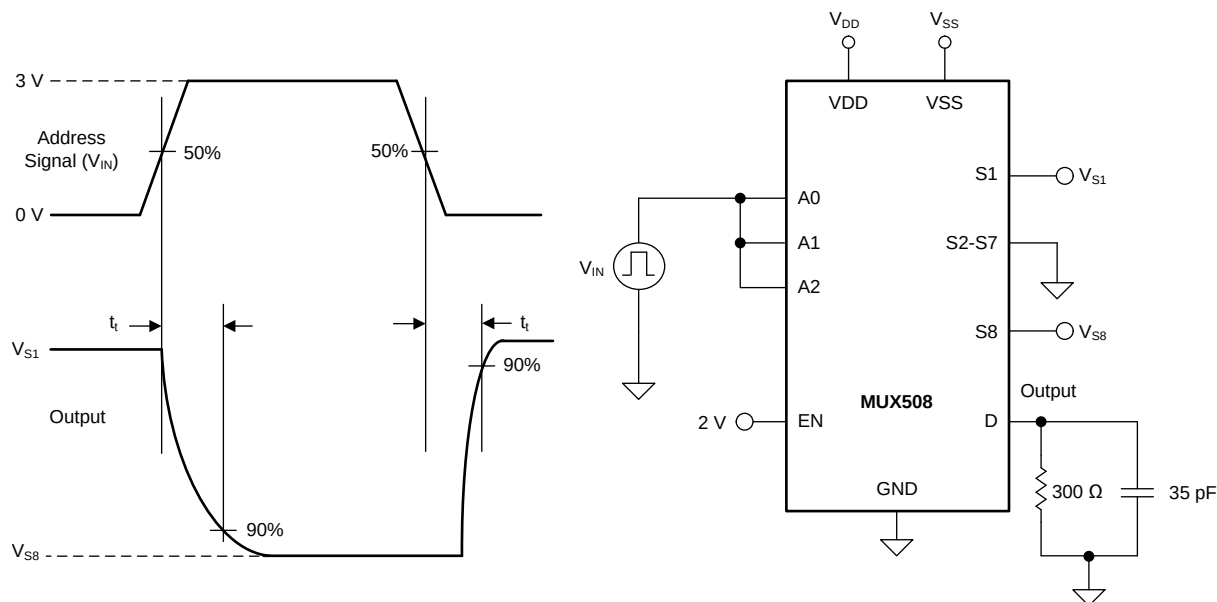


Figure 28. On-Leakage Measurement Setup

8.5 Transition Time

Transition time is defined as the time taken by the output of the MUX50x to rise or fall to 90% of the transition after the digital address signal has fallen or risen to the 50% of the transition. Figure 29 shows the setup used to measure transition time, denoted by the symbol t_t .

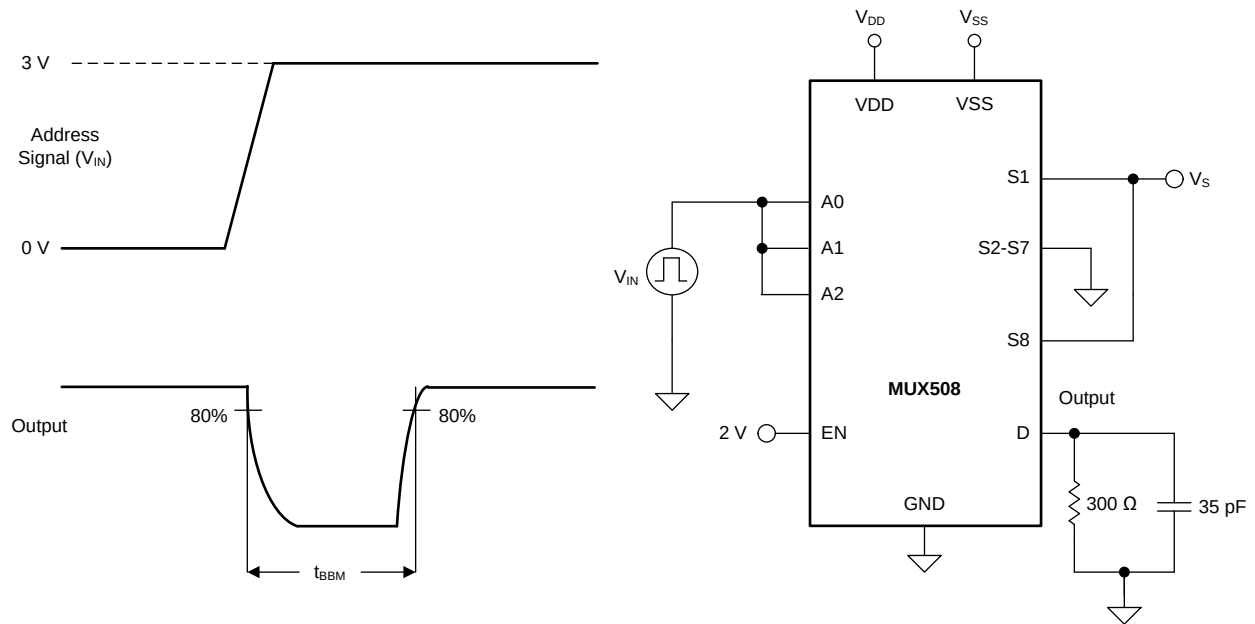


Copyright © 2016, Texas Instruments Incorporated

Figure 29. Transition-Time Measurement Setup

8.6 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the MUX50x is switching. The MUX50x output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as a break-before-make delay. Figure 30 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM} .



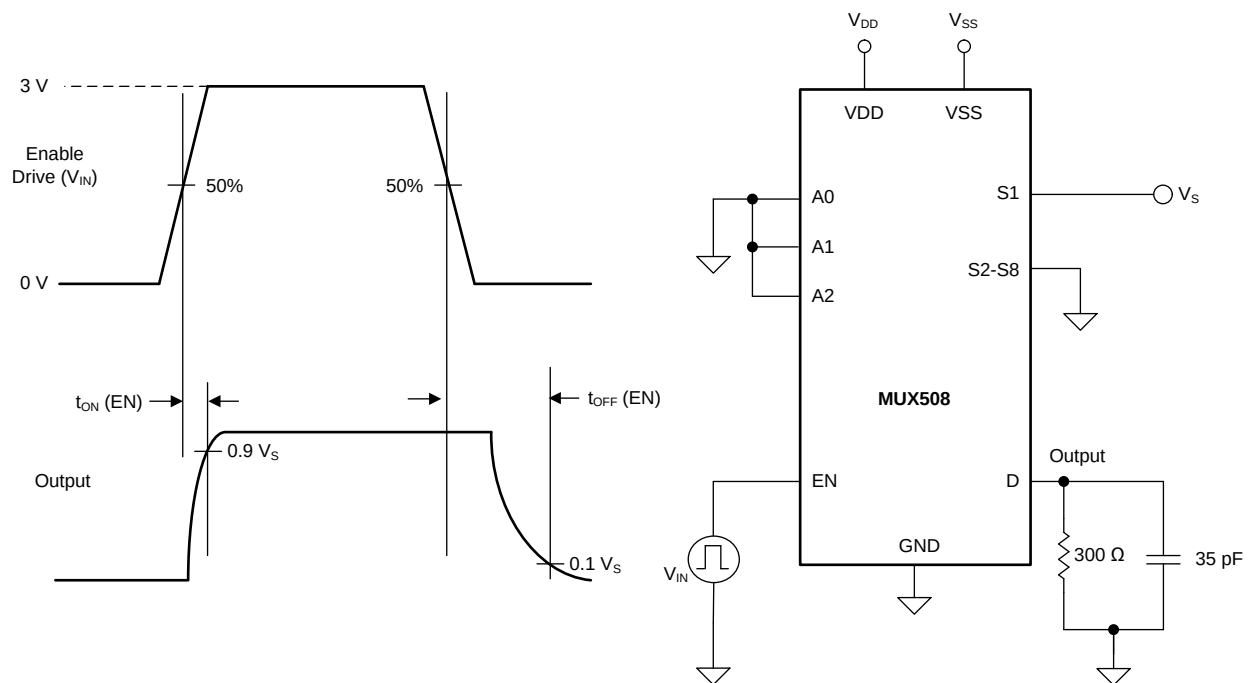
Copyright © 2016, Texas Instruments Incorporated

Figure 30. Break-Before-Make Delay Measurement Setup

8.7 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the MUX50x to rise to a 90% final value after the enable signal has risen to a 50% final value. Figure 31 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol t_{ON} .

Turn-off time is defined as the time taken by the output of the MUX50x to fall to a 10% initial value after the enable signal has fallen to a 50% initial value. Figure 31 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol t_{OFF} .



Copyright © 2016, Texas Instruments Incorporated

Figure 31. Turn-On and Turn-Off Time Measurement Setup

8.8 Charge Injection

The MUX50x have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ} . Figure 32 shows the setup used to measure charge injection.

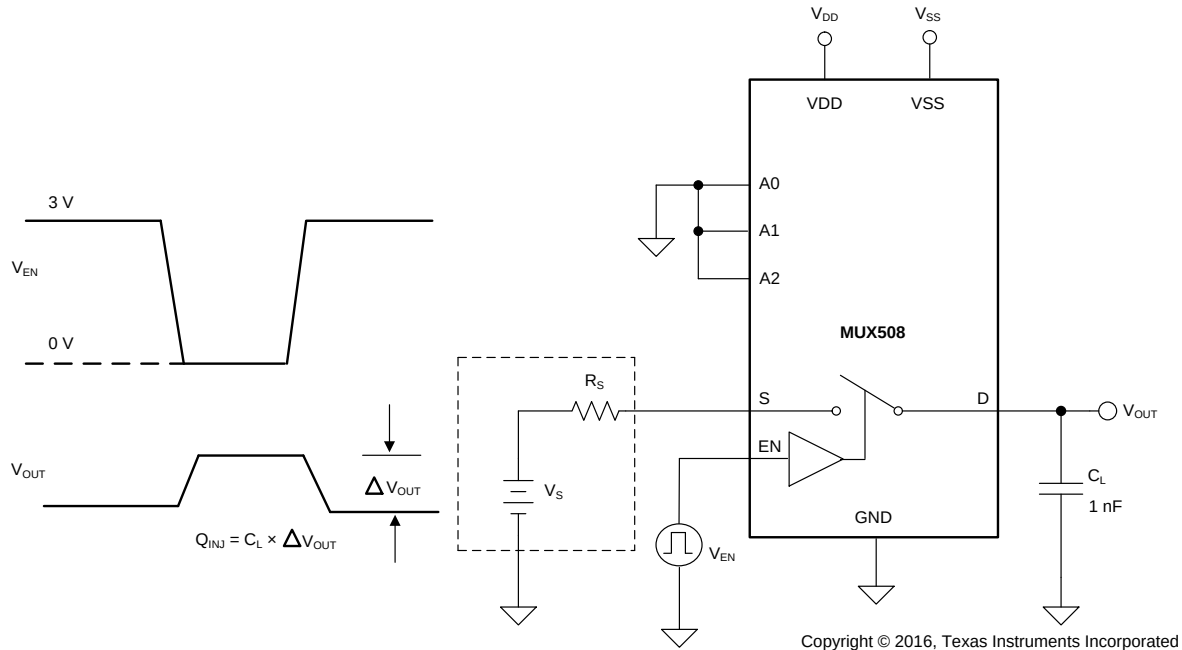


Figure 32. Charge-Injection Measurement Setup

8.9 Off Isolation

Off isolation is defined as the voltage at the drain pin (D, DA, or DB) of the MUX50x when a 1- V_{RMS} signal is applied to the source pin (Sx, SxA, or SxB) of an off-channel. Figure 33 shows the setup used to measure off isolation. Use Equation 2 to compute off isolation.

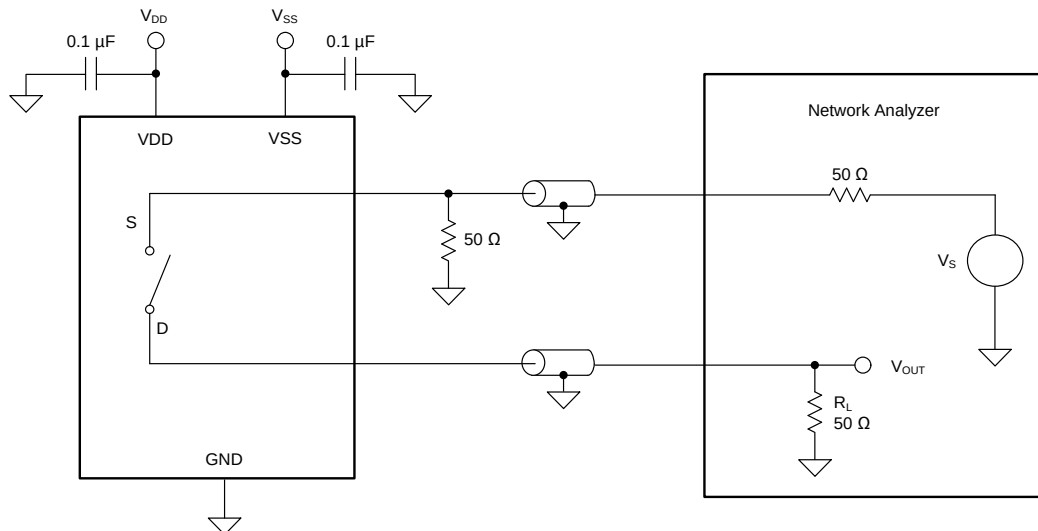


Figure 33. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log} \left(\frac{V_{OUT}}{V_S} \right) \quad (2)$$

8.10 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx, SxA, or SxB) of an off-channel, when a 1- V_{RMS} signal is applied at the source pin of an on-channel. Figure 34 shows the setup used to measure, and Equation 3 is the equation used to compute, channel-to-channel crosstalk.

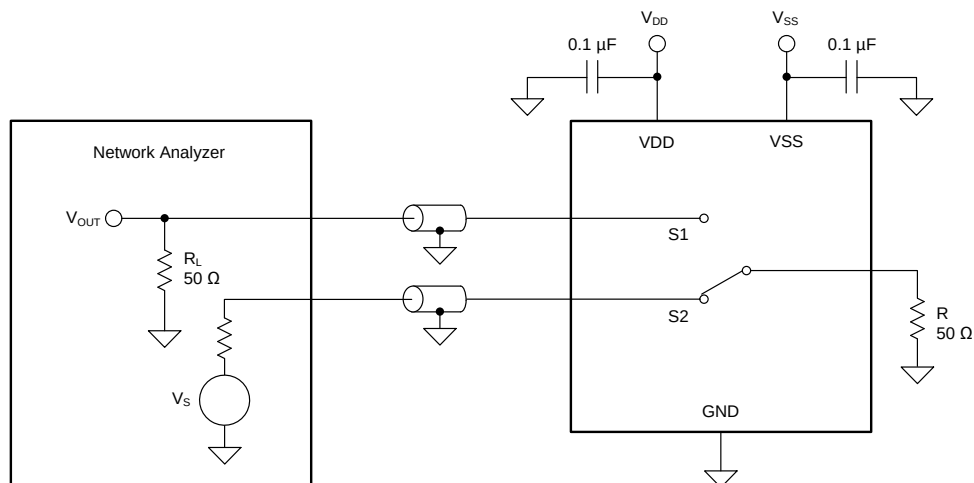


Figure 34. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log} \left(\frac{V_{OUT}}{V_S} \right) \quad (3)$$

8.11 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin of an on-channel and the output is measured at the drain pin of the MUX50x. [Figure 35](#) shows the setup used to measure bandwidth of the mux. Use [Equation 4](#) to compute the attenuation.

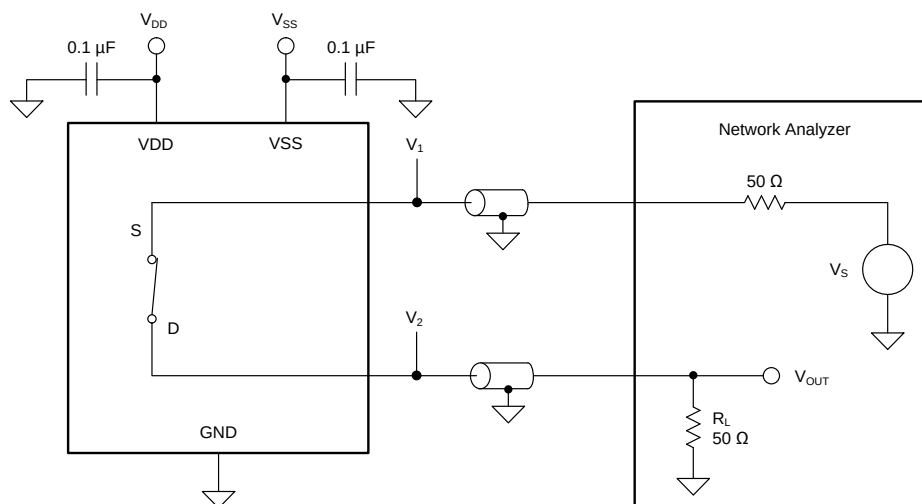


Figure 35. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log} \left(\frac{V_2}{V_1} \right) \quad (4)$$

8.12 THD + Noise

The total harmonic distortion (THD) of a signal is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the MUX50x varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. [Figure 36](#) shows the setup used to measure the THD+N of the MUX50x.

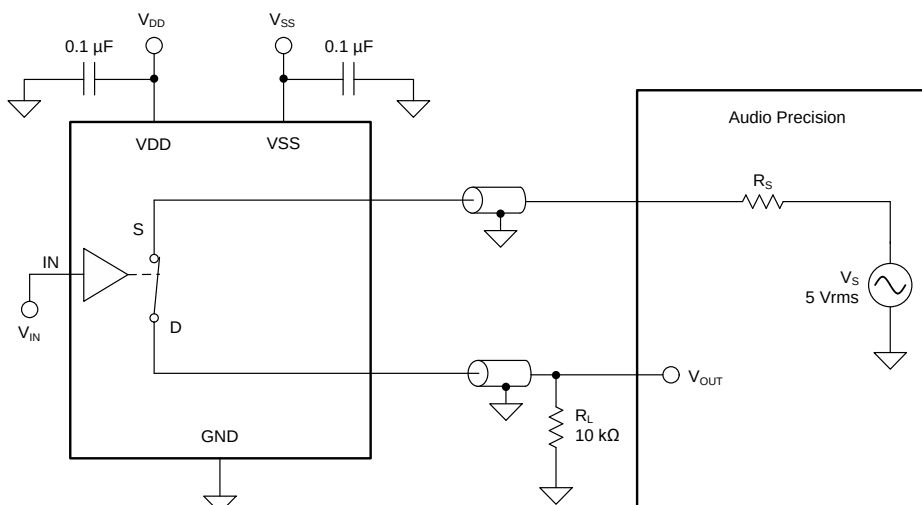


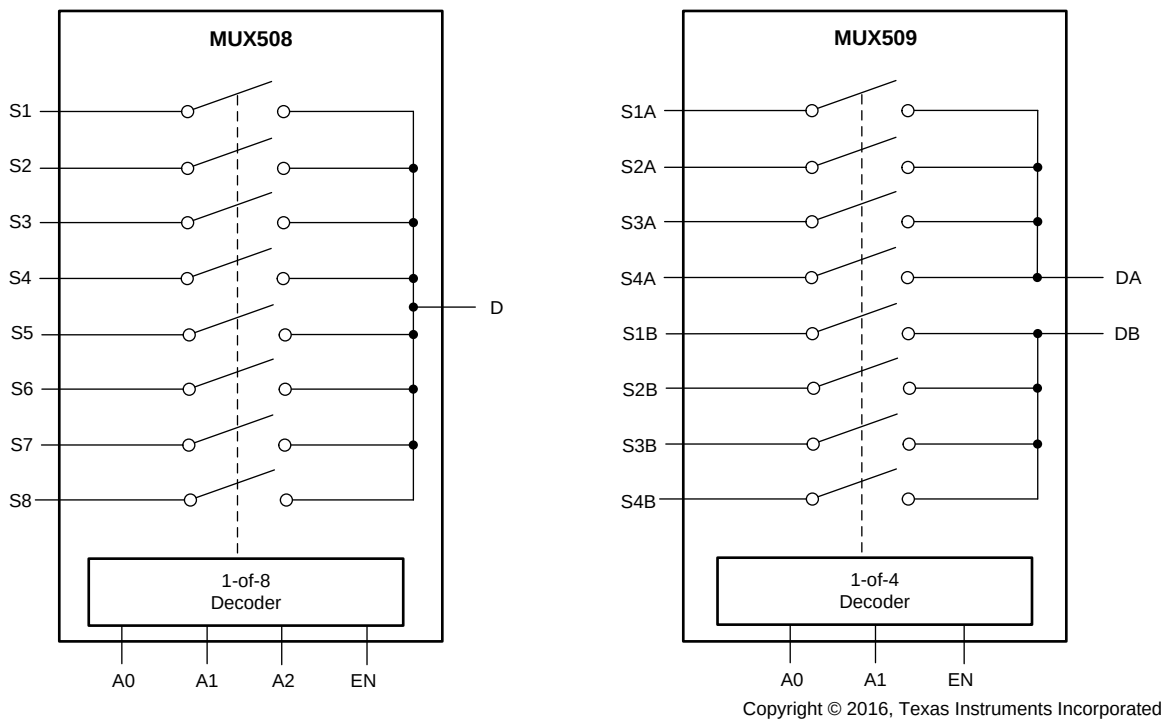
Figure 36. THD+N Measurement Setup

9 Detailed Description

9.1 Overview

The MUX50x are a family of analog multiplexers. The [Functional Block Diagram](#) section provides a top-level block diagram of both the MUX508 and MUX509. The MUX508 is an eight-channel, single-ended, analog mux. The MUX509 is a four-channel, differential or dual 4:1, single-ended, analog mux. Each channel is turned on or turned off based on the state of the address lines and enable pin.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Ultralow Leakage Current

The MUX50x provide extremely low on- and off-leakage currents. The MUX50x are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of these ultralow leakage currents. Figure 37 shows typical leakage currents of the MUX50x versus temperature.

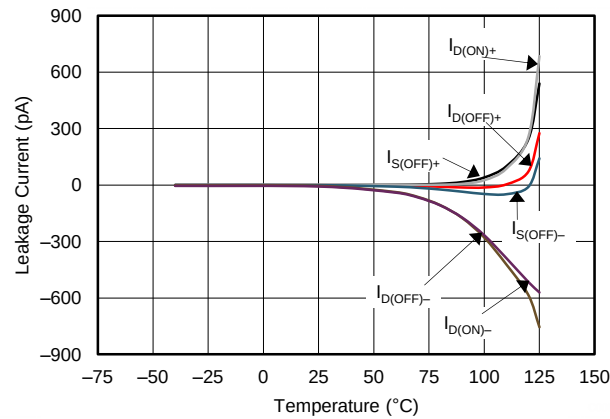


Figure 37. Leakage Current vs Temperature

9.3.2 Ultralow Charge Injection

The MUX50x have a simple transmission gate topology, as shown in Figure 38. Any mismatch in the stray capacitance associated with the NMOS and PMOS transistors creates an output level change whenever the switch is opened or closed.

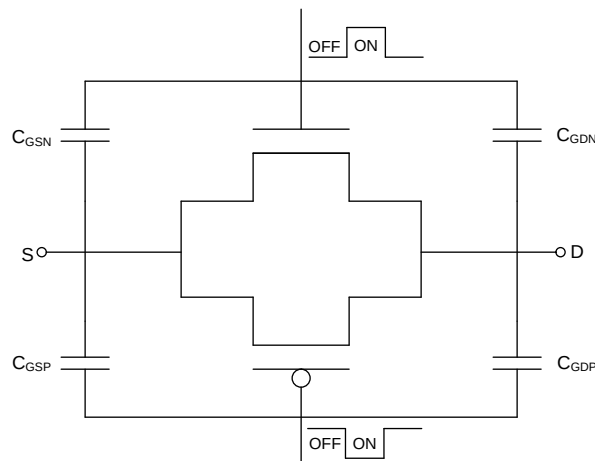


Figure 38. Transmission Gate Topology

Feature Description (continued)

The MUX50x have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to as low as 0.3 pC at $V_S = 0$ V, and ± 0.6 pC in the full signal range, as shown in Figure 39.

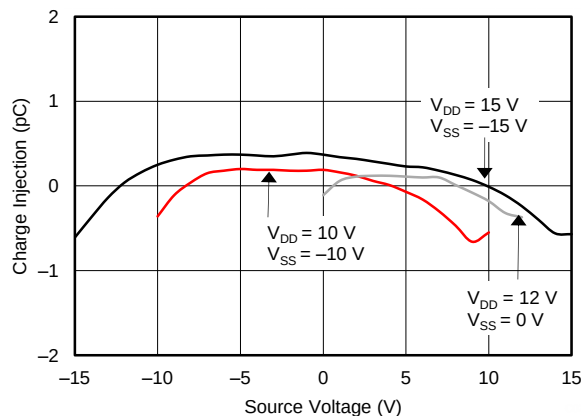


Figure 39. Source-to-Drain Charge Injection vs Source or Drain voltage

The drain-to-source charge injection becomes important when the device is used as a demultiplexer (demux), where D becomes the input and Sx becomes the output. Figure 40 shows the drain-to-source charge injection across the full signal range.

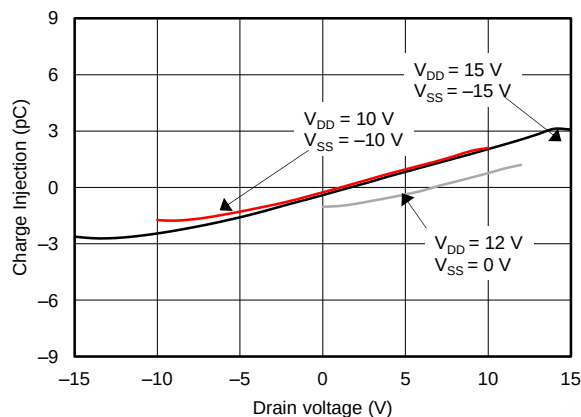


Figure 40. Drain-to-Source Charge Injection vs Source or Drain voltage

9.3.3 Bidirectional Operation

The MUX50x are operable as both a mux or demux. The source (Sx, SxA, SxB) and drain (D, DA, DB) pins of the MUX50x are used either as input or output. Each MUX50x channel has very similar characteristics in both directions.

Feature Description (continued)

9.3.4 Rail-to-Rail Operation

A valid analog signal for the MUX50x ranges from V_{SS} to V_{DD} . The input signal to the MUX50x can swing from V_{SS} to V_{DD} without any significant degradation in performance. The on-resistance of the MUX50x varies with input signal, as shown in Figure 41.

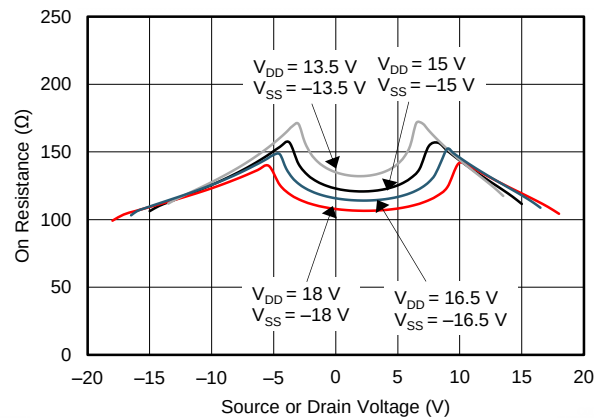


Figure 41. On-Resistance vs Source or Drain Voltage

9.4 Device Functional Modes

When the EN pin of the MUX50x is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state irrespective of the state of the address lines. The EN pin can be connected to V_{DD} (as high as 36 V).

10 Applications and Implementation

NOTE

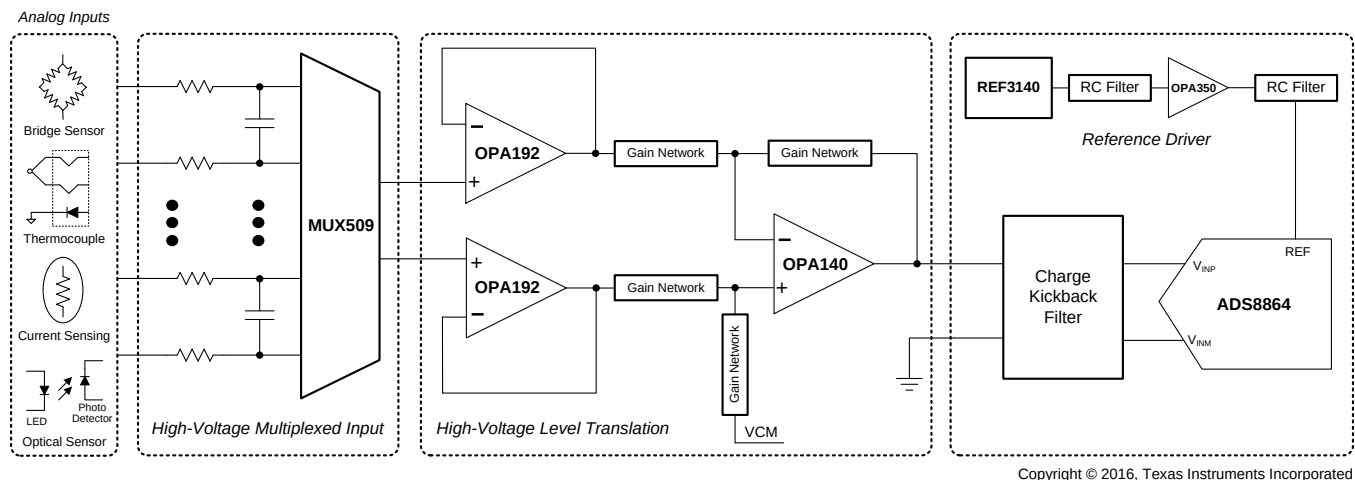
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The MUX50x family offers outstanding input/output leakage currents and ultralow charge injection. These devices operate up to 36 V, and offer true rail-to-rail input and output. The on-capacitance of the MUX50x is very low. These features makes the MUX50x a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

10.2 Typical Application

Figure 42 shows a 16-bit, differential, four-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a four-channel differential mux. This application example details the process for optimizing a precision, high-voltage, front-end drive circuit using the MUX509, OPA192 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.



Copyright © 2016, Texas Instruments Incorporated

Figure 42. 16-Bit Precision Multiplexed Data-Acquisition System for High-Voltage Inputs With Lowest Distortion

10.2.1 Design Requirements

The primary objective is to design a ± 20 V, differential, four-channel, multiplexed, data-acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure, sine-wave input. The design requirements for this block design are:

- System supply voltage: ± 15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 20 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

Typical Application (continued)

10.2.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in [Figure 42](#). The circuit is a multichannel, data-acquisition signal chain consisting of an input low-pass filter, mux, mux output buffer, attenuating SAR ADC driver, and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel.



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see [TI Precision Design T1PD151, 16-Bit, 400-kSPS, 4-Channel Multiplexed Data-Acquisition System for High-Voltage Inputs with Lowest Distortion](#).

10.2.3 Application Curve

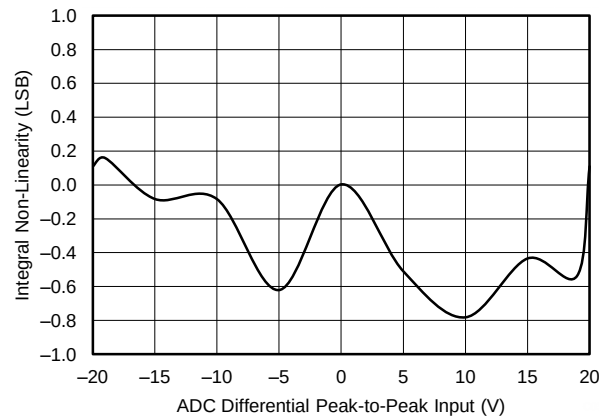


Figure 43. ADC 16-Bit Linearity Error for the Multiplexed Data-Acquisition Block

11 Power-Supply Recommendations

The MUX50x operates across a wide supply range of ± 5 V to ± 18 V (10 V to 36 V in single-supply mode). The MUX508 and MUX509 operate equally well with either dual supplies (± 5 V to ± 18 V), or a single supply (10 V to 36 V). They also perform well with unsymmetric supplies such as $V_{DD} = 12$ V and $V_{SS} = -5$ V. For reliable operation, use a supply decoupling capacitor with a capacitance between 0.1 μ F to 10 μ F at both the VDD and VSS pins to ground.

The on-resistance of the MUX50x varies with supply voltage, as shown in Figure 44.

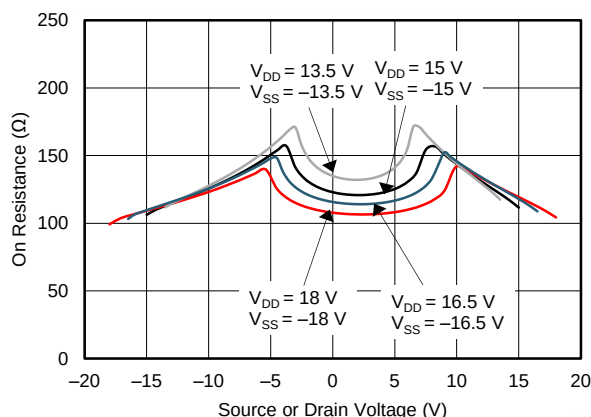


Figure 44. On-Resistance Variation With Supply and Input Voltage

12 Layout

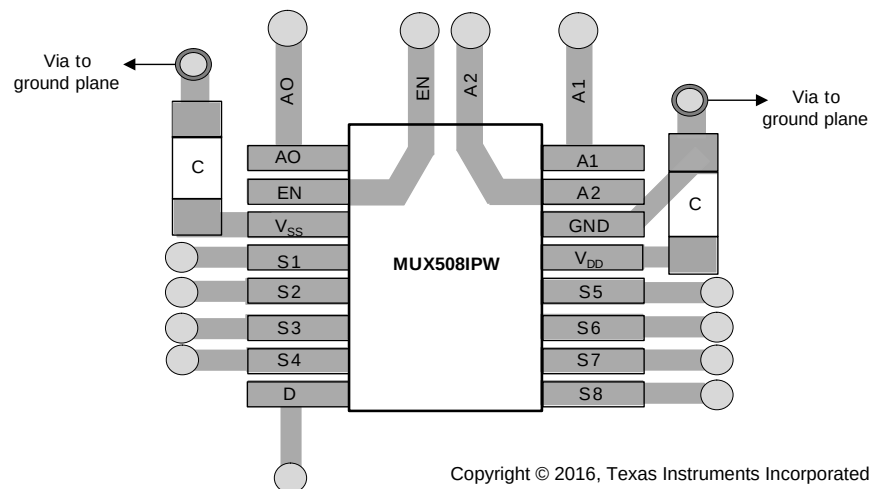
12.1 Layout Guidelines

Figure 45 shows an example of a PCB layout with the MUX508IPW, and Figure 46 shows an example of a PCB layout with MUX509IPW. The guidelines provided in this section are also applicable to the SOIC MUX508ID and MUX509ID package variants as well.

Some key considerations are:

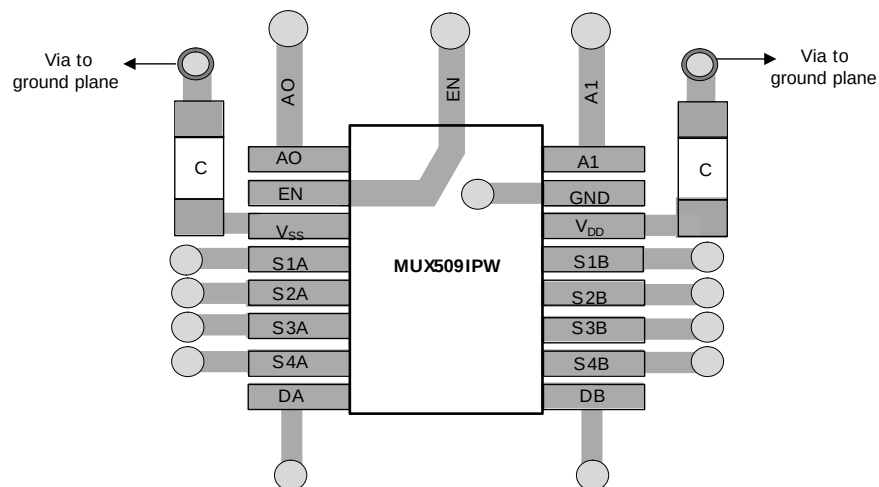
1. Decouple the VDD and VSS pins with a 0.1- μ F capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as small as possible. For the MUX509 differential signals, make sure the A inputs and B inputs are as symmetric as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible and only make perpendicular crossings when necessary.

12.2 Layout Example



Copyright © 2016, Texas Instruments Incorporated

Figure 45. MUX508IPW Layout Example



Copyright © 2016, Texas Instruments Incorporated

Figure 46. MUX509IPW Layout Example

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

- 《[ADS866x](#) 支持双极输入范围的 12 位、500kSPS、4 通道和 8 通道单电源 SAR ADC》（文献编号：SBAS492）
- 《[OPAx140](#) 高精度、低噪声、轨到轨输出、11 MHz JFET 运算放大器》（文献编号：SBOS498）
- 《[OPAx192](#) 具有 e-trim™ 的 36V、精密、轨到轨输入/输出、低偏移电压、低输入偏置电流运算放大器》（文献编号：SBOS620）

13.2 相关链接

表 3 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片与购买的快速访问。

表 3. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
MUX508	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MUX509	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.3 接收文档更新通知

如需接收文档更新通知，请访问 [www.ti.com.cn](#) 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

13.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内, 且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息, 不能构成从 TI 获得使用这些产品或服务 的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时, 如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分, 则会失去相关 TI 组件 或服务的所有明示或暗示授权, 且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由 TI 提供, 但他们将独力负责满足与其产品及其应用中使用的 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中, 为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备) 的授权许可, 除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意, 对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com.cn/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122
Copyright © 2016, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MUX508ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	M36508D	Samples
MUX508IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	M36508D	Samples
MUX508IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX508B	Samples
MUX508IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX508B	Samples
MUX509ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	M36509D	Samples
MUX509IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	M36509D	Samples
MUX509IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX509C	Samples
MUX509IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX509C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

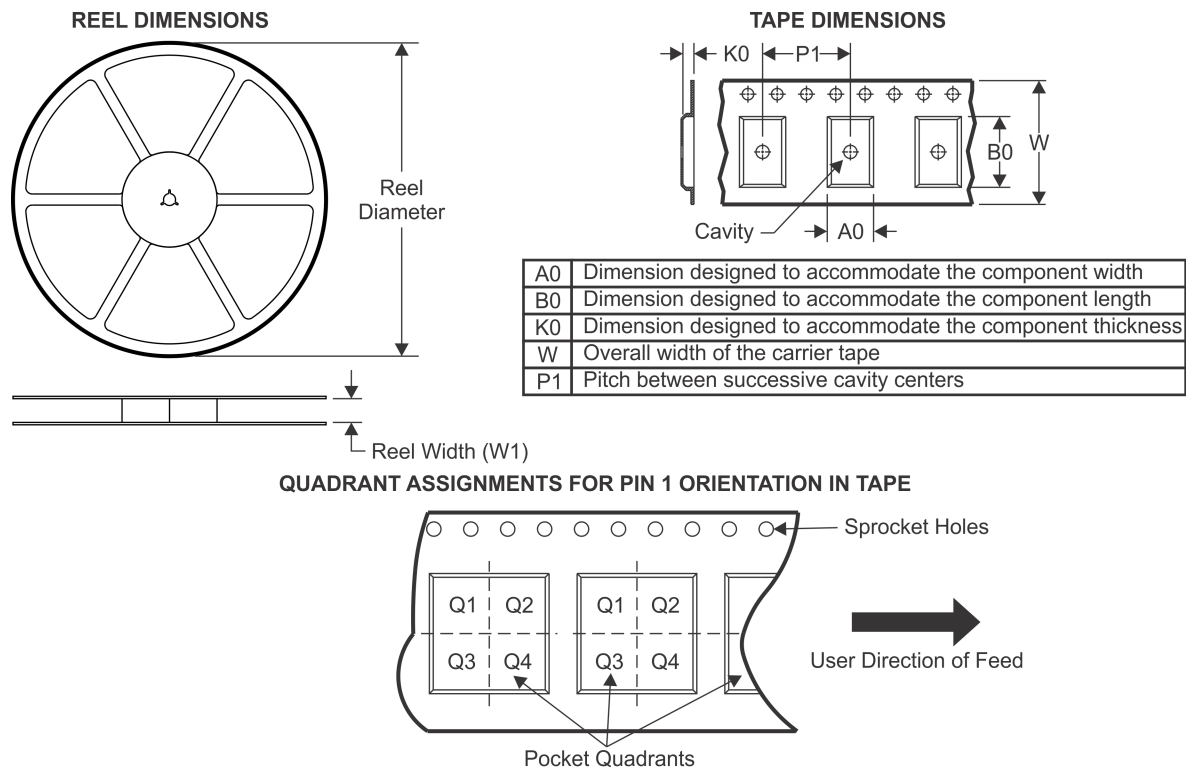
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

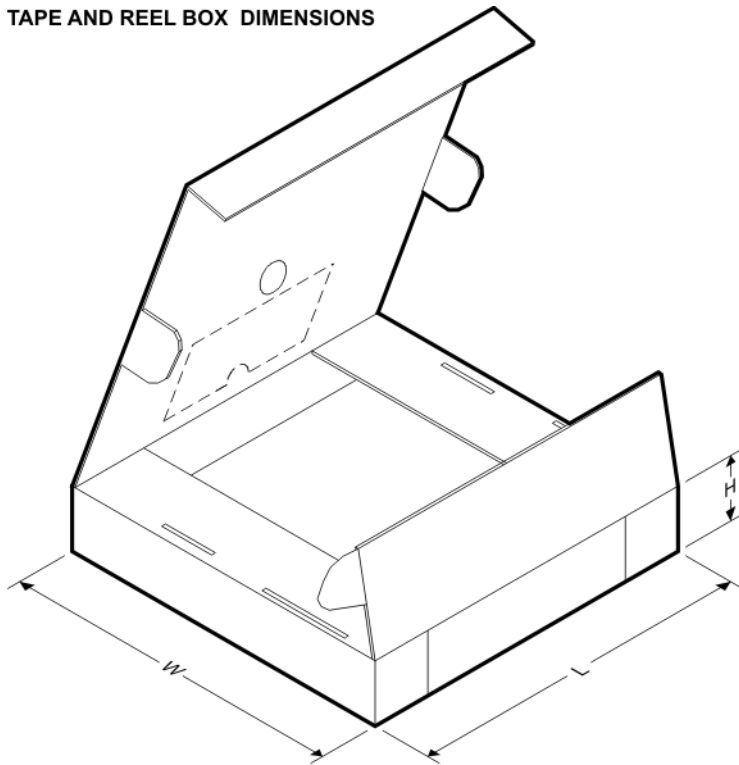
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MUX508IDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
MUX508IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MUX509IDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
MUX509IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

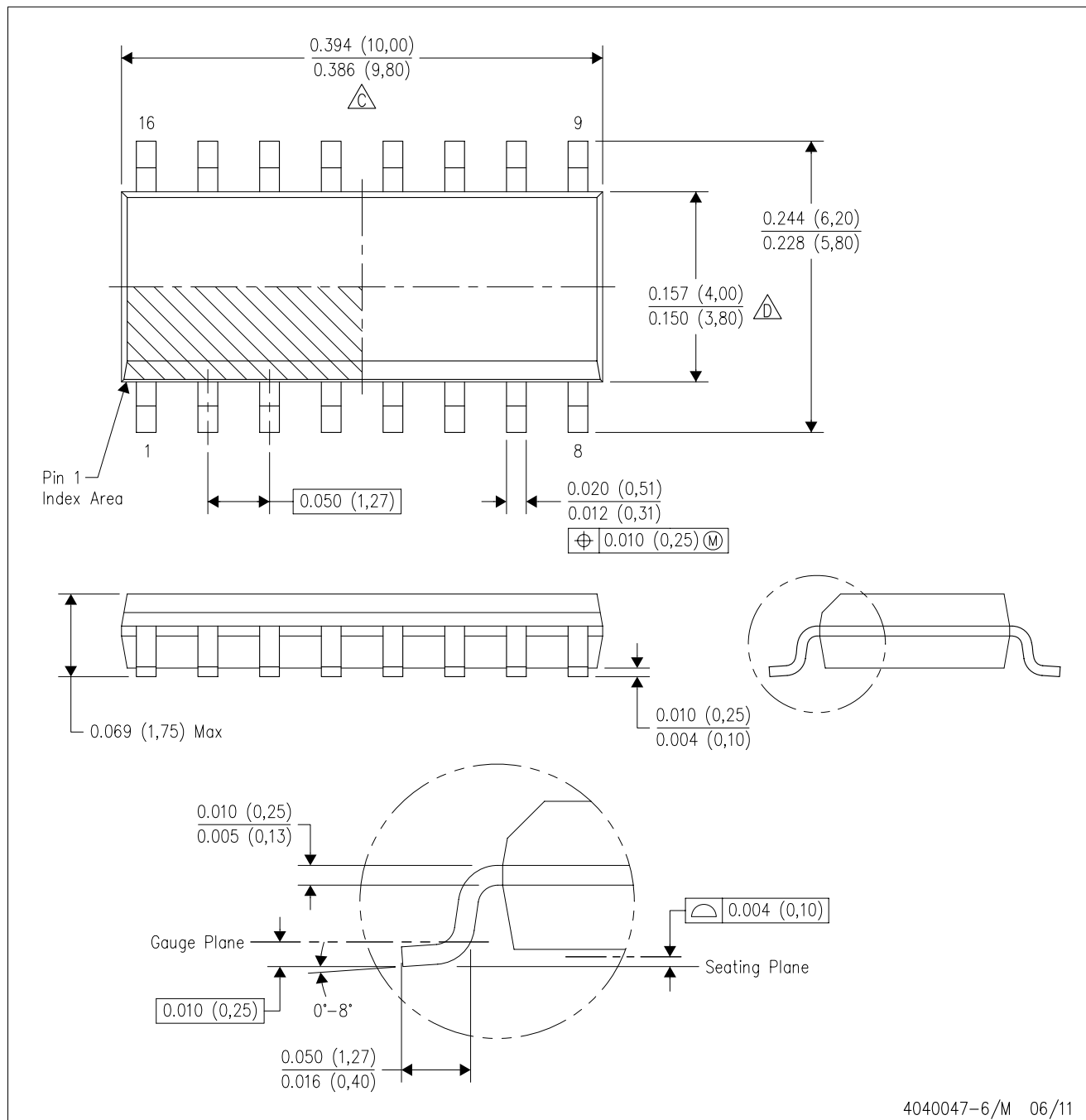


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MUX508IDR	SOIC	D	16	2500	366.0	364.0	50.0
MUX508IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MUX509IDR	SOIC	D	16	2500	366.0	364.0	50.0
MUX509IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

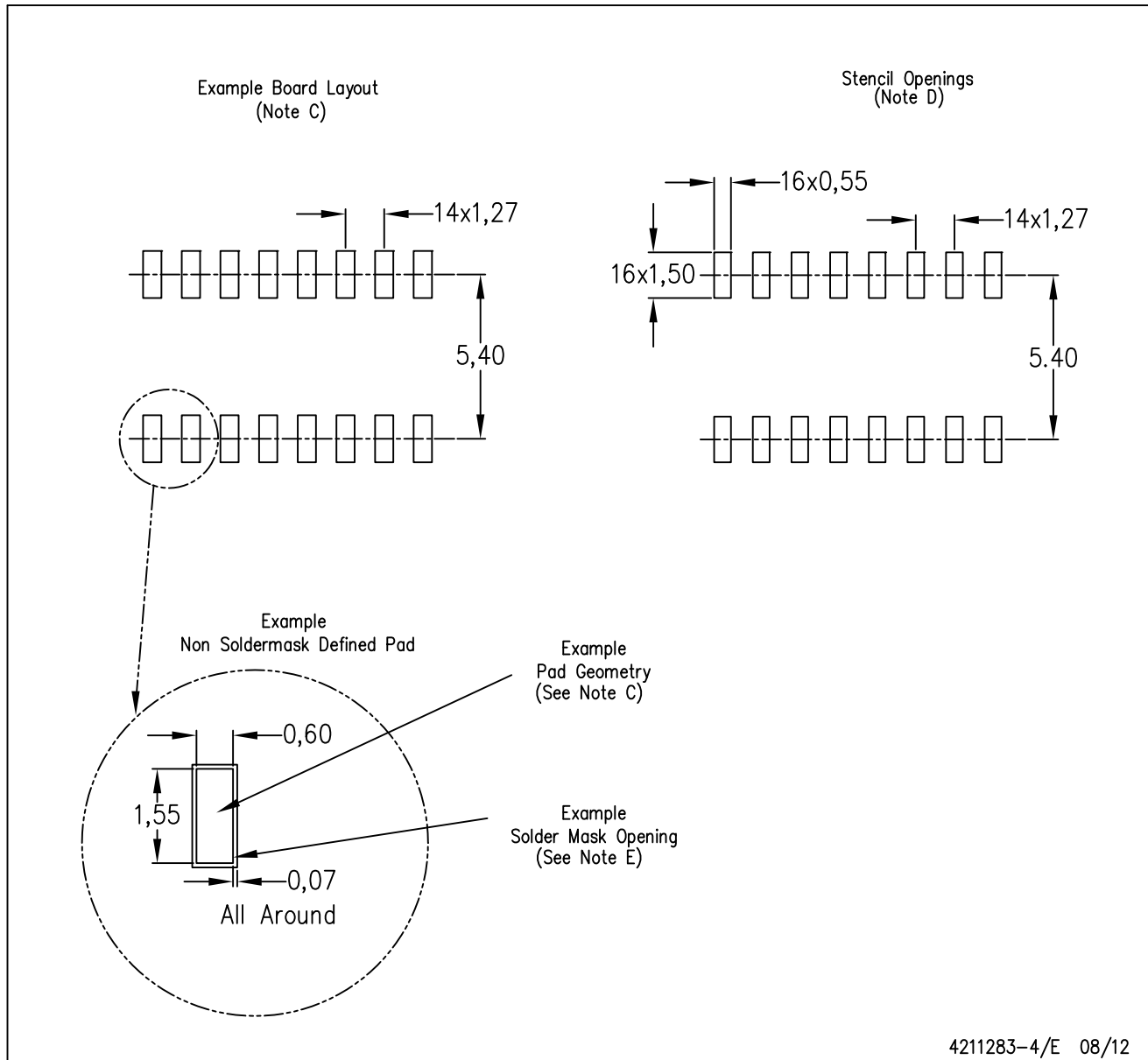
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

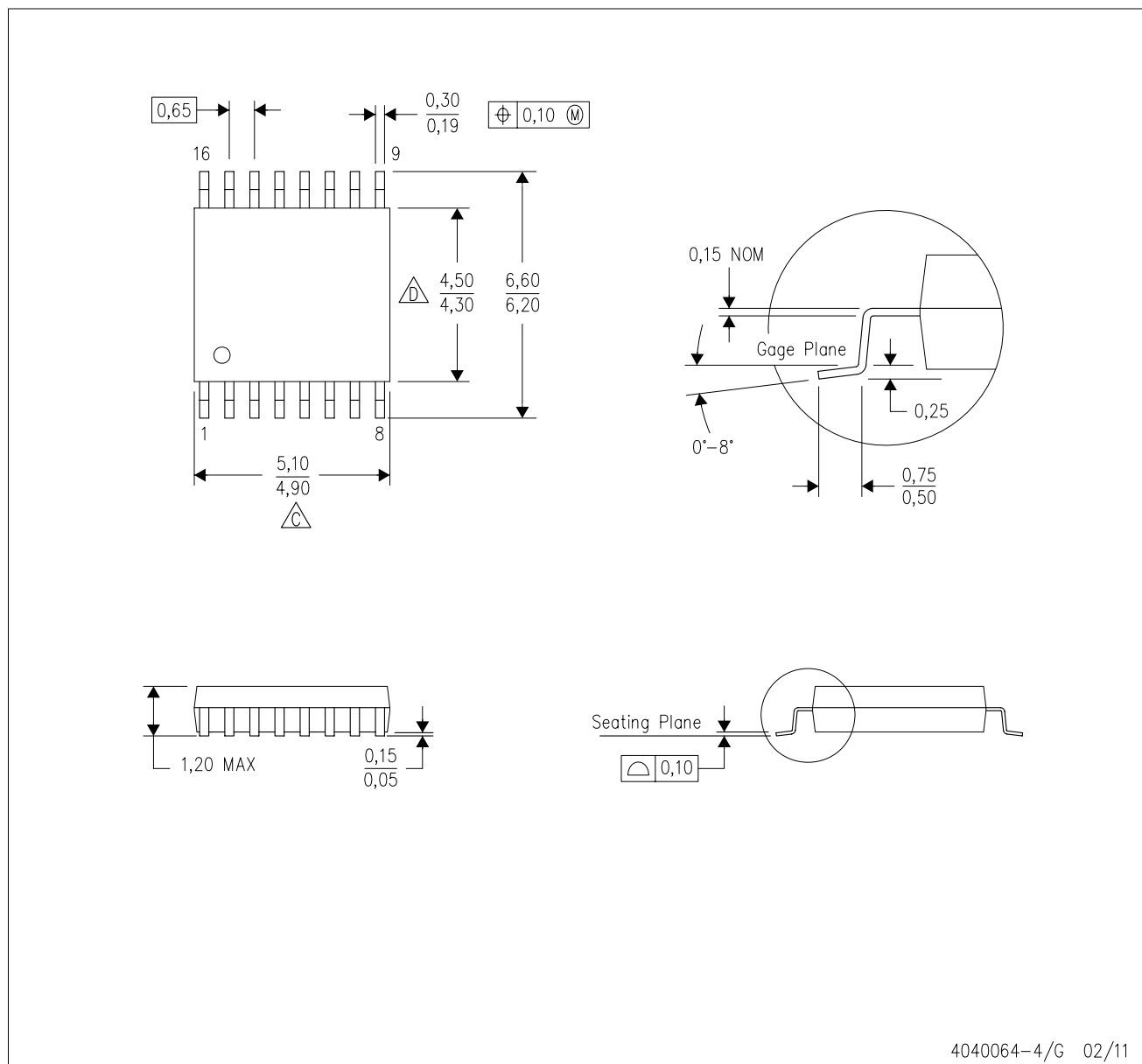
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

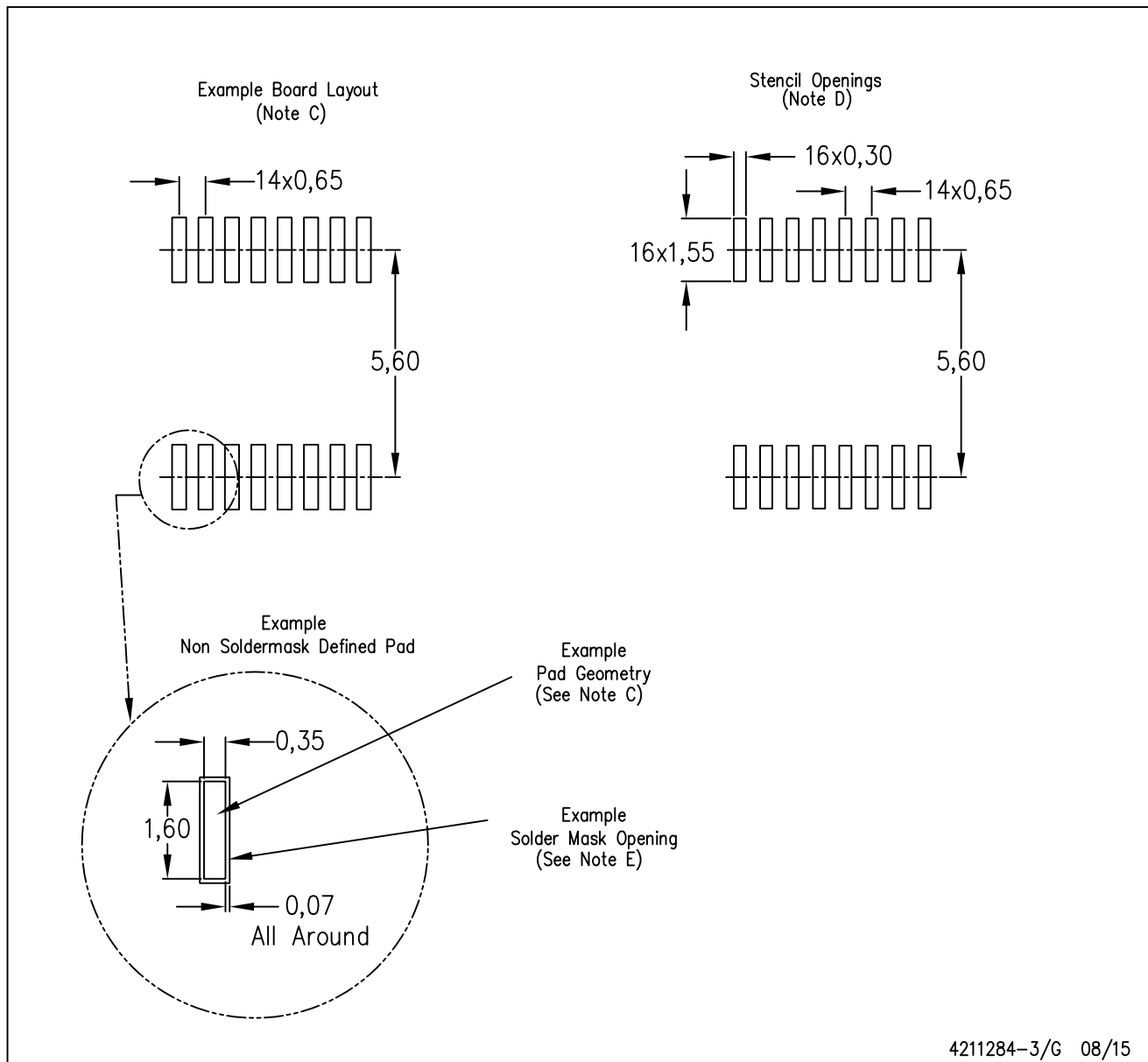
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - Δ C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - Δ D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内, 且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息, 不能构成从 TI 获得使用这些产品或服务 的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时, 如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分, 则会失去相关 TI 组件 或服务的所有明示或暗示授权, 且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由 TI 提供, 但他们将独力负责满足与其产品及其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中, 为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备) 的授权许可, 除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意, 对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 ISO/TS16949 要 求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated