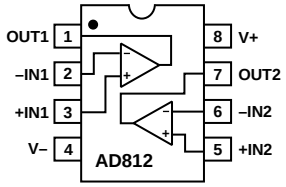
Dual, Current Feedback Low Power Op Amp

AD812

FEATURES
Two Video Amplifiers in One 8-Lead SOIC Package
Optimized for Driving Cables in Video Systems
Excellent Video Specifications (R_L = 150 Ω):
Gain Flatness 0.1 dB to 40 MHz
0.02% Differential Gain Error
0.02° Differential Phase Error
Low Power
Operates on Single +3 V Supply
5.5 mA/Amplifier Max Power Supply Current
High Speed
145 MHz Unity Gain Bandwidth (3 dB)
1600 V/μs Slew Rate
Easy to Use
50 mA Output Current
Output Swing to 1 V of Rails (150 Ω Load)

APPLICATIONS
Video Line Driver
Professional Cameras
Video Switchers
Special Effects

PIN CONFIGURATION
8-Lead Plastic
Mini-DIP and SOIC



PRODUCT DESCRIPTION
The AD812 is a low power, single supply, dual video amplifier. Each of the amplifiers have 50 mA of output current and are optimized for driving one back-terminated video load (150 Ω) each. Each amplifier is a current feedback amplifier and features gain flatness of 0.1 dB to 40 MHz while offering differential gain and phase error of 0.02% and 0.02°. This makes the AD812 ideal for professional video electronics such as cameras and video switchers.

The AD812 offers low power of 4.0 mA per amplifier max (V_S = +5 V) and can run on a single +3 V power supply. The outputs of each amplifier swing to within one volt of either supply rail to easily accommodate video signals of 1 V p-p. Also, at gains of +2 the AD812 can swing 3 V p-p on a single +5 V power supply. All this is offered in a small 8-lead plastic DIP or 8-lead SOIC package. These features make this dual amplifier ideal for portable and battery powered applications where size and power is critical.

The outstanding bandwidth of 145 MHz along with 1600 V/μs of slew rate make the AD812 useful in many general purpose high speed applications where a single +5 V or dual power supplies up to ±15 V are available. The AD812 is available in the industrial temperature range of –40°C to +85°C.

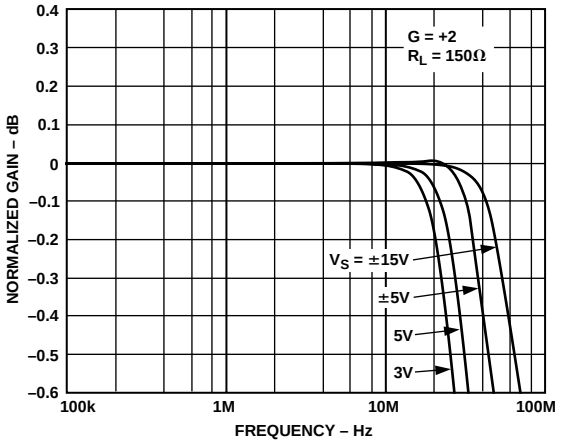


Figure 1. Fine-Scale Gain Flatness vs. Frequency, Gain = +2, R_L = 150 Ω

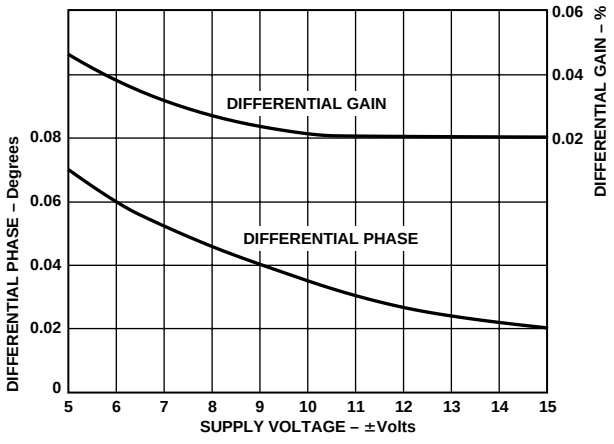


Figure 2. Differential Gain and Phase vs. Supply Voltage, Gain = +2, R_L = 150 Ω

REV. B

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AD812–SPECIFICATIONS

Dual Supply (@ T_A = +25°C, R_L = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD812A Min	AD812A Typ	AD812A Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	±5 V	50	65		MHz
		±15 V	75	100		MHz
	Gain = +1	±15 V	100	145		MHz
Bandwidth for 0.1 dB Flatness	G = +2	±5 V	20	30		MHz
		±15 V	25	40		MHz
Slew Rate[1]	G = +2, R_L = 1 kΩ	±5 V	275	425		V/µs
	20 V Step	±15 V	1400	1600		V/µs
	G = –1, R_L = 1 kΩ	±5 V		250		V/µs
		±15 V		600		V/µs
Settling Time to 0.1%	G = –1, R_L = 1 kΩ					
	V_O = 3 V Step	±5 V		50		ns
	V_O = 10 V Step	±15 V		40		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f_C = 1 MHz, R_L = 1 kΩ	±15 V		–90		dBc
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		3.5		nV/√Hz
Input Current Noise	f = 10 kHz, +In	±5 V, ±15 V		1.5		pA/√Hz
	f = 10 kHz, –In	±5 V, ±15 V		18		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω	±5 V		0.05	0.1	%
		±15 V		0.02	0.06	%
Differential Phase Error		±5 V		0.07	0.15	Degrees
		±15 V		0.02	0.06	Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V, ±15 V		2	5	mV
	T_{MIN}–T_{MAX}				12	mV
Offset Drift		±5 V, ±15 V		15		µV/°C
–Input Bias Current		±5 V, ±15 V		7	25	µA
	T_{MIN}–T_{MAX}				38	µA
+Input Bias Current		±5 V, ±15 V		0.3	1.5	µA
	T_{MIN}–T_{MAX}				2.0	µA
Open-Loop Voltage Gain	V_O = ±2.5 V, R_L = 150 Ω	±5 V	68	76		dB
	T_{MIN}–T_{MAX}		69			dB
	V_O = ±10 V, R_L = 1 kΩ	±15 V	76	82		dB
	T_{MIN}–T_{MAX}		75			dB
Open-Loop Transresistance	V_O = ±2.5 V, R_L = 150 Ω	±5 V	350	550		kΩ
	T_{MIN}–T_{MAX}		270			kΩ
	V_O = ±10 V, R_L = 1 kΩ	±15 V	450	800		kΩ
	T_{MIN}–T_{MAX}		370			kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	±15 V		15		MΩ
	–Input			65		Ω
Input Capacitance	+Input			1.7		pF
Input Common Mode		±5 V		4.0		±V
Voltage Range		±15 V		13.5		±V
Common-Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = ±2.5 V	±5 V	51	58		dB
–Input Current				2	3.0	µA/V
+Input Current				0.07	0.15	µA/V
Input Offset Voltage	V_{CM} = ±12 V	±15 V	55	60		dB
–Input Current				1.5	3.3	µA/V
+Input Current				0.05	0.15	µA/V

Model	Conditions	V_S	AD812A Min	Typ	Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 150 Ω, T_{MIN}–T_{MAX}	±5 V	3.5	3.8		±V
	R_L = 1 kΩ, T_{MIN}–T_{MAX}	±15 V	13.6	14.0		±V
Output Current		±5 V	30	40		mA
		±15 V	40	50		mA
Short Circuit Current	G = +2, R_F = 715 Ω	±15 V		100		mA
	V_{IN} = 2 V					
Output Resistance	Open-Loop	±15 V		15		Ω
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	±5 V, ±15 V		–75		dB
Gain Flatness Match	G = +2, f = 40 MHz	±15 V		0.1		dB
DC						
Input offset Voltage	T_{MIN}–T_{MAX}	±5 V, ±15 V		0.5	3.6	mV
–Input Bias Current	T_{MIN}–T_{MAX}	±5 V, ±15 V		2	25	µA
POWER SUPPLY						
Operating Range			±1.2		±18	V
Quiescent Current	Per Amplifier	±5 V		3.5	4.0	mA
		±15 V		4.5	5.5	mA
	T_{MIN}–T_{MAX}	±15 V			6.0	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = ±1.5 V to ±15 V		70	80		dB
–Input Current				0.3	0.6	µA/V
+Input Current				0.005	0.05	µA/V

NOTES
[1]Slew rate measurement is based on 10% to 90% rise time in the specified closed-loop gain.
Specifications subject to change without notice.

Single Supply (@ T_A = +25°C, R_L = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD812A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	+5 V	35	50		MHz
		+3 V	30	40		MHz
Bandwidth for 0.1 dB						
Flatness	G = +2	+5 V	13	20		MHz
		+3 V	10	18		MHz
Slew Rate[1]	G = +2, R_L = 1 kΩ	+5 V		125		V/µs
		+3 V		60		V/µs
NOISE/HARMONIC PERFORMANCE						
Input Voltage Noise	f = 10 kHz	+5 V, +3 V		3.5		nV/√Hz
Input Current Noise	f = 10 kHz, +In	+5 V, +3 V		1.5		pA/√Hz
	f = 10 kHz, –In	+5 V, +3 V		18		pA/√Hz
Differential Gain Error[2]	NTSC, G = +2, R_L = 150 Ω	+5 V		0.07		%
	G = +1	+3 V		0.15		%
Differential Phase Error[2]	G = +2	+5 V		0.06		Degrees
	G = +1	+3 V		0.15		Degrees

AD812–SPECIFICATIONS
Single Supply (Continued)

Model	Conditions	V_S	AD812A Min	AD812A Typ	AD812A Max	Units
DC PERFORMANCE						
Input Offset Voltage		+5 V, +3 V		1.5	4.5	mV
	T_{MIN}–T_{MAX}				7.0	mV
Offset Drift		+5 V, +3 V		7		µV/°C
–Input Bias Current		+5 V, +3 V		2	20	µA
	T_{MIN}–T_{MAX}				30	µA
+Input Bias Current		+5 V, +3 V		0.2	1.5	µA
	T_{MIN}–T_{MAX}				2.0	µA
Open-Loop Voltage Gain	V_O = +2.5 V p-p	+5 V	67	73		dB
	V_O = +0.7 V p-p	+3 V		70		dB
Open-Loop Transresistance	V_O = +2.5 V p-p	+5 V	250	400		kΩ
	V_O = +0.7 V p-p	+3 V		300		kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	+5 V		15		MΩ
	–Input	+5 V		90		Ω
Input Capacitance	+Input			2		pF
Input Common Mode		+5 V	1.0		4.0	V
Voltage Range		+3 V	1.0		2.0	V
Common-Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = 1.25 V to 3.75 V	+5 V	52	55		dB
–Input Current				3	5.5	µA/V
+Input Current				0.1	0.2	µA/V
Input Offset Voltage	V_{CM} = 1 V to 2 V	+3 V		52		dB
–Input Current				3.5		µA/V
+Input Current				0.1		µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing p-p	R_L = 1 kΩ, T_{MIN}–T_{MAX}	+5 V	3.0	3.2		V p-p
	R_L = 150 Ω, T_{MIN}–T_{MAX}	+5 V	2.8	3.1		V p-p
		+3 V	1.0	1.3		V p-p
Output Current		+5 V	20	30		mA
		+3 V	15	25		mA
Short Circuit Current	G = +2, R_F = 715 Ω	+5 V		40		mA
	V_{IN} = 1 V					
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	+5 V, +3 V		–72		dB
Gain Flatness Match	G = +2, f = 20 MHz	+5 V, +3 V		0.1		dB
DC						
Input offset Voltage	T_{MIN}–T_{MAX}	+5 V, +3 V		0.5	3.5	mV
–Input Bias Current	T_{MIN}–T_{MAX}	+5 V, +3 V		2	25	µA
POWER SUPPLY						
Operating Range			2.4		36	V
Quiescent Current	Per Amplifier	+5 V		3.2	4.0	mA
		+3 V		3.0	3.5	mA
	T_{MIN}–T_{MAX}	+5 V			4.5	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = +3 V to +30 V		70	80		dB
–Input Current				0.3	0.6	µA/V
+Input Current				0.005	0.05	µA/V
TRANSISTOR COUNT				56		

NOTES
[1]Slew rate measurement is based on 10% to 90% rise time in the specified closed-loop gain.
[2]Single supply differential gain and phase are measured with the ac coupled circuit of Figure 53.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic (N) . . . . . 1.3 Watts
  Small Outline (R) . . . . . 0.9 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±1.2 V
Output Short Circuit Duration
  . . . . . Observe Power Derating Curves
Storage Temperature Range N, R . . . . . –65°C to +125°C
Operating Temperature Range . . . . . –40°C to +85°C
Lead Temperature Range (Soldering, 10 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

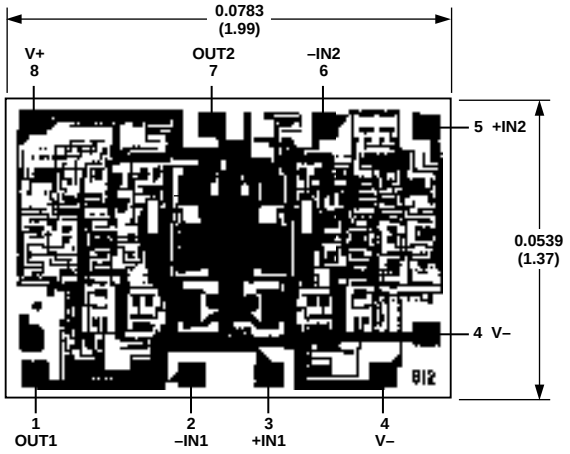
[2]Specification is for device in free air: 8-lead plastic package: θ_{JA} = 90°C/Watt; 8-lead SOIC package: θ_{JA} = 150°C/Watt.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD812AN	–40°C to +85°C	8-Lead Plastic DIP	N-8
AD812AR	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD812AR-REEL		13" Reel	
AD812AR-REEL7		7" Reel	

METALIZATION PHOTO

Dimensions shown in inches and (mm).



MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD812 is limited by the associated rise in junction temperature. The maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD812 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150 degrees) is not exceeded under all conditions. To ensure proper operation, it is important to observe the derating curves.

It must also be noted that in high (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.

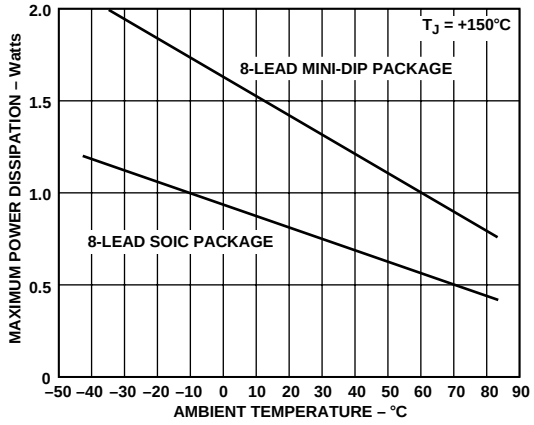


Figure 3. Plot of Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD812 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD812–Typical Performance Characteristics

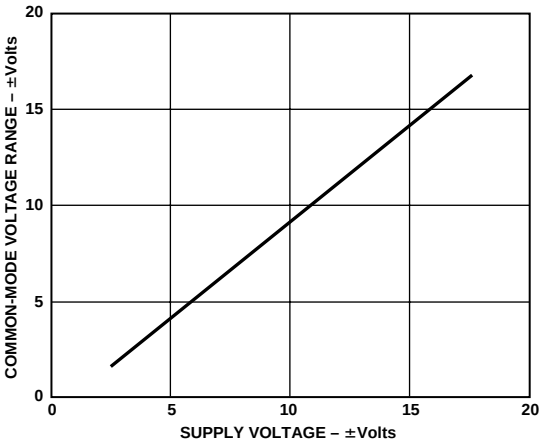


Figure 4. Input Common-Mode Voltage Range vs. Supply Voltage

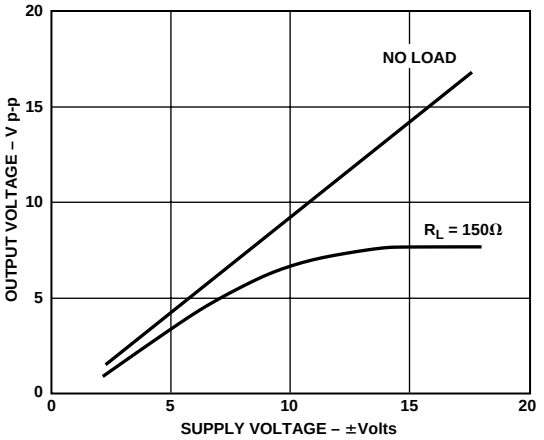


Figure 5. Output Voltage Swing vs. Supply Voltage

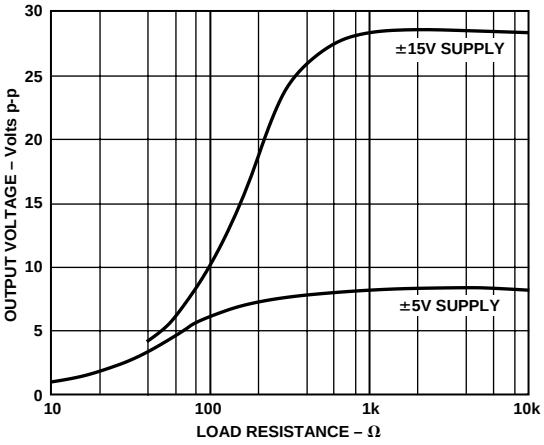


Figure 6. Output Voltage Swing vs. Load Resistance

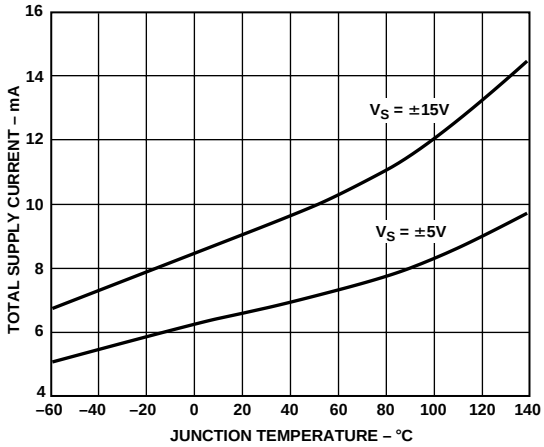


Figure 7. Total Supply Current vs. Junction Temperature

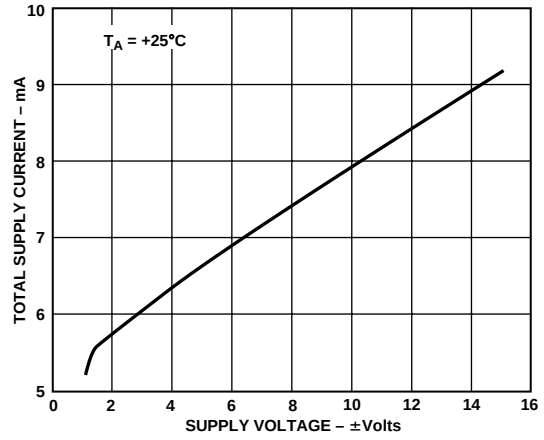


Figure 8. Total Supply Current vs. Supply Voltage

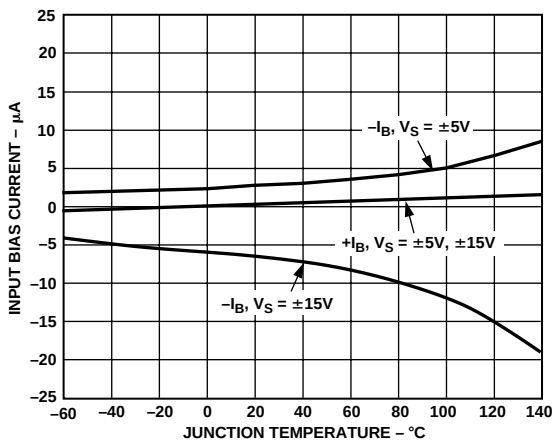


Figure 9. Input Bias Current vs. Junction Temperature

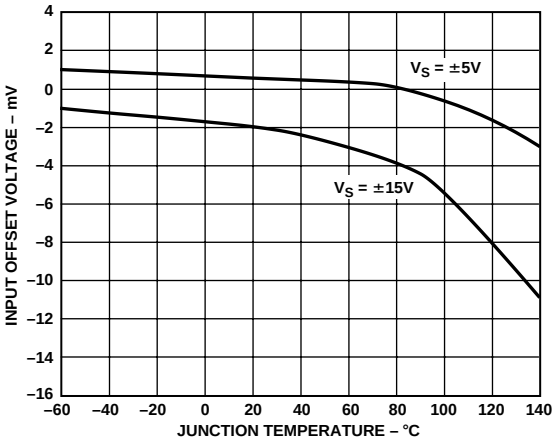


Figure 10. Input Offset Voltage vs. Junction Temperature

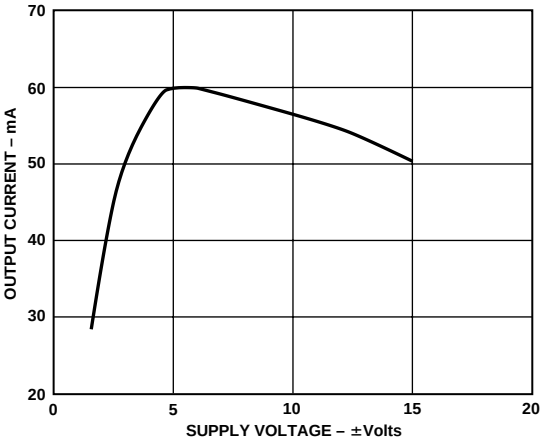


Figure 13. Linear Output Current vs. Supply Voltage

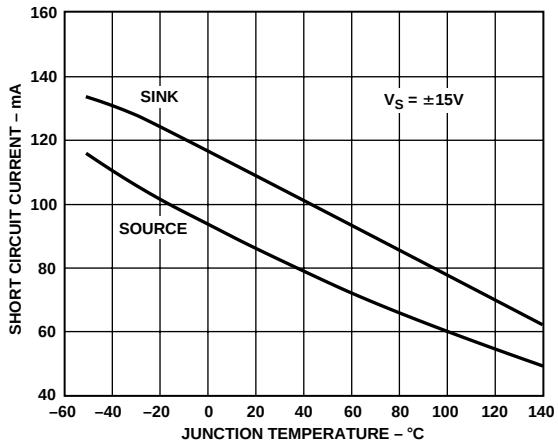


Figure 11. Short Circuit Current vs. Junction Temperature

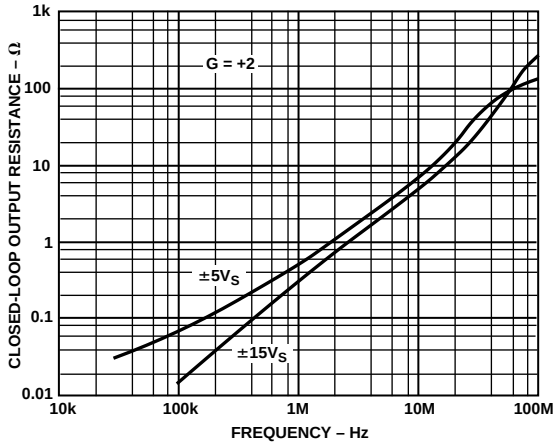


Figure 14. Closed-Loop Output Resistance vs. Frequency

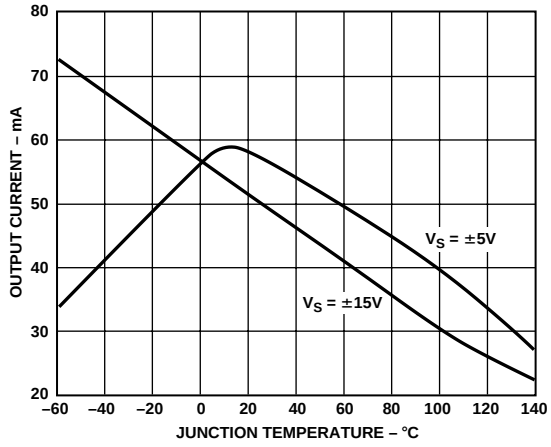


Figure 12. Linear Output Current vs. Junction Temperature

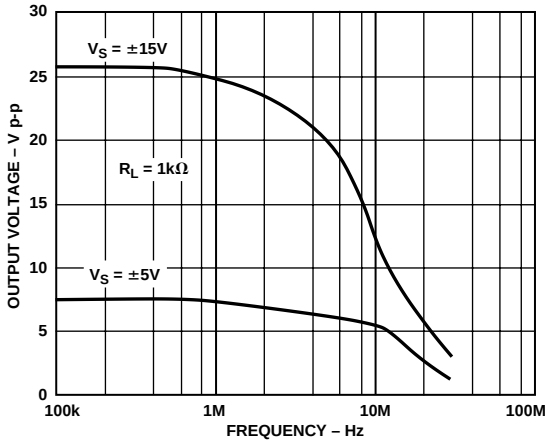


Figure 15. Large Signal Frequency Response

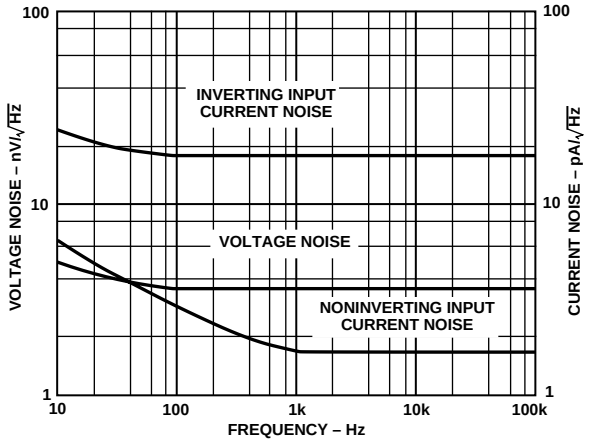


Figure 16. Input Current and Voltage Noise vs. Frequency

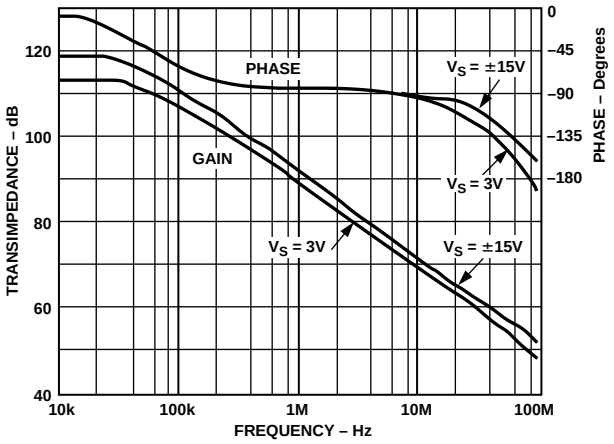


Figure 19. Open-Loop Transimpedance vs. Frequency (Relative to 1 Ω)

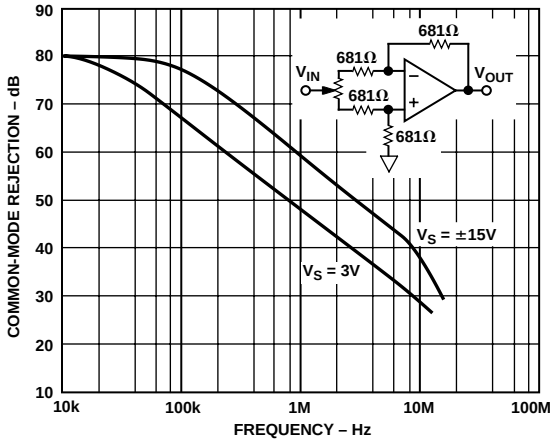


Figure 17. Common-Mode Rejection vs. Frequency

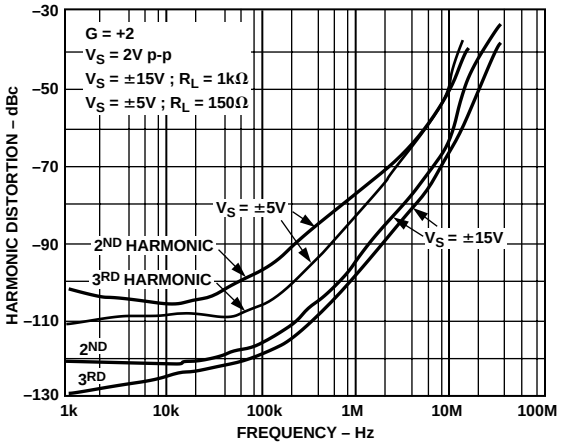


Figure 20. Harmonic Distortion vs. Frequency

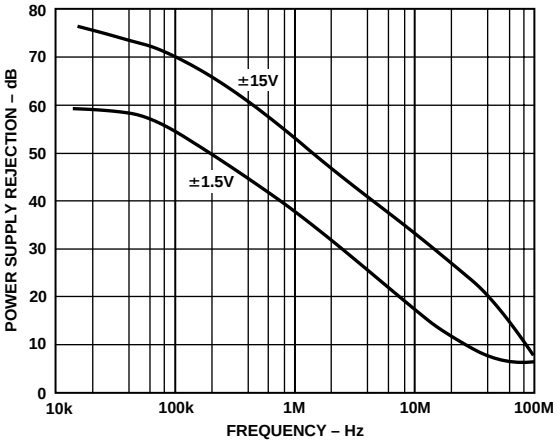


Figure 18. Power Supply Rejection vs. Frequency

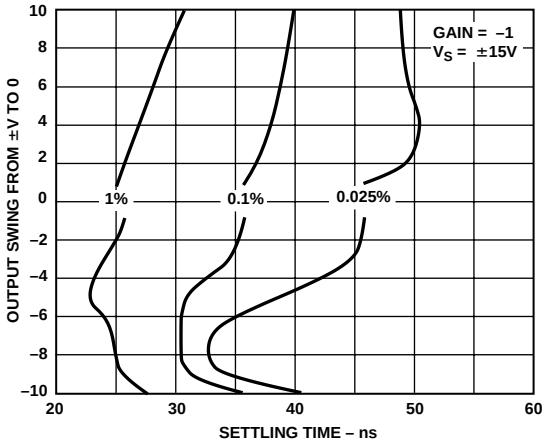


Figure 21. Output Swing and Error vs. Settling Time

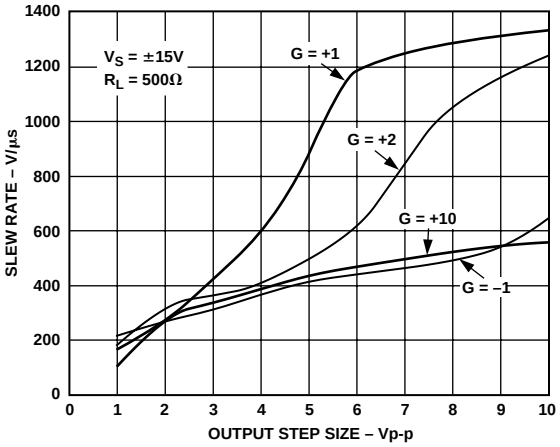


Figure 22. Slew Rate vs. Output Step Size

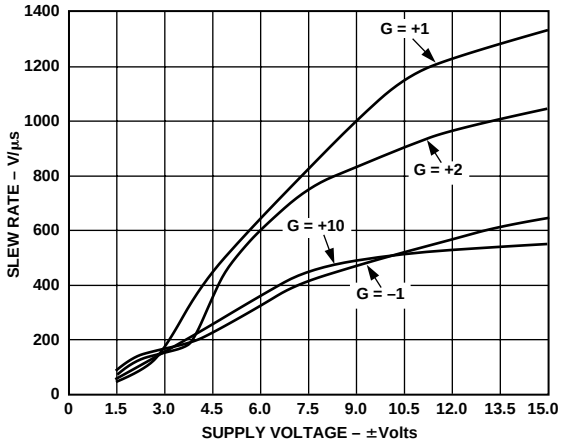


Figure 25. Maximum Slew Rate vs. Supply Voltage

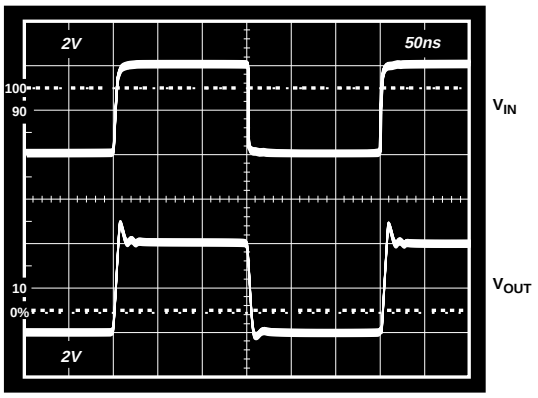


Figure 23. Large Signal Pulse Response, Gain = +1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

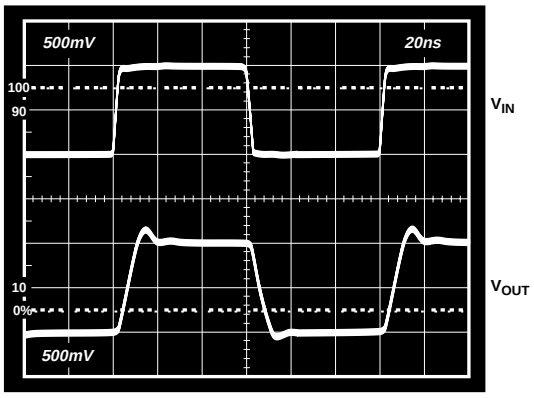


Figure 26. Small Signal Pulse Response, Gain = +1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

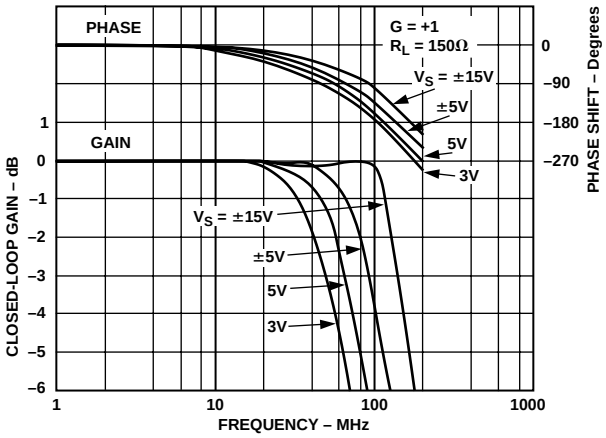


Figure 24. Closed-Loop Gain and Phase vs. Frequency, G = +1

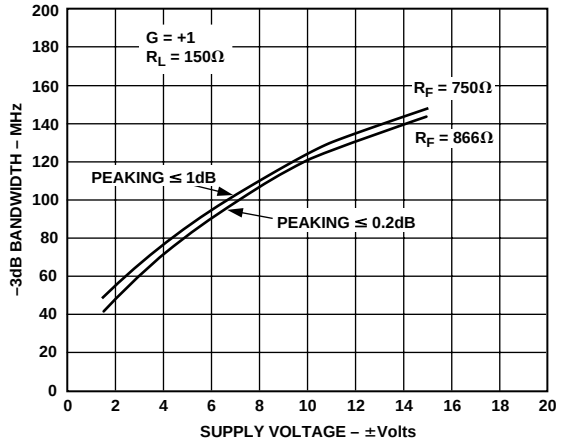


Figure 27. –3 dB Bandwidth vs. Supply Voltage, G = +1

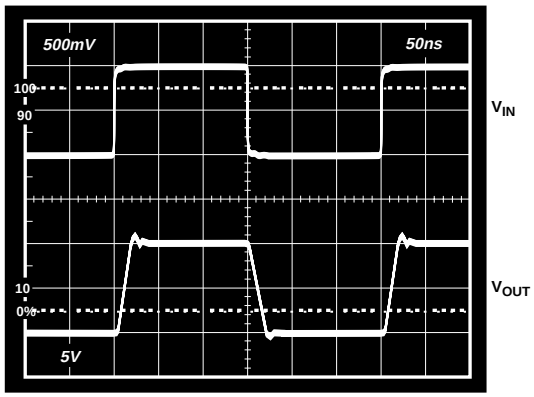


Figure 28. Large Signal Pulse Response, Gain = +10, (R_F = 357 Ω, R_L = 500 Ω, V_S = ±15 V)

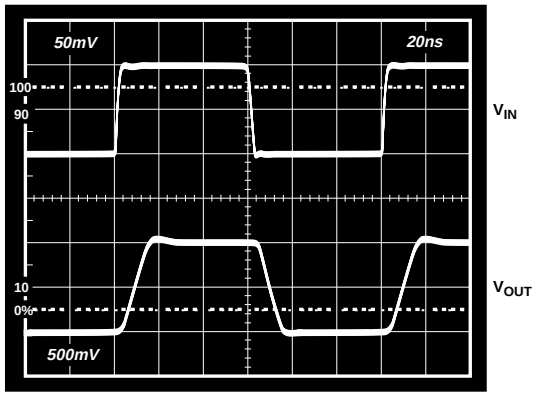


Figure 31. Small Signal Pulse Response, Gain = +10, (R_F = 357 Ω, R_L = 150 Ω, V_S = ±5 V)

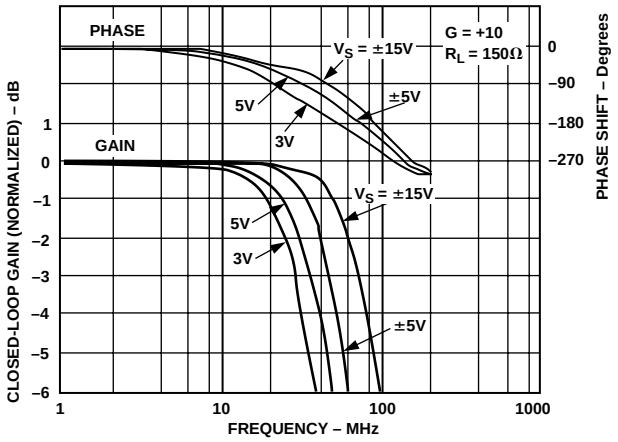


Figure 29. Closed-Loop Gain and Phase vs. Frequency, Gain = +10, R_L = 150 Ω

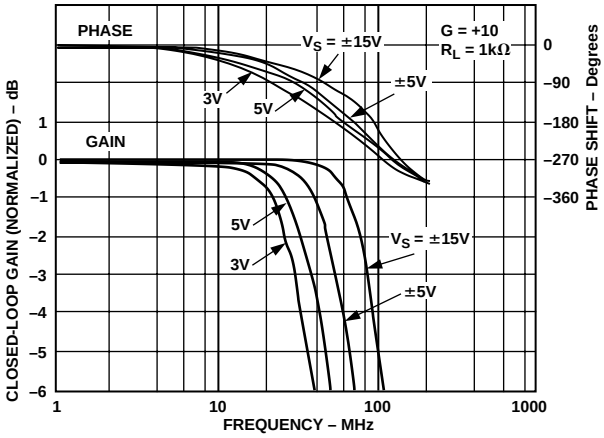


Figure 32. Closed-Loop Gain and Phase vs. Frequency, Gain = +10, R_L = 1 kΩ

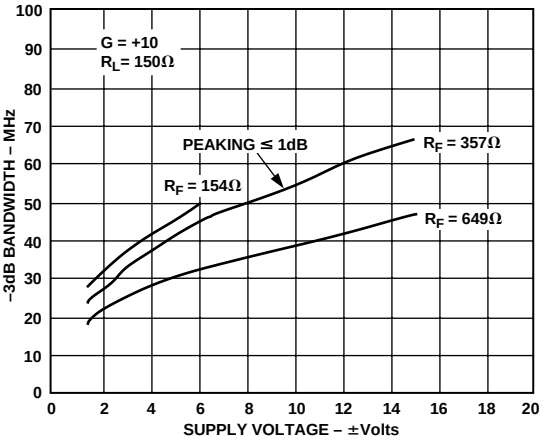


Figure 30. –3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 150 Ω

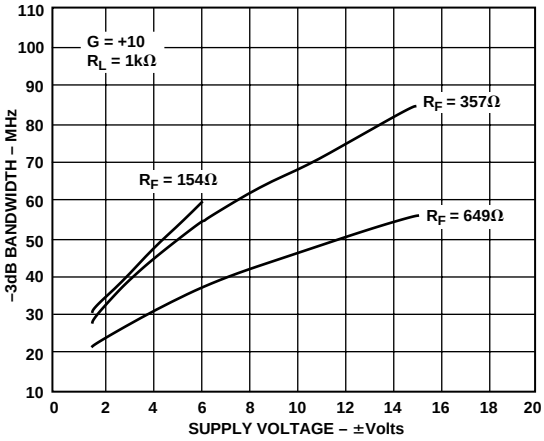


Figure 33. –3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 1 kΩ

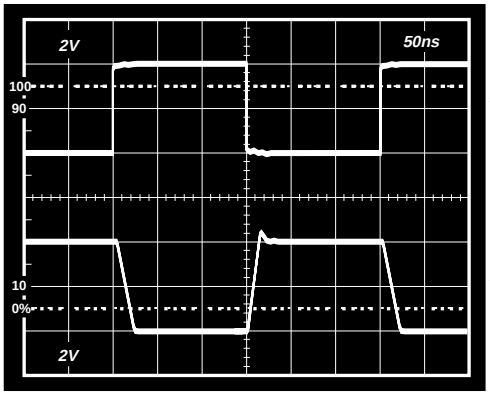


Figure 34. Large Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

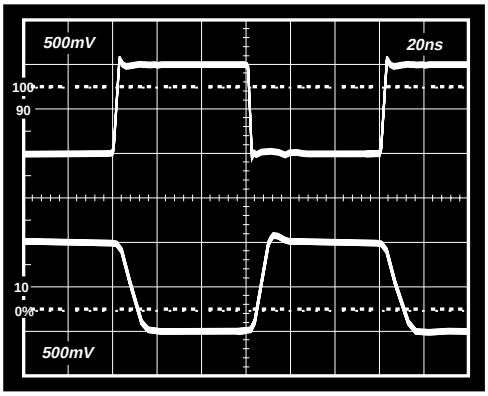


Figure 37. Small Signal Pulse Response, Gain = –1, (R_F = 750 Ω, R_L = 150 Ω, V_S = ±5 V)

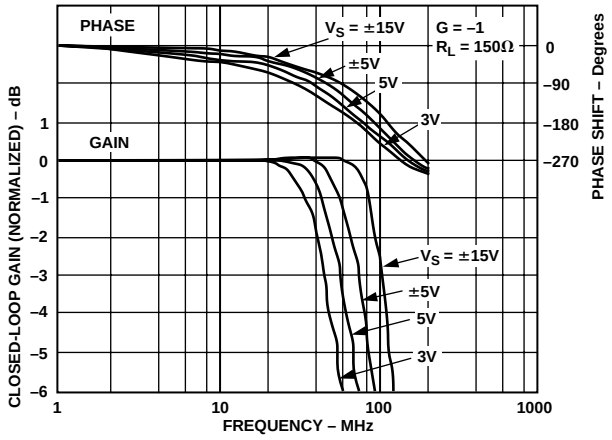


Figure 35. Closed-Loop Gain and Phase vs. Frequency, Gain = –1, R_L = 150 Ω

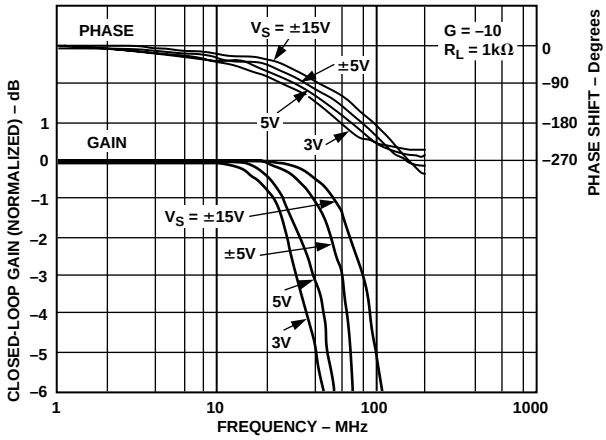


Figure 38. Closed-Loop Gain and Phase vs. Frequency, Gain = –10, R_L = 1 kΩ

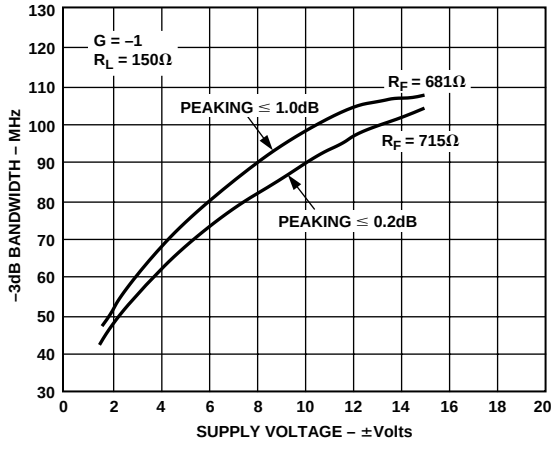


Figure 36. –3 dB Bandwidth vs. Supply Voltage, Gain = –1, R_L = 150 Ω

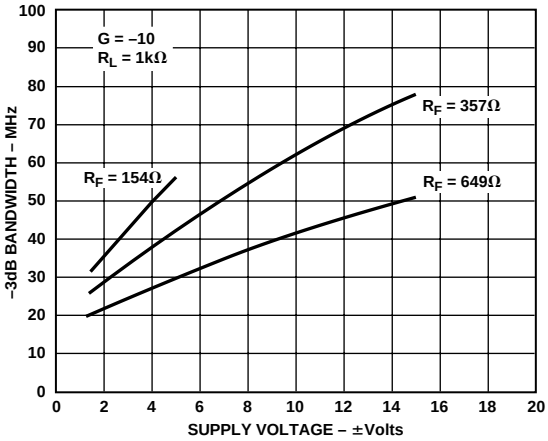


Figure 39. –3 dB Bandwidth vs. Supply Voltage, Gain = –10, R_L = 1 kΩ

General Considerations

The AD812 is a wide bandwidth, dual video amplifier which offers a high level of performance on less than 5.5 mA per amplifier of quiescent supply current. It is designed to offer outstanding performance at closed-loop inverting or noninverting gains of one or greater.

Built on a low cost, complementary bipolar process, and achieving bandwidth in excess of 100 MHz, differential gain and phase errors of better than 0.1% and 0.1° (into 150 Ω), and output current greater than 40 mA, the AD812 is an exceptionally efficient video amplifier. Using a conventional current feedback architecture, its high performance is achieved through careful attention to design details.

Choice of Feedback and Gain Resistors

Because it is a current feedback amplifier, the closed-loop bandwidth of the AD812 depends on the value of the feedback resistor. The bandwidth also depends on the supply voltage. In addition, attenuation of the open-loop response when driving load resistors less than about 250 Ω will affect the bandwidth. Table I contains data showing typical bandwidths at different supply voltages for some useful closed-loop gains when driving a load of 150 Ω. (Bandwidths will be about 20% greater for load resistances above a few hundred ohms.)

The choice of feedback resistor is not critical unless it is important to maintain the widest, flattest frequency response. The resistors recommended in the table are those (metal film values) that will result in the widest 0.1 dB bandwidth. In those applications where the best control of the bandwidth is desired, 1% metal film resistors are adequate. Wider bandwidths can be attained by reducing the magnitude of the feedback resistor (at the expense of increased peaking), while peaking can be reduced by increasing the magnitude of the feedback resistor.

Table I. –3 dB Bandwidth vs. Closed-Loop Gain and Feedback Resistor (R_L = 150 Ω)

V_S (V)	Gain	R_F (Ω)	BW (MHz)
±15	+1	866	145
	+2	715	100
	+10	357	65
	–1	715	100
	–10	357	60
±5	+1	750	90
	+2	681	65
	+10	154	45
	–1	715	70
	–10	154	45
+5	+1	750	60
	+2	681	50
	+10	154	35
	–1	715	50
	–10	154	35
+3	+1	750	50
	+2	681	40
	+10	154	30
	–1	715	40
	–10	154	25

To estimate the –3 dB bandwidth for closed-loop gains or feedback resistors not listed in the above table, the following two pole model for the AD812 many be used:

$$A_{CL} = \frac{G}{S^2\left[\frac{\left(R_F + Gr_{IN}\right)C_T}{2\pi f_2}\right] + S\left(R_F + Gr_{IN}\right)C_T + 1}$$

where: A_{CL} = closed-loop gain
G = 1 + R_F/R_G
r_{IN} = input resistance of the inverting input
C_T = "transcapacitance," which forms the open-loop dominant pole with the tranresistance
R_F = feedback resistor
R_G = gain resistor
f_2 = frequency of second (nondominant) pole
S = 2 $\pi j f$

Appropriate values for the model parameters at different supply voltages are listed in Table II. Reasonable approximations for these values at supply voltages not found in the table can be obtained by a simple linear interpolation between those tabulated values which "bracket" the desired condition.

Table II. Two-Pole Model Parameters at Various Supply Voltages

V_S	r_{IN} (Ω)	C_T (pF)	f_2 (MHz)
±15	85	2.5	150
±5	90	3.8	125
+5	105	4.8	105
+3	115	5.5	95

As discussed in many amplifier and electronics textbooks (such as Roberge's *Operational Amplifiers: Theory and Practice*), the –3 dB bandwidth for the 2-pole model can be obtained as:

$$f_3 = f_N\,[1 - 2d^2 + (2 - 4d^2 + 4d^4)^{1/2}]^{1/2}$$

where:

$$f_N = \left[\frac{f_2}{\left(R_F + Gr_{IN}\right)C_T}\right]^{1/2}$$

and:

$$d = (1/2)\,[f_2\,(R_F + Gr_{IN})\,C_T]^{1/2}$$

This model will predict –3 dB bandwidth within about 10 to 15% of the correct value when the load is 150 Ω. However, it is not an accurate enough to predict either the phase behavior or the frequency response peaking of the AD812.

Printed Circuit Board Layout Guidelines

As with all wideband amplifiers, printed circuit board parasitics can affect the overall closed-loop performance. Most important for controlling the 0.1 dB bandwidth are stray capacitances at the output and inverting input nodes. Increasing the space between signal lines and ground plane will minimize the coupling. Also, signal lines connecting the feedback and gain resistors should be kept short enough that their associated inductance does not cause high frequency gain errors.

Power Supply Bypassing

Adequate power supply bypassing can be very important when optimizing the performance of high speed circuits. Inductance in the supply leads can (for example) contribute to resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to a load, then large (greater than 1 μF) bypass capacitors are required to produce the best settling time and lowest distortion. Although 0.1 μF capacitors may be adequate in some applications, more elaborate bypassing is required in other cases.

When multiple bypass capacitors are connected in parallel, it is important to be sure that the capacitors themselves do not form resonant circuits. A small (say 5 Ω) resistor may be required in series with one of the capacitors to minimize this possibility.

As discussed below, power supply bypassing can have a significant impact on crosstalk performance.

Achieving Low Crosstalk

Measured crosstalk from the output of amplifier 2 to the input of amplifier 1 of the AD812 is shown in Figure 40. The crosstalk from the output of amplifier 1 to the input of amplifier 2 is a few dB better than this due to the additional distance between critical signal nodes.

A carefully laid-out PC board should be able to achieve the level of crosstalk shown in the figure. The most significant contributors to difficulty in achieving low crosstalk are inadequate power supply bypassing, overlapped input and/or output signal paths, and capacitive coupling between critical nodes.

The bypass capacitors must be connected to the ground plane at a point close to and between the ground reference points for the two loads. (The bypass of the negative power supply is particularly important in this regard.) There are two amplifiers in the package, and low impedance signal return paths must be provided for each load. (Using a parallel combination of 1 μF, 0.1 μF, and 0.01 μF bypass capacitors will help to achieve optimal crosstalk.)

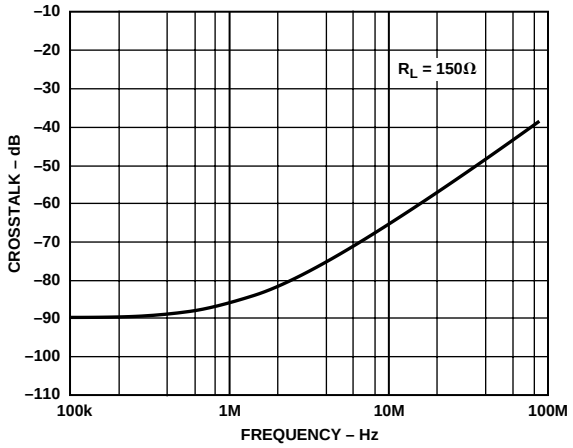


Figure 40. Crosstalk vs. Frequency

The input and output signal return paths must also be kept from overlapping. Since ground connections are not of perfectly zero impedance, current in one ground return path can produce a voltage drop in another ground return path if they are allowed to overlap.

Electric field coupling external to (and across) the package can be reduced by arranging for a narrow strip of ground plane to be run between the pins (parallel to the pin rows). Doing this on both sides of the board can reduce the high frequency crosstalk by about 5 dB or 6 dB.

Driving Capacitive Loads

When used with the appropriate output series resistor, any load capacitance can be driven without peaking or oscillation. In most cases, less than 50 Ω is all that is needed to achieve an extremely flat frequency response. As illustrated in Figure 44, the AD812 can be very attractive for driving largely capacitive loads. In this case, the AD812's high output short circuit current allows for a 150 V/μs slew rate when driving a 510 pF capacitor.

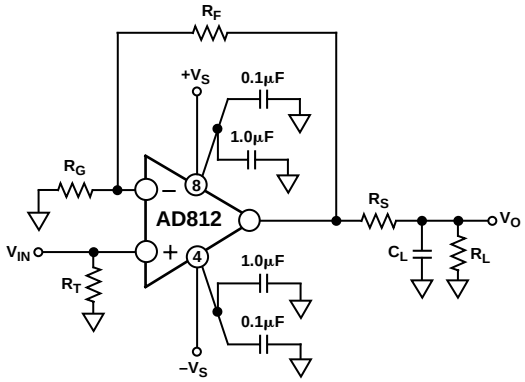


Figure 41. Circuit for Driving a Capacitive Load

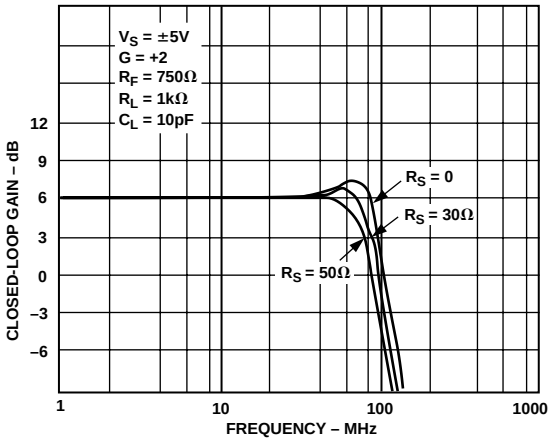


Figure 42. Response to a Small Load Capacitor at ±5 V

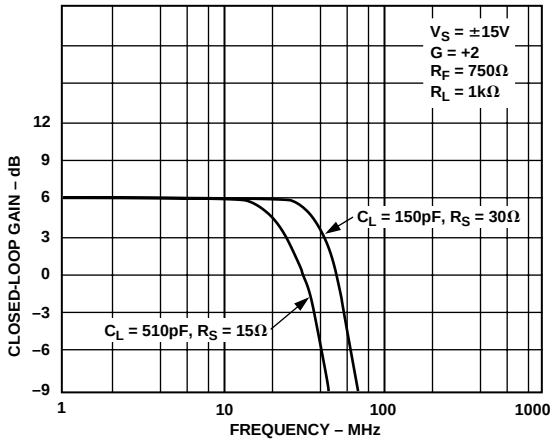


Figure 43. Response to Large Load Capacitor, V_S = ±15 V

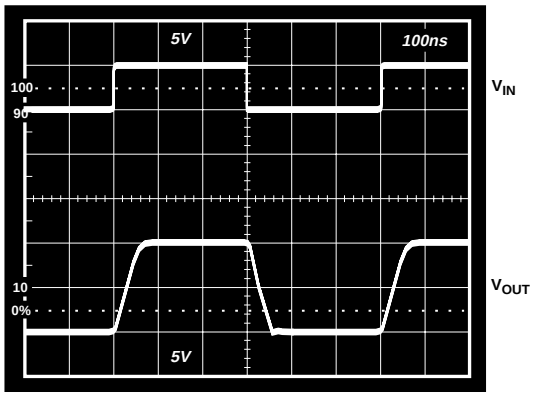


Figure 44. Pulse Response of Circuit of Figure 41 with C_L = 510 pF, R_L = 1 kΩ, R_F = R_G = 715 Ω, R_S = 15 Ω

Overload Recovery

There are three important overload conditions to consider. They are due to input common mode voltage overdrive, input current overdrive, and output voltage overdrive. When the amplifier is configured for low closed-loop gains, and its input common-mode voltage range is exceeded, the recovery time will be very fast, typically under 10 ns. When configured for a higher gain, and overloaded at the output, the recovery time will also be short. For example, in a gain of +10, with 6 dB of input overdrive, the recovery time of the AD812 is about 10 ns.

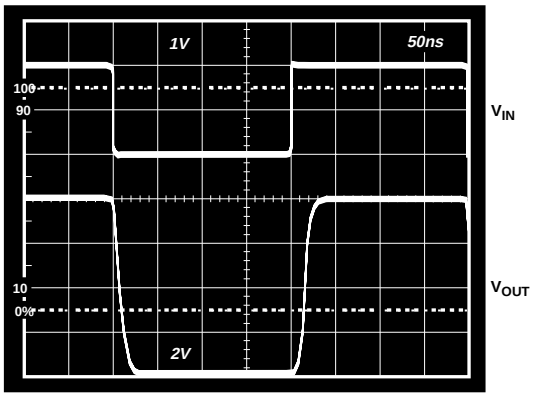


Figure 45. 6 dB Overload Recovery; G = 10, R_L = 500 Ω, V_S = ±5 V

In the case of high gains with very high levels of input overdrive, a longer recovery time may occur. For example, if the input common-mode voltage range is exceeded in a gain of +10, the recovery time will be on the order of 100 ns. This is primarily due to current overloading of the input stage.

As noted in the warning under "Maximum Power Dissipation," a high level of input overdrive in a high noninverting gain circuit can result in a large current flow in the input stage. For differential input voltages of less than about 1.25 V, this will be internally limited to less than 20 mA (decreasing with supply voltage). For input overdrives which result in higher differential input voltages, power dissipation in the input stage must be considered. It is recommended that external diode clamps be used in cases where the differential input voltage is expected to exceed 1.25 V.

High Performance Video Line Driver

At a gain of +2, the AD812 makes an excellent driver for a back-terminated 75 Ω video line. Low differential gain and phase errors and wide 0.1 dB bandwidth can be realized over a wide range of power supply voltage. Outstanding gain and group delay matching are also attainable over the full operating supply voltage range.

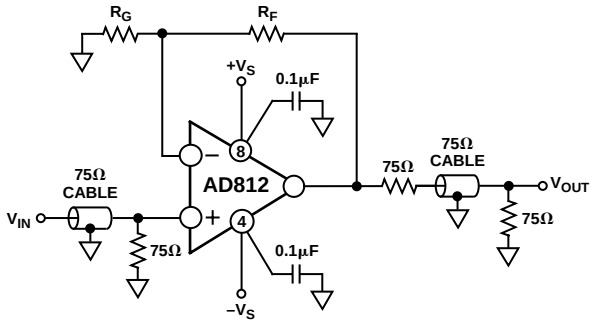


Figure 46. Gain of +2 Video Line Driver (R_F = R_G from Table I)

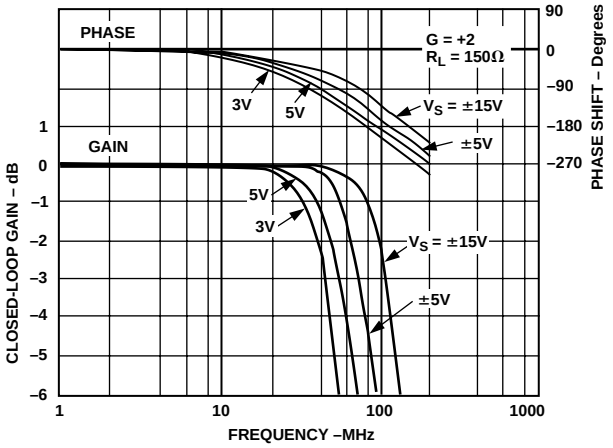


Figure 47. Closed-Loop Gain and Phase vs. Frequency for the Line Driver

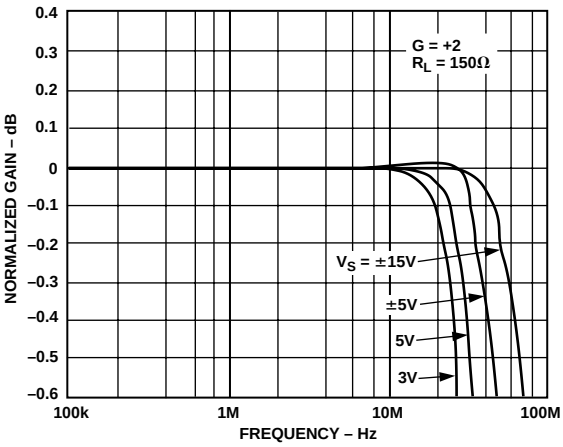


Figure 50. Fine-Scale Gain Flatness vs. Frequency, Gain = +2, R_L = 150 Ω

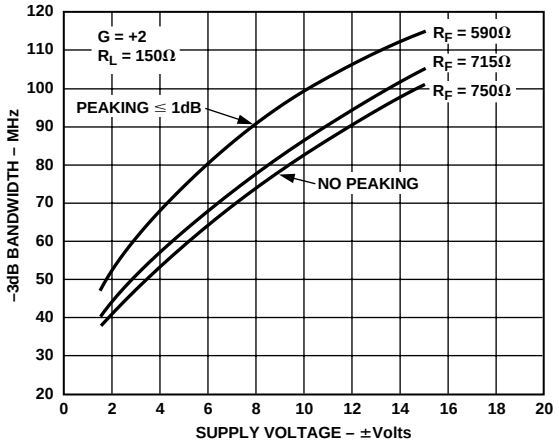


Figure 48. –3 dB Bandwidth vs. Supply Voltage, Gain = +2, R_L = 150 Ω

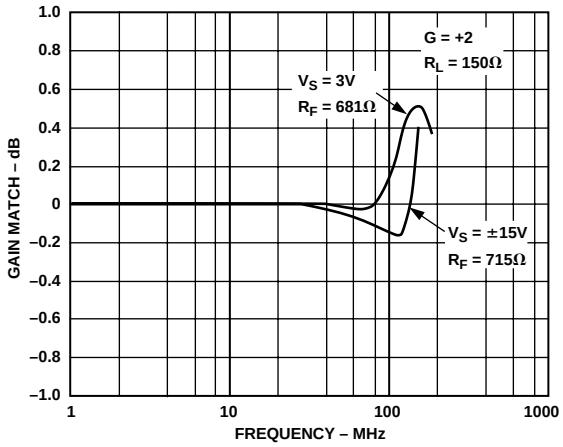


Figure 51. Closed-Loop Gain Matching vs. Frequency, Gain = +2, R_L = 150 Ω

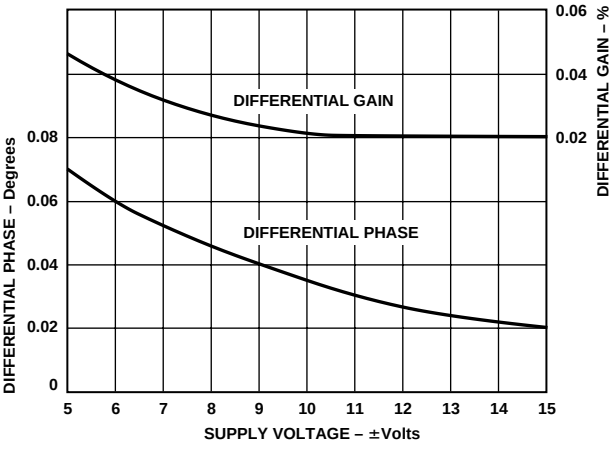


Figure 49. Differential Gain and Phase vs. Supply Voltage, Gain = +2, R_L = 150 Ω

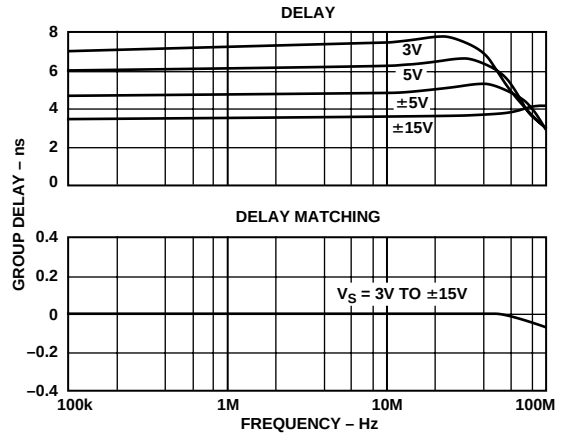


Figure 52. Group Delay and Group Delay Matching vs. Frequency, G = +2, R_L = 150 Ω

Operation Using a Single Supply

The AD812 will operate with total supply voltages from 36 V down to 2.4 V. With proper biasing (see Figure 53), it can be an outstanding single supply video amplifier. Since the input and output voltage ranges extend to within 1 volt of the supply rails, it will handle a 1.3 V p-p signal on a single 3.3 V supply, or a 3 V p-p signal on a single 5 V supply. The small signal, 0.1 dB bandwidths will exceed 10 MHz in either case, and the large signal bandwidths will exceed 6 MHz.

The capacitively coupled cable driver in Figure 53 will achieve outstanding differential gain and phase errors of 0.07% and 0.06 degrees respectively on a single 5 V supply. Resistor R2, in this circuit, is selected to optimize the differential gain and phase by operating the amplifier in its most linear region. To optimize the circuit for a 3 V supply, a value of 8 kΩ is recommended for R2.

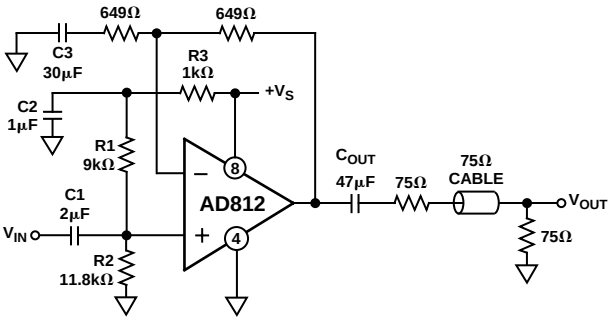


Figure 53. Biasing for Single Supply Operation

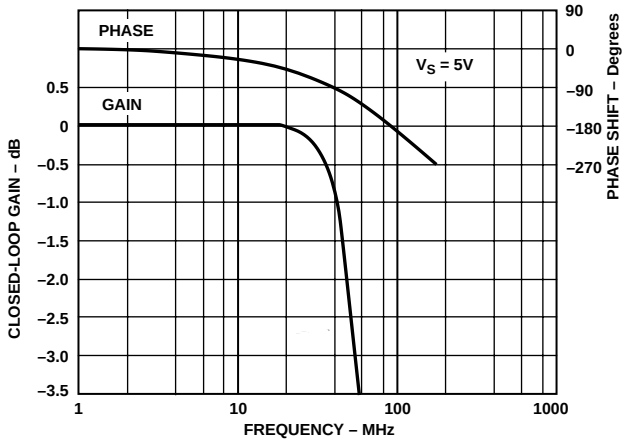


Figure 54. Closed-Loop Gain and Phase vs. Frequency, Circuit of Figure 53

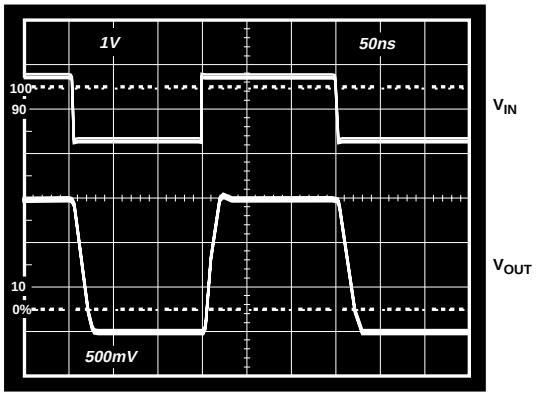
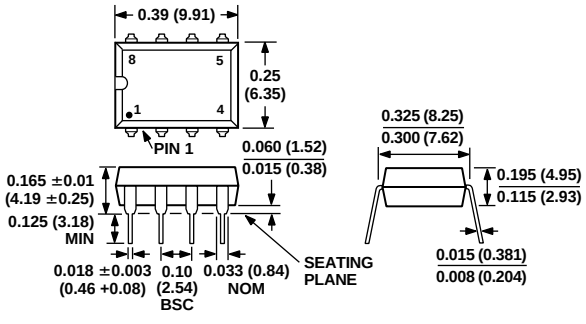


Figure 55. Pulse Response of the Circuit of Figure 53 with V_S = 5 V

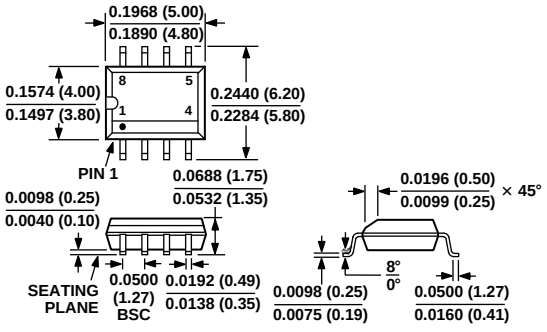
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead Plastic SOIC
(SO-8)



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