USB 3.0 and USB 2.0 Differential Switch 2:1/1:2 MUX/DEMUX

Check for Samples: HD3SS6126

FEATURES

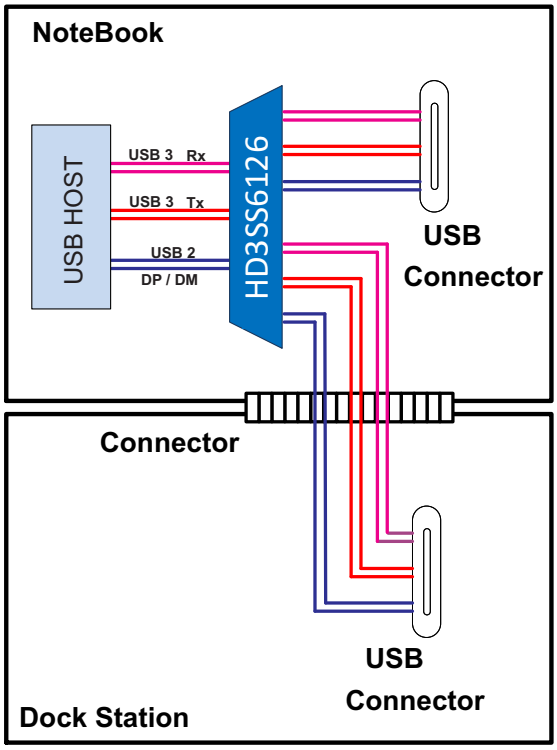
- **Ideal for USB Applications**
  - **Signal Switch for USB 3.0 (SuperSpeed USB and USB 2.0 HS/FS/LS)**
- **Three Bi-directional Differential Pair Channel MUX/DEMUX Switch Also Suitable for DisplayPort, PCIe Gen1/2/3, SATA 1.5/3/6G, SAS 1.5/3/6G and XAUI Applications**
- **Supports Data Rates up to 10 Gbps on High-bandwidth Path (SS)**
- **VCC Operating Range 3.3V ± 10%**
- **Wide –3dB Differential BW of Over 10 GHz on High-bandwidth Path (SS)**
- **Utilizes a unique adaptation method to maintain a constant channel impedance over the supported common mode voltage range**
- **Excellent High-bandwidth Path Dynamic Characteristics (at 2.5 GHz)**
  - **Crosstalk = –35 dB**
  - **Isolation = –23 dB**
  - **Insertion Loss = –1.1 dB**
  - **Return Loss = –11 dB**
- **Small 3.5mm x 9 mm, 42-Pin WQFN Package (RUA)**
- **Active Mode Power = 8 mW**

APPLICATIONS

- **Desktop PCs**
- **Notebook PCs**
- **Tablets**
- **Docking Station**
- **Telecommunications**
- **Televisions**

DESCRIPTION

The HD3SS6126 is a high speed passive switch that is designed for USB applications to route both SuperSpeed USB RX and TX and USB 2.0 DP/DM signals from a source to two destination or vice-versa. It can also be used for DisplayPort, PCI Express, SATA, SAS, and XAUI applications. The HD3SS6126 can be used in either sink side or source side applications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

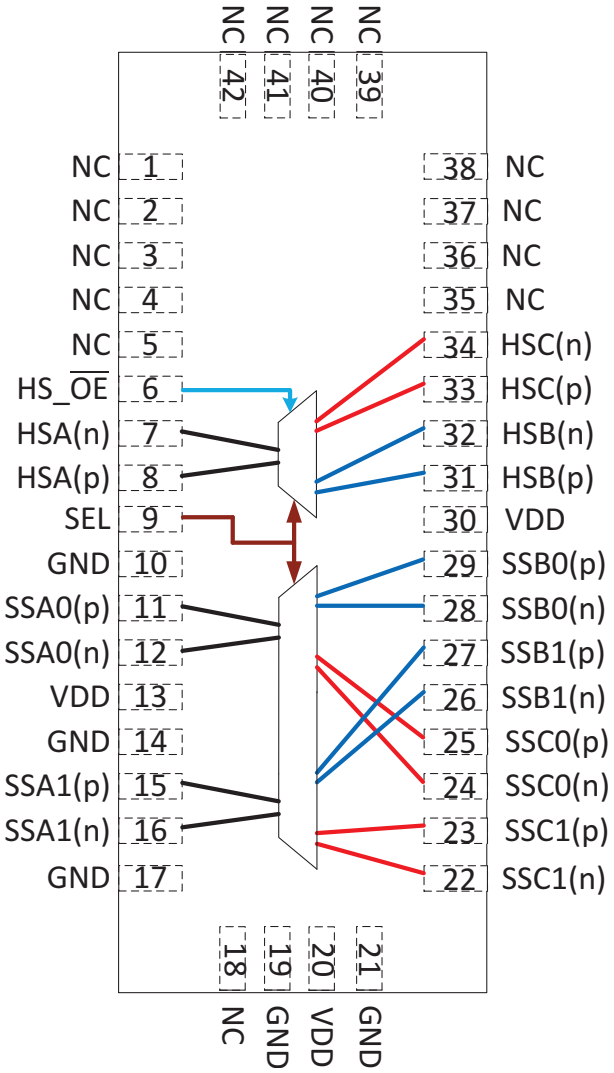
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTIONAL DIAGRAM



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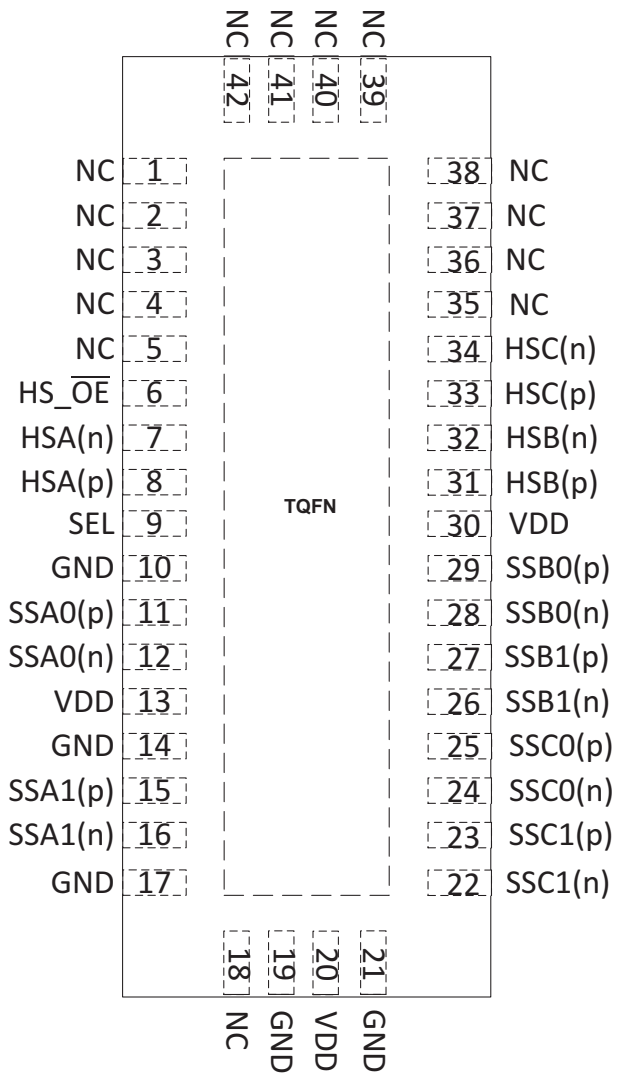
TRUTH TABLE USB 3.0 SuperSpeed USB

SEL	USB 3.0 Port Selection		
	SSA0/1	SSB0/1	SSC0/1
0	To/From SSB0/1	To/From SSA0/1	Off
1	To/From SSC0/1	Off	To/From SSA0/1

TRUTH TABLE USB 2.0 High-speed/Full-speed/Low-speed Path

HS_$\overline{OE}$	SEL	USB 2.0 Port Selection		
		HSA	HSB	HSC
0	0	To/From HSB	To/From HSA	Off
0	1	To/From HSC	Off	To/From HSA
1	X	Off	Off	Off

PINOUT
TOP VIEW



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PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	10, 14, 17, 19, 21	Supply	Ground
HSA(p)	8	I/O	Port A USB 2.0 positive signal
HSA(n)	7		Port A USB 2.0 negative signal
HSB(p)	31	I/O	Port B USB 2.0 positive signal
HSB(n)	32		Port B USB 2.0 negative signal
HSC(p)	33	I/O	Port C USB 2.0 positive signal
HSC(n)	34		Port C USB 2.0 negative signal
HS_$\overline{OE}$	6	I (Control)	Output Enable H = Power Down L = Normal Operation
NC	1, 2, 3, 4, 5, 18, 35, 36, 37, 38, 39, 40, 41, 42		Electrically No Connection
SEL	9	I (Control)	USB 3.0/2.0 Port Selection Control Pins
SSA0(p)	11	I/O	Port A, Channel 0, USB 3.0 Positive Signal
SSA0(n)	12		Port A, Channel 0, USB 3.0 Negative Signal
SSA1(p)	15	I/O	Port A, Channel 1, USB 3.0 Positive Signal
SSA1(n)	16		Port A, Channel 1, USB 3.0 Negative Signal
SSB0(p)	29	I/O	Port B, Channel 0, USB 3.0 Positive Signal
SSB0(n)	28		Port B, Channel 0, USB 3.0 Negative Signal
SSB1(p)	27	I/O	Port B, Channel 1, USB 3.0 Positive Signal
SSB1(n)	26		Port B, Channel 1, USB 3.0 Negative Signal
SSC0(p)	25	I/O	Port C, Channel 0, USB 3.0 Positive Signal
SSC0(n)	24		Port C, Channel 0, USB 3.0 Negative Signal
SSC1(p)	23	I/O	Port C, Channel 1, USB 3.0 Positive Signal
SSC1(n)	22		Port C, Channel 1, USB 3.0 Negative Signal
VDD	13, 20, 30	Supply	3.3V power supply voltage

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range(2), V_{DD}		–0.3	4	V
Voltage range	Differential I/O, High-bandwidth signal path: SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n)	–0.5	4	V
	Differential I/O, Low-bandwidth signal path: HSAp/n), HSB(p/n), HSC(p/n)	-0.5	7	
	Control pin and single ended I/O	–0.3	V_{DD} + 0.3	
Electrostatic discharge	Human body model(3)(4)		±2,000	V
	Charged-device model(5)		±500	
Continuous power dissipation		See Thermal Information Table		

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

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THERMAL INFORMATION

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance			53.8		°C/W
θ_{JB}	Junction-to-board thermal resistance			27.4		
θ_{JCT}	Junction-to-case-Top thermal resistance			38.2		
Ψ_{JB}	Junction-to-board thermal resistance Metric	High-K board (1)		27.3		
Ψ_{JT}	Junction-to-case-Top thermal resistance Metric	High-K board (1)		5.6		

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953A, *IC Package Thermal Metrics*. Test conditions for Ψ_{JB} and Ψ_{JT} are clarified in the application report.

RECOMMENDED OPERATING CONDITIONS

Typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C. All temp limits are specified by design.

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage	Control Pins	2.0		V_{DD}	V
V_{IL}	Input low voltage	Control Pins	–0.1		0.8	V
V_{I/O_Diff}	Differential voltage	Switch I/O differential voltage for High-bandwidth signal path only: SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n)	0		1.8	V_{p-p}
V_{I/O_CM}	Common voltage	Switch I/O common mode voltage for High-bandwidth signal path only: SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n)	0		2.0	V
T_A	Operating free-air temperature		0		70	°C

ELECTRICAL CHARACTERISTICS – DEVICE PARAMETERS

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	V_{DD} = 3.6 V, SEL = V_{DD} /GND; $\overline{OE}$ = GND; Outputs Floating		2.4	3	mA
SEL						
I_{IH}	Input high current	V_{DD} = 3.6V, V_{IN} = V_{DD}			95	µA
I_{IL}	Input high current	V_{DD} = 3.6V, V_{IN} = GND			1	µA
HS_$\overline{OE}$						
I_{IH}	Input high current	V_{DD} = 3.6V, V_{IN} = V_{DD}			1	µA
I_{IL}	Input high current	V_{DD} = 3.6V, V_{IN} = GND			1	µA
SSA0/1, SSB0/1, SSC0/1						
I_{LK}	High-impedance leakage current	V_{DD} = 3.6V, V_{IN} = 2V, V_{OUT}= 2V, (I_{LK} on open outputs Port B and C)			130	µA
		V_{DD} = 3.6V, V_{IN} = 2V, V_{OUT}= 2V, (I_{LK} on open outputs Port A)			4	µA
HSA, HSB, HSC						
I_{LK}	High-impedance leakage current	V_{DD} = 3.6V, V_{IN} = 0V, V_{OUT}= 0V to 4V, HS_$\overline{OE}$_IN = GND			1	µA

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ELECTRICAL CHARACTERISTICS – SIGNAL SWITCH PARAMETERS

under recommended operating conditions; R_L, R_{SC} = 50 Ω, C_L = 10pF (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n) Signal Path						
t_{on}	SEL-to-Switch t_{on}	R_{SC} and R_L = 50 Ω, See Figure 1		70	250	ns
t_{off}	SEL-to-Switch t_{off}			70	250	
t_{PD}	Switch propagation delay	R_{SC} and R_L = 50 Ω, See Figure 3			85	ps
$t_{SK(O)}$	Inter-pair output skew (CH-CH)	R_{SC} and R_L = 50 Ω, See Figure 3			20	ps
$t_{SK(b-b)}$	Intra-Pair Output Skew (bit-bit)				8	ps
C_{ON}	Outputs ON capacitance	V_{IN} = 0 V, Outputs Open, Switch ON		1.5		pF
C_{OFF}	Outputs OFF capacitance	V_{IN} = 0V, Outputs Open, Switch OFF		1		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3V, V_{CM} = 0V - 2V, I_O = –8 mA		5	8	Ω
ΔR_{ON}	ON resistance match between pairs of the same channel	V_{DD} = 3.3 V; 0 V ≤ V_{IN} ≤ 2 V; I_O = –8 mA			0.7	Ω
R_{FLAT_ON}	ON resistance flatness ($R_{ON(MAX)}$– $R_{ON(MIN)}$)	V_{DD} = 3.3 V; -0 V ≤ V_{IN} ≤ 2 V			1.15	Ω
R_L	Differential return loss (V_{CM} = 0 V)	f = 0.3 MHz		-25		dB
		f = 2.5 GHz		–11		
		f = 4 GHz		–11		
X_{TALK}	Differential crosstalk (V_{CM} = 0 V)	f = 0.3 MHz		-85		dB
		f = 2.5 GHz		–35		
		f = 4 GHz		–33		
O_{IRR}	Differential off-isolation (V_{CM} = 0 V)	f = 0.3 MHz		-85		dB
		f = 2.5 GHz		-23		
		f = 4 GHz		–21		
I_L	Differential insertion loss (V_{CM} = 0 V)	f = 0.3 MHz		-0.43		dB
		f = 2.5 GHz		–1.1		
		f = 4 GHz		–1.3		
BW	Bandwidth	At –3 dB		10		GHz
HSA(p/n), HSB(p/n), HSC(p/n) SIGNAL PATH						
t_{ON}	SEL to Switch t_{ON}	See Figure 2			30	ns
	HS_$\overline{OE}$ to Switch t_{ON}				17	
t_{OFF}	SEL to Switch t_{OFF}	See Figure 2			12	
	HS_$\overline{OE}$ to Switch t_{OFF}				10	
t_{PD} (1)	Switch propagation delay	See Figure 3		250		ps
$t_{SK(O)}$ (1)	Inter-pair output skew (CH-CH)			100	200	ps
$t_{SK(P)}$ (1)	Intra-Pair Output Skew (bit-bit)			100	200	
C_{ON}	Outputs ON capacitance	V_{IN} = 0 V, Outputs Open, Switch ON		6	7.5	pF
C_{OFF}	Outputs OFF capacitance	V_{IN} = 0 V, Outputs Open, Switch OFF		3.5	6	pF
R_{ON}	Output ON resistance	V_{DD} = 3 V, V_{IN} = 0 V, I_O = 30 mA		3	6	Ω
		V_{DD} = 3 V, V_{IN} = 2.4 V, I_O = 30 mA		3.4	6	
ΔR_{ON}	ON resistance match between pairs of the same channel	V_{DD} = 3 V; V_{IN} = 0 V; I_O = 30 mA		0.2		Ω
		V_{DD} = 3 V; V_{IN} = 1.7 V; I_O = -15 mA		0.2		

(1) Specified by design

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ELECTRICAL CHARACTERISTICS – SIGNAL SWITCH PARAMETERS (continued)

under recommended operating conditions; R_L, R_{SC} = 50 Ω, C_L = 10pF (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SSA0/1(p/n), SSB0/1(p/n), SSC0/1(p/n) Signal Path						
R_{FLAT_ON}	ON resistance flatness ($R_{ON(MAX)}$– $R_{ON(MIN)}$)	V_{DD} = 3 V; V_{IN} = 0 V; I_O = 30 mA		1		Ω
		V_{DD} = 3 V; V_{IN} = 1.7 V; I_O = -15 mA		1		
X_{TALK}	Differential crosstalk (V_{CM} = 0 V)	R_L = 50 Ω, f = 250 MHz		-40		dB
O_{IRR}	Differential off-isolation (V_{CM} = 0 V)	R_L = 50 Ω, f = 250 MHz		-41		dB
BW	Bandwidth	R_L = 50 Ω		0.9		GHz

TEST TIMING DIAGRAMS

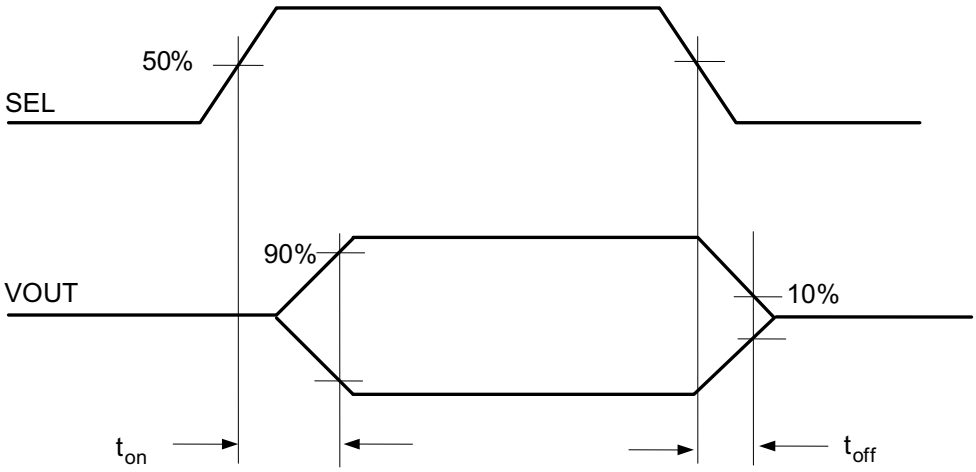
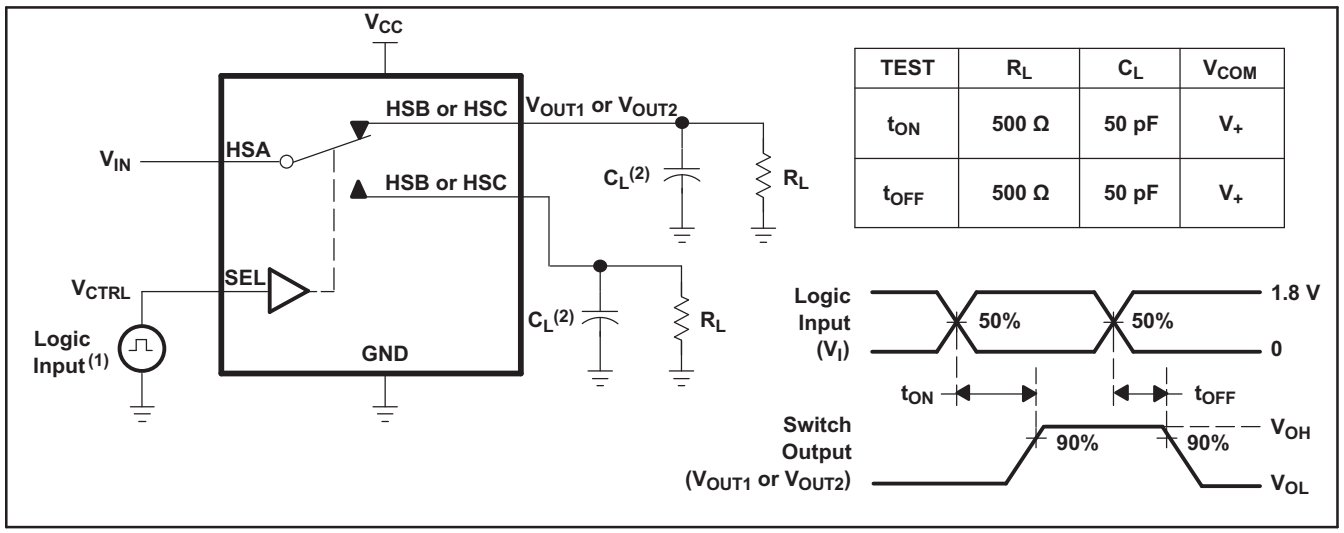


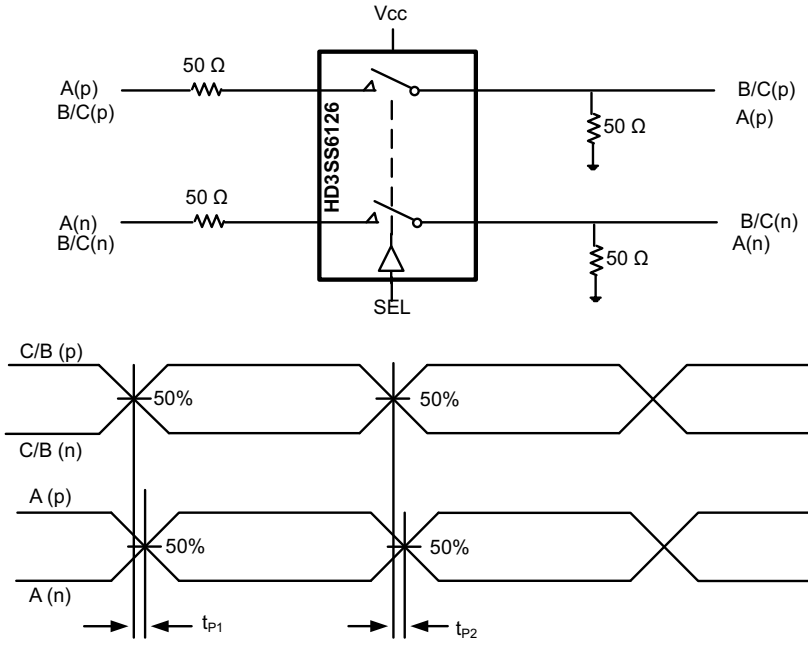
Figure 1. Select to Switch t_{on} and t_{off}



(1) All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHZ, Z_O = 50 Ω, t_r< 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 2. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

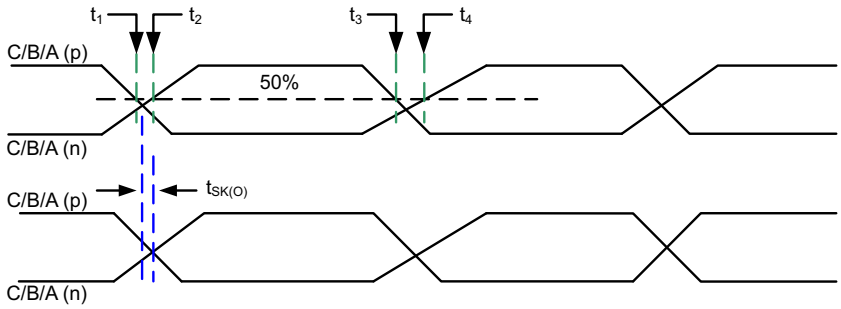
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Inter-pair skew

t_{PD} = Max(t_{p1}, t_{p2})

$t_{SK(O)}$ = Difference between t_{PD} for any two pairs of outputs



Intra-pair skew

$t_{SK(b\text{-}b)}$ = 0.5 X |(t_4 – t_3) + (t_1 – t_2)|

NOTES:

1. Measurements based on an ideal input with zero intra-pair skew on the input, i.e. the input at A to B/C or the input at B/C to A
2. Inter-pair skew is measured from lane to lane on the same channel, e.g. C0 to C1
3. Intra-pair skew is defined as the relative difference from the p and n signals of a single lane

Figure 3. Propagation Delay and Skew

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS6126RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	HD3SS6126	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

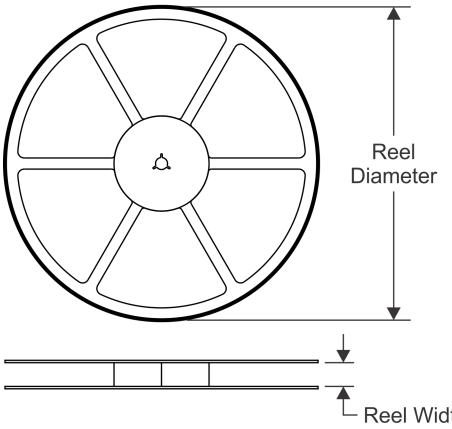
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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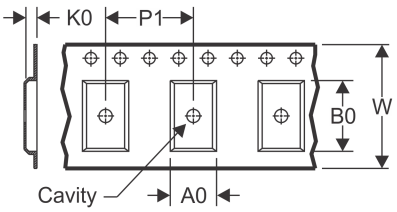
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

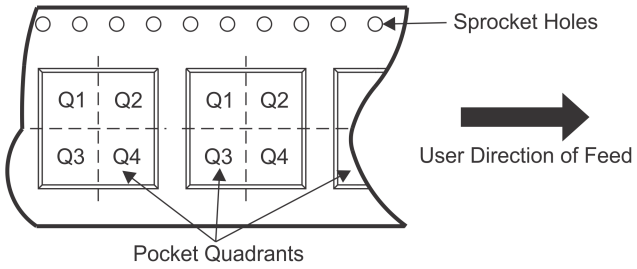


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

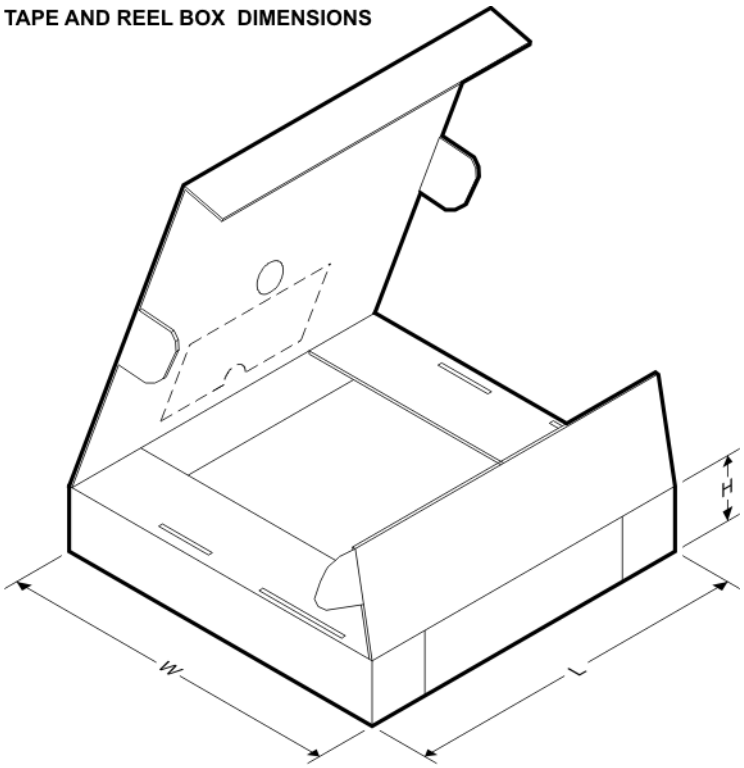
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS6126RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

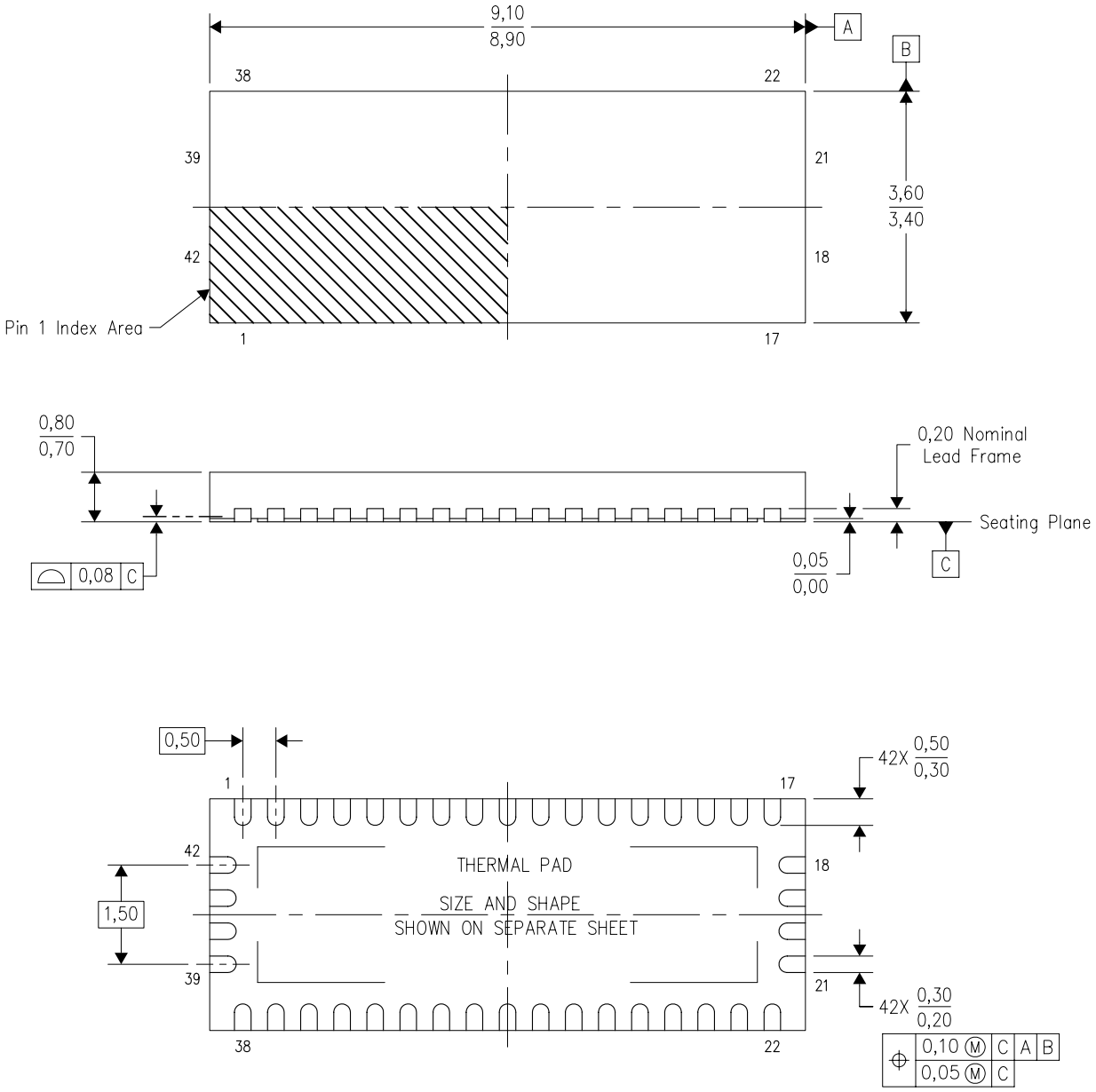
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS6126RUAR	WQFN	RUA	42	3000	367.0	367.0	38.0

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

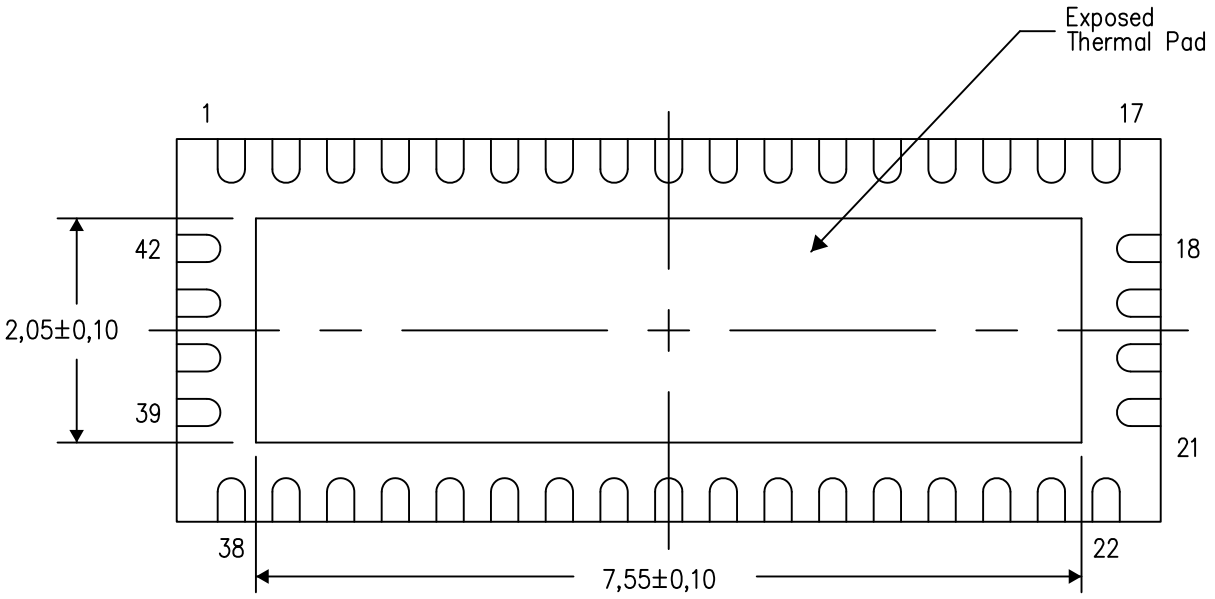
RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



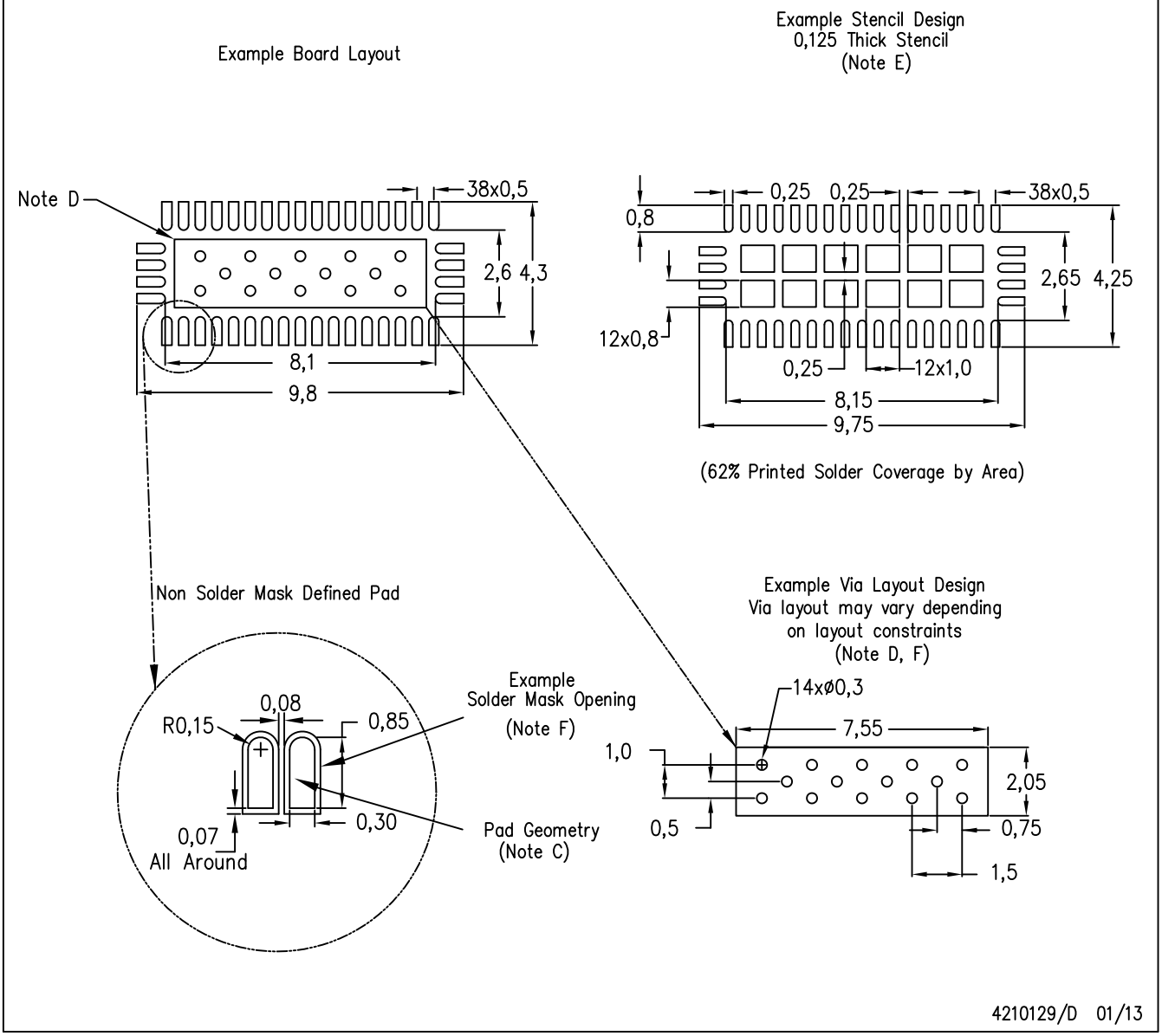
Bottom View

Exposed Thermal Pad Dimensions

4208352/E 01/13

NOTE: All linear dimensions are in millimeters

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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