Arm® Cortex®-M

32-bit Microcontroller

NuMicro® Family
M031/M032 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The new NuMicro® M031/M032 series 32-bit microcontroller based on Arm® Cortex®-M0 core features 1.8V ~ 3.6V operating voltage, 5V I/O tolerant and runs up to 48 MHz. It provides a solution for the applications that need low-voltage interface connection operation, such as mobile devices, application processor connected peripheral controllers, IoT sensor devices, motor control, industrial control, and consumer devices.

The M031/M032 series supports up to 128 Kbytes of Flash memory, up to 16 Kbytes of SRAM, for the program code and runtime storage. A special design 512 bytes SPROM (Security Protection ROM) is to protect user's code or library been read. It supports 4 Kbytes Flash memory of ISP (In-System Programming) to easily upgrade new firmware and the IAP (In-Application Programming) feature that can upgrade firmware while program is running.

The enhanced fast 2 MSPS conversion rate of 12-bit ADC, comparator and PWM control provide a fast and precise data conversion of the voltage, current, and sensor data, and fast response control for the external device, such as the current/voltage feedback from motor control or sensing devices.

The M031/M032 series provides plenty peripherals such as Universal Serial Control Interface (USCI) that can be set as UART/SPI/I^2C flexibly, up to 4-ch UART, 2-ch SPI/I^2S, 3-ch I^2C, USB, 16-ch 12-bit ADC, 12-ch 16-bit PWM, Hardware Divider and Comparator, etc. Besides, it offers EBI, PDMA and One-Wire UART special features for various application demands.

The M032 series is all based on the M031 and enhanced with the crystal-less USB 2.0 full-speed device feature to provide more possibilities of USB related application.

The M031/M032 series supports different package sizes from TSSOP 20-pin, TSSOP 28-pin, QFN 33-pin, to LQFP 48-pin and LQFP 64-pin. Different part numbers with same package are pin-to-pin compatible. It is easy for users to find the suitable part number for the application.

The NuMicro® M031/M032 series is suitable for a wide range of applications such as:

- Laser Distance Meter
- Air Detector/Cleaner
- Mobile LCD Panel Controller
- IoT Sensing Device
- HMI Controller
- Micro Printer
- Gaming Keyboard and Mouse
- WPC Wireless Charger

2 FEATURES

2.1 M031/M032 Features

Core and System	
Arm® Cortex®-M0	• Arm® Cortex®-M0 processor, running up to 48 MHz • Built-in Nested Vectored Interrupt Controller (NVIC) • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions
Hardware Divider (HDIV)	• Signed (two's complement) integer calculation • 32-bit dividend with 16-bit divisor calculation capacity • 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit) • 6 HCLK clocks taken for one cycle calculation
Brown-out Detector (BOD)	• Two-level BOD with brown-out interrupt and reset option. (2.5V/2.0V)
Low Voltage Reset (LVR)	• LVR with 1.7V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Flash	• Up to 128 KB application ROM (APROM) • Up to 4 KB Flash for user program loader (LDROM) • 512 bytes page erase for all embedded flash • Supports CRC-32 checksum calculation function • Hardware external read protection of whole flash memory by Security Lock Bit • Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded flash memory • Supports 2-wired ICP update through SWD/ICE interface
SRAM	• Up to 16 KB embedded SRAM • Supports byte-, half-word- and word-access • Supports PDMA mode
Cyclic Redundancy Calculation (CRC)	• Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32

	• Programmable initial value • Supports programmable order reverse setting for input data and CRC checksum • Supports programmable 1's complement setting for input data and CRC checksum. • Supports 8/16/32-bit of data width • Interrupt generated once checksum error occurs • Programmable seed value • 8-bit write mode: 1-AHB clock cycle operation • 16-bit write mode: 2-AHB clock cycle operation • 32-bit write mode: 4-AHB clock cycle operation • Supports using PDMA to write data to perform CRC operation
Peripheral DMA (PDMA)	• Supports up to 5 independent configurable channels for automatic data transfer between memories and peripherals • Channel 0, 1 supports time-out function • Basic and Scatter-Gather Transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Two types of priorities modes: Fixed-priority and Round-robin modes • Transfer data width of 8, 16, and 32 bits • Single and burst transfer type • Source and destination address can be increment or fixed. • PDMA transfer count up to 65536 • Request source can be from software, SPI/I^{2}S, USPI, UART, UUART, I^{2}C, ADC, PWM and Timer
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC) trimmed to 2% accuracy that can optionally be used as a system clock • 38.4 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Up to 96 MHz on-chip PLL, sourced from HIRC or HXT, allows CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal
Timers	

32-bit Timer	**TIMER** • Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter • Independent clock source for each timer • Provides one-shot, periodic, toggle-output and continuous counting operation modes • 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0]) • Supports event counting function from external pin. • Supports event counting source from internal USB SOF signal • 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0]) • Supports external capture pin event for interval measurement • Supports external capture pin event to reset 24-bit up counter • Supports internal capture triggered while internal ACMP output signal and LIRC transition • Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated • Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, ADC, PDMA function • Supports Inter-Timer trigger mode **PWM** • Supports maximum clock source frequency up to 96 MHz • Supports up to two PWM modules, each module provides 6 output channels. • Supports independent mode for PWM output/Capture input channel • Supports complementary mode for 3 complementary paired PWM output channels • Dead-time insertion with 12-bit resolution • Two compared values during one period • Supports 12-bit pre-scalar from 1 to 4096 • Supports 16-bit resolution PWM counter • Up, down and up/down counter operation type • Supports mask function and tri-state enable for each PWM pin • Supports brake function • Brake source from pin, ACMP and system safety events: clock failed, Brown-out detection and CPU lockup. • Noise filter for brake source from pin • Edge detect brake source to control brake state until brake interrupt cleared • Level detect brake source to auto recover function after brake condition removed • Supports interrupt on the following events:

	• PWM counter match zero, period value or compared value • Brake condition happened • Supports trigger ADC on the following events: • PWM counter match zero, period value or compared value • Supports up to 12 capture input channels with 16-bit resolution • Supports rising or falling capture condition • Supports input rising/falling capture interrupt • Supports rising/falling capture with counter reload option • Supports PDMA request from input capture event
Watchdog	• 20-bit free running up counter for WDT time-out interval. • Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 416us ~ 27.3 s if WDT_CLK = 38.4 kHz (LIRC). • System kept in reset state for a period of (1 / WDT_CLK) * 63. • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out • Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period. • Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register. • Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT.
Window Watchdog	• Clock sources from HCLK/2048 (default selection) or LIRC • Window set by 6-bit down counter with 11-bit prescale • WWDT counter suspends in Idle/Power-down mode • Supports Interrupt
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• Analog input voltage range: 0 ~ AV_{DD}. • Analog input voltage range: 0 ~ AV_{DD} • 12-bit resolution and 10-bit accuracy is guaranteed. • Up to 16 single-end analog input channels or 8 differential analog input channels • Maximum ADC peripheral clock frequency is 48 MHz. • Up to 2 MSPS sampling rate. • Four operation modes: • Single mode: A/D conversion is performed one time on a specified channel. • Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO. • Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the

	smallest numbered channel to the largest numbered channel. • Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion. • An A/D conversion can be started by: • Software Write 1 to ADST bit. • External pin (STADC). • Timer 0~3 overflow pulse trigger. • PWM trigger. • Each conversion result is held in data register of each channel with valid and overrun indicators. • Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting. • 1 internal channels, they are band-gap voltage (VBG). • Supports PDMA transfer mode. • Supports Calibration mode.
Analog Comparator (ACMP)	• Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin) • Up to two rail-to-rail analog comparators • Supports hysteresis function • Supports wake-up function • Selectable input sources of positive input and negative input • **ACMP0 supports:** – 4 multiplexed I/O pins at positive sources: ◆ ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3 – 3 negative sources: ◆ ACMP0_N ◆ Comparator Reference Voltage (CRV) • Internal band-gap voltage (VBG) • **ACMP1 supports** – 4 multiplexed I/O pins at positive sources: ◆ ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3 – 3 negative sources: • **ACMP1_N** – Comparator Reference Voltage (CRV) – Internal band-gap voltage (VBG) • Shares one ACMP interrupt vector for all comparators • Interrupts generated when compare results change (Interrupt event condition is programmable) • Supports triggers for break events and cycle-by-cycle control for PWM

	• Supports window compare mode and window latch mode
Communication Interfaces	
UART	• Supports up to 3 UARTs: UART0, UART1, UART2 • UART baud rate clock from LXT(32.768 KHz) with 9600bps can work normally in power down mode even system clock is stopped (UART0/UART1 support) • Support Single-wire function mode • Full-duplex asynchronous communications • Separates receive and transmit 16/16 bytes entry FIFO for data payloads (UART0/UART1 support) • Supports hardware auto-flow control (RX, TX, CTS and RTS) and programmable receiver buffer trigger level (UART0/UART1 support) • Supports programmable baud rate generator for each channel individually • Supports 8-bit receiver buffer time-out detection function (UART0/UART1 support) • Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8]) (UART0/UART1 support) • Supports Auto-Baud Rate measurement and baud rate compensation function(UART0/UART1 support) • Supports break error, frame error, parity error and receive/transmit buffer overflow detection function • Fully programmable serial-interface characteristics • Programmable number of data bit, 5-, 6-, 7-, 8- bit character • Programmable parity bit, even, odd, no parity or stick parity bit generation and detection • Programmable stop bit, 1, 1.5, or 2 stop bit generation • Supports IrDA SIR function mode (UART0/UART1 support) • Supports for 3/16 bit duration for normal mode • Supports RS-485 mode (UART0/UART1 support) • Supports RS-485 9-bit mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 • Address Match (AAD mode) wake-up function (UART0/UART1 support) • Supports PDMA mode
I^2C	• Up to 2 sets of I^2C devices • Master/Slave mode • Bidirectional data transfer between masters and slaves

	• Multi-master bus (no central master) • 7-bit addressing mode • Standard mode (100 kbps) and Fast mode (400 kbps). • Arbitration between simultaneously transmitting masters without corruption of serial data on the bus • Serial clock synchronization allows devices with different bit rates to communicate via one serial bus • Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer • Supports 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows • Programmable clocks allow versatile rate control • Multiple address recognition (four slave addresses with mask option) • Supports setup/hold time programmable • Multi-address Power-down wake-up function • Supports PDMA transfer
SPI/I^2S	• Supports one SPI/ I^2S controller • Pin defined in SPI and I^2S mode: **SPI** • Supports Master or Slave mode operation • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 4-level of 32-bit (or 8-level of 16-bit) depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports Byte Reorder function • Byte or Word Suspend mode • Master and slave mode up to 24 MHz (when chip works at V_{DD} = 1.8 ~3.6V) • Supports one data channel half-duplex transfer • Support receive-only mode • SPI Supports PDMA transfer **I^2S** • Supports Master or Slave mode operation • Capable of handling 8-, 16-, 24- and 32-bit word sizes in I^2S mode • Provides separate 4-level depth transmit and receive FIFO buffers in I^2S mode • Generates interrupt requests when buffer levels cross a programmable boundary • Supports monaural and stereo audio data in I^2S mode • Supports PCM mode A, PCM mode B, I^2S and MSB justified data format in I^2S mode

	• Supports PDMA transfer
Universal Serial Control Interface (USCI)	• Supports one set of USCI • USCI supports UART, SPI and I^2C function • Single byte TX and RX buffer mode **UART** • One transmit buffer and two receive buffer for data payload • Hardware auto flow control function and programmable flow control trigger level • Programmable baud-rate generator • Support 9-bit Data Transfer • Baud rate detection possible by built-in capture event of baud rate generator • Supports Wake-up function (Data and nCTS Wakeup Only) • Supports PDMA transfer **SPI** • Master or Slave mode operation (maximum frequency: master = fPCLK / 2, slave < fPCLK / 5) • Configurable bit length of a transfer word from 4 to 16-bit • One transmit buffer and two receive buffer for data payload • MSB first or LSB first transfer sequence • Word suspend function • Supports PDMA transfer • Supports 3-wire, no slave select signal, bi-direction interface • Wake-up function: input slave select transition • Supports one data channel half-duplex transfer **I^2C** • Full master and slave device capability • 7-bit addressing mode (Not support 10-bit mode) • Communication in standard mode (100 kbps) or in fast mode (up to 400 kbps) • Multi-master bus • One transmit buffer and two receive buffer for data payload • Supports 10-bit bus time-out capability • Supports Bus monitor mode • Power-down wake-up by data toggle or address match • Multiple address recognition • Device address flag • Setup/hold time programmable
External Bus Interface (EBI)	• Up to two memory banks • Dedicated external chip select pin with polarity control for each

	bank • Two dedicated external chip select pins for each memory block • Accessible space up to 1 M bytes for each bank, actually external addressable space is dependent on package pin out • 8-/16-bit data width • Byte write in 16-bit data width mode • Supports Address/Data multiplexed Mode • Timing parameters individual adjustment for each memory block • Supports LCD interface i80 mode • Supports Continuous Data Access Mode • Supports PDMA mode
GPIO	• Four I/O modes: – Quasi-bidirectional mode – Push-Pull Output mode – Open-Drain Output mode – Input only with high impendence mode • Schmitt trigger input • I/O pin configured as interrupt source with edge/level trigger setting • Supports high drive and high sink current I/O • I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode • Maximum I/O Speed is 24 MHz when V_{DD} = 1.8 ~ 3.6V. • Supports input 5V tolerance, except analog pin (PA.10 ~ 11; PB.0 ~ 15; PF.2 ~ 5; all USB pin and nRESET pin). • Supports up to 15/23/27/42/55 GPIOs for TSSOP20/28, QFN33 and LQFP48/64 respectively • Enabling the pin interrupt function will also enable the wake-up function
Advanced Connectivity	
USB 2.0 Full Speed	• One set of USB 2.0 FS Device (12 Mbps) • On-chip USB Transceiver • Provides 1 interrupt source with 4 interrupt events • Supports Control, Bulk In/Out, Interrupt and Isochronous transfers • Auto suspend function when no bus signaling for 3 ms • Provides 8 programmable endpoints • Includes 512 Bytes internal SRAM as USB buffer • Provides remote wake-up capability • Supports Crystal-less function

• Start of Frame (SOF) locked clock pulse generation

3 PARTS INFORMATION

3.1 Summary

Part No.	USB FS
M031	–
M032	√

3.2 Package Type

Part No.	TSSOP20	TSSOP28	QFN33	LQFP48	LQFP64
M031 Control Series	M031FB0AE M031FC1AE	M031EB0AE M031EC1AE	M031TB0AE M031TC1AE M031TD2AE	M031LC2AE M031LD2AE M031LE3AE	M031SC2AE M031SD2AE M031SE3AE
M032 USB Series	-	-	-	M032LE3AE	M032SE3AE

3.3 M031/M032 Series Selection Guide

3.3.1 M031 Control Series

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer	PWM	PDMA	Connectivity				EBI	PLL	LXT	ACMP	ADC (12-bit)	Package
								USCI*	UART	SPI / I^2S	I^2C						
M031FB0AE	16	2	2	15	2	6	-	-	3	1	2	-	-	-	-	7-ch	TSSOP20
M031EB0AE	16	2	2	23	2	6	-	-	3	1	2	-	-	-	-	9-ch	TSSOP28
M031TB0AE	16	2	2	27	2	6	-	-	3	1	2	-	-	-	-	10-ch	QFN33
M031FC1AE	32	4	2	15	4	6	2	-	3	1	2	-	-	-	-	7-ch	TSSOP20
M031EC1AE	32	4	2	23	4	6	2	-	3	1	2	-	-	-	-	9-ch	TSSOP28
M031TC1AE	32	4	2	27	4	6	2	-	3	1	2	-	-	√	-	10-ch	QFN33
M031LC2AE	32	8	2	42	4	12	5	1	3	1	2	-	√	√	2	12-ch	LQFP48
M031SC2AE	32	8	2	55	4	12	5	1	3	1	2	-	√	√	2	16-ch	LQFP64
M031TD2AE	64	8	2	27	4	12	5	1	3	1	2	-	√	√	2	10-ch	QFN33
M031LD2AE	64	8	2	42	4	12	5	1	3	1	2	-	√	√	2	12-ch	LQFP48
M031SD2AE	64	8	2	55	4	12	5	1	3	1	2	-	√	√	2	16-ch	LQFP64
M031LE3AE	128	16	4	42	4	12	5	1	3	1	2	√	√	√	2	12-ch	LQFP48
M031SE3AE	128	16	4	55	4	12	5	1	3	1	2	√	√	√	2	16-ch	LQFP64

USCI*: supports UART, SPI or I^2C

3.3.2 M032 USB Series

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer	PWM	PDMA	Connectivity					EBI	PLL	ACMP	ADC (12-bit)	Package
								USBD	USCI*	UART	SPI / I^2S	I^2C					
M032LE3AE	128	16	4	42	4	12	5	1	1	3	1	2	√	√	2	12-ch	LQFP48
M032SE3AE	128	16	4	55	4	12	5	1	1	3	1	2	√	√	2	16-ch	LQFP64

USCI*: supports UART, SPI or I^2C

3.3.3 M031/M032 Selection Code

M03	1	S	E	3	A	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserved**	**Temperature**
Cortex®-M0	**1:** Control Line **2:** USB Line	**F:** TSSOP20 (4.4x6.5 mm) **E:** TSSOP28 (4.4x9.7 mm) **T:** QFN33 (4x4 mm) **L:** LQFP48 (7x7 mm) **S:** LQFP64 (7x7 mm)	**B:** 16 KB **C:** 32 KB **D:** 64 KB **E:** 128 KB	**0:** 2 KB **1:** 4 KB **2:** 8/12 KB **3:** 16 KB		**E:** -40°C~105°C

Table 3.3-1 M031/M032 Series Selection Code

4 PIN CONFIGURATION

Users can find pin configuration information in chapter 4 or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 M031 Series Pin Diagram

4.1.1.1 TSSOP20 Package

Corresponding Part Number: M031FB0AE, M031FC1AE

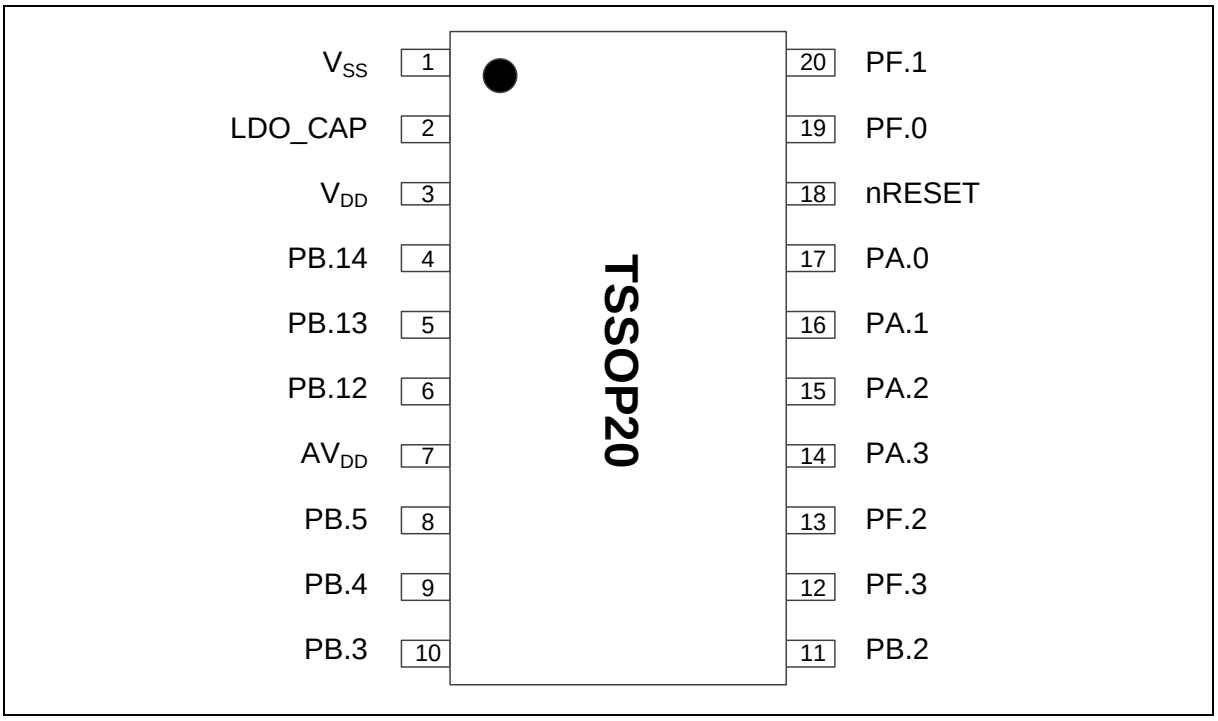


Figure 4.1-1 M031 Series TSSOP 20-pin Diagram

4.1.1.2 TSSOP28 Package

Corresponding Part Number: M031EB0AE, M031EC1AE

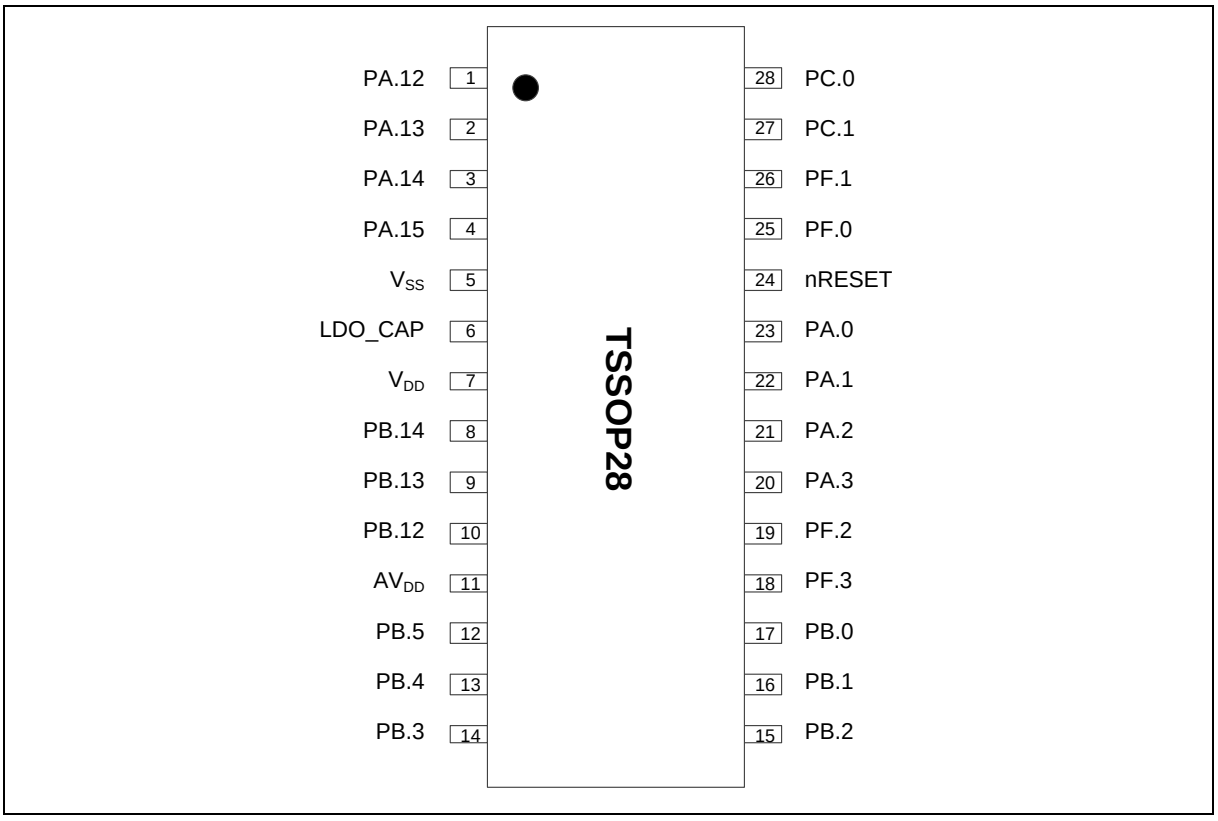


Figure 4.1-2 M031 Series TSSOP 28-pin Diagram

4.1.1.3 QFN33 Package

Corresponding Part Number: M031TB0AE, M031TC1AE, M031TD2AE

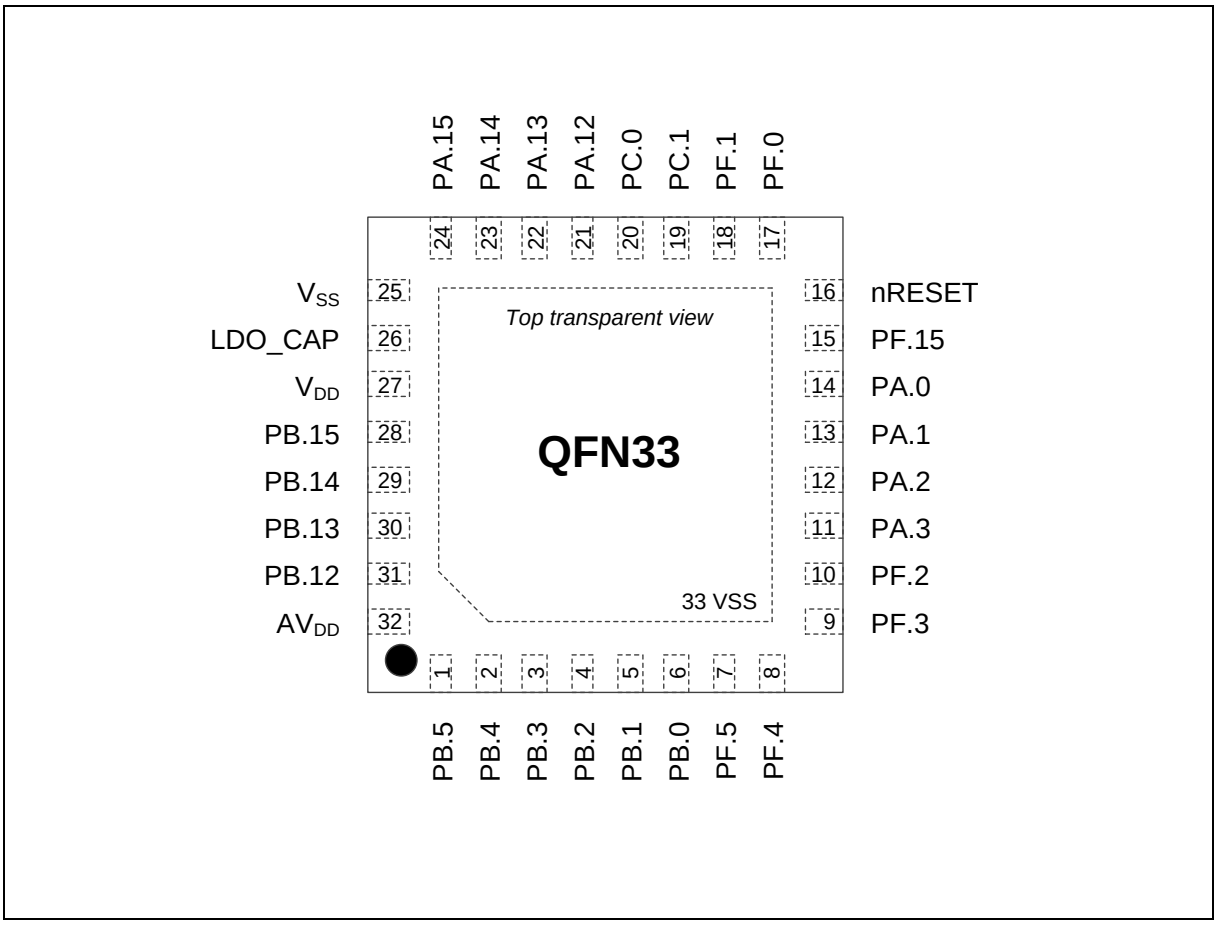


Figure 4.1-3 M031 Series QFN 33-pin Diagram

4.1.1.4 LQFP48 Package

Corresponding Part Number: M031LC2AE, M031LD2AE, M031LE3AE

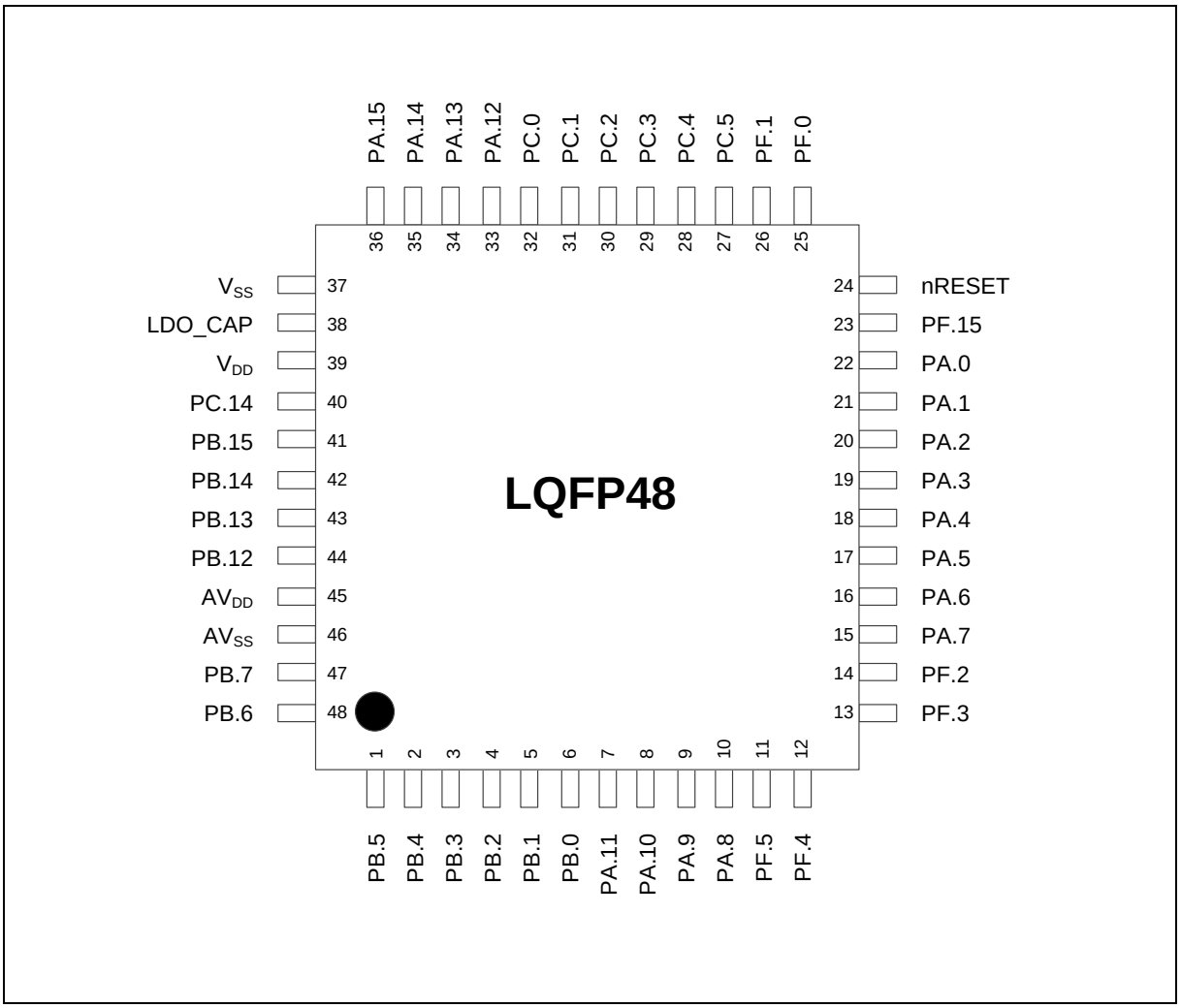


Figure 4.1-4 M031 Series LQFP 48-pin Diagram

4.1.1.5 LQFP64 Package

Corresponding Part Number: M031SC2AE, M031SD2AE, M031SE3AE

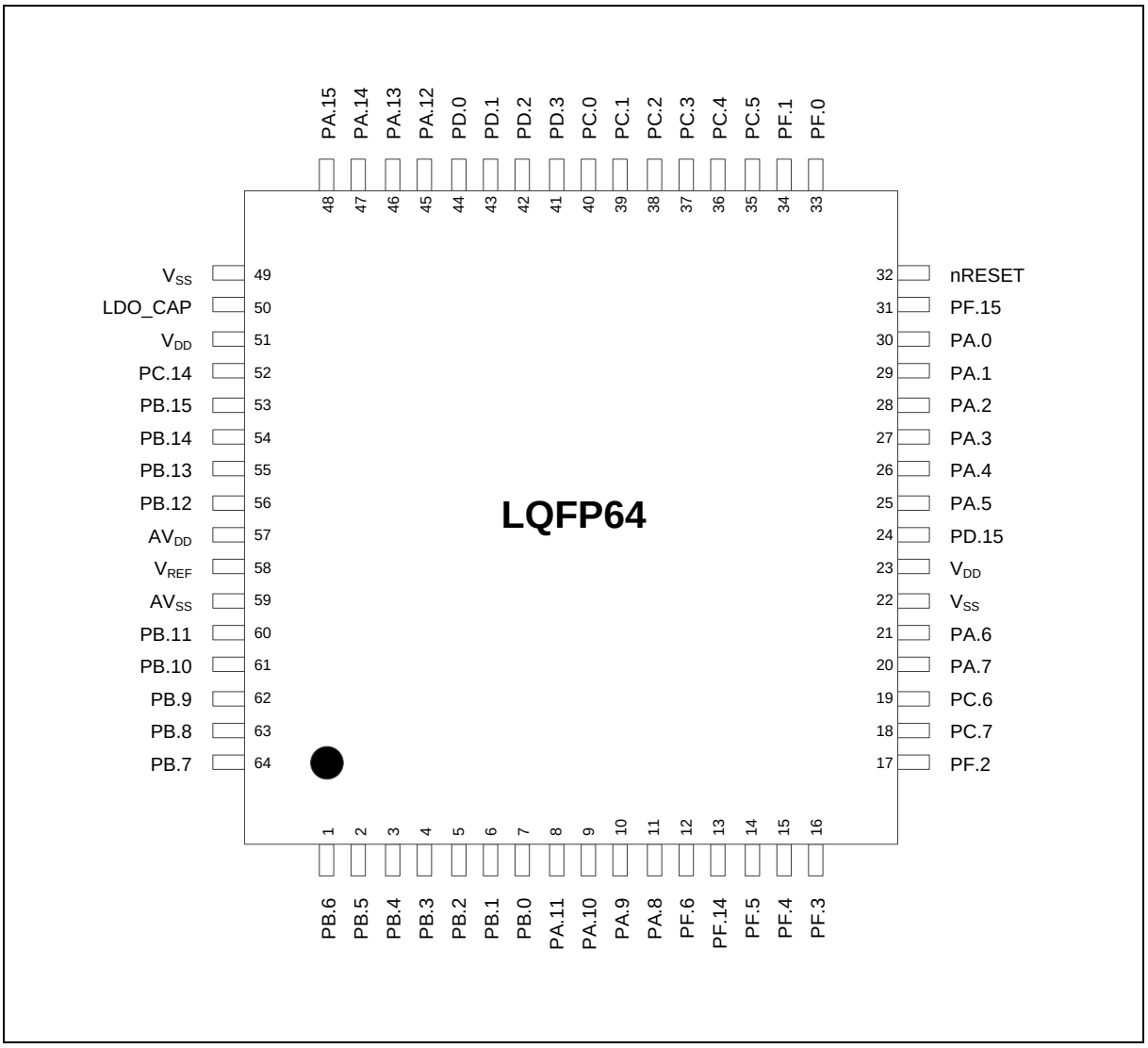


Figure 4.1-5 M031 Series LQFP 64-pin Diagram

4.1.2 M031 Series Function Pin Diagram

4.1.2.1 TSSOP20 Package

Corresponding Part Number: M031FB0AE, M031FC1AE

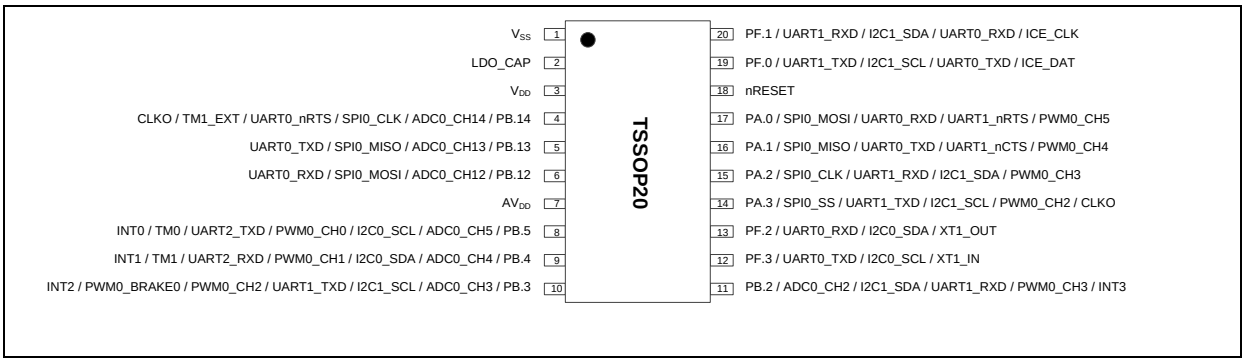


Figure 4.1-6 M031FB0AE Function Pin Diagram

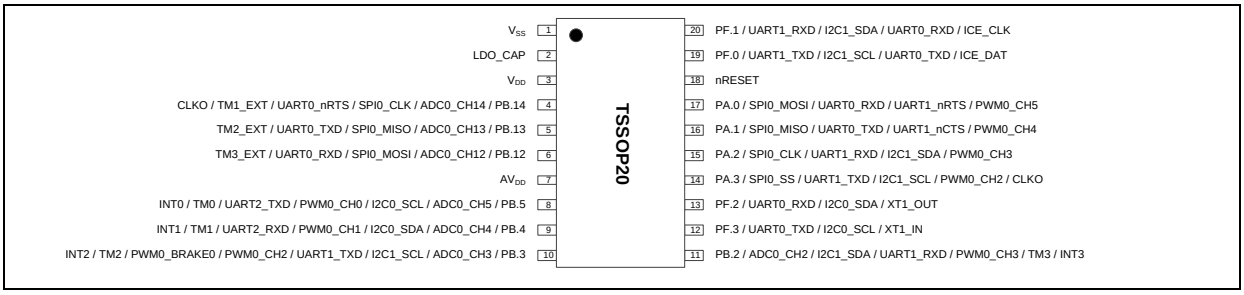


Figure 4.1-7 M031FC1AE Function Pin Diagram

4.1.2.2 TSSOP28 Package

Corresponding Part Number: M031EB0AE, M031EC1AE

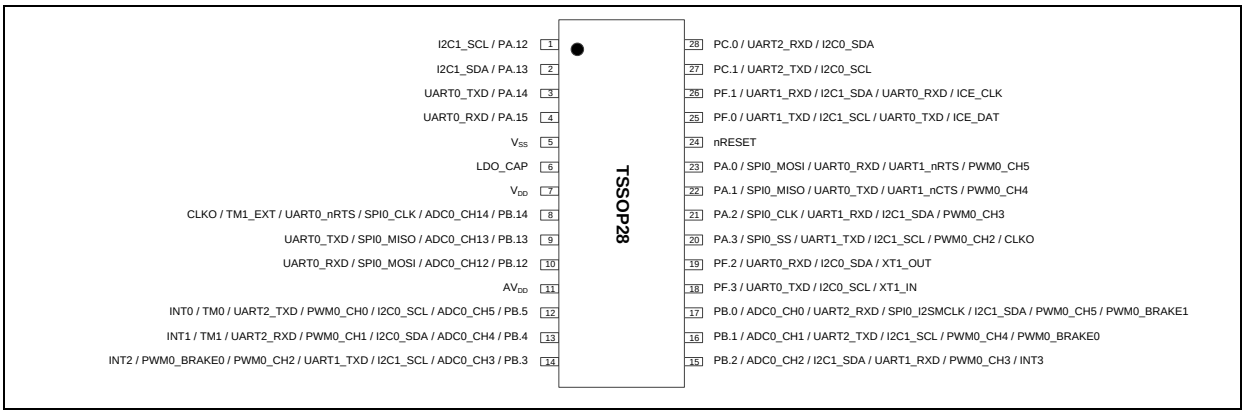


Figure 4.1-8 M031EB0AE Function Pin Diagram

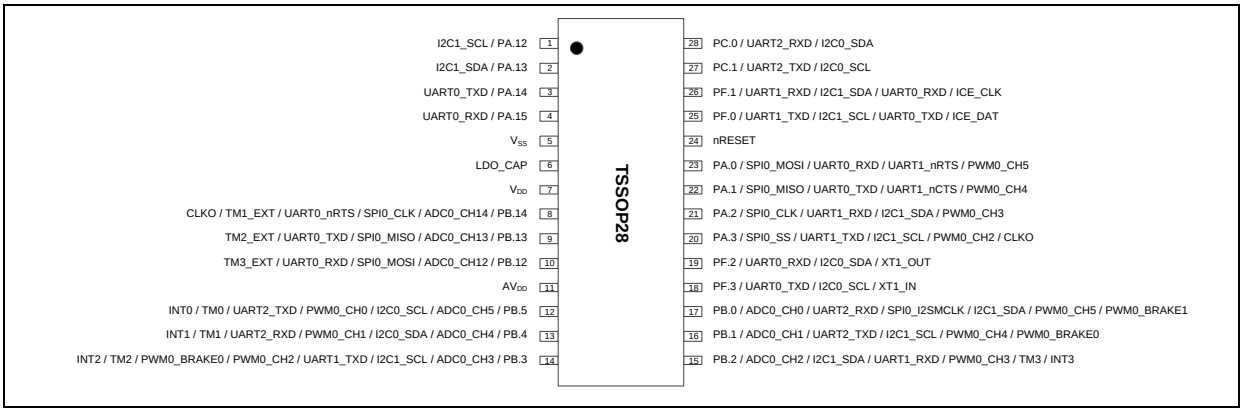


Figure 4.1-9 M031EC1AE Function Pin Diagram

4.1.2.3 QFN33 Package

Corresponding Part Number: M031TB0AE, M031TC1AE, M031TD2AE

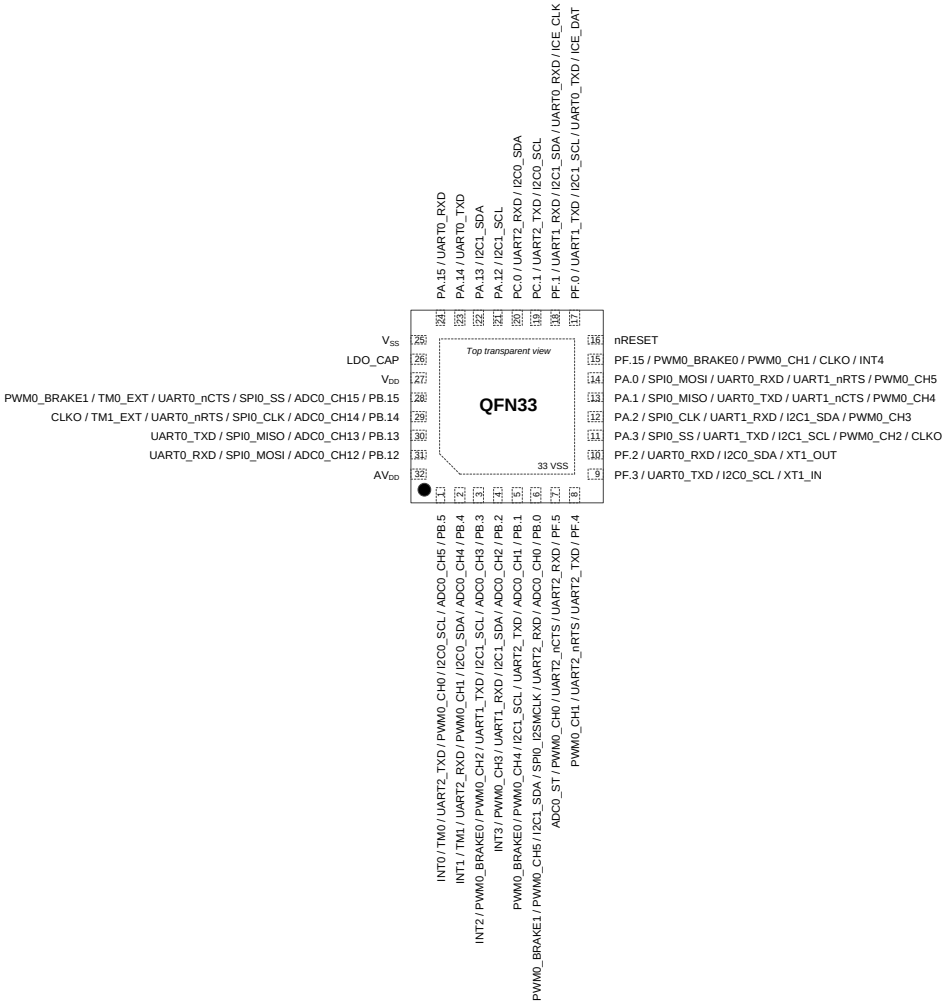


Figure 4.1-10 M031TB0AE Function Pin Diagram

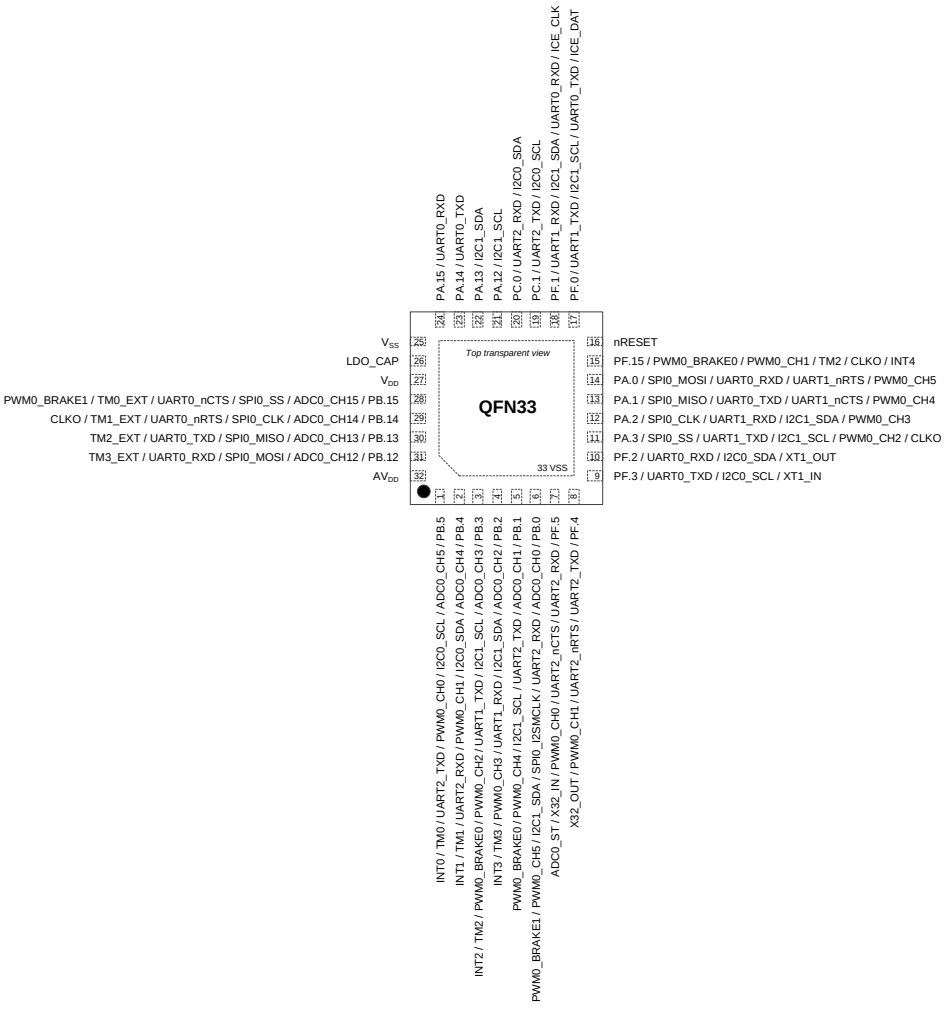


Figure 4.1-11 M031TC1AE Function Pin Diagram

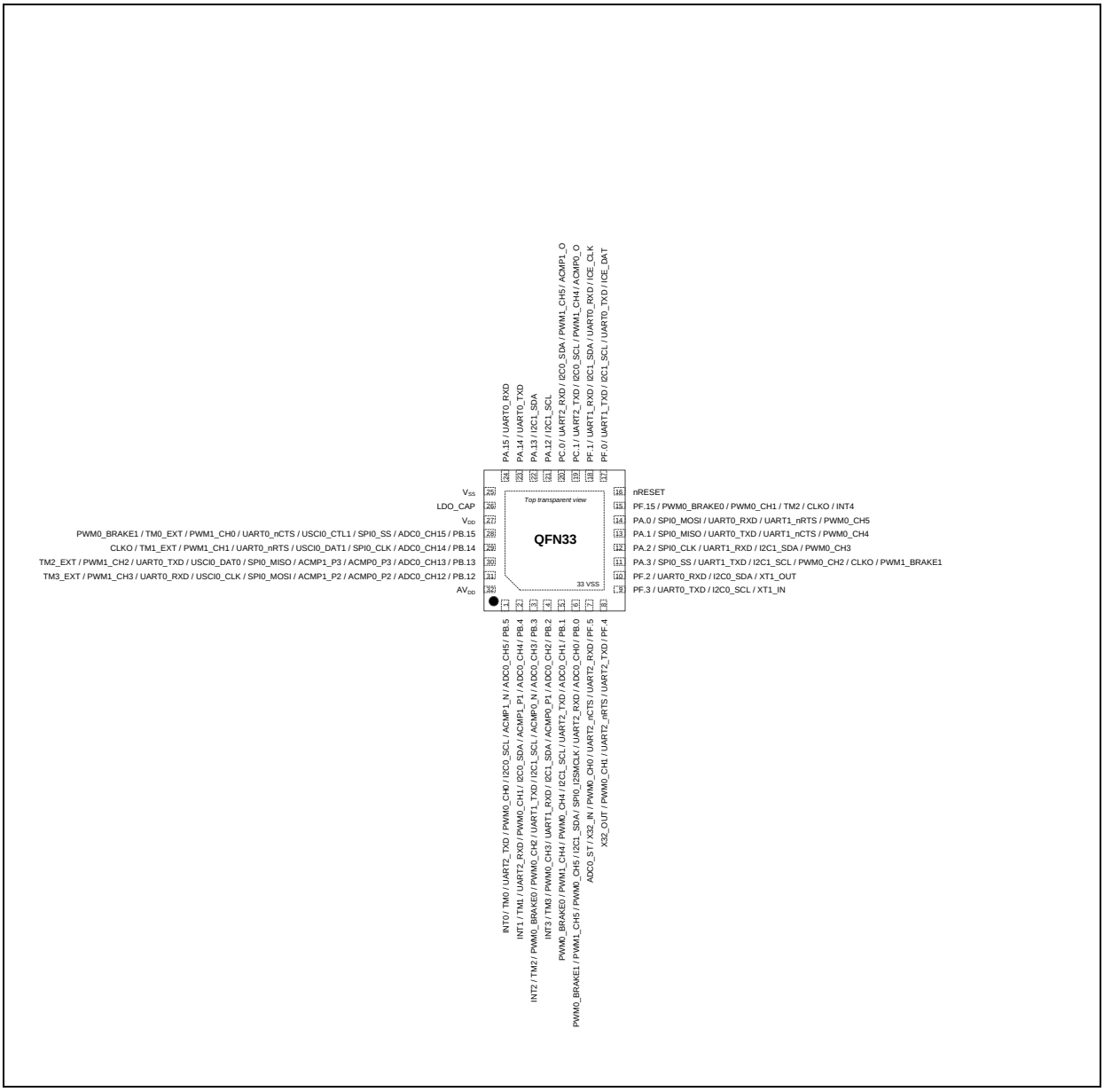


Figure 4.1-12 M031TD2AE Function Pin Diagram

4.1.2.4 LQFP48 Package

Corresponding Part Number: M031LC2AE, M031LD2AE, M031LE3AE

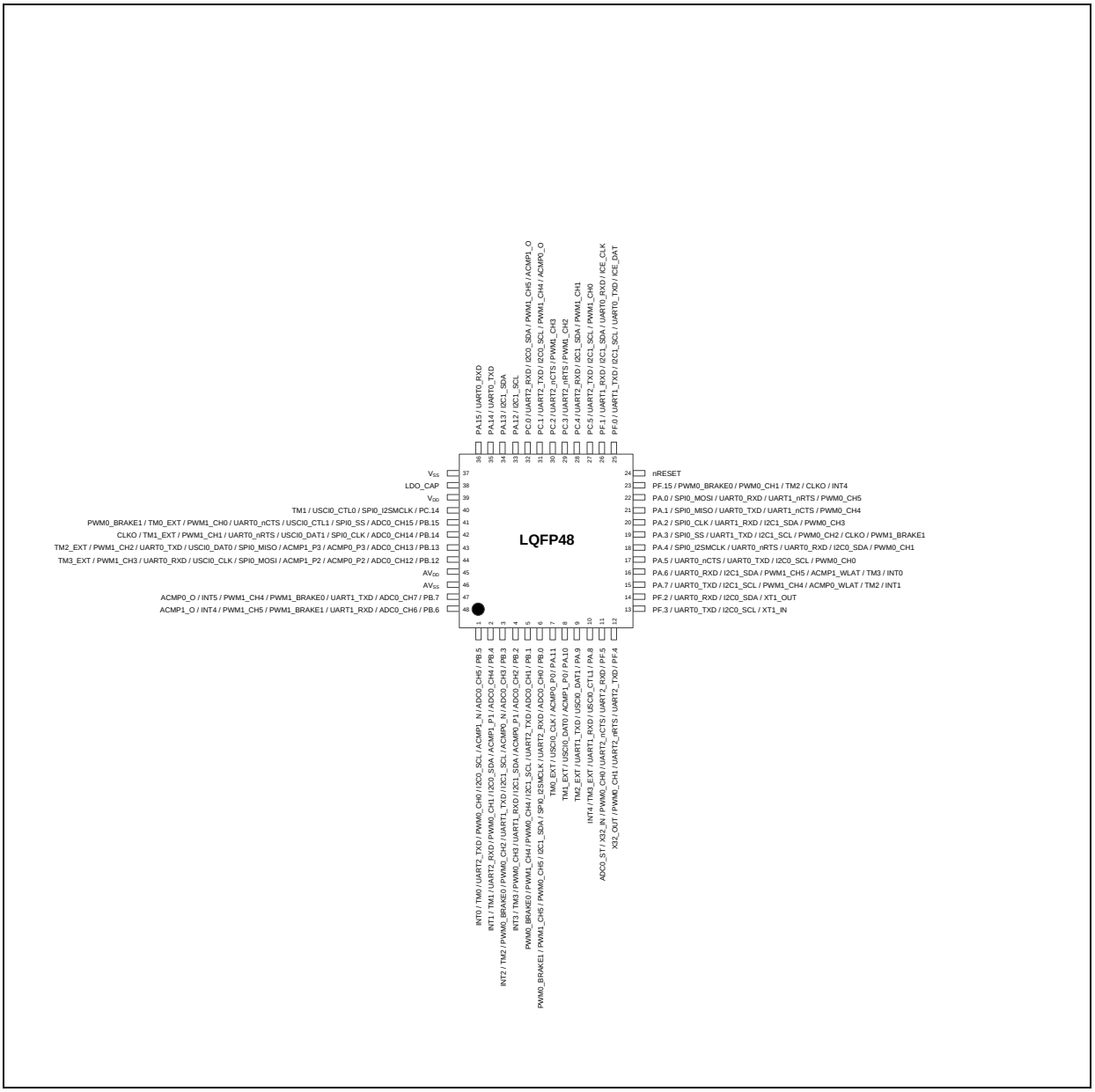


Figure 4.1-13 M031LC2AE Function Pin Diagram

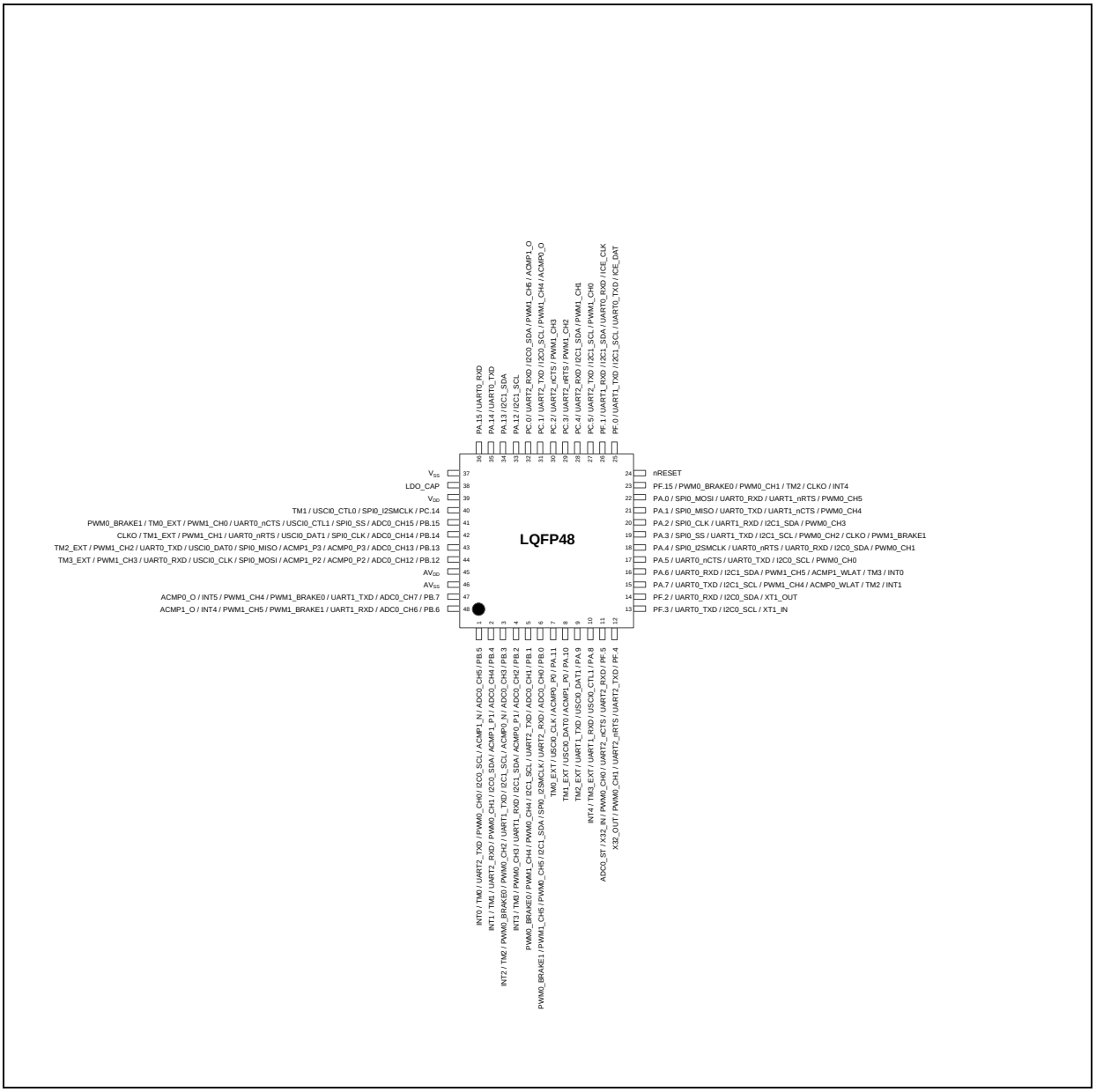


Figure 4.1-14 M031LD2AE Function Pin Diagram

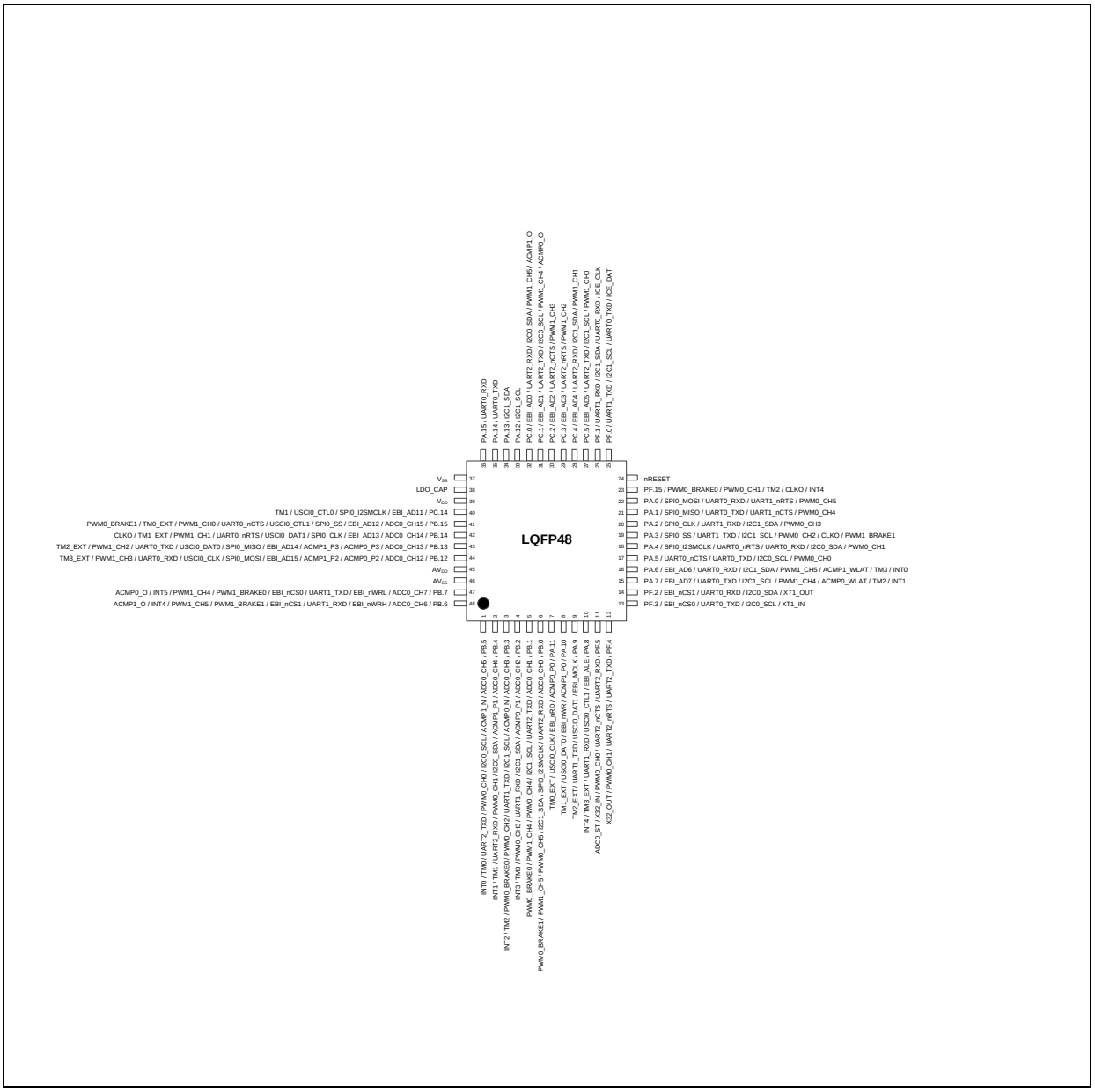


Figure 4.1-15 M031LE3AE Function Pin Diagram

4.1.2.5 LQFP64 Package

Corresponding Part Number: M031SC2AE, M031SD2AE, M031SE3AE

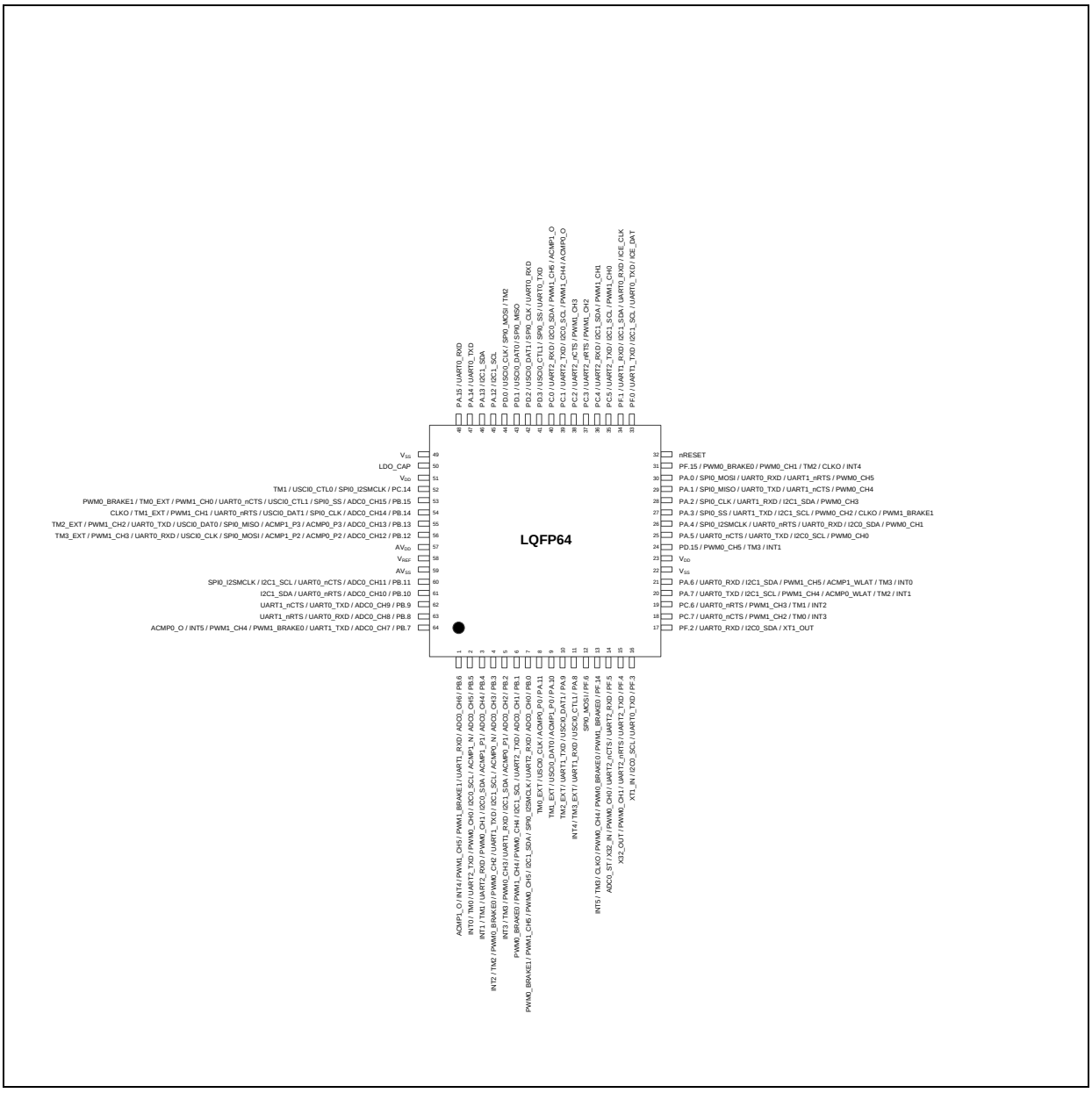


Figure 4.1-16 M031SC2AE Funcion pin Diagram

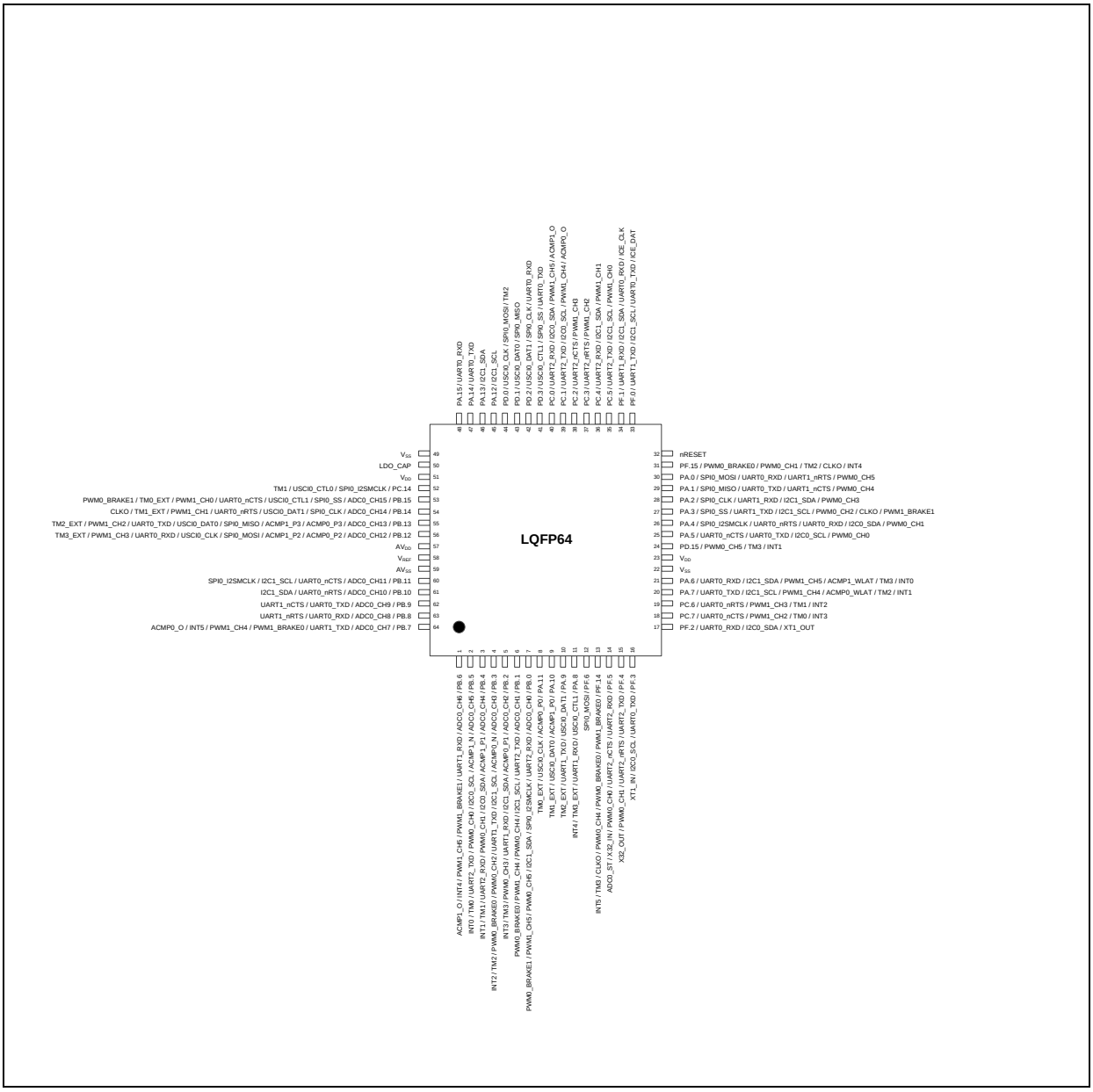


Figure 4.1-17 M031SD2AE Funcion pin Diagram

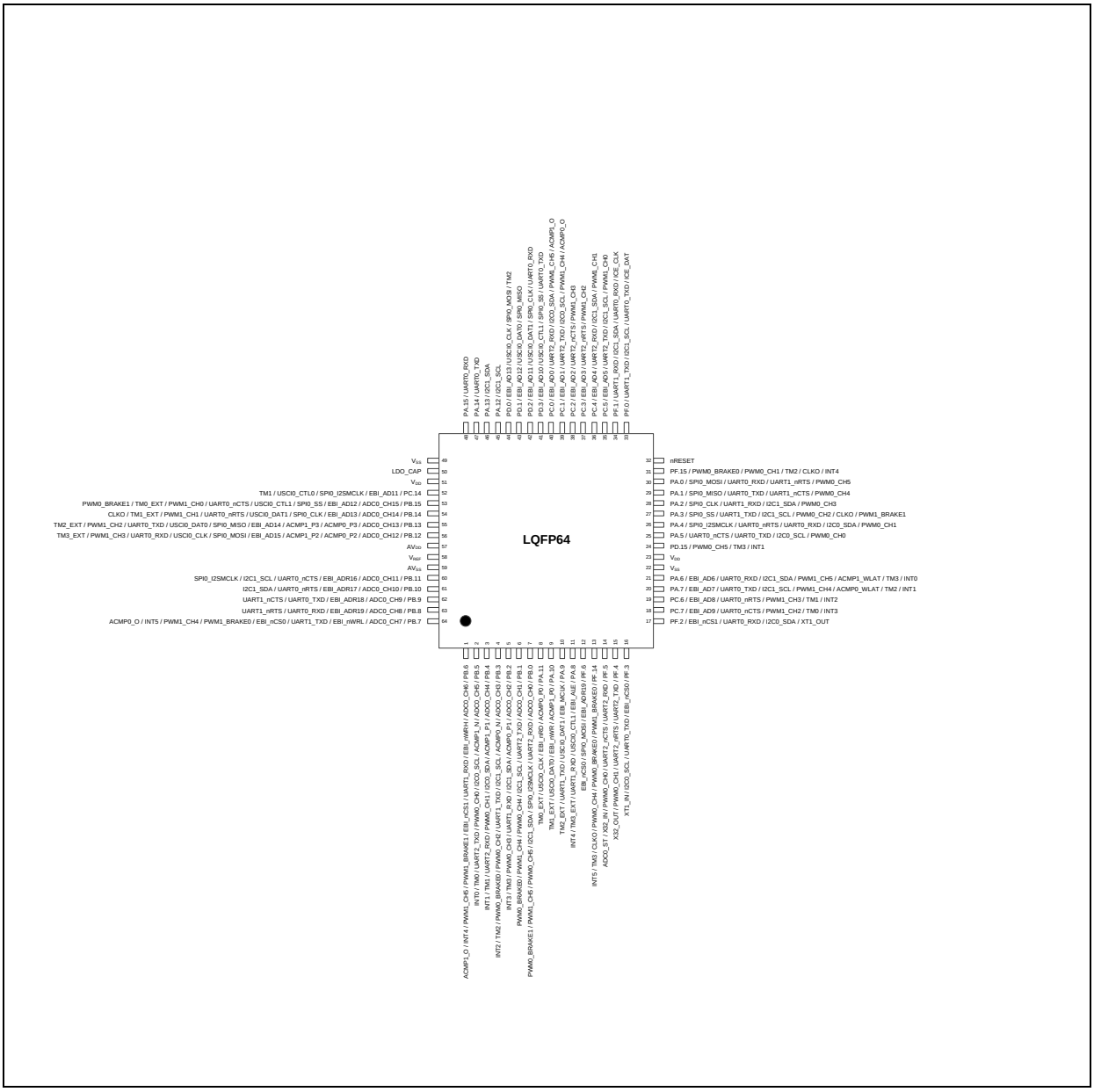


Figure 4.1-18 M031SE3AE Function Pin Diagram

4.1.3 M032 Series Pin Diagram

4.1.3.1 LQFP48 Package

Corresponding Part Number: M032LE3AE

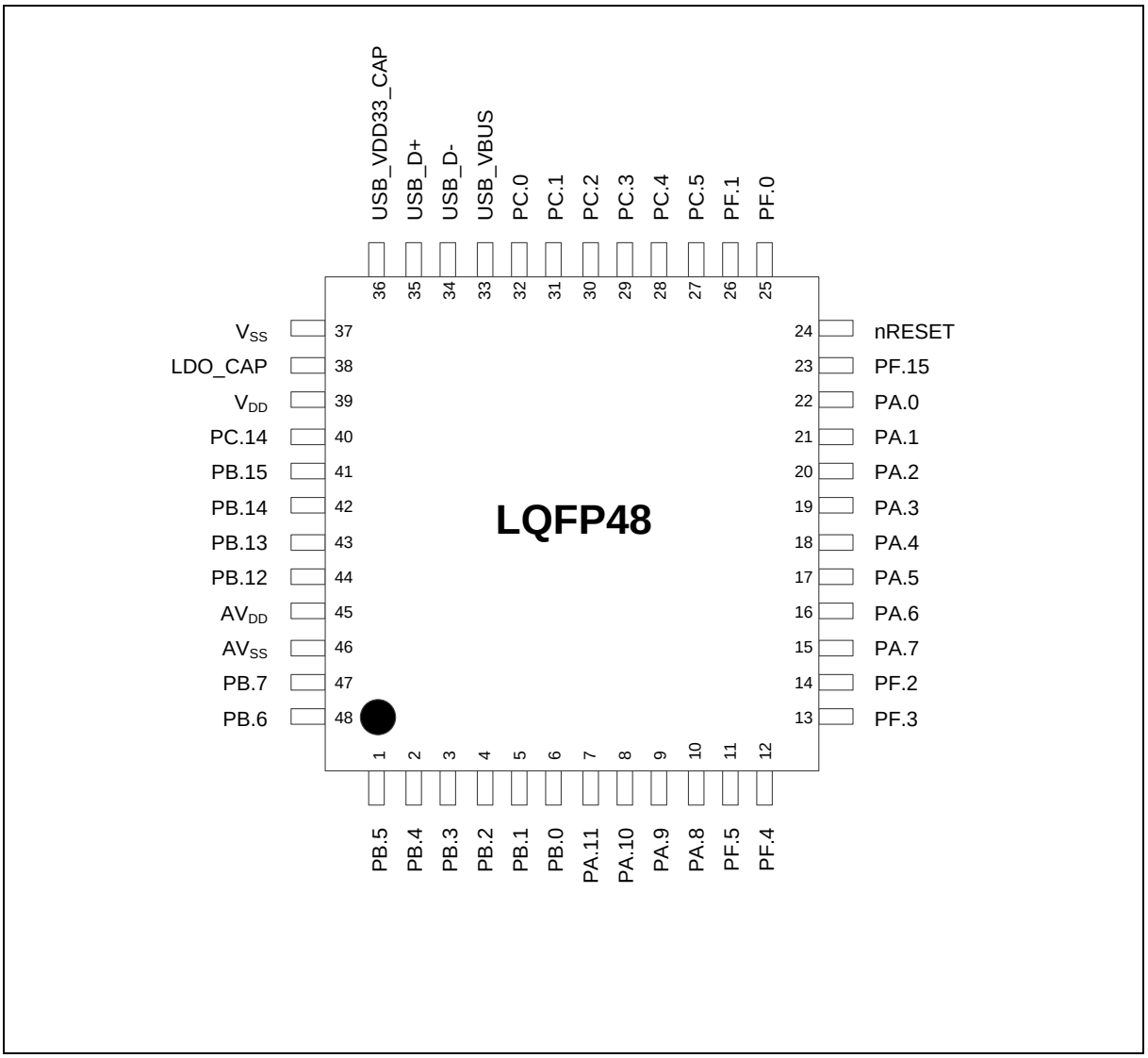


Figure 4.1-19 M032 Series LQFP 48-pin Diagram

4.1.3.2 LQFP64 Package

Corresponding Part Number: M032SE3AE

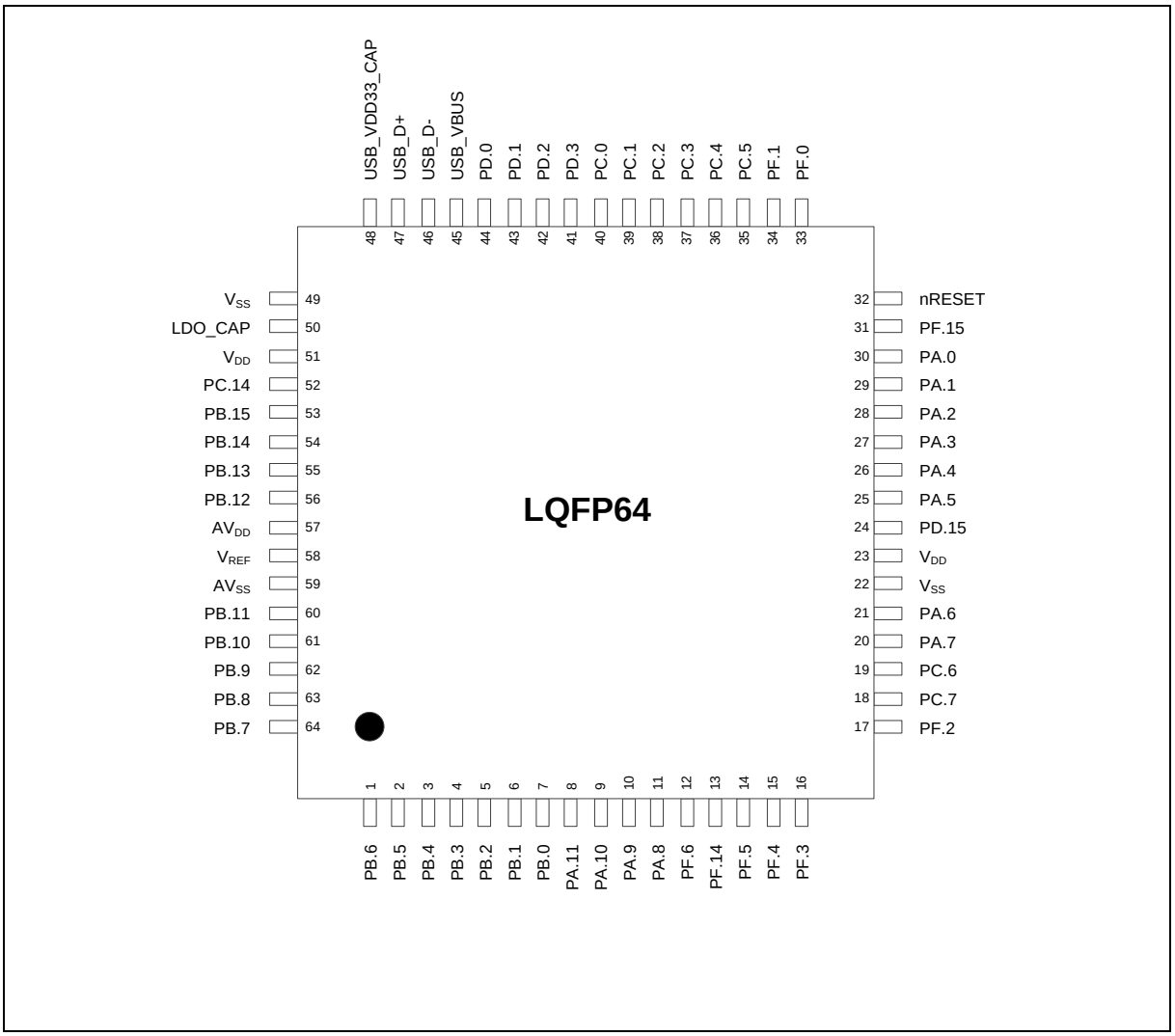


Figure 4.1-20 M032 Series LQFP 64-pin Diagram

4.1.4 M032 Series Function Pin Diagram

4.1.4.1 LQFP48 Package

Corresponding Part Number: M032LE3AE

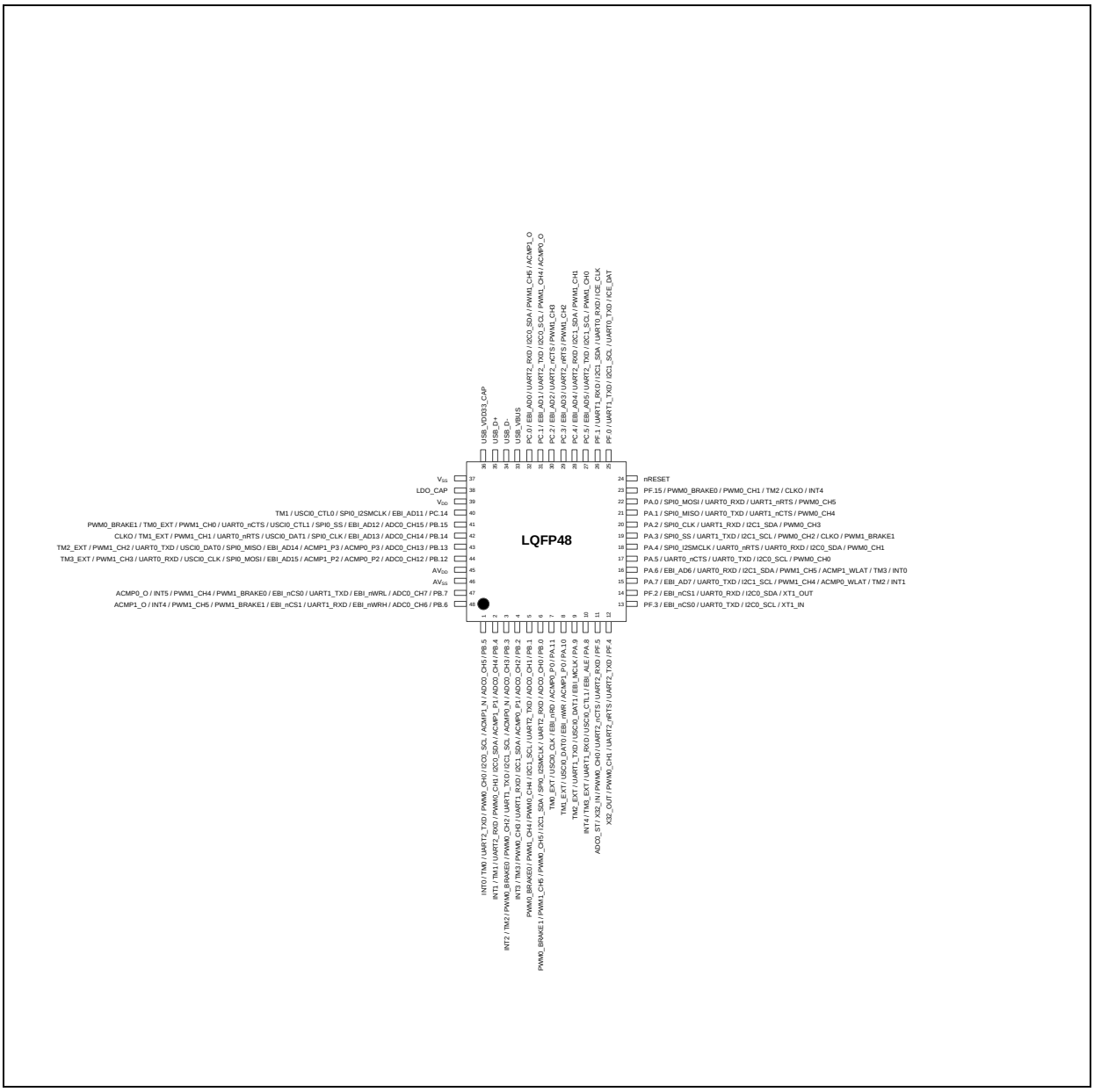


Figure 4.1-21 M032LE3AE Function Pin Diagram

4.1.4.2 LQFP64 Package

Corresponding Part Number: M032SE3AE

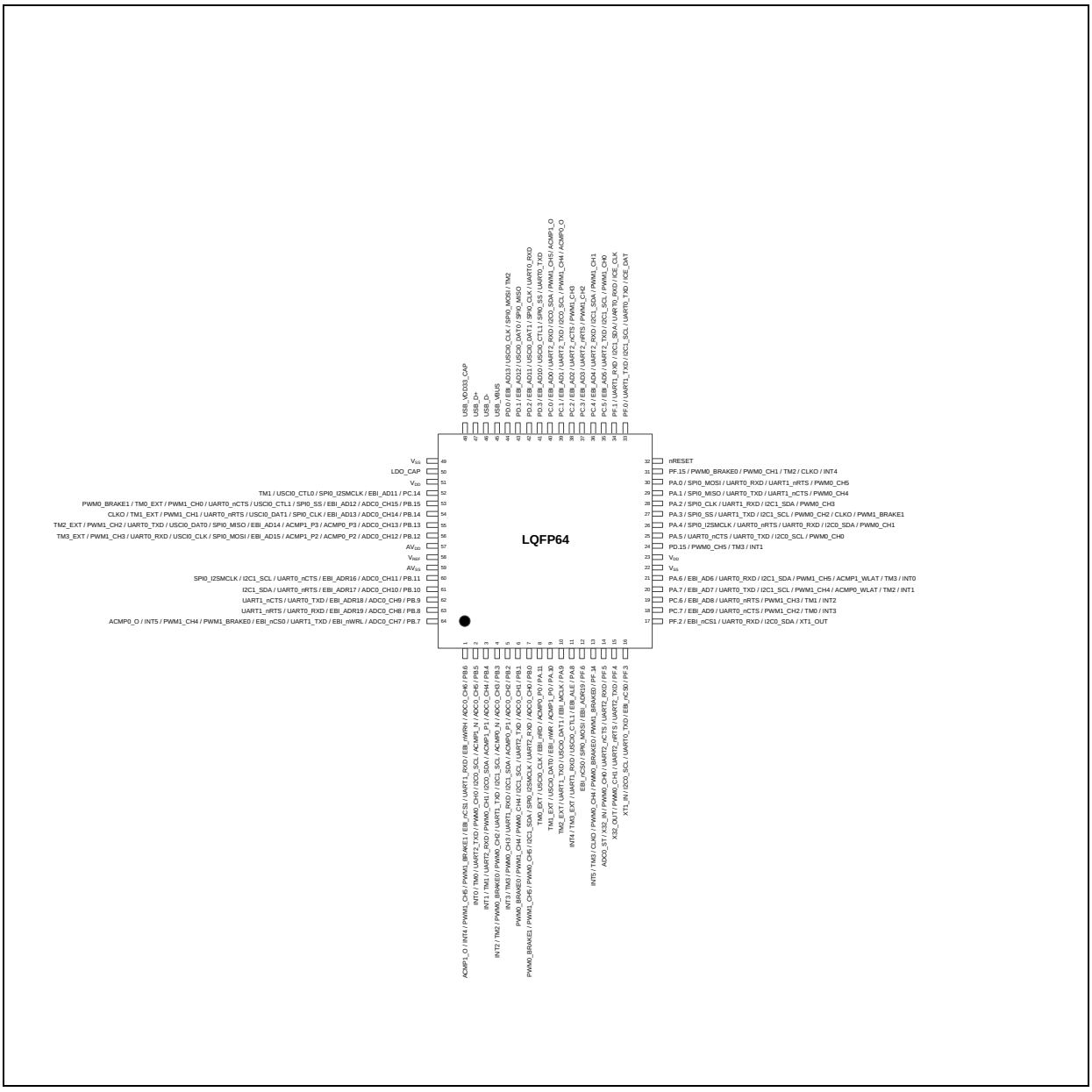


Figure 4.1-22 M032SE3AE Funcion Pin Diagram

4.2 Pin Description

Different part number with the same package might have a different function. Please refer to the selection guide in section 3.3.

4.2.1 M031/M032 Series Pin Description

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
							PB.6	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH6	A	MFP1	ADC0 channel 6 analog input.
							EBI_nWRH	O	MFP2	EBI high byte write enable output pin
							UART1_RXD	I	MFP6	UART1 data receiver input pin.
			48	48	1	1	EBI_nCS1	O	MFP8	EBI chip select 1 output pin.
							PWM1_BRAKE1	I	MFP11	PWM1 Brake 1 input pin.
							PWM1_CH5	I/O	MFP12	PWM1 channel 5 output/capture input.
							INT4	I	MFP13	External interrupt 4 input pin.
							ACMP1_O	O	MFP15	Analog comparator 1 output pin.
							PB.5	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH5	A	MFP1	ADC0 channel 5 analog input.
							ACMP1_N	A	MFP1	Analog comparator 1 negative input pin.
8	12	1	1	1	2	2	I2C0_SCL	I/O	MFP6	I2C0 clock pin.
							PWM0_CH0	I/O	MFP11	PWM0 channel 0 output/capture input.
							UART2_TXD	O	MFP13	UART2 data transmitter output pin.
							TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
							INT0	I	MFP15	External interrupt 0 input pin.
							PB.4	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
							ACMP1_P1	A	MFP1	Analog comparator 1 positive input 1 pin.
9	13	2	2	2	3	3	I2C0_SDA	I/O	MFP6	I2C0 data input/output pin.
							PWM0_CH1	I/O	MFP11	PWM0 channel 1 output/capture input.
							UART2_RXD	I	MFP13	UART2 data receiver input pin.
							TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
							INT1	I	MFP15	External interrupt 1 input pin.
10	14	3	3	3	4	4	PB.3	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
							ACMP0_N	A	MFP1	Analog comparator 0 negative input pin.
							I2C1_SCL	I/O	MFP4	I2C1 clock pin.
							UART1_TXD	O	MFP6	UART1 data transmitter output pin.
							PWM0_CH2	I/O	MFP11	PWM0 channel 2 output/capture input.
							PWM0_BRAKE0	I	MFP13	PWM0 Brake 0 input pin.
							TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
							INT2	I	MFP15	External interrupt 2 input pin.
11	15	4	4	4	5	5	PB.2	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
							ACMP0_P1	A	MFP1	Analog comparator 0 positive input 1 pin.
							I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
							UART1_RXD	I	MFP6	UART1 data receiver input pin.
							PWM0_CH3	I/O	MFP11	PWM0 channel 3 output/capture input.
							TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
							INT3	I	MFP15	External interrupt 3 input pin.
	16	5	5	5	6	6	PB.1	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
							UART2_TXD	O	MFP7	UART2 data transmitter output pin.
							I2C1_SCL	I/O	MFP9	I2C1 clock pin.
							PWM0_CH4	I/O	MFP11	PWM0 channel 4 output/capture input.
							PWM1_CH4	I/O	MFP12	PWM1 channel 4 output/capture input.
							PWM0_BRAKE0	I	MFP13	PWM0 Brake 0 input pin.
	17	6	6	6	7	7	PB.0	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH0	A	MFP1	ADC0 channel 0 analog input.
							UART2_RXD	I	MFP7	UART2 data receiver input pin.
							SPI0_I2SMCLK	I/O	MFP8	SPI0 I^2S master clock output pin
							I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
							PWM0_CH5	I/O	MFP11	PWM0 channel 5 output/capture input.
							PWM1_CH5	I/O	MFP12	PWM1 channel 5 output/capture input.
							PWM0_BRAKE1	I	MFP13	PWM0 Brake 1 input pin.
			7	7	8	8	PA.11	I/O	MFP0	General purpose digital I/O pin.
							ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
							EBI_nRD	O	MFP2	EBI read enable output pin.
							USCI0_CLK	I/O	MFP6	USCI0 clock pin.
							TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
			8	8	9	9	PA.10	I/O	MFP0	General purpose digital I/O pin.
							ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
							EBI_nWR	O	MFP2	EBI write enable output pin.
							USCI0_DAT0	I/O	MFP6	USCI0 data 0 pin.
							TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
			9	9	10	10	PA.9	I/O	MFP0	General purpose digital I/O pin.
							EBI_MCLK	O	MFP2	EBI external clock output pin.
							USCI0_DAT1	I/O	MFP6	USCI0 data 1 pin.
							UART1_TXD	O	MFP7	UART1 data transmitter output pin.
							TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
			10	10	11	11	PA.8	I/O	MFP0	General purpose digital I/O pin.
							EBI_ALE	O	MFP2	EBI address latch enable output pin.
							USCI0_CTL1	I/O	MFP6	USCI0 control 1 pin.
							UART1_RXD	I	MFP7	UART1 data receiver input pin.
							TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
							INT4	I	MFP15	External interrupt 4 input pin.
					12	12	PF.6	I/O	MFP0	General purpose digital I/O pin.
							EBI_ADR19	O	MFP2	EBI address bus bit 19.
							SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
							EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
					13	13	PF.14	I/O	MFP0	General purpose digital I/O pin.
							PWM1_BRAKE0	I	MFP9	PWM1 Brake 0 input pin.
							PWM0_BRAKE0	I	MFP10	PWM0 Brake 0 input pin.
							PWM0_CH4	I/O	MFP12	PWM0 channel 4 output/capture input.
							CLKO	O	MFP13	Clock Out
							TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
							INT5	I	MFP15	External interrupt 5 input pin.
		7	11	11	14	14	PF.5	I/O	MFP0	General purpose digital I/O pin.
							UART2_RXD	I	MFP2	UART2 data receiver input pin.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
							UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
							PWM0_CH0	I/O	MFP7	PWM0 channel 0 output/capture input.
							X32_IN	I	MFP10	External 32.768 kHz crystal input pin.
							ADC0_ST	I	MFP11	ADC0 external trigger input.
		8	12	12	15	15	PF.4	I/O	MFP0	General purpose digital I/O pin.
							UART2_TXD	O	MFP2	UART2 data transmitter output pin.
							UART2_nRTS	O	MFP4	UART2 request to Send output pin.
							PWM0_CH1	I/O	MFP7	PWM0 channel 1 output/capture input.
							X32_OUT	O	MFP10	External 32.768 kHz crystal output pin.
12	18	9	13	13	16	16	PF.3	I/O	MFP0	General purpose digital I/O pin.
							EBI_nCS0	O	MFP2	EBI chip select 0 output pin.
							UART0_TXD	O	MFP3	UART0 data transmitter output pin.
							I2C0_SCL	I/O	MFP4	I2C0 clock pin.
							XT1_IN	I	MFP10	External 4~32 MHz (high speed) crystal input pin.
13	19	10	14	14	17	17	PF.2	I/O	MFP0	General purpose digital I/O pin.
							EBI_nCS1	O	MFP2	EBI chip select 1 output pin.
							UART0_RXD	I	MFP3	UART0 data receiver input pin.
							I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
							XT1_OUT	O	MFP10	External 4~32 MHz (high speed) crystal output pin.
					18	18	PC.7	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD9	I/O	MFP2	EBI address/data bus bit 9.
							UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
							PWM1_CH2	I/O	MFP11	PWM1 channel 2 output/capture input.
							TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
							INT3	I	MFP15	External interrupt 3 input pin.
					19	19	PC.6	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD8	I/O	MFP2	EBI address/data bus bit 8.
							UART0_nRTS	O	MFP7	UART0 request to Send output pin.
							PWM1_CH3	I/O	MFP11	PWM1 channel 3 output/capture input.
							TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
							INT2	I	MFP15	External interrupt 2 input pin.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
			15	15	20	20	PA.7	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD7	I/O	MFP2	EBI address/data bus bit 7.
							UART0_TXD	O	MFP7	UART0 data transmitter output pin.
							I2C1_SCL	I/O	MFP8	I2C1 clock pin.
							PWM1_CH4	I/O	MFP11	PWM1 channel 4 output/capture input.
							ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
							TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
							INT1	I	MFP15	External interrupt 1 input pin.
			16	16	21	21	PA.6	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD6	I/O	MFP2	EBI address/data bus bit 6.
							UART0_RXD	I	MFP7	UART0 data receiver input pin.
							I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
							PWM1_CH5	I/O	MFP11	PWM1 channel 5 output/capture input.
							ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
							TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
							INT0	I	MFP15	External interrupt 0 input pin.
					22	22	V_{SS}	P	MFP0	Ground pin for digital circuit.
					23	23	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
					24	24	PD.15	I/O	MFP0	General purpose digital I/O pin.
							PWM0_CH5	I/O	MFP12	PWM0 channel 5 output/capture input.
							TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
							INT1	I	MFP15	External interrupt 1 input pin.
			17	17	25	25	PA.5	I/O	MFP0	General purpose digital I/O pin.
							UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
							UART0_TXD	O	MFP8	UART0 data transmitter output pin.
							I2C0_SCL	I/O	MFP9	I2C0 clock pin.
							PWM0_CH0	I/O	MFP13	PWM0 channel 0 output/capture input.
			18	18	26	26	PA.4	I/O	MFP0	General purpose digital I/O pin.
							SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
							UART0_nRTS	O	MFP7	UART0 request to Send output pin.
							UART0_RXD	I	MFP8	UART0 data receiver input pin.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
							I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
							PWM0_CH1	I/O	MFP13	PWM0 channel 1 output/capture input.
14	20	11	19	19	27	27	PA.3	I/O	MFP0	General purpose digital I/O pin.
							SPI0_SS	I/O	MFP4	SPI0 slave select pin.
							UART1_TXD	O	MFP8	UART1 data transmitter output pin.
							I2C1_SCL	I/O	MFP9	I2C1 clock pin.
							PWM0_CH2	I/O	MFP13	PWM0 channel 2 output/capture input.
							CLKO	O	MFP14	Clock Out
							PWM1_BRAKE1	I	MFP15	PWM1 Brake 1 input pin.
15	21	12	20	20	28	28	PA.2	I/O	MFP0	General purpose digital I/O pin.
							SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
							UART1_RXD	I	MFP8	UART1 data receiver input pin.
							I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
							PWM0_CH3	I/O	MFP13	PWM0 channel 3 output/capture input.
16	22	13	21	21	29	29	PA.1	I/O	MFP0	General purpose digital I/O pin.
							SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
							UART0_TXD	O	MFP7	UART0 data transmitter output pin.
							UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
							PWM0_CH4	I/O	MFP13	PWM0 channel 4 output/capture input.
17	23	14	22	22	30	30	PA.0	I/O	MFP0	General purpose digital I/O pin.
							SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
							UART0_RXD	I	MFP7	UART0 data receiver input pin.
							UART1_nRTS	O	MFP8	UART1 request to Send output pin.
							PWM0_CH5	I/O	MFP13	PWM0 channel 5 output/capture input.
		15	23	23	31	31	PF.15	I/O	MFP0	General purpose digital I/O pin.
							PWM0_BRAKE0	I	MFP11	PWM0 Brake 0 input pin.
							PWM0_CH1	I/O	MFP12	PWM0 channel 1 output/capture input.
							TM2	I/O	MFP13	Timer2 event counter input/toggle output pin.
							CLKO	O	MFP14	Clock Out
							INT4	I	MFP15	External interrupt 4 input pin.
18	24	16	24	24	32	32	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
19	25	17	25	25	33	33	PF.0	I/O	MFP0	General purpose digital I/O pin.
							UART1_TXD	O	MFP2	UART1 data transmitter output pin.
							I2C1_SCL	I/O	MFP3	I2C1 clock pin.
							UART0_TXD	O	MFP4	UART0 data transmitter output pin.
							ICE_DAT	O	MFP14	Serial wired debugger data pin.
20	26	18	26	26	34	34	PF.1	I/O	MFP0	General purpose digital I/O pin.
							UART1_RXD	I	MFP2	UART1 data receiver input pin.
							I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
							UART0_RXD	I	MFP4	UART0 data receiver input pin.
							ICE_CLK	I	MFP14	Serial wired debugger clock pin.
			27	27	35	35	PC.5	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD5	I/O	MFP2	EBI address/data bus bit 5.
							UART2_TXD	O	MFP8	UART2 data transmitter output pin.
							I2C1_SCL	I/O	MFP9	I2C1 clock pin.
							PWM1_CH0	I/O	MFP12	PWM1 channel 0 output/capture input.
			28	28	36	36	PC.4	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD4	I/O	MFP2	EBI address/data bus bit 4.
							UART2_RXD	I	MFP8	UART2 data receiver input pin.
							I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
							PWM1_CH1	I/O	MFP12	PWM1 channel 1 output/capture input.
			29	29	37	37	PC.3	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD3	I/O	MFP2	EBI address/data bus bit 3.
							UART2_nRTS	O	MFP8	UART2 request to Send output pin.
							PWM1_CH2	I/O	MFP12	PWM1 channel 2 output/capture input.
			30	30	38	38	PC.2	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD2	I/O	MFP2	EBI address/data bus bit 2.
							UART2_nCTS	I	MFP8	UART2 clear to Send input pin.
							PWM1_CH3	I/O	MFP12	PWM1 channel 3 output/capture input.
	27	19	31	31	39	39	PC.1	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD1	I/O	MFP2	EBI address/data bus bit 1.
							UART2_TXD	O	MFP8	UART2 data transmitter output pin.
							I2C0_SCL	I/O	MFP9	I2C0 clock pin.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
							PWM1_CH4	I/O	MFP12	PWM1 channel 4 output/capture input.
							ACMP0_O	O	MFP14	Analog comparator 0 output pin.
	28	20	32	32	40	40	PC.0	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD0	I/O	MFP2	EBI address/data bus bit 0.
							UART2_RXD	I	MFP8	UART2 data receiver input pin.
							I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
							PWM1_CH5	I/O	MFP12	PWM1 channel 5 output/capture input.
							ACMP1_O	O	MFP14	Analog comparator 1 output pin.
					41	41	PD.3	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD10	I/O	MFP2	EBI address/data bus bit 10.
							USCI0_CTL1	I/O	MFP3	USCI0 control 1 pin.
							SPI0_SS	I/O	MFP4	SPI0 slave select pin.
							UART0_TXD	O	MFP9	UART0 data transmitter output pin.
					42	42	PD.2	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
							USCI0_DAT1	I/O	MFP3	USCI0 data 1 pin.
							SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
							UART0_RXD	I	MFP9	UART0 data receiver input pin.
					43	43	PD.1	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
							USCI0_DAT0	I/O	MFP3	USCI0 data 0 pin.
							SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
					44	44	PD.0	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
							USCI0_CLK	I/O	MFP3	USCI0 clock pin.
							SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
							TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	1	21	33		45		PA.12	I/O	MFP0	General purpose digital I/O pin.
							I2C1_SCL	I/O	MFP4	I2C1 clock pin.
	2	22	34		46		PA.13	I/O	MFP0	General purpose digital I/O pin.
							I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
	3	23	35		47		PA.14	I/O	MFP0	General purpose digital I/O pin.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
							UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	4	24	36		48		PA.15	I/O	MFP0	General purpose digital I/O pin.
							UART0_RXD	I	MFP3	UART0 data receiver input pin.
				33		45	USB_VBUS	P	MFP0	Power supply from USB host or HUB.
				34		46	USB_D-	A	MFP0	USB differential signal D-.
				35		47	USB_D+	A	MFP0	USB differential signal D+.
				36		48	USB_VDD33_CAP	A	MFP0	Internal power regulator output 3.3V decoupling pin.
1	5	25	37	37	49	49	V_{SS}	P	MFP0	Ground pin for digital circuit.
2	6	26	38	38	50	50	LDO_CAP	A	MFP0	LDO output pin.
3	7	27	39	39	51	51	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
			40	40	52	52	PC.14	I/O	MFP0	General purpose digital I/O pin.
							EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
							SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
							USCI0_CTL0	I/O	MFP5	USCI0 control 0 pin.
							TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.
		28	41	41	53	53	PB.15	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH15	A	MFP1	ADC0 channel 15 analog input.
							EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
							SPI0_SS	I/O	MFP4	SPI0 slave select pin.
							USCI0_CTL1	I/O	MFP5	USCI0 control 1 pin.
							UART0_nCTS	I	MFP6	UART0 clear to Send input pin.
							PWM1_CH0	I/O	MFP11	PWM1 channel 0 output/capture input.
							TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
							PWM0_BRAKE1	I	MFP15	PWM0 Brake 1 input pin.
4	8	29	42	42	54	54	PB.14	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH14	A	MFP1	ADC0 channel 14 analog input.
							EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
							SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
							USCI0_DAT1	I/O	MFP5	USCI0 data 1 pin.
							UART0_nRTS	O	MFP6	UART0 request to Send output pin.
							PWM1_CH1	I/O	MFP11	PWM1 channel 1 output/capture input.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
							TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
							CLKO	O	MFP14	Clock Out
5	9	30	43	43	55	55	PB.13	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH13	A	MFP1	ADC0 channel 13 analog input.
							ACMP0_P3	A	MFP1	Analog comparator 0 positive input 3 pin.
							ACMP1_P3	A	MFP1	Analog comparator 1 positive input 3 pin.
							EBI_AD14	I/O	MFP2	EBI address/data bus bit 14.
							SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
							USCI0_DAT0	I/O	MFP5	USCI0 data 0 pin.
							UART0_TXD	O	MFP6	UART0 data transmitter output pin.
							PWM1_CH2	I/O	MFP11	PWM1 channel 2 output/capture input.
							TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
6	10	31	44	44	56	56	PB.12	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH12	A	MFP1	ADC0 channel 12 analog input.
							ACMP0_P2	A	MFP1	Analog comparator 0 positive input 2 pin.
							ACMP1_P2	A	MFP1	Analog comparator 1 positive input 2 pin.
							EBI_AD15	I/O	MFP2	EBI address/data bus bit 15.
							SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
							USCI0_CLK	I/O	MFP5	USCI0 clock pin.
							UART0_RXD	I	MFP6	UART0 data receiver input pin.
							PWM1_CH3	I/O	MFP11	PWM1 channel 3 output/capture input.
							TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
7	11	32	45	45	57	57	AV_{DD}	P	MFP0	Power supply for internal analog circuit.
					58	58	V_{REF}	A	MFP0	ADC reference voltage input. Note: This pin needs to be connected with a 1uF capacitor.
			46	46	59	59	AV_{SS}	P	MFP0	Ground pin for analog circuit.
					60	60	PB.11	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH11	A	MFP1	ADC0 channel 11 analog input.
							EBI_ADR16	O	MFP2	EBI address bus bit 16.
							UART0_nCTS	I	MFP5	UART0 clear to Send input pin.
							I2C1_SCL	I/O	MFP7	I2C1 clock pin.

20 Pin	28 Pin	32 Pin	48 Pin	48 Pin (M032)	64 Pin	64 Pin (M032)	Pin Name	Type	MFP	Description
							SPI0_I2SMCLK	I/O	MFP9	SPI0 I^{2}S master clock output pin
					61	61	PB.10	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH10	A	MFP1	ADC0 channel 10 analog input.
							EBI_ADR17	O	MFP2	EBI address bus bit 17.
							UART0_nRTS	O	MFP5	UART0 request to Send output pin.
							I2C1_SDA	I/O	MFP7	I2C1 data input/output pin.
					62	62	PB.9	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH9	A	MFP1	ADC0 channel 9 analog input.
							EBI_ADR18	O	MFP2	EBI address bus bit 18.
							UART0_TXD	O	MFP5	UART0 data transmitter output pin.
					63	63	UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
							PB.8	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH8	A	MFP1	ADC0 channel 8 analog input.
							EBI_ADR19	O	MFP2	EBI address bus bit 19.
							UART0_RXD	I	MFP5	UART0 data receiver input pin.
							UART1_nRTS	O	MFP6	UART1 request to Send output pin.
			47	47	64	64	PB.7	I/O	MFP0	General purpose digital I/O pin.
							ADC0_CH7	A	MFP1	ADC0 channel 7 analog input.
							EBI_nWRL	O	MFP2	EBI low byte write enable output pin.
							UART1_TXD	O	MFP6	UART1 data transmitter output pin.
							EBI_nCS0	O	MFP8	EBI chip select 0 output pin.
							PWM1_BRAKE0	I	MFP11	PWM1 Brake 0 input pin.
							PWM1_CH4	I/O	MFP12	PWM1 channel 4 output/capture input.
							INT5	I	MFP13	External interrupt 5 input pin.

4.2.2 M031/M032 Series Multi-function Summary Table

Group	Pin Name	GPIO	MFP	Type	Description
ACMP0	ACMP0_N	PB.3	MFP1	A	Analog comparator 0 negative input pin.
	ACMP0_O	PC.1	MFP14	O	Analog comparator 0 output pin.
		PB.7	MFP15	O	
	ACMP0_P0	PA.11	MFP1	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	PB.2	MFP1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	PB.12	MFP1	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	PB.13	MFP1	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	PA.7	MFP13	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	PB.5	MFP1	A	Analog comparator 1 negative input pin.
	ACMP1_O	PC.0	MFP14	O	Analog comparator 1 output pin.
		PB.6	MFP15	O	
	ACMP1_P0	PA.10	MFP1	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	PB.4	MFP1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	PB.12	MFP1	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	PB.13	MFP1	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	PA.6	MFP13	I	Analog comparator 1 window latch input pin
CLKO	CLKO	PF.14	MFP13	O	Clock Out
		PA.3	MFP14	O	
		PF.15	MFP14	O	
		PB.14	MFP14	O	
ADC0	ADC0_CH0	PB.0	MFP1	A	ADC0 channel 0 analog input.
	ADC0_CH1	PB.1	MFP1	A	ADC0 channel 1 analog input.
	ADC0_CH2	PB.2	MFP1	A	ADC0 channel 2 analog input.
	ADC0_CH3	PB.3	MFP1	A	ADC0 channel 3 analog input.
	ADC0_CH4	PB.4	MFP1	A	ADC0 channel 4 analog input.
	ADC0_CH5	PB.5	MFP1	A	ADC0 channel 5 analog input.
	ADC0_CH6	PB.6	MFP1	A	ADC0 channel 6 analog input.
	ADC0_CH7	PB.7	MFP1	A	ADC0 channel 7 analog input.
	ADC0_CH8	PB.8	MFP1	A	ADC0 channel 8 analog input.
	ADC0_CH9	PB.9	MFP1	A	ADC0 channel 9 analog input.
	ADC0_CH10	PB.10	MFP1	A	ADC0 channel 10 analog input.
	ADC0_CH11	PB.11	MFP1	A	ADC0 channel 11 analog input.
	ADC0_CH12	PB.12	MFP1	A	ADC0 channel 12 analog input.

Group	Pin Name	GPIO	MFP	Type	Description
	ADC0_CH13	PB.13	MFP1	A	ADC0 channel 13 analog input.
	ADC0_CH14	PB.14	MFP1	A	ADC0 channel 14 analog input.
	ADC0_CH15	PB.15	MFP1	A	ADC0 channel 15 analog input.
	ADC0_ST	PF.5	MFP11	I	ADC0 external trigger input.
EBI	EBI_AD0	PC.0	MFP2	I/O	EBI address/data bus bit 0.
	EBI_AD1	PC.1	MFP2	I/O	EBI address/data bus bit 1.
	EBI_AD2	PC.2	MFP2	I/O	EBI address/data bus bit 2.
	EBI_AD3	PC.3	MFP2	I/O	EBI address/data bus bit 3.
	EBI_AD4	PC.4	MFP2	I/O	EBI address/data bus bit 4.
	EBI_AD5	PC.5	MFP2	I/O	EBI address/data bus bit 5.
	EBI_AD6	PA.6	MFP2	I/O	EBI address/data bus bit 6.
	EBI_AD7	PA.7	MFP2	I/O	EBI address/data bus bit 7.
	EBI_AD8	PC.6	MFP2	I/O	EBI address/data bus bit 8.
	EBI_AD9	PC.7	MFP2	I/O	EBI address/data bus bit 9.
	EBI_AD10	PD.3	MFP2	I/O	EBI address/data bus bit 10.
	EBI_AD11	PD.2	MFP2	I/O	EBI address/data bus bit 11.
		PC.14	MFP2	I/O	
	EBI_AD12	PD.1	MFP2	I/O	EBI address/data bus bit 12.
		PB.15	MFP2	I/O	
	EBI_AD13	PD.0	MFP2	I/O	EBI address/data bus bit 13.
		PB.14	MFP2	I/O	
	EBI_AD14	PB.13	MFP2	I/O	EBI address/data bus bit 14.
	EBI_AD15	PB.12	MFP2	I/O	EBI address/data bus bit 15.
	EBI_ADR16	PB.11	MFP2	O	EBI address bus bit 16.
	EBI_ADR17	PB.10	MFP2	O	EBI address bus bit 17.
	EBI_ADR18	PB.9	MFP2	O	EBI address bus bit 18.
	EBI_ADR19	PF.6	MFP2	O	EBI address bus bit 19.
		PB.8	MFP2	O	
	EBI_ALE	PA.8	MFP2	O	EBI address latch enable output pin.
	EBI_MCLK	PA.9	MFP2	O	EBI external clock output pin.
	EBI_nCS0	PF.6	MFP7	O	EBI chip select 0 output pin.
		PF.3	MFP2	O	
		PB.7	MFP8	O	
	EBI_nCS1	PF.2	MFP2	O	EBI chip select 1 output pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PB.6	MFP8	O	
	EBI_nRD	PA.11	MFP2	O	EBI read enable output pin.
	EBI_nWR	PA.10	MFP2	O	EBI write enable output pin.
	EBI_nWRH	PB.6	MFP2	O	EBI high byte write enable output pin
	EBI_nWRL	PB.7	MFP2	O	EBI low byte write enable output pin.
I2C0	I2C0_SCL	PB.5	MFP6	I/O	I2C0 clock pin.
		PF.3	MFP4	I/O	
		PA.5	MFP9	I/O	
		PC.1	MFP9	I/O	
	I2C0_SDA	PB.4	MFP6	I/O	I2C0 data input/output pin.
		PF.2	MFP4	I/O	
		PA.4	MFP9	I/O	
		PC.0	MFP9	I/O	
I2C1	I2C1_SCL	PB.3	MFP4	I/O	I2C1 clock pin.
		PB.1	MFP9	I/O	
		PA.7	MFP8	I/O	
		PA.3	MFP9	I/O	
		PF.0	MFP3	I/O	
		PC.5	MFP9	I/O	
		PA.12	MFP4	I/O	
		PB.11	MFP7	I/O	
	I2C1_SDA	PB.2	MFP4	I/O	I2C1 data input/output pin.
		PB.0	MFP9	I/O	
		PA.6	MFP8	I/O	
		PA.2	MFP9	I/O	
		PF.1	MFP3	I/O	
		PC.4	MFP9	I/O	
		PA.13	MFP4	I/O	
		PB.10	MFP7	I/O	
ICE	ICE_CLK	PF.1	MFP14	I	Serial wired debugger clock pin.
	ICE_DAT	PF.0	MFP14	O	Serial wired debugger data pin.
INT0	INT0	PB.5	MFP15	I	External interrupt 0 input pin.
		PA.6	MFP15	I	
INT1	INT1	PB.4	MFP15	I	External interrupt 1 input pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PA.7	MFP15	I	
		PD.15	MFP15	I	
INT2	INT2	PB.3	MFP15	I	External interrupt 2 input pin.
		PC.6	MFP15	I	
INT3	INT3	PB.2	MFP15	I	External interrupt 3 input pin.
		PC.7	MFP15	I	
INT4	INT4	PA.8	MFP15	I	External interrupt 4 input pin.
		PF.15	MFP15	I	
		PB.6	MFP13	I	
INT5	INT5	PF.14	MFP15	I	External interrupt 5 input pin.
		PB.7	MFP13	I	
PWM0	PWM0_BRAKE0	PB.3	MFP13	I	PWM0 Brake 0 input pin.
		PB.1	MFP13	I	
		PF.14	MFP10	I	
		PF.15	MFP11	I	
	PWM0_BRAKE1	PB.0	MFP13	I	PWM0 Brake 1 input pin.
		PB.15	MFP15	I	
	PWM0_CH0	PB.5	MFP11	I/O	PWM0 channel 0 output/capture input.
		PF.5	MFP7	I/O	
		PA.5	MFP13	I/O	
	PWM0_CH1	PB.4	MFP11	I/O	PWM0 channel 1 output/capture input.
		PF.4	MFP7	I/O	
		PA.4	MFP13	I/O	
		PF.15	MFP12	I/O	
	PWM0_CH2	PB.3	MFP11	I/O	PWM0 channel 2 output/capture input.
		PA.3	MFP13	I/O	
	PWM0_CH3	PB.2	MFP11	I/O	PWM0 channel 3 output/capture input.
		PA.2	MFP13	I/O	
	PWM0_CH4	PB.1	MFP11	I/O	PWM0 channel 4 output/capture input.
		PF.14	MFP12	I/O	
		PA.1	MFP13	I/O	
	PWM0_CH5	PB.0	MFP11	I/O	PWM0 channel 5 output/capture input.
		PD.15	MFP12	I/O	
		PA.0	MFP13	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
PWM1	PWM1_BRAKE0	PF.14	MFP9	I	PWM1 Brake 0 input pin.
		PB.7	MFP11	I	
	PWM1_BRAKE1	PA.3	MFP15	I	PWM1 Brake 1 input pin.
		PB.6	MFP11	I	
	PWM1_CH0	PC.5	MFP12	I/O	PWM1 channel 0 output/capture input.
		PB.15	MFP11	I/O	
	PWM1_CH1	PC.4	MFP12	I/O	PWM1 channel 1 output/capture input.
		PB.14	MFP11	I/O	
	PWM1_CH2	PC.7	MFP11	I/O	PWM1 channel 2 output/capture input.
		PC.3	MFP12	I/O	
		PB.13	MFP11	I/O	
	PWM1_CH3	PC.6	MFP11	I/O	PWM1 channel 3 output/capture input.
		PC.2	MFP12	I/O	
		PB.12	MFP11	I/O	
	PWM1_CH4	PB.1	MFP12	I/O	PWM1 channel 4 output/capture input.
		PA.7	MFP11	I/O	
		PC.1	MFP12	I/O	
		PB.7	MFP12	I/O	
	PWM1_CH5	PB.0	MFP12	I/O	PWM1 channel 5 output/capture input.
		PA.6	MFP11	I/O	
		PC.0	MFP12	I/O	
		PB.6	MFP12	I/O	
SPI0	SPI0_CLK	PA.2	MFP4	I/O	SPI0 serial clock pin.
		PD.2	MFP4	I/O	
		PB.14	MFP4	I/O	
	SPI0_I2SMCLK	PB.0	MFP8	I/O	SPI0 I^2S master clock output pin
		PA.4	MFP4	I/O	
		PC.14	MFP4	I/O	
		PB.11	MFP9	I/O	
	SPI0_MISO	PA.1	MFP4	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PD.1	MFP4	I/O	
		PB.13	MFP4	I/O	
	SPI0_MOSI	PF.6	MFP5	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PA.0	MFP4	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PD.0	MFP4	I/O	
		PB.12	MFP4	I/O	
	SPI0_SS	PA.3	MFP4	I/O	SPI0 slave select pin.
		PD.3	MFP4	I/O	
		PB.15	MFP4	I/O	
TM0	TM0	PB.5	MFP14	I/O	Timer0 event counter input/toggle output pin.
		PC.7	MFP14	I/O	
	TM0_EXT	PA.11	MFP13	I/O	Timer0 external capture input/toggle output pin.
		PB.15	MFP13	I/O	
TM1	TM1	PB.4	MFP14	I/O	Timer1 event counter input/toggle output pin.
		PC.6	MFP14	I/O	
		PC.14	MFP13	I/O	
	TM1_EXT	PA.10	MFP13	I/O	Timer1 external capture input/toggle output pin.
		PB.14	MFP13	I/O	
TM2	TM2	PB.3	MFP14	I/O	Timer2 event counter input/toggle output pin.
		PA.7	MFP14	I/O	
		PF.15	MFP13	I/O	
		PD.0	MFP14	I/O	
	TM2_EXT	PA.9	MFP13	I/O	Timer2 external capture input/toggle output pin.
		PB.13	MFP13	I/O	
TM3	TM3	PB.2	MFP14	I/O	Timer3 event counter input/toggle output pin.
		PF.14	MFP14	I/O	
		PA.6	MFP14	I/O	
		PD.15	MFP14	I/O	
	TM3_EXT	PA.8	MFP13	I/O	Timer3 external capture input/toggle output pin.
		PB.12	MFP13	I/O	
UART0	UART0_RXD	PF.2	MFP3	I	UART0 data receiver input pin.
		PA.6	MFP7	I	
		PA.4	MFP8	I	
		PA.0	MFP7	I	
		PF.1	MFP4	I	
		PD.2	MFP9	I	
		PA.15	MFP3	I	
		PB.12	MFP6	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PB.8	MFP5	I	
	UART0_TXD	PF.3	MFP3	O	UART0 data transmitter output pin.
		PA.7	MFP7	O	
		PA.5	MFP8	O	
		PA.1	MFP7	O	
		PF.0	MFP4	O	
		PD.3	MFP9	O	
		PA.14	MFP3	O	
		PB.13	MFP6	O	
		PB.9	MFP5	O	
	UART0_nCTS	PC.7	MFP7	I	UART0 clear to Send input pin.
		PA.5	MFP7	I	
		PB.15	MFP6	I	
		PB.11	MFP5	I	
	UART0_nRTS	PC.6	MFP7	O	UART0 request to Send output pin.
		PA.4	MFP7	O	
		PB.14	MFP6	O	
		PB.10	MFP5	O	
UART1	UART1_RXD	PB.2	MFP6	I	UART1 data receiver input pin.
		PA.8	MFP7	I	
		PA.2	MFP8	I	
		PF.1	MFP2	I	
		PB.6	MFP6	I	
	UART1_TXD	PB.3	MFP6	O	UART1 data transmitter output pin.
		PA.9	MFP7	O	
		PA.3	MFP8	O	
		PF.0	MFP2	O	
		PB.7	MFP6	O	
	UART1_nCTS	PA.1	MFP8	I	UART1 clear to Send input pin.
		PB.9	MFP6	I	
	UART1_nRTS	PA.0	MFP8	O	UART1 request to Send output pin.
		PB.8	MFP6	O	
UART2	UART2_RXD	PB.4	MFP13	I	UART2 data receiver input pin.
		PB.0	MFP7	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PF.5	MFP2	I	
		PC.4	MFP8	I	
		PC.0	MFP8	I	
	UART2_TXD	PB.5	MFP13	O	UART2 data transmitter output pin.
		PB.1	MFP7	O	
		PF.4	MFP2	O	
		PC.5	MFP8	O	
		PC.1	MFP8	O	
	UART2_nCTS	PF.5	MFP4	I	UART2 clear to Send input pin.
		PC.2	MFP8	I	
	UART2_nRTS	PF.4	MFP4	O	UART2 request to Send output pin.
		PC.3	MFP8	O	
USCI0	USCI0_CLK	PA.11	MFP6	I/O	USCI0 clock pin.
		PD.0	MFP3	I/O	
		PB.12	MFP5	I/O	
	USCI0_CTL0	PC.14	MFP5	I/O	USCI0 control 0 pin.
	USCI0_CTL1	PA.8	MFP6	I/O	USCI0 control 1 pin.
		PD.3	MFP3	I/O	
		PB.15	MFP5	I/O	
	USCI0_DAT0	PA.10	MFP6	I/O	USCI0 data 0 pin.
		PD.1	MFP3	I/O	
		PB.13	MFP5	I/O	
	USCI0_DAT1	PA.9	MFP6	I/O	USCI0 data 1 pin.
		PD.2	MFP3	I/O	
		PB.14	MFP5	I/O	
X32	X32_IN	PF.5	MFP10	I	External 32.768 kHz crystal input pin.
	X32_OUT	PF.4	MFP10	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PF.3	MFP10	I	External 4~32 MHz (high speed) crystal input pin.
	XT1_OUT	PF.2	MFP10	O	External 4~32 MHz (high speed) crystal output pin.

4.2.3 M031/M032 Series Multi-function Summary Table Sorted by GPIO

	Pin Name	Type	MFP	Description
PA.0	PA.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	UART1_nRTS	O	MFP8	UART1 request to Send output pin.
	PWM0_CH5	I/O	MFP13	PWM0 channel 5 output/capture input.
PA.1	PA.1	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
	PWM0_CH4	I/O	MFP13	PWM0 channel 4 output/capture input.
PA.2	PA.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	PWM0_CH3	I/O	MFP13	PWM0 channel 3 output/capture input.
PA.3	PA.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	PWM0_CH2	I/O	MFP13	PWM0 channel 2 output/capture input.
	CLKO	O	MFP14	Clock Out
	PWM1_BRAKE1	I	MFP15	PWM1 Brake 1 input pin.
PA.4	PA.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	UART0_RXD	I	MFP8	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	PWM0_CH1	I/O	MFP13	PWM0 channel 1 output/capture input.
PA.5	PA.5	I/O	MFP0	General purpose digital I/O pin.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	PWM0_CH0	I/O	MFP13	PWM0 channel 0 output/capture input.

	Pin Name	Type	MFP	Description
PA.6	PA.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD6	I/O	MFP2	EBI address/data bus bit 6.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
	PWM1_CH5	I/O	MFP11	PWM1 channel 5 output/capture input.
	ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PA.7	PA.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD7	I/O	MFP2	EBI address/data bus bit 7.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I2C1 clock pin.
	PWM1_CH4	I/O	MFP11	PWM1 channel 4 output/capture input.
	ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PA.8	PA.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_ALE	O	MFP2	EBI address latch enable output pin.
	USCI0_CTL1	I/O	MFP6	USCI0 control 1 pin.
	UART1_RXD	I	MFP7	UART1 data receiver input pin.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
	INT4	I	MFP15	External interrupt 4 input pin.
PA.9	PA.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_MCLK	O	MFP2	EBI external clock output pin.
	USCI0_DAT1	I/O	MFP6	USCI0 data 1 pin.
	UART1_TXD	O	MFP7	UART1 data transmitter output pin.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
PA.10	PA.10	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
	EBI_nWR	O	MFP2	EBI write enable output pin.
	USCI0_DAT0	I/O	MFP6	USCI0 data 0 pin.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
PA.11	PA.11	I/O	MFP0	General purpose digital I/O pin.
	ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.

	Pin Name	Type	MFP	Description
	EBI_nRD	O	MFP2	EBI read enable output pin.
	USCI0_CLK	I/O	MFP6	USCI0 clock pin.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
PA.12	PA.12	I/O	MFP0	General purpose digital I/O pin.
	I2C1_SCL	I/O	MFP4	I2C1 clock pin.
PA.13	PA.13	I/O	MFP0	General purpose digital I/O pin.
	I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
PA.14	PA.14	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
PA.15	PA.15	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
PB.0	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP1	ADC0 channel 0 analog input.
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	SPI0_I2SMCLK	I/O	MFP8	SPI0 I^2S master clock output pin
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	PWM0_CH5	I/O	MFP11	PWM0 channel 5 output/capture input.
	PWM1_CH5	I/O	MFP12	PWM1 channel 5 output/capture input.
	PWM0_BRAKE1	I	MFP13	PWM0 Brake 1 input pin.
PB.1	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	PWM0_CH4	I/O	MFP11	PWM0 channel 4 output/capture input.
	PWM1_CH4	I/O	MFP12	PWM1 channel 4 output/capture input.
	PWM0_BRAKE0	I	MFP13	PWM0 Brake 0 input pin.
PB.2	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
	ACMP0_P1	A	MFP1	Analog comparator 0 positive input 1 pin.
	I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	PWM0_CH3	I/O	MFP11	PWM0 channel 3 output/capture input.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.

	Pin Name	Type	MFP	Description
PB.3	PB.3	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
	ACMP0_N	A	MFP1	Analog comparator 0 negative input pin.
	I2C1_SCL	I/O	MFP4	I2C1 clock pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	PWM0_CH2	I/O	MFP11	PWM0 channel 2 output/capture input.
	PWM0_BRAKE0	I	MFP13	PWM0 Brake 0 input pin.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PB.4	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
	ACMP1_P1	A	MFP1	Analog comparator 1 positive input 1 pin.
	I2C0_SDA	I/O	MFP6	I2C0 data input/output pin.
	PWM0_CH1	I/O	MFP11	PWM0 channel 1 output/capture input.
	UART2_RXD	I	MFP13	UART2 data receiver input pin.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PB.5	PB.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH5	A	MFP1	ADC0 channel 5 analog input.
	ACMP1_N	A	MFP1	Analog comparator 1 negative input pin.
	I2C0_SCL	I/O	MFP6	I2C0 clock pin.
	PWM0_CH0	I/O	MFP11	PWM0 channel 0 output/capture input.
	UART2_TXD	O	MFP13	UART2 data transmitter output pin.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PB.6	PB.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH6	A	MFP1	ADC0 channel 6 analog input.
	EBI_nWRH	O	MFP2	EBI high byte write enable output pin
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	EBI_nCS1	O	MFP8	EBI chip select 1 output pin.
	PWM1_BRAKE1	I	MFP11	PWM1 Brake 1 input pin.
	PWM1_CH5	I/O	MFP12	PWM1 channel 5 output/capture input.
	INT4	I	MFP13	External interrupt 4 input pin.
	ACMP1_O	O	MFP15	Analog comparator 1 output pin.

	Pin Name	Type	MFP	Description
PB.7	PB.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH7	A	MFP1	ADC0 channel 7 analog input.
	EBI_nWRL	O	MFP2	EBI low byte write enable output pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	EBI_nCS0	O	MFP8	EBI chip select 0 output pin.
	PWM1_BRAKE0	I	MFP11	PWM1 Brake 0 input pin.
	PWM1_CH4	I/O	MFP12	PWM1 channel 4 output/capture input.
	INT5	I	MFP13	External interrupt 5 input pin.
	ACMP0_O	O	MFP15	Analog comparator 0 output pin.
PB.8	PB.8	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH8	A	MFP1	ADC0 channel 8 analog input.
	EBI_ADR19	O	MFP2	EBI address bus bit 19.
	UART0_RXD	I	MFP5	UART0 data receiver input pin.
	UART1_nRTS	O	MFP6	UART1 request to Send output pin.
PB.9	PB.9	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH9	A	MFP1	ADC0 channel 9 analog input.
	EBI_ADR18	O	MFP2	EBI address bus bit 18.
	UART0_TXD	O	MFP5	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
PB.10	PB.10	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH10	A	MFP1	ADC0 channel 10 analog input.
	EBI_ADR17	O	MFP2	EBI address bus bit 17.
	UART0_nRTS	O	MFP5	UART0 request to Send output pin.
	I2C1_SDA	I/O	MFP7	I2C1 data input/output pin.
PB.11	PB.11	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH11	A	MFP1	ADC0 channel 11 analog input.
	EBI_ADR16	O	MFP2	EBI address bus bit 16.
	UART0_nCTS	I	MFP5	UART0 clear to Send input pin.
	I2C1_SCL	I/O	MFP7	I2C1 clock pin.
	SPI0_I2SMCLK	I/O	MFP9	SPI0 I^2S master clock output pin
PB.12	PB.12	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH12	A	MFP1	ADC0 channel 12 analog input.
	ACMP0_P2	A	MFP1	Analog comparator 0 positive input 2 pin.
	ACMP1_P2	A	MFP1	Analog comparator 1 positive input 2 pin.

	Pin Name	Type	MFP	Description
	EBI_AD15	I/O	MFP2	EBI address/data bus bit 15.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	USCI0_CLK	I/O	MFP5	USCI0 clock pin.
	UART0_RXD	I	MFP6	UART0 data receiver input pin.
	PWM1_CH3	I/O	MFP11	PWM1 channel 3 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
PB.13	PB.13	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH13	A	MFP1	ADC0 channel 13 analog input.
	ACMP0_P3	A	MFP1	Analog comparator 0 positive input 3 pin.
	ACMP1_P3	A	MFP1	Analog comparator 1 positive input 3 pin.
	EBI_AD14	I/O	MFP2	EBI address/data bus bit 14.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	USCI0_DAT0	I/O	MFP5	USCI0 data 0 pin.
	UART0_TXD	O	MFP6	UART0 data transmitter output pin.
	PWM1_CH2	I/O	MFP11	PWM1 channel 2 output/capture input.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
PB.14	PB.14	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH14	A	MFP1	ADC0 channel 14 analog input.
	EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	USCI0_DAT1	I/O	MFP5	USCI0 data 1 pin.
	UART0_nRTS	O	MFP6	UART0 request to Send output pin.
	PWM1_CH1	I/O	MFP11	PWM1 channel 1 output/capture input.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	CLKO	O	MFP14	Clock Out
PB.15	PB.15	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH15	A	MFP1	ADC0 channel 15 analog input.
	EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	USCI0_CTL1	I/O	MFP5	USCI0 control 1 pin.
	UART0_nCTS	I	MFP6	UART0 clear to Send input pin.
	PWM1_CH0	I/O	MFP11	PWM1 channel 0 output/capture input.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
	PWM0_BRAKE1	I	MFP15	PWM0 Brake 1 input pin.

	Pin Name	Type	MFP	Description
PC.0	PC.0	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD0	I/O	MFP2	EBI address/data bus bit 0.
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	PWM1_CH5	I/O	MFP12	PWM1 channel 5 output/capture input.
	ACMP1_O	O	MFP14	Analog comparator 1 output pin.
PC.1	PC.1	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD1	I/O	MFP2	EBI address/data bus bit 1.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	PWM1_CH4	I/O	MFP12	PWM1 channel 4 output/capture input.
	ACMP0_O	O	MFP14	Analog comparator 0 output pin.
PC.2	PC.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD2	I/O	MFP2	EBI address/data bus bit 2.
	UART2_nCTS	I	MFP8	UART2 clear to Send input pin.
	PWM1_CH3	I/O	MFP12	PWM1 channel 3 output/capture input.
PC.3	PC.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD3	I/O	MFP2	EBI address/data bus bit 3.
	UART2_nRTS	O	MFP8	UART2 request to Send output pin.
	PWM1_CH2	I/O	MFP12	PWM1 channel 2 output/capture input.
PC.4	PC.4	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD4	I/O	MFP2	EBI address/data bus bit 4.
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	PWM1_CH1	I/O	MFP12	PWM1 channel 1 output/capture input.
PC.5	PC.5	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD5	I/O	MFP2	EBI address/data bus bit 5.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	PWM1_CH0	I/O	MFP12	PWM1 channel 0 output/capture input.
PC.6	PC.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD8	I/O	MFP2	EBI address/data bus bit 8.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	PWM1_CH3	I/O	MFP11	PWM1 channel 3 output/capture input.

	Pin Name	Type	MFP	Description
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PC.7	PC.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD9	I/O	MFP2	EBI address/data bus bit 9.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	PWM1_CH2	I/O	MFP11	PWM1 channel 2 output/capture input.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PC.14	PC.14	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
	USCI0_CTL0	I/O	MFP5	USCI0 control 0 pin.
	TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.
PD.0	PD.0	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
	USCI0_CLK	I/O	MFP3	USCI0 clock pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
PD.1	PD.1	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
	USCI0_DAT0	I/O	MFP3	USCI0 data 0 pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
PD.2	PD.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
	USCI0_DAT1	I/O	MFP3	USCI0 data 1 pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
PD.3	PD.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD10	I/O	MFP2	EBI address/data bus bit 10.
	USCI0_CTL1	I/O	MFP3	USCI0 control 1 pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART0_TXD	O	MFP9	UART0 data transmitter output pin.
PD.15	PD.15	I/O	MFP0	General purpose digital I/O pin.
	PWM0_CH5	I/O	MFP12	PWM0 channel 5 output/capture input.

	Pin Name	Type	MFP	Description
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PF.0	PF.0	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP3	I2C1 clock pin.
	UART0_TXD	O	MFP4	UART0 data transmitter output pin.
	ICE_DAT	O	MFP14	Serial wired debugger data pin.
PF.1	PF.1	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
	UART0_RXD	I	MFP4	UART0 data receiver input pin.
	ICE_CLK	I	MFP14	Serial wired debugger clock pin.
PF.2	PF.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS1	O	MFP2	EBI chip select 1 output pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	XT1_OUT	O	MFP10	External 4~32 MHz (high speed) crystal output pin.
PF.3	PF.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS0	O	MFP2	EBI chip select 0 output pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	XT1_IN	I	MFP10	External 4~32 MHz (high speed) crystal input pin.
PF.4	PF.4	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MFP2	UART2 data transmitter output pin.
	UART2_nRTS	O	MFP4	UART2 request to Send output pin.
	PWM0_CH1	I/O	MFP7	PWM0 channel 1 output/capture input.
	X32_OUT	O	MFP10	External 32.768 kHz crystal output pin.
PF.5	PF.5	I/O	MFP0	General purpose digital I/O pin.
	UART2_RXD	I	MFP2	UART2 data receiver input pin.
	UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
	PWM0_CH0	I/O	MFP7	PWM0 channel 0 output/capture input.
	X32_IN	I	MFP10	External 32.768 kHz crystal input pin.
	ADC0_ST	I	MFP11	ADC0 external trigger input.
PF.6	PF.6	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	EBI_ADR19	O	MFP2	EBI address bus bit 19.
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
	EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
PF.14	PF.14	I/O	MFP0	General purpose digital I/O pin.
	PWM1_BRAKE0	I	MFP9	PWM1 Brake 0 input pin.
	PWM0_BRAKE0	I	MFP10	PWM0 Brake 0 input pin.
	PWM0_CH4	I/O	MFP12	PWM0 channel 4 output/capture input.
	CLKO	O	MFP13	Clock Out
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT5	I	MFP15	External interrupt 5 input pin.
PF.15	PF.15	I/O	MFP0	General purpose digital I/O pin.
	PWM0_BRAKE0	I	MFP11	PWM0 Brake 0 input pin.
	PWM0_CH1	I/O	MFP12	PWM0 channel 1 output/capture input.
	TM2	I/O	MFP13	Timer2 event counter input/toggle output pin.
	CLKO	O	MFP14	Clock Out
	INT4	I	MFP15	External interrupt 4 input pin.

5 BLOCK DIAGRAM

5.1 M031/M032 Block Diagram

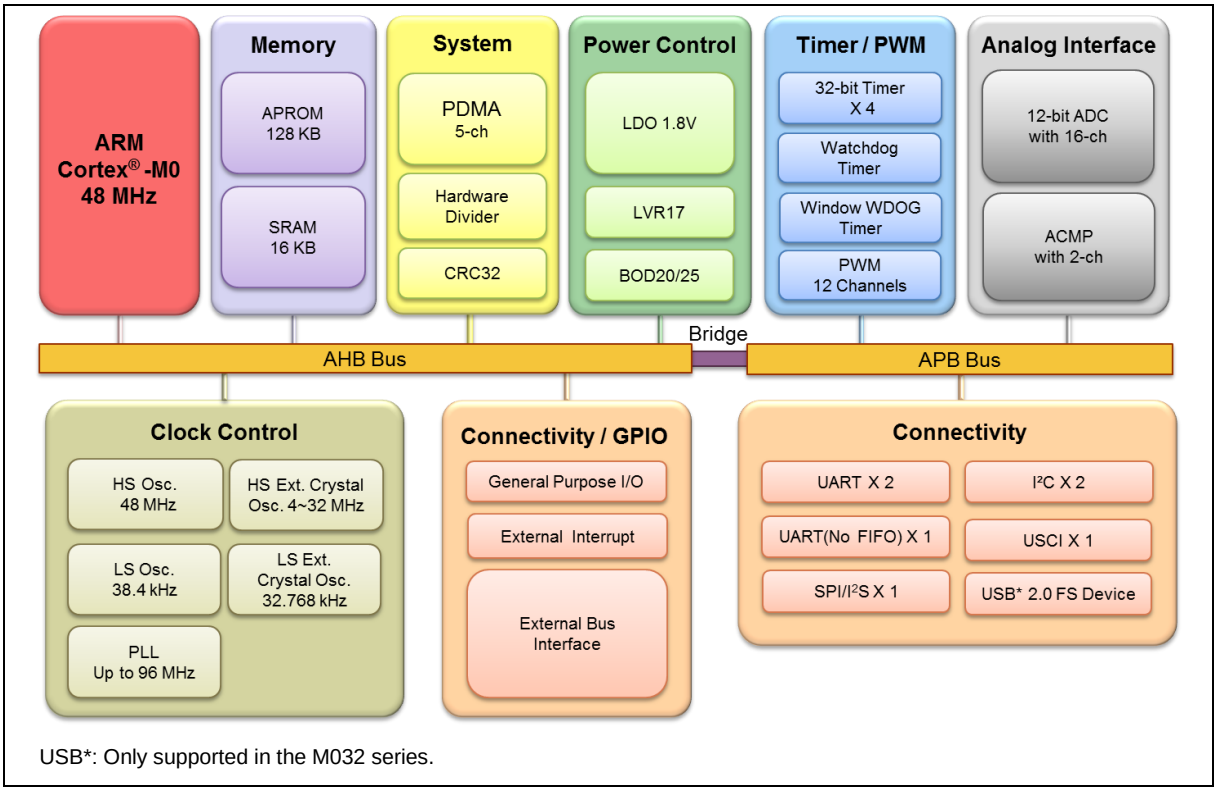


Figure 5.1-1 M031/M032 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

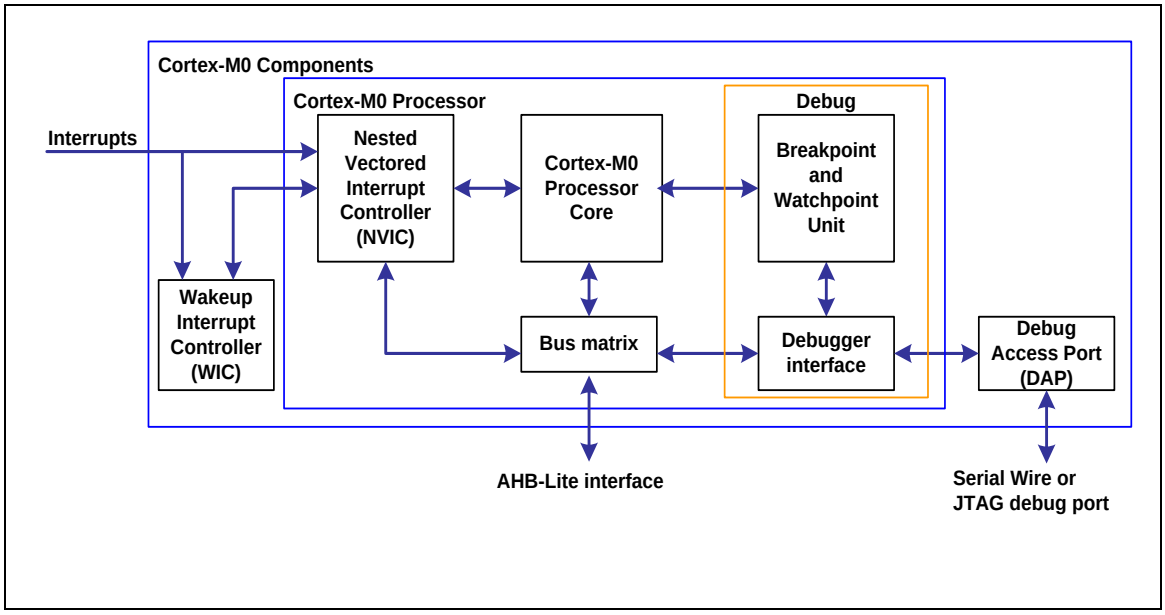


Figure 6.1-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor:
  - Arm®6-M Thumb® instruction set
  - Thumb-2 technology
  - Arm®6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the Armv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event

(WFE) instructions, or return from interrupt sleep-on-exit feature

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sourcces are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS_IPRST0[1])
  - nRESET glitch filter time 32us

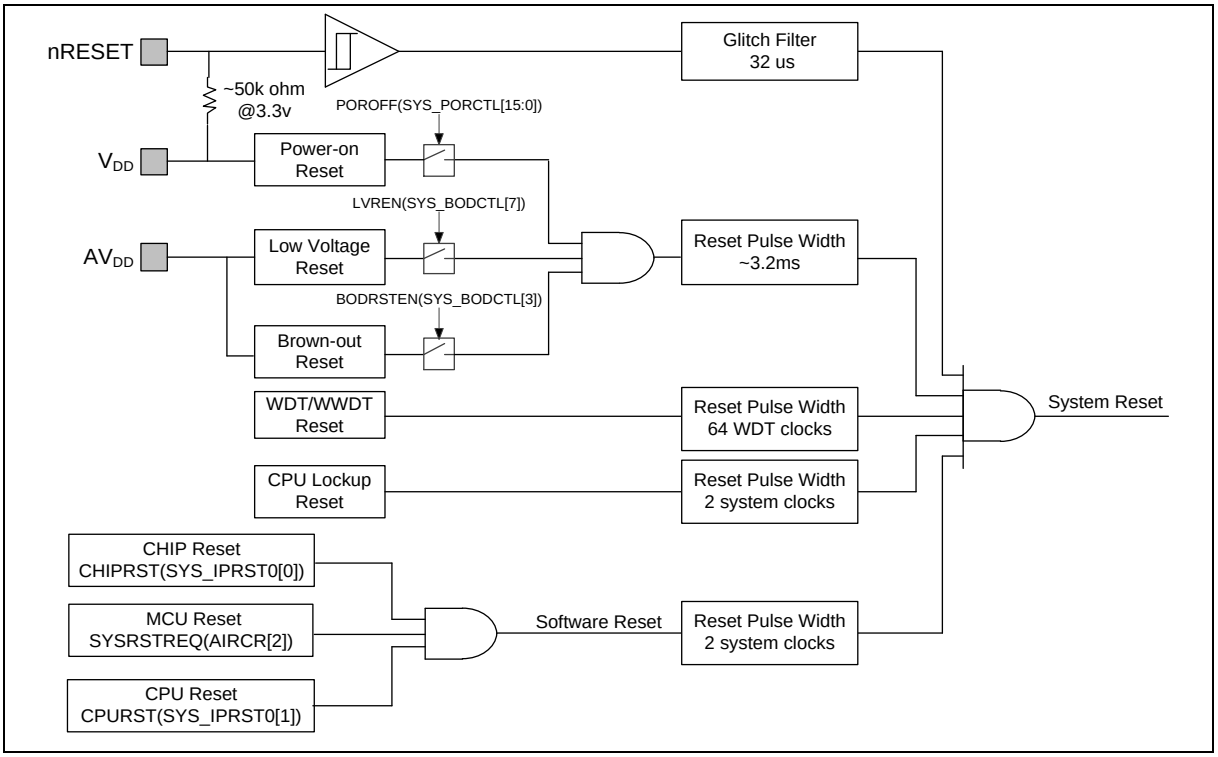


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[16])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL	Reload	Reload	Reload	Reload	Reload	Reload	Reload	Reload	-

(CLK_CLKSEL0[2:0])	from CONFIG0	from CONFIG0	from CONFIG0	from CONFIG0	from CONFIG0	from CONFIG0	from CONFIG0	from CONFIG0	
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1))	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Table 6.2-2 shows the nRESET reset waveform.

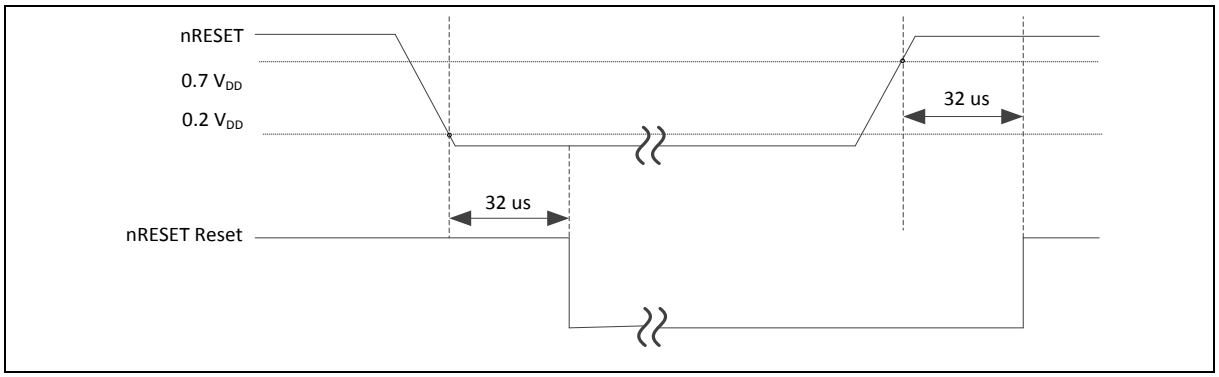


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

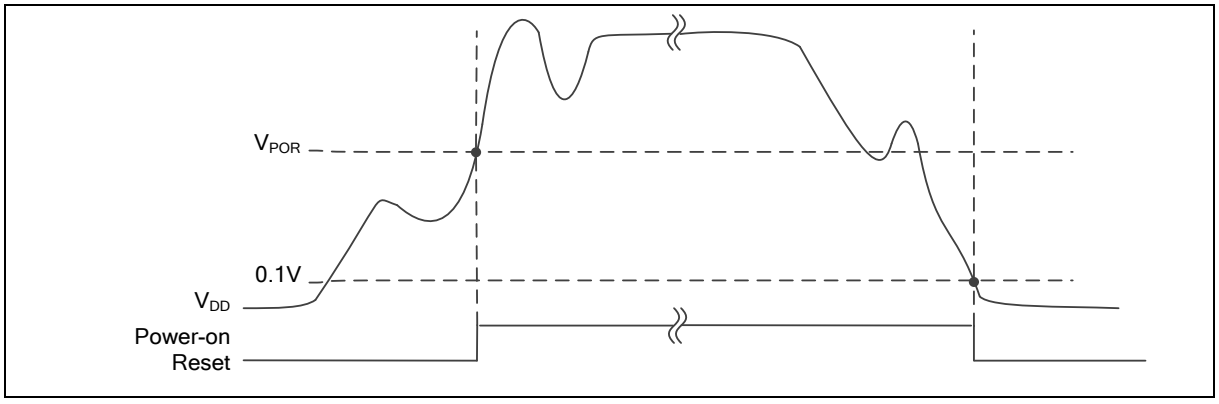


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the

AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

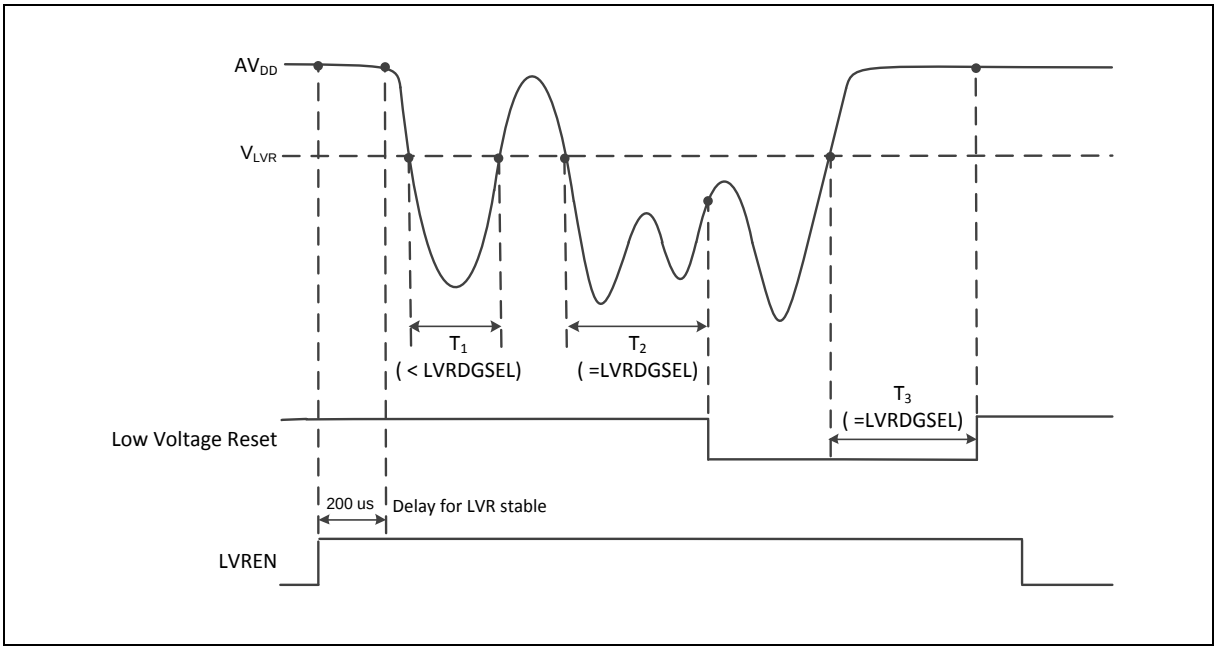


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

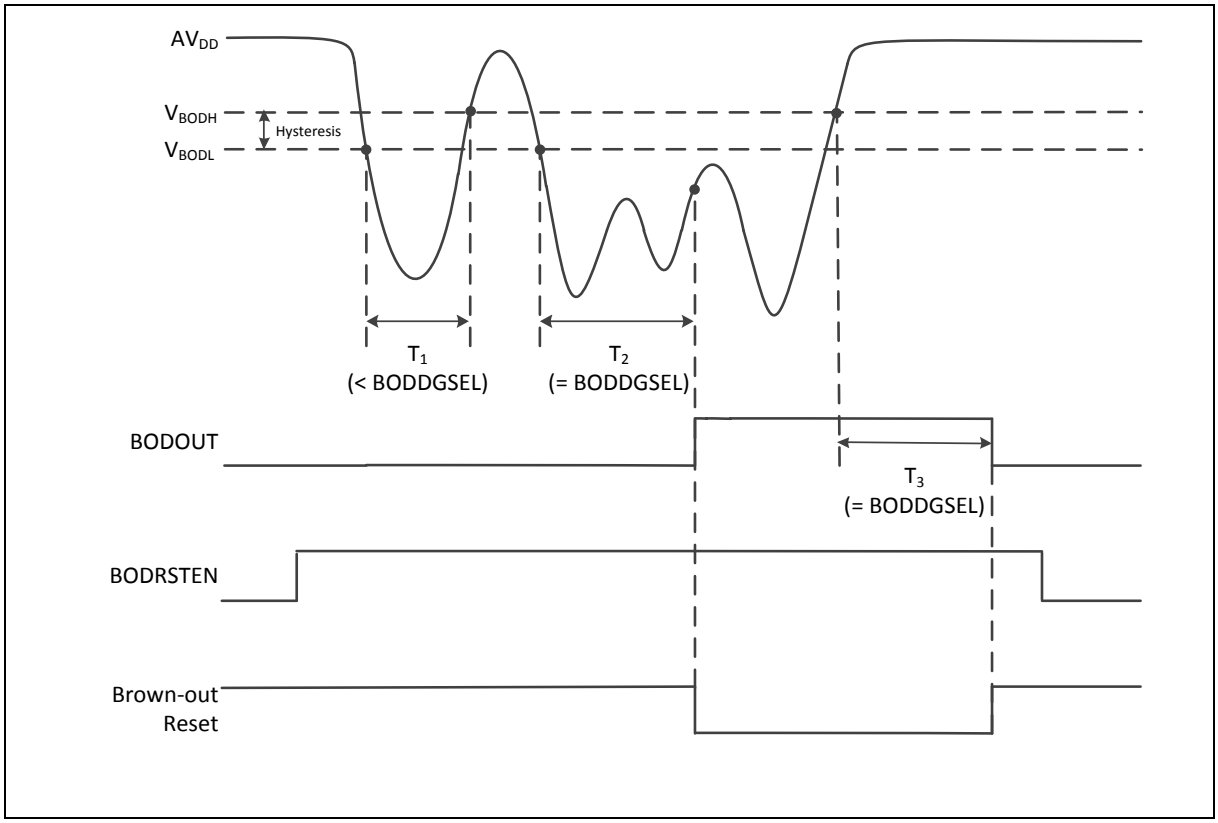


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into three segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and V_{DD}, require an external capacitor which should be located close to the corresponding pin. Figure 6.2-6 shows the NuMicro® M031 power distribution.

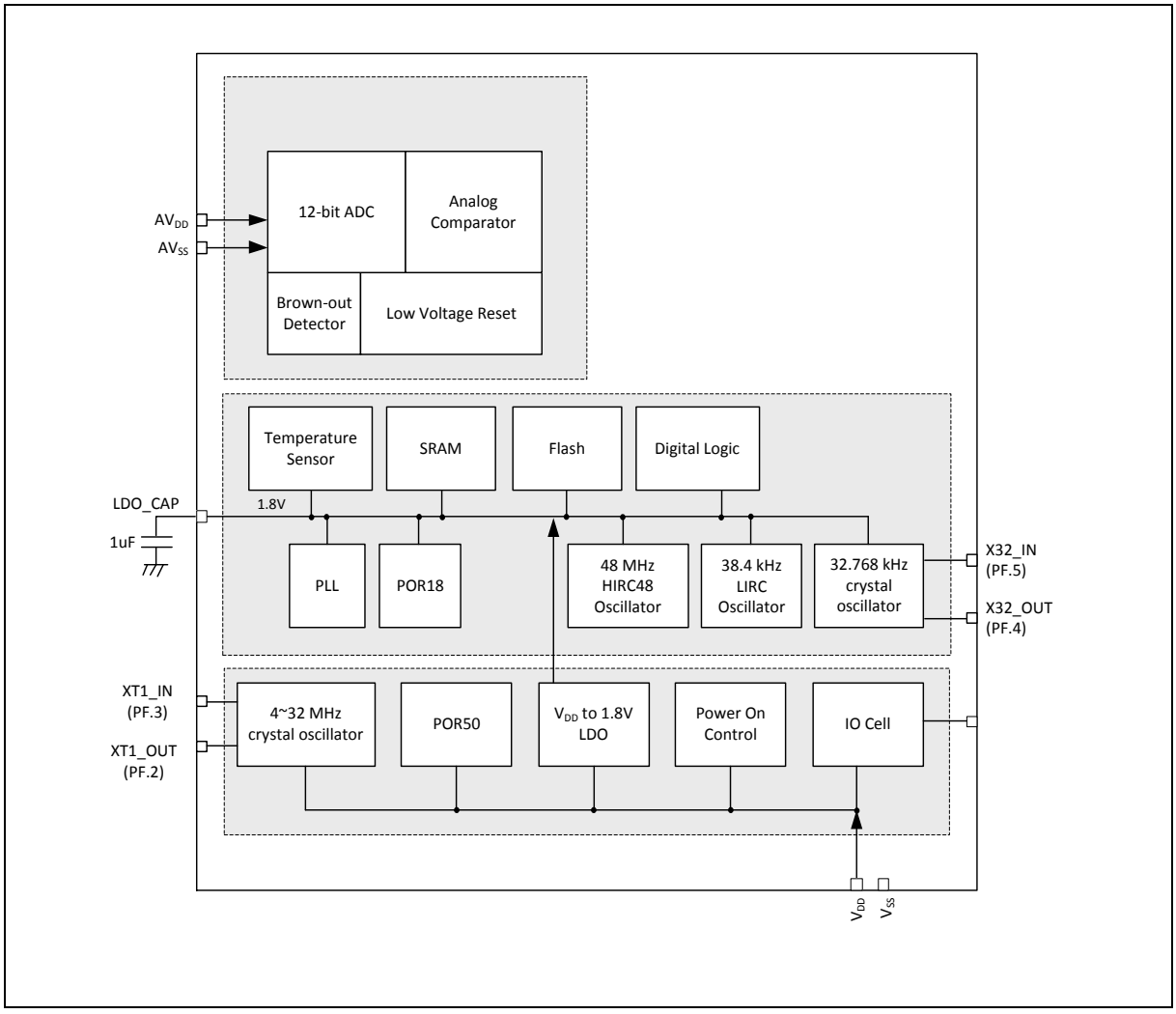


Figure 6.2-6 NuMicro® M031 Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

The M031 series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power mode in the M031 series.

Mode	CPU Operating Maximum Speed(MHz)	LDO_CAP(V)	Clock Disable
Normal mode	48	1.8	All clocks are disabled by control register.

Idle mode	CPU enter Sleep mode	1.8	Only CPU clock is disabled.
Power-down mode	CPU enters Power-down mode	1.8	Most clocks are disabled except LIRC/LXT, and only WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.

Table 6.2-2 Power Mode Table

There are different power mode entry settings and leaving condition for each power mode. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT:[7]) and execute WFI instruction.

Register/Instruction Mode	**SLEEPDEEP (SCR[2])**	**PDEN (CLK_PWRCTL[7])**	**CPU Run WFI Instruction**
Normal mode	0	0	NO
Idle mode (CPU enter Sleep mode)	0	0	YES
Power-down mode (CPU enters Deep Sleep mode)	1	1	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	**Normal Mode**	**Idle Mode**	**Power-Down Mode**
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI, USBD, and ACMP
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Difference Table

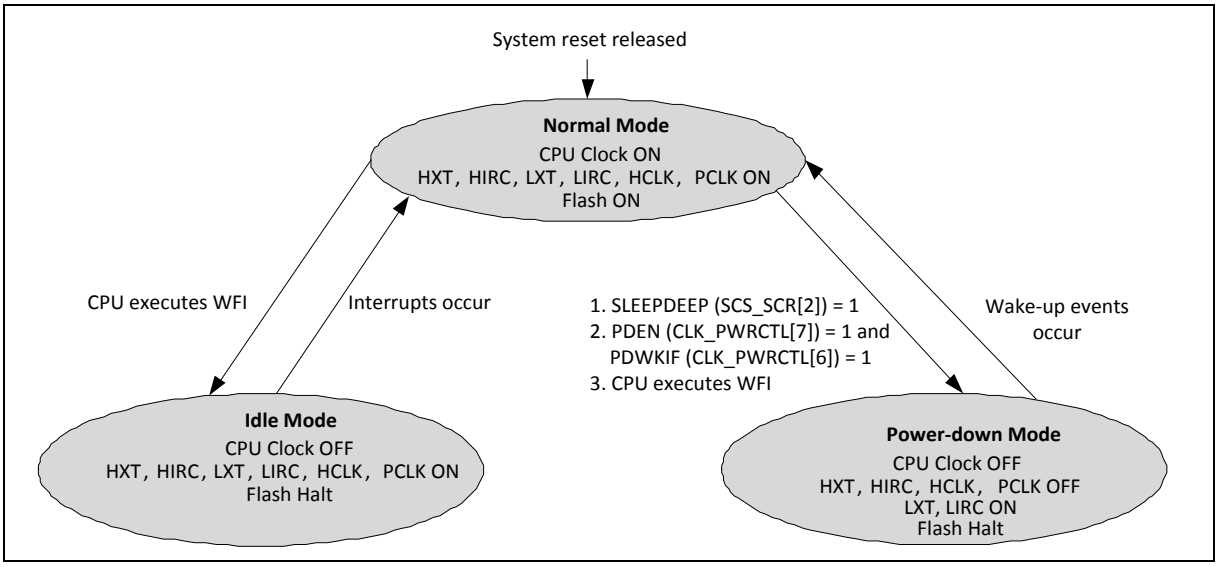


Figure 6.2-7 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in normal mode.
2. LIRC (38.4 kHz OSC) ON or OFF depends on S/W setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If UART clock source is selected as LXT and LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~32 MHz XTL)	ON	ON	Halt
HIRC48 (48 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (38.4 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON/OFF	ON/OFF	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
WWDT	ON	ON	Halt
UART	ON	ON	ON/OFF[6]

USCI	ON	ON	Halt
I^2C	ON	ON	Halt
SPI	ON	ON	Halt
USBD	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt

Table 6.2-5 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, USCI, BOD, GPIO, USBD, and ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-5 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear (SYS_BODCTL[4]).
INT	External Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
UART0/1	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
UART2	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
I^2C	Address match or GC mode match wake-up.	After software writes 1 to clear WKIF(I2C_WKSTS[0]).
USBD	Remote Wake-up	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).

Table 6.2-6 Condition of Entering Power-down Mode Again

6.2.5 System Memory Map

The NuMicro® M031 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown inTable 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M031 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (192KB)
0x2000_0000 – 0x2000_3FFF	SRAM0_BA	SRAM Memory Space (16KB)
0x6000_0000 – 0x6FFF_FFFF	EXTMEM_BA	External Memory Space (256MB)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4001_0000 – 0x4001_0FFF	EBI_BA	External Bus Interface Control Registers
0x4001_4000 – 0x4001_7FFF	HDIV_BA	Hardware Divider Register
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_3000 – 0x4004_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	PWM0_BA	PWM0 Control Registers
0x4005_9000 – 0x4005_9FFF	PWM1_BA	PWM1 Control Registers
0x4006_1000 – 0x4006_0FFF	SPI0_BA	SPI0 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I^2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I^2C1 Control Registers
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		

0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.6 SRAM Memory Orginization

The M031 supports embedded SRAM with total 16 Kbytes size

- Supports total 16 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

Table 6.2-10 shows the SRAM organization of M031. The address between 0x2000_4000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

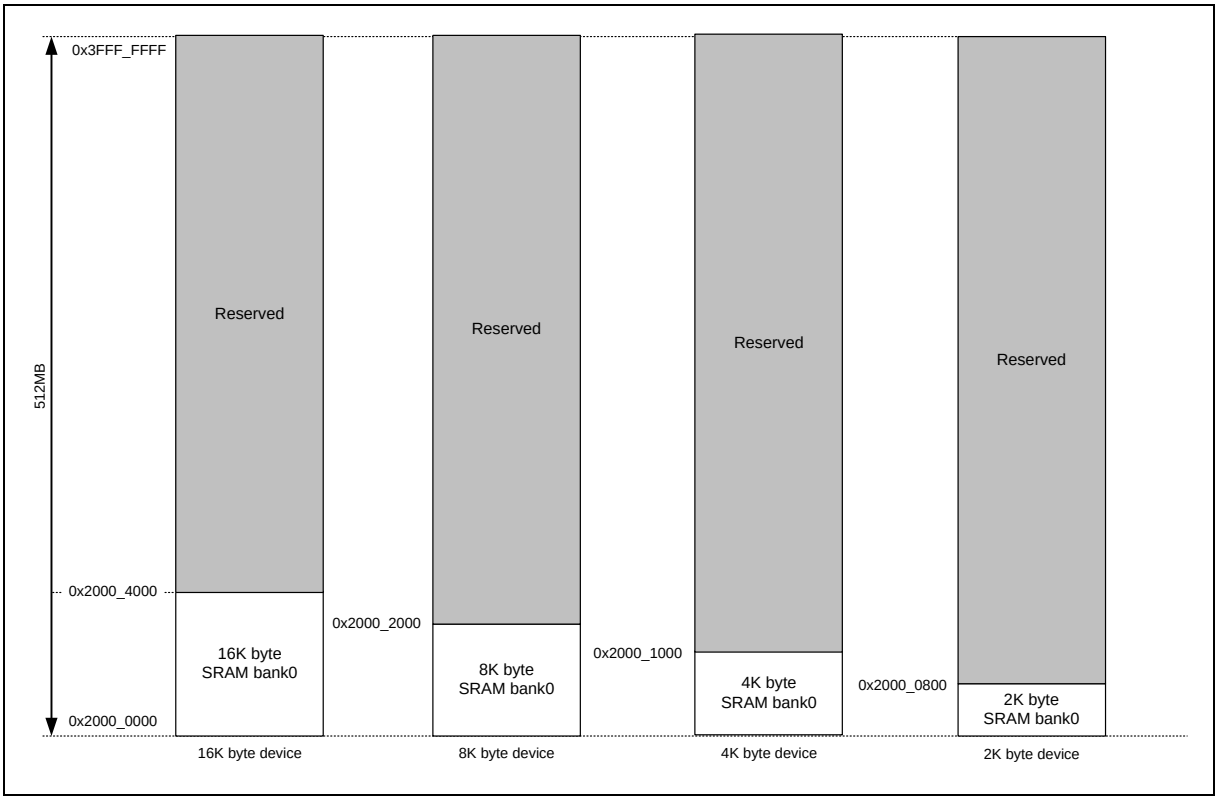


Figure 6.2-8 SRAM Memory Organization

6.2.7 Chip Bus Matrix

The M031 series supports Bus Matrix to manage the access arbitration between masters. The access arbitration use round-robin algorithm as the bus priority.

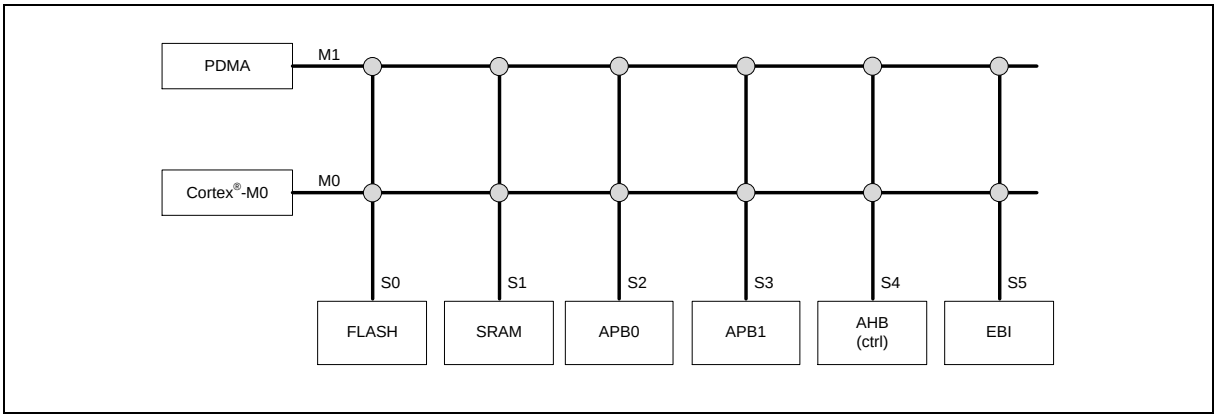


Figure 6.2-9 NuMicro® M031 Bus Matrix Diagram

6.2.8 IRC Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator), according to the accurate external 32.768 kHz crystal oscillator or internal USB synchronous mode, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.

In HIRC case, the system needs an accurate 48 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal or in system, user has to set REFCKSEL (SYS_HIRCTRIMCTL [10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTRIMCTL [1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTRIMSTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.2.9 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence. All proteced control registers are noted “(Write Protect)” and add an note “Note: This bit is write protected. Refer to the SYS_REGLCTL register “ in register description field.

Register	Bit	Description
SYS_IPRST0	[7] CRCRST	CRC Calculation Controller Reset (Write Protect)
SYS_IPRST0	[4] HDIV_RST	HDIV Controller Reset (Write Protect)
SYS_IPRST0	[3] EBIRST	EBI Controller Reset (Write Protect)
SYS_IPRST0	[2] PDMARST	PDMA Controller Reset (Write Protect)
SYS_IPRST0	[1] CPURST	Processor Core One-shot Reset (Write Protect)
SYS_IPRST0	[0] CHIPRST	Chip One-shot Reset (Write Protect)
SYS_BODCTL	[20] LVRVL	LVR Detector Threshold Voltage Selection (Write Protect)
SYS_BODCTL	[16] BODVL	Brown-out Detector Threshold Voltage Selection (Write Protect)
SYS_BODCTL	[14:12] LVRDGSEL	LVR Output De-glitch Time Select (Write Protect)
SYS_BODCTL	[10:8] BODDGSEL	Brown-out Detector Output De-glitch Time Select (Write Protect)
SYS_BODCTL	[7] LVREN	Low Voltage Reset Enable Bit (Write Protect)
SYS_BODCTL	[5] BODLPM	Brown-out Detector Low Power Mode (Write Protect)
SYS_BODCTL	[3] BODRSTEN	Brown-out Reset Enable Bit (Write Protect)
SYS_BODCTL	[0] BODEN	Brown-out Detector Enable Bit (Write Protect)
SYS_PORCTL	[15:0] POROFF	Power-on Reset Enable Bit (Write Protect)
SYS_SRAM_BISTCTL	[7] PDMABIST	PDMA BIST Enable Bit (Write Protect)
SYS_SRAM_BISTCTL	[4] USBBIST	USB BIST Enable Bit (Write Protect)
SYS_PORDISAN	[15:0] POROFFAN	Power-on Reset Enable Bit (Write Protect)
NMIEN	[15] UART1_INT	UART1 NMI Source Enable (Write Protect)
NMIEN	[14] UART0_INT	UART0 NMI Source Enable (Write Protect)
NMIEN	[13] EINT5	External Interrupt From PB.7 or PF.14 Pin NMI Source Enable (Write Protect)
NMIEN	[12] EINT4	External Interrupt From PA.8, PB.6 or PF.15 Pin NMI Source Enable (Write Protect)
NMIEN	[11] EINT3	External Interrupt From PB.2 or PC.7 Pin NMI Source Enable (Write Protect)
NMIEN	[10] EINT2	External Interrupt From PB.3 or PC.6 Pin NMI Source Enable (Write Protect)
NMIEN	[9] EINT1	External Interrupt From PA.7, PB.4 or PD.15 Pin NMI Source Enable (Write Protect)

NMIEN	[8] EINT0	External Interrupt From PA.6 or PB.5 Pin NMI Source Enable (Write Protect)
NMIEN	[4] CLKFAIL	Clock Fail Detected and IRC Auto Trim Interrupt NMI Source Enable (Write Protect)
NMIEN	[2] PWRWU_INT	Power-down Mode Wake-up NMI Source Enable (Write Protect)
NMIEN	[1] IRC_INT	IRC TRIM NMI Source Enable (Write Protect)
NMIEN	[0] BODOUT	BOD NMI Source Enable (Write Protect)
CLK_PWRCTL	[26:25] LXTGAIN	LXT Gain Control Bit (Write Protect)
CLK_PWRCTL	[22:20] HXTGAIN	HXT Gain Control Bit (Write Protect)
CLK_PWRCTL	[7] PDEN	System Power-down Enable (Write Protect)
CLK_PWRCTL	[5] PDWKIEN	Power-down Mode Wake-up Interrupt Enable Bit (Write Protect)
CLK_PWRCTL	[4] PDWKDLY	Enable the Wake-up Delay Counter (Write Protect)
CLK_PWRCTL	[3] LIRCEN	LIRC Enable Bit (Write Protect)
CLK_PWRCTL	[2] HIRCEN	HIRC Enable Bit (Write Protect)
CLK_PWRCTL	[1] LXTEN	LXT Enable Bit (Write Protect)
CLK_PWRCTL	[0] HXTEN	HXT Enable Bit (Write Protect)
CLK_APBCLK0	[0] WDTCKEN	Watchdog Timer Clock Enable Bit (Write Protect)
CLK_CLKSEL0	[8] USBDSEL	USB Device Clock Source Selection (Write Protect)
CLK_CLKSEL0	[5:3] STCLKSEL	Cortex®-M0 SysTick Clock Source Selection (Write Protect)
CLK_CLKSEL0	[2:0] HCLKSEL	HCLK Clock Source Selection (Write Protect)
CLK_CLKSEL1	[3:2] WWDTSEL	Window Watchdog Timer Clock Source Selection (Write Protect)
CLK_CLKSEL1	[1:0] WDTSEL	Watchdog Timer Clock Source Selection (Write Protect)
CLK_PLLCTL	[23] STBSEL	PLL Stable Counter Selection (Write Protect)
CLK_PLLCTL	[19] PLLSRC	PLL Source Clock Selection (Write Protect)
CLK_PLLCTL	[18] OE	PLL OE (FOUT Enable) Pin Control (Write Protect)
CLK_PLLCTL	[17] BP	PLL Bypass Control (Write Protect)
CLK_PLLCTL	[16] PD	Power-down Mode (Write Protect)
CLK_PLLCTL	[15:14] OUTDIV	PLL Output Divider Control (Write Protect)
CLK_PLLCTL	[13:9] INDIV	PLL Input Divider Control (Write Protect)
CLK_PLLCTL	[8:0] FBDIV	PLL Feedback Divider Control (Write Protect)
CLK_CLKDSTS	[8] HXTFQIF	HXT Clock Frequency Range Detector Interrupt Flag (Write Protect)
CLK_CLKDSTS	[1] LXTFIF	LXT Clock Fail Interrupt Flag (Write Protect)
CLK_CLKDSTS	[0] HXTFIF	HXT Clock Fail Interrupt Flag (Write Protect)
FMC_ISPCTL	[6] ISPFF	ISP Fail Flag (Write Protect)
FMC_ISPCTL	[5] LDUEN	LDROM Update Enable Bit (Write Protect)
FMC_ISPCTL	[4] CFGUEN	CONFIG Update Enable Bit (Write Protect)

FMC_ISPCTL	[3] APUEN	APROM Update Enable Bit (Write Protect)
FMC_ISPCTL	[2] SPUEN	SPROM Update Enable Bit (Write Protect)
FMC_ISPCTL	[1] BS	Boot Select (Write Protect)
FMC_ISPCTL	[0] ISPEN	ISP Enable Bit (Write Protect)
FMC_ISPTRG	[0] ISPGO	ISP Start Trigger (Write Protect)
FMC_FTCTL	[6:4] FOM	Frequency Optimization Mode (Write Protect)
FMC_ISPSTS	[6] ISPFF	ISP Fail Flag (Write Protect)
TIMER0_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
TIMER1_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
TIMER2_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
TIMER3_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
WDT_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
WDT_CTL	[11:8] TOUTSEL	WDT Time-out Interval Selection (Write Protect)
WDT_CTL	[7] WDTEN	WDT Enable Bit (Write Protect)
WDT_CTL	[6] INTEN	WDT Time-out Interrupt Enable Bit (Write Protect)
WDT_CTL	[5] WKF	WDT Time-out Wake-up Flag (Write Protect)
WDT_CTL	[4] WKEN	WDT Time-out Wake-up Function Control (Write Protect)
WDT_CTL	[1] RSTEN	WDT Time-out Reset Enable Bit (Write Protect)
WDT_ALTCTL	[1:0] RSTDSEL	WDT Reset Delay Selection (Write Protect)
PWM_CTL0	[31] DBGTRIOFF	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
PWM_CTL0	[30] DBGHALT	ICE Debug Mode Counter Halt (Write Protect)
PWM_DTCTL0_1	[24] DTCKSEL	Dead-time Clock Select (Write Protect)
PWM_DTCTL0_1	[16] DTEN	Enable Dead-time Insertion for PWM Pair (PWM_CH0, PWM_CH1) (PWM_CH2, PWM_CH3) (PWM_CH4, PWM_CH5) (Write Protect)
PWM_DTCTL0_1	[11:0] DTCNT	Dead-time Counter (Write Protect)
PWM_DTCTL2_3	[24] DTCKSEL	Dead-time Clock Select (Write Protect)
PWM_DTCTL2_3	[16] DTEN	Enable Dead-time Insertion for PWM Pair (PWM_CH0, PWM_CH1) (PWM_CH2, PWM_CH3) (PWM_CH4, PWM_CH5) (Write Protect)
PWM_DTCTL2_3	[11:0] DTCNT	Dead-time Counter (Write Protect)
PWM_DTCTL4_5	[24] DTCKSEL	Dead-time Clock Select (Write Protect)
PWM_DTCTL4_5	[16] DTEN	Enable Dead-time Insertion for PWM Pair (PWM_CH0, PWM_CH1) (PWM_CH2, PWM_CH3) (PWM_CH4, PWM_CH5) (Write Protect)
PWM_DTCTL4_5	[11:0] DTCNT	Dead-time Counter (Write Protect)
PWM_BRKCTL0_1	[19:18] BRKAODD	PWM Brake Action Select for Odd Channel (Write Protect)
PWM_BRKCTL0_1	[17:16] BRKAEVEN	PWM Brake Action Select for Even Channel (Write Protect)
PWM_BRKCTL0_1	[15] SYSLBEN	Enable System Fail As Level-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[13] BRKP1LEN	Enable BKP1 Pin As Level-detect Brake Source (Write Protect)

PWM_BRKCTL0_1	[12] BRKP0LEN	Enable BKP0 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[9] CPO1LBEN	Enable ACMP1_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[8] CPO0LBEN	Enable ACMP0_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[7] SYSEBEN	Enable System Fail As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[5] BRKP1EEN	Enable PWMx_BRAKE1 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[4] BRKP0EEN	Enable PWMx_BRAKE0 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[1] CPO1EBEN	Enable ACMP1_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL0_1	[0] CPO0EBEN	Enable ACMP0_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[19:18] BRKAODD	PWM Brake Action Select for Odd Channel (Write Protect)
PWM_BRKCTL2_3	[17:16] BRKAEVEN	PWM Brake Action Select for Even Channel (Write Protect)
PWM_BRKCTL2_3	[15] SYSLBEN	Enable System Fail As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[13] BRKP1LEN	Enable BKP1 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[12] BRKP0LEN	Enable BKP0 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[9] CPO1LBEN	Enable ACMP1_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[8] CPO0LBEN	Enable ACMP0_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[7] SYSEBEN	Enable System Fail As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[5] BRKP1EEN	Enable PWMx_BRAKE1 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[4] BRKP0EEN	Enable PWMx_BRAKE0 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[1] CPO1EBEN	Enable ACMP1_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL2_3	[0] CPO0EBEN	Enable ACMP0_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[19:18] BRKAODD	PWM Brake Action Select for Odd Channel (Write Protect)
PWM_BRKCTL4_5	[17:16] BRKAEVEN	PWM Brake Action Select for Even Channel (Write Protect)
PWM_BRKCTL4_5	[15] SYSLBEN	Enable System Fail As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[13] BRKP1LEN	Enable BKP1 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[12] BRKP0LEN	Enable BKP0 Pin As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[9] CPO1LBEN	Enable ACMP1_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[8] CPO0LBEN	Enable ACMP0_O Digital Output As Level-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[7] SYSEBEN	Enable System Fail As Edge-detect Brake Source (Write Protect)

PWM_BRKCTL4_5	[5] BRKP1EEN	Enable PWMx_BRAKE1 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[4] BRKP0EEN	Enable PWMx_BRAKE0 Pin As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[1] CPO1EBEN	Enable ACMP1_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_BRKCTL4_5	[0] CPO0EBEN	Enable ACMP0_O Digital Output As Edge-detect Brake Source (Write Protect)
PWM_SWBRK	[8+n/2] n=0,2,4 BRKLTRGn	PWM Level Brake Software Trigger (Write Only) (Write Protect)
PWM_SWBRK	[n/2] n=0,2,4 BRKETRGn	PWM Edge Brake Software Trigger (Write Only) (Write Protect)
PWM_INTEN1	[10] BRKLIEN4_5	PWM Level-detect Brake Interrupt Enable for Channel4/5 (Write Protect)
PWM_INTEN1	[9] BRKLIEN2_3	PWM Level-detect Brake Interrupt Enable for Channel2/3 (Write Protect)
PWM_INTEN1	[8] BRKLIEN0_1	PWM Level-detect Brake Interrupt Enable for Channel0/1 (Write Protect)
PWM_INTEN1	[2] BRKEIEN4_5	PWM Edge-detect Brake Interrupt Enable for Channel4/5 (Write Protect)
PWM_INTEN1	[1] BRKEIEN2_3	PWM Edge-detect Brake Interrupt Enable for Channel2/3 (Write Protect)
PWM_INTEN1	[0] BRKEIEN0_1	PWM Edge-detect Brake Interrupt Enable for Channel0/1 (Write Protect)
PWM_INTSTS1	[8+n] n=0,1..5 BRKLIFn	PWM Channel n Level-detect Brake Interrupt Flag (Write Protect)
PWM_INTSTS1	[n] n=0,1..5 BRKEIFn	PWM Channel n Edge-detect Brake Interrupt Flag (Write Protect)
ADC_ADCR	[12] RESET	ADC RESET (Write Protect)

Table 6.2-8 Protected Register List

6.2.10 UART0_TXD/USCI0_DAT0 modulation with PWM

This chip supports UART0_TXD/USCI_DAT0 to modulate with PWM channel. User can set MODPWMSEL(SYS_MODCTL[7:4]) to choose which PWM0 channel to modulate with UART0_TXD/USCI0_DAT0 and set MODEN(SYS_MODCTL[0]) to enable modulation function. User can set TXDINV(UART_LINE[8]) to inverse UART0_TXD or DATOINV(UUART_LINECTL[5]) to inverse USCI0_DAT0 before modulating with PWM.

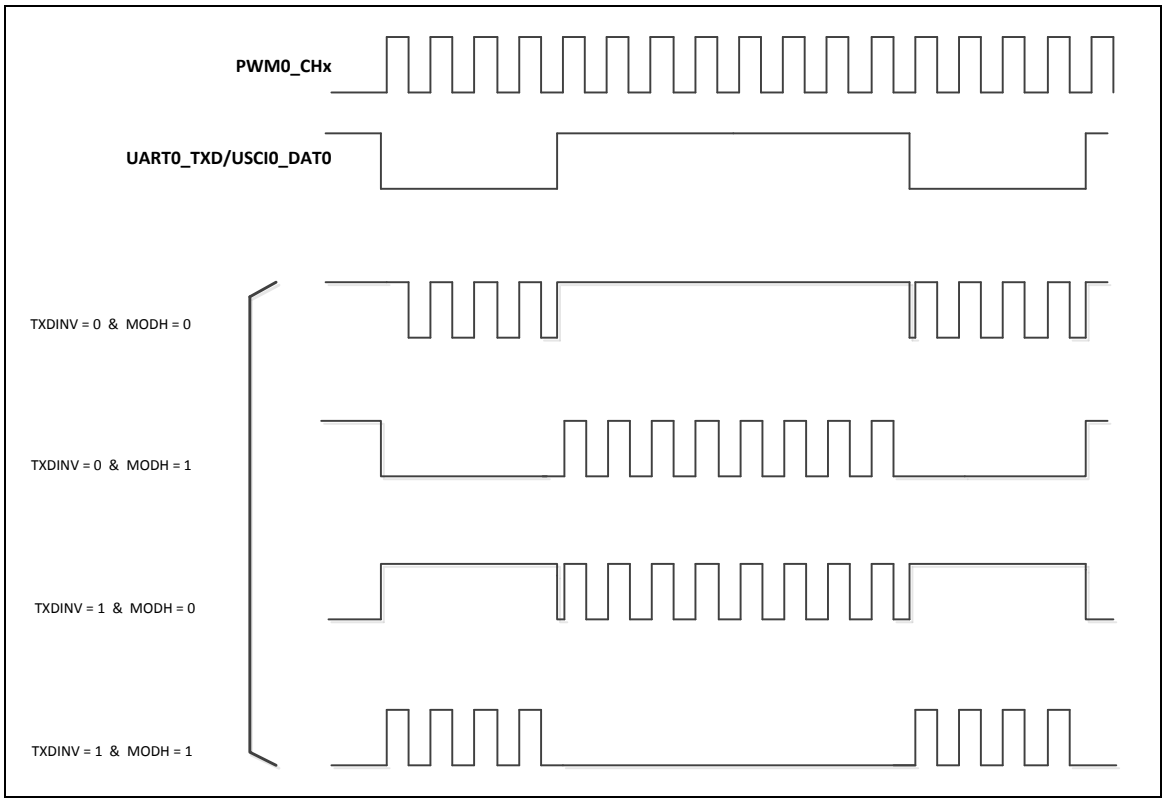


Figure 6.2-11 UART0_TXD/USCI0_DAT0 Modulated with PWM Channel

6.2.11 Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
SYS Base Address: **SYS_BA = 0x4000_0000**				
SYS_PDID	SYS_BA+0x00	R	Part Device Identification Number Register	0xXXXX_XXXX
SYS_RSTSTS	SYS_BA+0x04	R/W	System Reset Status Register	0x0000_0043
SYS_IPRST0	SYS_BA+0x08	R/W	Peripheral Reset Control Register 0	0x0000_0000
SYS_IPRST1	SYS_BA+0x0C	R/W	Peripheral Reset Control Register 1	0x0000_0000
SYS_IPRST2	SYS_BA+0x10	R/W	Peripheral Reset Control Register 2	0x0000_0000
SYS_BODCTL	SYS_BA+0x18	R/W	Brown-out Detector Control Register	0x00XX_038X
SYS_PORCTL	SYS_BA+0x24	R/W	Power-On-reset Controller Register	0x0000_0000
SYS_GPA_MFPL	SYS_BA+0x30	R/W	GPIOA Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPA_MFPH	SYS_BA+0x34	R/W	GPIOA High Byte Multiple Function Control Register	0x0000_0000
SYS_GPB_MFPL	SYS_BA+0x38	R/W	GPIOB Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPB_MFPH	SYS_BA+0x3C	R/W	GPIOB High Byte Multiple Function Control Register	0x0000_0000
SYS_GPC_MFPL	SYS_BA+0x40	R/W	GPIOC Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPC_MFPH	SYS_BA+0x44	R/W	GPIOC High Byte Multiple Function Control Register	0x0000_0000
SYS_GPD_MFPL	SYS_BA+0x48	R/W	GPIOD Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPD_MFPH	SYS_BA+0x4C	R/W	GPIOD High Byte Multiple Function Control Register	0x0000_0000
SYS_GPF_MFPL	SYS_BA+0x58	R/W	GPIOF Low Byte Multiple Function Control Register	0x0000_00ee
SYS_GPF_MFPH	SYS_BA+0x5C	R/W	GPIOF High Byte Multiple Function Control Register	0x0000_0000
SYS_MODCTL	SYS_BA+0xC0	R/W	Modulation Control Register	0x0000_0000
SYS_SRAM_BISTCTL	SYS_BA+0xD0	R/W	System SRAM BIST Test Control Register	0x0000_0000
SYS_SRAM_BISTSTS	SYS_BA+0xD4	R	System SRAM BIST Test Status Register	0x00xx_00xx
SYS_HIRCTRIMCTL	SYS_BA+0xF0	R/W	HIRC Trim Control Register	0x0008_0000
SYS_HIRCTRIMIEN	SYS_BA+0xF4	R/W	HIRC Trim Interrupt Enable Register	0x0000_0000
SYS_HIRCTRIMSTS	SYS_BA+0xF8	R/W	HIRC Trim Interrupt Status Register	0x0000_0000
SYS_REGLCTL	SYS_BA+0x100	R/W	Register Lock Control Register	0x0000_0000
SYS_PORDISAN	SYS_BA+0x1EC	R/W	Analog POR Disable Control Register	0x0000_0000

6.2.12 Register Description

Part Device Identification Number Register (SYS_PDID)

Register	Offset	R/W	Description	Reset Value
SYS_PDID	SYS_BA+0x00	R	Part Device Identification Number Register	0xXXXX_XXXX

[1] Every part number has a unique default reset value.

31	30	29	28	27	26	25	24
PDID							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PDID							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PDID							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PDID							

Bits	Description	
[31:0]	**PDID**	**Part Device Identification Number (Read Only)** This register reflects device part number code. Software can read this register to identify which device is used.

System Reset Status Register (SYS_RSTSTS)

This register provides specific information for software to identify this chip's reset source from last operation.

Register	Offset	R/W	Description	Reset Value
SYS_RSTSTS	SYS_BA+0x04	R/W	System Reset Status Register	0x0000_0043

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							CPULKRF
7	6	5	4	3	2	1	0
CPURF	Reserved	SYSRF	BODRF	LVRF	WDTRF	PINRF	PORF

Bits	Description	
[31:9]	**Reserved**	Reserved.
[8]	**CPULKRF**	**CPU Lockup Reset Flag** 0 = No reset from CPU lockup happened. 1 = The Cortex®-M0 lockup happened and chip is reset. **Note:** Write 1 to clear this bit to 0. **Note2:** When CPU lockup happened under ICE is connected, This flag will set to 1 but chip will not reset.
[7]	**CPURF**	**CPU Reset Flag** The CPU reset flag is set by hardware if software writes CPURST (SYS_IPRST0[1]) 1 to reset Cortex®- M0 Core and Flash Memory Controller (FMC). 0 = No reset from CPU. 1 = The Cortex®-M0 Core and FMC are reset by software setting CPURST to 1. **Note:** Write to clear this bit to 0.
[6]	**Reserved**	Reserved.
[5]	**SYSRF**	**System Reset Flag** The system reset flag is set by the "Reset Signal" from the Cortex®-M0 Core to indicate the previous reset source. 0 = No reset from Cortex®-M0. 1 = The Cortex®- M0 had issued the reset signal to reset the system by writing 1 to the bit SYSRESETREQ(AIRCR[2], Application Interrupt and Reset Control Register, address = 0xE000ED0C) in system control registers of Cortex®-M0 core. **Note:** Write 1 to clear this bit to 0.

Bits	Description	
[4]	**BODRF**	**BOD Reset Flag** The BOD reset flag is set by the “Reset Signal” from the Brown-Out Detector to indicate the previous reset source. 0 = No reset from BOD. 1 = The BOD had issued the reset signal to reset the system. **Note:** Write 1 to clear this bit to 0.
[3]	**LVRF**	**LVR Reset Flag** The LVR reset flag is set by the “Reset Signal” from the Low Voltage Reset Controller to indicate the previous reset source. 0 = No reset from LVR. 1 = LVR controller had issued the reset signal to reset the system. **Note:** Write 1 to clear this bit to 0.
[2]	**WDTRF**	**WDT Reset Flag** The WDT reset flag is set by the “Reset Signal” from the Watchdog Timer or Window Watchdog Timer to indicate the previous reset source. 0 = No reset from watchdog timer or window watchdog timer. 1 = The watchdog timer or window watchdog timer had issued the reset signal to reset the system. **Note1:** Write 1 to clear this bit to 0. **Note2:** Watchdog Timer register RSTF(WDT_CTL[2]) bit is set if the system has been reset by WDT time-out reset. Window Watchdog Timer register WWDTRF(WWDT_STATUS[1]) bit is set if the system has been reset by WWDT time-out reset.
[1]	**PINRF**	**NRESET Pin Reset Flag** The nRESET pin reset flag is set by the “Reset Signal” from the nRESET Pin to indicate the previous reset source. 0 = No reset from nRESET pin. 1 = Pin nRESET had issued the reset signal to reset the system. **Note:** Write 1 to clear this bit to 0.
[0]	**PORF**	**POR Reset Flag** The POR reset flag is set by the “Reset Signal” from the Power-on Reset (POR) Controller or bit CHIPRST (SYS_IPRST0[0]) to indicate the previous reset source. 0 = No reset from POR or CHIPRST. 1 = Power-on Reset (POR) or CHIPRST had issued the reset signal to reset the system. **Note:** Write 1 to clear this bit to 0.

Peripheral Reset Control Register 0 (SYS_IPRST0)

Register	Offset	R/W	Description	Reset Value
SYS_IPRST0	SYS_BA+0x08	R/W	Peripheral Reset Control Register 0	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
CRCRST	Reserved		HDIV_RST	EBIRST	PDMARST	CPURST	CHIPRST

Bits	Description	
[31:8]	**Reserved**	Reserved.
[7]	**CRCRST**	**CRC Calculation Controller Reset (Write Protect)** Set this bit to 1 will generate a reset signal to the CRC calculation controller. User needs to set this bit to 0 to release from the reset state. 0 = CRC calculation controller normal operation. 1 = CRC calculation controller reset. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[6:5]	**Reserved**	Reserved.
[4]	**HDIV_RST**	**HDIV Controller Reset (Write Protect)** Set this bit to 1 will generate a reset signal to the hardware divider. User need to set this bit to 0 to release from the reset state. 0 = Hardware divider controller normal operation. 1 = Hardware divider controller reset. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[3]	**EBIRST**	**EBI Controller Reset (Write Protect)** Set this bit to 1 will generate a reset signal to the EBI. User needs to set this bit to 0 to release from the reset state. 0 = EBI controller normal operation. 1 = EBI controller reset. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[2]	**PDMARST**	**PDMA Controller Reset (Write Protect)** Setting this bit to 1 will generate a reset signal to the PDMA. User needs to set this bit to 0 to release from reset state. 0 = PDMA controller normal operation. 1 = PDMA controller reset. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[1]	**CPURST**	**Processor Core One-shot Reset (Write Protect)** Setting this bit will only reset the processor core and Flash Memory Controller(FMC), and

		this bit will automatically return to 0 after the 2 clock cycles. 0 = Processor core normal operation. 1 = Processor core one-shot reset. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[0]	**CHIPRST**	**Chip One-shot Reset (Write Protect)** Setting this bit will reset the whole chip, including Processor core and all peripherals, and this bit will automatically return to 0 after the 2 clock cycles. The CHIPRST is same as the POR reset, all the chip controllers is reset and the chip setting from flash are also reload. About the difference between CHIPRST and SYSRESETREQ(AIRCR[2]), please refer to section 6.2.2 0 = Chip normal operation. 1 = Chip one-shot reset. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register. Note : reset by powr on reset

Peripheral Reset Control Register 1 (SYS_IPRST1)

Setting these bits 1 will generate asynchronous reset signals to the corresponding module controller. Users need to set these bits to 0 to release corresponding module controller from reset state.

Register	Offset	R/W	Description	Reset Value
SYS_IPRST1	SYS_BA+0x0C	R/W	Peripheral Reset Control Register 1	0x0000_0000

31	30	29	28	27	26	25	24
Reserved			ADCRST	USBDRST	Reserved		
23	22	21	20	19	18	17	16
Reserved					UART2RST	UART1RST	UART0RST
15	14	13	12	11	10	9	8
Reserved		SPI0RST	Reserved			I2C1RST	I2C0RST
7	6	5	4	3	2	1	0
ACMP01RST	Reserved	TMR3RST	TMR2RST	TMR1RST	TMR0RST	GPIORST	Reserved

Bits	Description	
[31:29]	**Reserved**	Reserved.
[28]	**ADCRST**	**ADC Controller Reset** 0 = ADC controller normal operation. 1 = ADC controller reset.
[27]	**USBDRST**	**USBD Controller Reset** 0 = USBD controller normal operation. 1 = USBD controller reset.
[26:19]	**Reserved**	Reserved.
[18]	**UART2RST**	**UART2 Controller Reset** 0 = UART2 controller normal operation. 1 = UART2 controller reset.
[17]	**UART1RST**	**UART1 Controller Reset** 0 = UART1 controller normal operation. 1 = UART1 controller reset.
[16]	**UART0RST**	**UART0 Controller Reset** 0 = UART0 controller normal operation. 1 = UART0 controller reset.
[15:14]	**Reserved**	Reserved.
[13]	**SPI0RST**	**SPI0 Controller Reset** 0 = SPI0 controller normal operation. 1 = SPI0 controller reset.
[12:10]	**Reserved**	Reserved.
[9]	**I2C1RST**	**I2C1 Controller Reset**

		0 = I2C1 controller normal operation. 1 = I2C1 controller reset.
[8]	**I2C0RST**	**I2C0 Controller Reset** 0 = I2C0 controller normal operation. 1 = I2C0 controller reset.
[7]	**ACMP01RST**	**Analog Comparator 0/1 Controller Reset** 0 = Analog Comparator 0/1 controller normal operation. 1 = Analog Comparator 0/1 controller reset.
[6]	**Reserved**	Reserved.
[5]	**TMR3RST**	**Timer3 Controller Reset** 0 = Timer3 controller normal operation. 1 = Timer3 controller reset.
[4]	**TMR2RST**	**Timer2 Controller Reset** 0 = Timer2 controller normal operation. 1 = Timer2 controller reset.
[3]	**TMR1RST**	**Timer1 Controller Reset** 0 = Timer1 controller normal operation. 1 = Timer1 controller reset.
[2]	**TMR0RST**	**Timer0 Controller Reset** 0 = Timer0 controller normal operation. 1 = Timer0 controller reset.
[1]	**GPIORST**	**GPIO Controller Reset** 0 = GPIO controller normal operation. 1 = GPIO controller reset.
[0]	**Reserved**	Reserved.

Peripheral Reset Control Register 2 (SYS_IPRST2)

Setting these bits to 1 will generate asynchronous reset signals to the corresponding module controller. Users need to set these bits to 0 to release corresponding module controller from reset state.

Register	Offset	R/W	Description	Reset Value
SYS_IPRST2	SYS_BA+0x10	R/W	Peripheral Reset Control Register 2	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved						**PWM1RST**	**PWM0RST**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							**USCI0RST**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:18]	**Reserved**	Reserved.
[17]	**PWM1RST**	**PWM1 Controller Reset** 0 = PWM1 controller normal operation. 1 = PWM1 controller reset.
[16]	**PWM0RST**	**PWM0 Controller Reset** 0 = PWM0 controller normal operation. 1 = PWM0 controller reset.
[15:9]	**Reserved**	Reserved.
[8]	**USCI0RST**	**USCI0 Controller Reset** 0 = USCI0 controller normal operation. 1 = USCI0 controller reset.
[7:0]	**Reserved**	Reserved.

Brown-out Detector Control Register (SYS_BODCTL)

Partial of the SYS_BODCTL control registers values are initiated by the flash configuration and partial bits are write-protected bit.

Register	Offset	R/W	Description	Reset Value
SYS_BODCTL	SYS_BA+0x18	R/W	Brown-out Detector Control Register	0x00XX_038X

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			LVRVL	Reserved			BODVL
15	14	13	12	11	10	9	8
Reserved	LVRDGSEL			Reserved	BODDGSEL		
7	6	5	4	3	2	1	0
LVREN	BODOUT	BODLPM	BODIF	BODRSTEN	Reserved		BODEN

Bits	Description	
[31:21]	**Reserved**	Reserved.
[20]	**LVRVL**	**LVR Detector Threshold Voltage Selection (Write Protect)** The default value is set by flash controller user configuration register LVRLVSEL (CONFIG0 [29]). 0 = LVR-Out Detector threshold voltage is 1.6V. 1 = LVR-Out Detector threshold voltage is 1.7V. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register. **Note:** This bit is only for special case. **Note:** reset by powr on reset
[19:17]	**Reserved**	Reserved.
[16]	**BODVL**	**Brown-out Detector Threshold Voltage Selection (Write Protect)** The default value is set by flash controller user configuration register CBOV (CONFIG0 [21]). 0 = Brown-Out Detector threshold voltage is 2.0V. 1 = Brown-Out Detector threshold voltage is 2.5V. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register. Note : reset by powr on reset
[15]	**Reserved**	Reserved.

Bits	Description	
[14:12]	**LVRDGSEL**	**LVR Output De-glitch Time Select (Write Protect)** 000 = Without de-glitch function. 001 = 64 system clock (HCLK). 010 = 128 system clock (HCLK). 011 = 256 system clock (HCLK). 100 = 512 system clock (HCLK). 101 = 1024 system clock (HCLK). 110 = 2048 system clock (HCLK). 111 = 4096 system clock (HCLK). **Note:** These bits are write protected. Refer to the SYS_REGLCTL register.
[11]	**Reserved**	Reserved.
[10:8]	**BODDGSEL**	**Brown-out Detector Output De-glitch Time Select (Write Protect)** 000 = BOD output is sampled by LIRC clock. 001 = 64 system clock (HCLK). 010 = 128 system clock (HCLK). 011 = 256 system clock (HCLK). 100 = 512 system clock (HCLK). 101 = 1024 system clock (HCLK). 110 = 2048 system clock (HCLK). 111 = 4096 system clock (HCLK). **Note:** These bits are write protected. Refer to the SYS_REGLCTL register.
[7]	**LVREN**	**Low Voltage Reset Enable Bit (Write Protect)** The LVR function resets the chip when the input power voltage is lower than LVR circuit setting. LVR function is enabled by default. 0 = Low Voltage Reset function Disabled. 1 = Low Voltage Reset function Enabled. **Note1:** After enabling the bit, the LVR function will be active with 200us delay for LVR output stable (default). **Note2:** This bit is write protected. Refer to the SYS_REGLCTL register.
[6]	**BODOUT**	**Brown-out Detector Output Status** 0 = Brown-out Detector output status is 0. It means the detected voltage is higher than BODVL setting or BODEN is 0. 1 = Brown-out Detector output status is 1. It means the detected voltage is lower than BODVL setting. If the BODEN is 0, BOD function disabled , this bit always responds 0000.
[5]	**BODLPM**	**Brown-out Detector Low Power Mode (Write Protect)** 0 = BOD operate in normal mode (default). 1 = BOD Low Power mode Enabled. **Note1:** The BOD consumes about 100uA in normal mode, the low power mode can reduce the current to about 1/10 but slow the BOD response. **Note2:** This bit is write protected. Refer to the SYS_REGLCTL register.

Bits	Description	
[4]	**BODIF**	**Brown-out Detector Interrupt Flag** 0 = Brown-out Detector does not detect any voltage draft at V_{DD} down through or up through the voltage of BODVL setting. 1 = When Brown-out Detector detects the V_{DD} is dropped down through the voltage of BODVL setting or the V_{DD} is raised up through the voltage of BODVL setting, this bit is set to 1 and the brown-out interrupt is requested if brown-out interrupt is enabled. **Note:** Write 1 to clear this bit to 0.
[3]	**BODRSTEN**	**Brown-out Reset Enable Bit (Write Protect)** The default value is set by flash controller user configuration register CBORST(CONFIG0[20]) bit . 0 = Brown-out "INTERRUPT" function Enabled. 1 = Brown-out "RESET" function Enabled. **Note1:** While the Brown-out Detector function is enabled (BODEN high) and BOD reset function is enabled (BODRSTEN high), BOD will assert a signal to reset chip when the detected voltage is lower than the threshold (BODOUT high). While the BOD function is enabled (BODEN high) and BOD interrupt function is enabled (BODRSTEN low), BOD will assert an interrupt if BODOUT is high. BOD interrupt will keep till to the BODEN set to 0. BOD interrupt can be blocked by disabling the NVIC BOD interrupt or disabling BOD function (set BODEN low). **Note2:** This bit is write protected. Refer to the SYS_REGLCTL register. Note : reset by powr on reset
[2:1]	**Reserved**	Reserved.
[0]	**BODEN**	**Brown-out Detector Enable Bit (Write Protect)** The default value is set by flash controller user configuration register CBODEN (CONFIG0 [19]). 0 = Brown-out Detector function Disabled. 1 = Brown-out Detector function Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register. Note : reset by powr on reset

Power-on Reset Controller Register (SYS_PORCTL)

Register	Offset	R/W	Description	Reset Value
SYS_PORCTL	SYS_BA+0x24	R/W	Power-On-reset Controller Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POROFF							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POROFF							

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15:0]	**POROFF**	**Power-on Reset Enable Bit (Write Protect)** When powered on, the POR circuit generates a reset signal to reset the whole chip function, but noise on the power may cause the POR active again. User can disable internal POR circuit to avoid unpredictable noise to cause chip reset by writing 0x5AA5 to this field. The POR function will be active again when this field is set to another value or chip is reset by other reset source, including: nRESET, Watchdog, LVR reset, BOD reset, ICE reset command and the software-chip reset function. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

GPIOA Low Byte Multiple Function Control Register (SYS_GPA_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPA_MFPL	SYS_BA+0x30	R/W	GPIOA Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PA7MFP				PA6MFP			
23	22	21	20	19	18	17	16
PA5MFP				PA4MFP			
15	14	13	12	11	10	9	8
PA3MFP				PA2MFP			
7	6	5	4	3	2	1	0
PA1MFP				PA0MFP			

Bits	Description	
[31:28]	PA7MFP	PA.7 Multi-function Pin Selection
[27:24]	PA6MFP	PA.6 Multi-function Pin Selection
[23:20]	PA5MFP	PA.5 Multi-function Pin Selection
[19:16]	PA4MFP	PA.4 Multi-function Pin Selection
[15:12]	PA3MFP	PA.3 Multi-function Pin Selection
[11:8]	PA2MFP	PA.2 Multi-function Pin Selection
[7:4]	PA1MFP	PA.1 Multi-function Pin Selection
[3:0]	PA0MFP	PA.0 Multi-function Pin Selection

GPIOA High Byte Multiple Function Control Register (SYS_GPA_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPA_MFPH	SYS_BA+0x34	R/W	GPIOA High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PA15MFP				PA14MFP			
23	22	21	20	19	18	17	16
PA13MFP				PA12MFP			
15	14	13	12	11	10	9	8
PA11MFP				PA10MFP			
7	6	5	4	3	2	1	0
PA9MFP				PA8MFP			

Bits	Description	
[31:28]	PA15MFP	PA.15 Multi-function Pin Selection
[27:24]	PA14MFP	PA.14 Multi-function Pin Selection
[23:20]	PA13MFP	PA.13 Multi-function Pin Selection
[19:16]	PA12MFP	PA.12 Multi-function Pin Selection
[15:12]	PA11MFP	PA.11 Multi-function Pin Selection
[11:8]	PA10MFP	PA.10 Multi-function Pin Selection
[7:4]	PA9MFP	PA.9 Multi-function Pin Selection
[3:0]	PA8MFP	PA.8 Multi-function Pin Selection

GPIOB Low Byte Multiple Function Control Register (SYS_GPB_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPB_MFPL	SYS_BA+0x38	R/W	GPIOB Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PB7MFP				PB6MFP			
23	22	21	20	19	18	17	16
PB5MFP				PB4MFP			
15	14	13	12	11	10	9	8
PB3MFP				PB2MFP			
7	6	5	4	3	2	1	0
PB1MFP				PB0MFP			

Bits	Description	
[31:28]	PB7MFP	PB.7 Multi-function Pin Selection
[27:24]	PB6MFP	PB.6 Multi-function Pin Selection
[23:20]	PB5MFP	PB.5 Multi-function Pin Selection
[19:16]	PB4MFP	PB.4 Multi-function Pin Selection
[15:12]	PB3MFP	PB.3 Multi-function Pin Selection
[11:8]	PB2MFP	PB.2 Multi-function Pin Selection
[7:4]	PB1MFP	PB.1 Multi-function Pin Selection
[3:0]	PB0MFP	PB.0 Multi-function Pin Selection

GPIOB High Byte Multiple Function Control Register (SYS_GPB_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPB_MFPH	SYS_BA+0x3C	R/W	GPIOB High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PB15MFP				PB14MFP			
23	22	21	20	19	18	17	16
PB13MFP				PB12MFP			
15	14	13	12	11	10	9	8
PB11MFP				PB10MFP			
7	6	5	4	3	2	1	0
PB9MFP				PB8MFP			

Bits	Description	
[31:28]	PB15MFP	PB.15 Multi-function Pin Selection
[27:24]	PB14MFP	PB.14 Multi-function Pin Selection
[23:20]	PB13MFP	PB.13 Multi-function Pin Selection
[19:16]	PB12MFP	PB.12 Multi-function Pin Selection
[15:12]	PB11MFP	PB.11 Multi-function Pin Selection
[11:8]	PB10MFP	PB.10 Multi-function Pin Selection
[7:4]	PB9MFP	PB.9 Multi-function Pin Selection
[3:0]	PB8MFP	PB.8 Multi-function Pin Selection

GPIOC Low Byte Multiple Function Control Register (SYS_GPC_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPC_MFPL	SYS_BA+0x40	R/W	GPIOC Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PC7MFP				PC6MFP			
23	22	21	20	19	18	17	16
PC5MFP				PC4MFP			
15	14	13	12	11	10	9	8
PC3MFP				PC2MFP			
7	6	5	4	3	2	1	0
PC1MFP				PC0MFP			

Bits	Description	
[31:28]	PC7MFP	PC.7 Multi-function Pin Selection
[27:24]	PC6MFP	PC.6 Multi-function Pin Selection
[23:20]	PC5MFP	PC.5 Multi-function Pin Selection
[19:16]	PC4MFP	PC.4 Multi-function Pin Selection
[15:12]	PC3MFP	PC.3 Multi-function Pin Selection
[11:8]	PC2MFP	PC.2 Multi-function Pin Selection
[7:4]	PC1MFP	PC.1 Multi-function Pin Selection
[3:0]	PC0MFP	PC.0 Multi-function Pin Selection

GPIOC High Byte Multiple Function Control Register (SYS_GPC_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPC_MFPH	SYS_BA+0x44	R/W	GPIOC High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PC15MFP				PC14MFP			
23	22	21	20	19	18	17	16
PC13MFP				PC12MFP			
15	14	13	12	11	10	9	8
PC11MFP				PC10MFP			
7	6	5	4	3	2	1	0
PC9MFP				PC8MFP			

Bits	Description	
[31:28]	PC15MFP	PC.15 Multi-function Pin Selection
[27:24]	PC14MFP	PC.14 Multi-function Pin Selection
[23:20]	PC13MFP	PC.13 Multi-function Pin Selection
[19:16]	PC12MFP	PC.12 Multi-function Pin Selection
[15:12]	PC11MFP	PC.11 Multi-function Pin Selection
[11:8]	PC10MFP	PC.10 Multi-function Pin Selection
[7:4]	PC9MFP	PC.9 Multi-function Pin Selection
[3:0]	PC8MFP	PC.8 Multi-function Pin Selection

GPIOD Low Byte Multiple Function Control Register (SYS_GPD_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPD_MFPL	SYS_BA+0x48	R/W	GPIOD Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PD7MFP				PD6MFP			
23	22	21	20	19	18	17	16
PD5MFP				PD4MFP			
15	14	13	12	11	10	9	8
PD3MFP				PD2MFP			
7	6	5	4	3	2	1	0
PD1MFP				PD0MFP			

Bits	Description	
[31:28]	PD7MFP	PD.7 Multi-function Pin Selection
[27:24]	PD6MFP	PD.6 Multi-function Pin Selection
[23:20]	PD5MFP	PD.5 Multi-function Pin Selection
[19:16]	PD4MFP	PD.4 Multi-function Pin Selection
[15:12]	PD3MFP	PD.3 Multi-function Pin Selection
[11:8]	PD2MFP	PD.2 Multi-function Pin Selection
[7:4]	PD1MFP	PD.1 Multi-function Pin Selection
[3:0]	PD0MFP	PD.0 Multi-function Pin Selection

GPIOD High Byte Multiple Function Control Register (SYS_GPD_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPD_MFPH	SYS_BA+0x4C	R/W	GPIOD High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PD15MFP				PD14MFP			
23	22	21	20	19	18	17	16
PD13MFP				PD12MFP			
15	14	13	12	11	10	9	8
PD11MFP				PD10MFP			
7	6	5	4	3	2	1	0
PD9MFP				PD8MFP			

Bits	Description	
[31:28]	PD15MFP	PD.15 Multi-function Pin Selection
[27:24]	PD14MFP	PD.14 Multi-function Pin Selection
[23:20]	PD13MFP	PD.13 Multi-function Pin Selection
[19:16]	PD12MFP	PD.12 Multi-function Pin Selection
[15:12]	PD11MFP	PD.11 Multi-function Pin Selection
[11:8]	PD10MFP	PD.10 Multi-function Pin Selection
[7:4]	PD9MFP	PD.9 Multi-function Pin Selection
[3:0]	PD8MFP	PD.8 Multi-function Pin Selection

GPIOF Low Byte Multiple Function Control Register (SYS_GPF_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPF_MFPL	SYS_BA+0x58	R/W	GPIOF Low Byte Multiple Function Control Register	0x0000_00ee

31	30	29	28	27	26	25	24
PF7MFP				PF6MFP			
23	22	21	20	19	18	17	16
PF5MFP				PF4MFP			
15	14	13	12	11	10	9	8
PF3MFP				PF2MFP			
7	6	5	4	3	2	1	0
PF1MFP				PF0MFP			

Bits	Description	
[31:28]	PF7MFP	PF.7 Multi-function Pin Selection
[27:24]	PF6MFP	PF.6 Multi-function Pin Selection
[23:20]	PF5MFP	PF.5 Multi-function Pin Selection
[19:16]	PF4MFP	PF.4 Multi-function Pin Selection
[15:12]	PF3MFP	PF.3 Multi-function Pin Selection
[11:8]	PF2MFP	PF.2 Multi-function Pin Selection
[7:4]	PF1MFP	PF.1 Multi-function Pin Selection
[3:0]	PF0MFP	PF.0 Multi-function Pin Selection

GPIOF High Byte Multiple Function Control Register (SYS_GPF_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPF_MFPH	SYS_BA+0x5C	R/W	GPIOF High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PF15MFP				PF14MFP			
23	22	21	20	19	18	17	16
PF13MFP				PF12MFP			
15	14	13	12	11	10	9	8
PF11MFP				PF10MFP			
7	6	5	4	3	2	1	0
PF9MFP				PF8MFP			

Bits	Description	
[31:28]	PF15MFP	PF.15 Multi-function Pin Selection
[27:24]	PF14MFP	PF.14 Multi-function Pin Selection
[23:20]	PF13MFP	PF.13 Multi-function Pin Selection
[19:16]	PF12MFP	PF.12 Multi-function Pin Selection
[15:12]	PF11MFP	PF.11 Multi-function Pin Selection
[11:8]	PF10MFP	PF.10 Multi-function Pin Selection
[7:4]	PF9MFP	PF.9 Multi-function Pin Selection
[3:0]	PF8MFP	PF.8 Multi-function Pin Selection

Modulation Control Register (SYS_MODCTL)

Register	Offset	R/W	Description	Reset Value
SYS_MODCTL	SYS_BA+0xC0	R/W	Modulation Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
MODPWMSEL				Reserved		MODH	MODEN

Bits	Description	
[31:8]	**Reserved**	Reserved.
[7:4]	**MODPWMSEL**	**PWM0 Channel Select for Modulation** Select the PWM0 channel to modulate with the UART0_TXD or USCI0_DAT0. 0000: PWM0 Channel 0 modulate with UART0_TXD. 0001: PWM0 Channel 1 modulate with UART0_TXD. 0010: PWM0 Channel 2 modulate with UART0_TXD. 0011: PWM0 Channel 3 modulete with UART0_TXD. 0100: PWM0 Channel 4 modulete with UART0_TXD. 0101: PWM0 Channel 5 modulete with UART0_TXD. 0110: Reserved. 0111: Reserved. 1000: PWM0 Channel 0 modulate with USCI0_DAT0. 1001: PWM0 Channel 1 modulate with USCI0_DAT0. 1010: PWM0 Channel 2 modulate with USCI0_DAT0. 1011: PWM0 Channel 3 modulete with USCI0_DAT0. 1100: PWM0 Channel 4 modulete with USCI0_DAT0. 1101: PWM0 Channel 5 modulete with USCI0_DAT0. 1110: Reserved. 1111: Reserved. **Note:** This bis is valid while MODEN (SYS_MODCTL[0]) is set to 1.
[3:2]	**Reserved**	Reserved.
[1]	**MODH**	**Modulation at Data High** Select modulation pulse(PWM0) at high or low of UART0_TXD or USCI0_DAT0 0: Modulation pulse at UART0_TXD low or USCI0_DAT0 low. 1: Modulation pulse at UART0_TXD high or USCI0_DAT0 high.
[0]	**MODEN**	**Modulation Function Enable Bit** This bit enables modulation funcion by modulating with PWM0 channel output and

		USCI0(USCI0_DAT0) or UART0(UART0_TXD) output. 0 = Modulation Function Disabled. 1 = Modulation Function Enabled.

System SRAM BIST Test Control Register (SYS_SRAM_BISTCTL)

Register	Offset	R/W	Description	Reset Value
SYS_SRAM_BISTCTL	SYS_BA+0xD0	R/W	System SRAM BIST Test Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PDMABIST	Reserved		USBBIST	Reserved			SRBIST

Bits	Description	
[31:8]	**Reserved**	Reserved.
[7]	**PDMABIST**	**PDMA BIST Enable Bit (Write Protect)** This bit enables BIST test for PDMA RAM 0 = system PDMA BIST Disabled. 1 = system PDMA BIST Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[6:5]	**Reserved**	Reserved.
[4]	**USBBIST**	**USB BIST Enable Bit (Write Protect)** This bit enables BIST test for USB RAM 0 = system USB BIST Disabled. 1 = system USB BIST Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[3:0]	**Reserved**	Reserved.

System SRAM BIST Test Status Register (SYS_SRAM_BISTSTS)

Register	Offset	R/W	Description	Reset Value
SYS_SRAM_BISTSTS	SYS_BA+0xD4	R	System SRAM BIST Test Status Register	0x00xx_00xx

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
PDMAEND	Reserved		USBBEND	Reserved			SRBEND
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PDMABISTF	Reserved		USBBEF	Reserved			SRBISTEF

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23]	**PDMAEND**	**PDMA SRAM BIST Test Finish** 0 = PDMA SRAM BIST is active. 1 = PDMA SRAM BIST test finish.
[22:21]	**Reserved**	Reserved.
[20]	**USBBEND**	**USB SRAM BIST Test Finish** 0 = USB SRAM BIST is active. 1 = USB SRAM BIST test finish.
[19:8]	**Reserved**	Reserved.
[7]	**PDMABISTF**	**PDMA SRAM BIST Failed Flag** 0 = PDMA SRAM BIST pass. 1 = PDMA SRAM BIST failed.
[6:5]	**Reserved**	Reserved.
[4]	**USBBEF**	**USB SRAM BIST Fail Flag** 0 = USB SRAM BIST test pass. 1 = USB SRAM BIST test fail.
[3:0]	**Reserved**	Reserved.

HIRC Trim Control Register (SYS_HIRCTRIMCTL)

Register	Offset	R/W	Description	Reset Value
SYS_HIRCTRIMCTL	SYS_BA+0xF0	R/W	HIRC Trim Control Register	0x0008_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			BOUNDARY				
15	14	13	12	11	10	9	8
Reserved					REFCKSEL	BOUNDEN	CESTOPEN
7	6	5	4	3	2	1	0
RETRYCNT		LOOPSEL		Reserved		FREQSEL	

Bits	Description	
[31:21]	**Reserved**	Reserved.
[20:16]	**BOUNDARY**	**Boundary Selection** Fill the boundary range from 0x1 to 0x1F, 0x0 is reserved. **Note:** This field is effective only when the BOUNDEN(SYS_HIRCTRIMCTL[9]) is enable.
[15:11]	**Reserved**	Reserved.
[10]	**REFCKSEL**	**Reference Clock Selection** 0 = HIRC trim reference clock is from LXT (32.768 kHz). 1 = HIRC trim reference clock is from internal USB synchronous mode. **Note1:** HIRC trim reference clock supports LXT or internal USB synchronous mode depending on the chip spec. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information. **Note2:** If there is no reference clock (LXT or internal USB synchronous mode) when the rc_trim is enabled, **CLKERIF (SYS_HIRCTRIMCTL[2]) will be set to 1.**
[9]	**BOUNDEN**	**Boundary Enable Bit** 0 = Boundary function Disabled. 1 = Boundary function Enabled.
[8]	**CESTOPEN**	**Clock Error Stop Enable Bit** 0 = The trim operation is keep going if clock is inaccuracy. 1 = The trim operation is stopped if clock is inaccuracy.
[7:6]	**RETRYCNT**	**Trim Value Update Limitation Count** This field defines that how many times the auto trim circuit will try to update the HIRC trim value before the frequency of HIRC locked. Once the HIRC locked, the internal trim value update counter will be reset. If the trim value update counter reached this limitation value and frequency of HIRC still doesn't lock, the auto trim operation will be disabled and FREQSEL will be cleared to 00. 00 = Trim retry count limitation is 64 loops. 01 = Trim retry count limitation is 128 loops.

		10 = Trim retry count limitation is 256 loops. 11 = Trim retry count limitation is 512 loops.
[5:4]	**LOOPSEL**	**Trim Calculation Loop Selection** This field defines that trim value calculation is based on how many reference clocks. 00 = Trim value calculation is based on average difference in 4 clocks of reference clock. 01 = Trim value calculation is based on average difference in 8 clocks of reference clock. 10 = Trim value calculation is based on average difference in 16 clocks of reference clock. 11 = Trim value calculation is based on average difference in 32 clocks of reference clock. **Note:** For example, if LOOPSEL is set as 00, auto trim circuit will calculate trim value based on the average frequency difference in 4 clocks of reference clock.
[3:2]	**Reserved**	Reserved.
[1:0]	**FREQSEL**	**Trim Frequency Selection** This field indicates the target frequency of 48 MHz internal high speed RC oscillator (HIRC) auto trim. During auto trim operation, if clock error detected with CESTOPEN is set to 1 or trim retry limitation count reached, this field will be cleared to 00 automatically. 00 = Disable HIRC auto trim function. 01 = Enable HIRC auto trim function and trim HIRC to 48 MHz. 10 = Reserved.. 11 = Reserved.

HIRC Trim Interrupt Enable Register (SYS_HIRCTRIMIEN)

Register	Offset	R/W	Description	Reset Value
SYS_HIRCTRIMIEN	SYS_BA+0xF4	R/W	HIRC Trim Interrupt Enable Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					CLKEIEN	TFALIEN	Reserved

Bits	Description	
[31:3]	**Reserved**	Reserved.
[2]	**CLKEIEN**	**Clock Error Interrupt Enable Bit** This bit controls if CPU would get an interrupt while clock is inaccuracy during auto trim operation. If this bit is set to1, and CLKERRIF(SYS_HIRCTRIMSTS[2]) is set during auto trim operation, an interrupt will be triggered to notify the clock frequency is inaccuracy. 0 = Disable CLKERRIF(SYS_HIRCTRIMSTS[2]) status to trigger an interrupt to CPU. 1 = Enable CLKERRIF(SYS_HIRCTRIMSTS[2]) status to trigger an interrupt to CPU.
[1]	**TFALIEN**	**Trim Failure Interrupt Enable Bit** This bit controls if an interrupt will be triggered while HIRC trim value update limitation count reached and HIRC frequency still not locked on target frequency set by FREQSEL(SYS_HIRCTRIMCTL[1:0]). If this bit is high and TFAILIF(SYS_HIRCTRIMSTS[1]) is set during auto trim operation, an interrupt will be triggered to notify that HIRC trim value update limitation count was reached. 0 = Disable TFAILIF(SYS_HIRCTRIMSTS[1]) status to trigger an interrupt to CPU. 1 = Enable TFAILIF(SYS_HIRCTRIMSTS[1]) status to trigger an interrupt to CPU.
[0]	**Reserved**	Reserved.

HIRC Trim Interrupt Status Register (SYS_HIRCTRIMSTS)

Register	Offset	R/W	Description	Reset Value
SYS_HIRCTRIMSTS	SYS_BA+0xF8	R/W	HIRC Trim Interrupt Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				OVBDIF	CLKERIF	TFAILIF	FREQLOCK

Bits	Description	
[31:4]	**Reserved**	Reserved.
[3]	**OVBDIF**	**Over Boundary Status** When the over boundary function is set, if there occurs the over boundary condition, this flag will be set. 0 = Over boundary coundition did not occur. 1 = Over boundary coundition occurred. **Note:** Write 1 to clear this flag.
[2]	**CLKERIF**	**Clock Error Interrupt Status** When the frequency relation between reference clock (LXT or USB sync signals) and 48 MHz internal high speed RC oscillator (HIRC) is shift larger to unreasonable value, this bit will be set and to be an indicate that clock frequency is inaccuracy Once this bit is set to 1, the auto trim operation stopped and FREQSEL(SYS_HIRCTRIMCTL[1:0]) will be cleared to 00 by hardware automatically if CESTOPEN(SYS_HIRCTRIMCTL[8]) is set to 1. If this bit is set and CLKEIEN(SYS_HIRCTIEN[2]) is high, an interrupt will be triggered to notify the clock frequency is inaccuracy. Write 1 to clear this to 0. 0 = Clock frequency is accuracy. 1 = Clock frequency is inaccuracy. **Note** : reset by powr on reset
[1]	**TFAILIF**	**Trim Failure Interrupt Status** This bit indicates that HIRC trim value update limitation count reached and the HIRC clock frequency still doesn't be locked. Once this bit is set, the auto trim operation stopped and FREQSEL(SYS_HIRCTRIMCTL[1:0]) will be cleared to 00 by hardware automatically. If this bit is set and TFAILIEN(SYS_HIRCIEN[1]) is high, an interrupt will be triggered to notify that HIRC trim value update limitation count was reached. Write 1 to clear this to 0. 0 = Trim value update limitation count does not reach. 1 = Trim value update limitation count reached and HIRC frequency still not locked. **Note** : reset by powr on reset
[0]	**FREQLOCK**	**HIRC Frequency Lock Status**

		This bit indicates the HIRC frequency is locked. This is a status bit and doesn't trigger any interrupt Write 1 to clear this to 0. This bit will be set automatically, if the frequecy is lock and the RC_TRIM is enabled. 0 = The internal high-speed oscillator frequency doesn't lock at 48 MHz yet. 1 = The internal high-speed oscillator frequency locked at 48 MHz. **Note** : Reset by powr on reset.

Register Lock Control Register (SYS_REGLCTL)

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, user can check the protection disable bit at address 0x4000_0100 bit0, 1 is protection disable, and 0 is protection enable. Then user can update the target protected register value and then write any data to the address “0x4000_0100” to enable register protection.

This register is writen to disable/enable register protection and read for the REGLCTL status.

Register	Offset	R/W	Description	Reset Value
SYS_REGLCTL	SYS_BA+0x100	R/W	Register Lock Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REGLCTL							

Bits	Description	
[31:8]	**Reserved**	Reserved.
[7:0]	**REGLCTL**	**Register Lock Control Code (Write Only)** Some registers have write-protection function. Writing these registers have to disable the protected function by writing the sequence value “59h”, “16h”, “88h” to this field. After this sequence is completed, the REGLCTL bit will be set to 1 and write-protection registers can be normal write. **REGLCTL[0]** **Register Lock Control Disable Index (Read Only)** 0 = Write-protection Enabled for writing protected registers. Any write to the protected register is ignored. 1 = Write-protection Disabled for writing protected registers.

Analog POR Disable Control Register (SYS_PORDISAN)

Register	Offset	R/W	Description	Reset Value
SYS_PORDISAN	SYS_BA+0x1EC	R/W	Analog POR Disable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
POROFFAN							
7	6	5	4	3	2	1	0
POROFFAN							

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15:0]	**POROFFAN**	**Power-on Reset Enable Bit (Write Protect)** After powered on, User can turn off internal analog POR circuit to save power by writing 0x5AA5 to this field. The analog POR circuit will be active again when this field is set to another value or chip is reset by other reset source, including: nRESET, Watchdog, LVR reset, BOD reset, ICE reset command and the software-chip reset function. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

6.2.13 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “Arm® Cortex®-M0 Technical Reference Manual” and “Arm® v6-M Architecture Reference Manual”.

6.2.13.1 System Timer Control Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
SYST Base Address: **SCS_BA = 0xE000_E000**				
SYST_CTRL	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000
SYST_LOAD	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX
SYST_VAL	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

6.2.13.2 System Timer Control Register Description

SysTick Control and Status Register (SYST_CTRL)

Register	Offset	R/W	Description	Reset Value
SYST_CTRL	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							**COUNTFLAG**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					**CLKSRC**	**TICKINT**	**ENABLE**

Bits	Description	
[31:17]	**Reserved**	Reserved.
[16]	**COUNTFLAG**	**System Tick Counter Flag** Returns 1 if timer counted to 0 since last time this register was read. COUNTFLAG is set by a count transition from 1 to 0. COUNTFLAG is cleared on read or by a write to the Current Value register.
[15:3]	**Reserved**	Reserved.
[2]	**CLKSRC**	**System Tick Clock Source Selection** 0 = Clock source is the (optional) external reference clock. 1 = Core clock used for SysTick.
[1]	**TICKINT**	**System Tick Interrupt Enabled** 0 = Counting down to 0 does not cause the SysTick exception to be pended. Software can use COUNTFLAG to determine if a count to zero has occurred. 1 = Counting down to 0 will cause the SysTick exception to be pended. Clearing the SysTick current value register by a register write in software will not cause SysTick to be pended.
[0]	**ENABLE**	**System Tick Counter Enabled** 0 = Counter Disabled. 1 = Counter will operate in a multi-shot manner.

SysTick Reload Value Register (SYST_LOAD)

Register	Offset	R/W	Description	Reset Value
SYST_LOAD	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RELOAD							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RELOAD							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RELOAD							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**RELOAD**	**System Tick Reload Value** The value to load into the Current Value register when the counter reaches 0.

SysTick Current Value Register (SYST_VAL)

Register	Offset	R/W	Description	Reset Value
SYST_VAL	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CURRENT							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CURRENT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURRENT							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**CURRENT**	**System Tick Current Value** Current counter value. This is the value of the counter at the time it is sampled. The counter does not provide read-modify-write protection. The register is write-clear. A software write of any value will clear the register to 0.

6.2.14 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "Arm® Cortex®-M0 Technical Reference Manual" and "Arm® v6-M Architecture Reference Manual".

6.2.14.1 Exception Model and System Interrupt Map

Table 6.2-9 lists the exception model supported by the M031 series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable

SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-9 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-Out low voltage detected interrupt
17	1	WDT_INT	Watchdog Timer interrupt
18	2	EINT024	External interrupt fromEINT0,2,4.
19	3	EINT135	External interrupt fromEINT1.3.5
20	4	GPAB_INT	External interrupt from PA, PB pin
21	5	GPCDEF_INT	External interrupt from PC, PB pin
22	6	PWM0_INT	PWM0 interrupt
23	7	PWM1_INT	PWM1 interrupt
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART02_INT	UART0,2 interrupt
29	13	UART1_INT	UART1 interrupt
30	14	SPI0_INT	SPI0 interrupt
31	15	Reserved	Reserved
32	16	Reserved	Reserved
33	17	Reserved	Reserved
34	18	I2C0_INT	I2C0 interrupt
35	19	I2C1_INT	I2C1 interrupt
36	20	Reserved	Reserved
37	21	Reserved	Reserved
38	22	USCI0	USCI0 interrupt
39	23	USBD_INT	USB device interrupt
40	24	Reserved	Reserved
41	25	ACMP01_INT	ACMP0 and ACMP1 interrupt
42	26	PDMA_INT	PDMA interrupt

43	27	Reserved	Reserved
44	28	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
45	29	ADC_INT	ADC interrupt
46	30	CLKFAIL	Clock fail detected or IRC Auto Trim interrupt
47	31	Reserved	Reserved

Table 6.2-10 Interrupt Number Table

6.2.14.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For Armv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6.2-11 Vector Figure Format

6.2.14.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.14.4 NVIC Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NVIC Base Address: **NVIC_BA = 0xE000_E100**				
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-enable Control Register	0x0000_0000
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-enable Control Register	0x0000_0000
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-pending Control Register	0x0000_0000
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-pending Control Register	0x0000_0000
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ31 Active Bit Register	0x0000_0000
NVIC_IPRn **n=0,1..7**	0xE000E400 +0x4*n	R/W	IRQ0 ~ IRQ31 Priority Control Register	0x0000_0000
STIR	0xE000EF00	R/W	Software Trigger Interrupt Registers	0x0000_0000

IRQ0 ~ IRQ31 Set-enable Control Register (NVIC_ISER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ31 Clear-enable Control Register (NVIC_ICER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ31 Set-pending Control Register (NVIC_ISPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0 registers force interrupts into the pending state, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ31 Clear-pending Control Register (NVIC_ICPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0 registers remove the pending state from interrupts, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ31 Active Bit Register (NVIC_IABR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ31 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0 registers indicate which interrupts are active. 0 = interrupt not active. 1 = interrupt active.

IRQ0 ~ IRQ31 Interrupt Priority Register (NVIC_IPRn)

Register	Offset	R/W	Description	Reset Value
NVIC_IPRn **n=0,1..7**	0xE000E400 +0x4*n	R/W	IRQ0 ~ IRQ31 Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_4n_3		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_4n_2		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_4n_1		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_4n_0		**Reserved**					

Bits	Description	
[31:30]	**PRI_4n_3**	**Priority of IRQ_4n+3** "0" denotes the highest priority and "3" denotes the lowest priority
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_4n_2**	**Priority of IRQ_4n+2** "0" denotes the highest priority and "3" denotes the lowest priority
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_4n_1**	**Priority of IRQ_4n+1** "0" denotes the highest priority and "3" denotes the lowest priority
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_4n_0**	**Priority of IRQ_4n+0** "0" denotes the highest priority and "3" denotes the lowest priority
[5:0]	**Reserved**	Reserved.

Software Trigger Interrupt Register (STIR)

Register	Offset	R/W	Description	Reset Value
STIR	0xE000EF00	R/W	Software Trigger Interrupt Registers	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							**INTID**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTID							

Bits	Description	
[31:9]	**Reserved**	Reserved.
[8:0]	**INTID**	**Interrupt ID** Write to the STIR To Generate An Interrupt from Software When the USERSETMPEND bit in the SCR is set to 1, unprivileged software can access the STIR Interrupt ID of the interrupt to trigger, in the range 0-31. For example, a value of 0x03 specifies interrupt IRQ3.

6.2.14.5 NMI Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NMI Base Address: **NMI_BA = 0x4000_0300**				
NMIEN	NMI_BA+0x00	R/W	NMI Source Interrupt Enable Register	0x0000_0000
NMISTS	NMI_BA+0x04	R	NMI Source Interrupt Status Register	0x0000_0000

NMI Source Interrupt Enable Register (NMIEN)

Register	Offset	R/W	Description	Reset Value
NMIEN	NMI_BA+0x00	R/W	NMI Source Interrupt Enable Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UART1_INT	**UART0_INT**	**EINT5**	**EINT4**	**EINT3**	**EINT2**	**EINT1**	**EINT0**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			**CLKFAIL**	**Reserved**	**PWRWU_INT**	**IRC_INT**	**BODOUT**

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15]	**UART1_INT**	**UART1 NMI Source Enable (Write Protect)** 0 = UART1 NMI source Disabled. 1 = UART1 NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[14]	**UART0_INT**	**UART0 NMI Source Enable (Write Protect)** 0 = UART0 NMI source Disabled. 1 = UART0 NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[13]	**EINT5**	**External Interrupt From PB.7 or PF.14 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PB.7 or PF.14 pin NMI source Disabled. 1 = External interrupt from PB.7 or PF.14 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[12]	**EINT4**	**External Interrupt From PA.8, PB.6 or PF.15 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PA.8, PB.6 or PF.15 pin NMI source Disabled. 1 = External interrupt from PA.8, PB.6 or PF.15 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[11]	**EINT3**	**External Interrupt From PB.2 or PC.7 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PB.2 or PC.7 pin NMI source Disabled. 1 = External interrupt from PB.2 or PC.7 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[10]	**EINT2**	**External Interrupt From PB.3 or PC.6 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PB.3 or PC.6 pin NMI source Disabled. 1 = External interrupt from PB.3 or PC.6 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[9]	**EINT1**	**External Interrupt From PA.7, PB.4 or PD.15 Pin NMI Source Enable (Write Protect)**

		0 = External interrupt from PA.7, PB.4 or PD.15 pin NMI source Disabled. 1 = External interrupt from PA.7, PB.4 or PD.15 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[8]	**EINT0**	**External Interrupt From PA.6 or PB.5 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PA.6 or PB.5 pin NMI source Disabled. 1 = External interrupt from PA.6 or PB.5 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[7:5]	**Reserved**	Reserved.
[4]	**CLKFAIL**	**Clock Fail Detected and IRC Auto Trim Interrupt NMI Source Enable (Write Protect)** 0 = Clock fail detected and IRC Auto Trim interrupt NMI source Disabled. 1 = Clock fail detected and IRC Auto Trim interrupt NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[3]	**Reserved**	Reserved.
[2]	**PWRWU_INT**	**Power-down Mode Wake-up NMI Source Enable (Write Protect)** 0 = Power-down mode wake-up NMI source Disabled. 1 = Power-down mode wake-up NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[1]	**IRC_INT**	**IRC TRIM NMI Source Enable (Write Protect)** 0 = IRC TRIM NMI source Disabled. 1 = IRC TRIM NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[0]	**BODOUT**	**BOD NMI Source Enable (Write Protect)** 0 = BOD NMI source Disabled. 1 = BOD NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

NMI Source Interrupt Status Register (NMISTS)

Register	Offset	R/W	Description	Reset Value
NMISTS	NMI_BA+0x04	R	NMI Source Interrupt Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
UART1_INT	UART0_INT	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
7	6	5	4	3	2	1	0
Reserved			CLKFAIL	Reserved	PWRWU_INT	IRC_INT	BODOUT

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15]	**UART1_INT**	**UART1 Interrupt Flag (Read Only)** 0 = UART1 interrupt is deasserted. 1 = UART1 interrupt is asserted.
[14]	**UART0_INT**	**UART0 Interrupt Flag (Read Only)** 0 = UART1 interrupt is deasserted. 1 = UART1 interrupt is asserted.
[13]	**EINT5**	**External Interrupt From PB.7 or PF.14 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PB.7 or PF.14 interrupt is deasserted. 1 = External Interrupt from PB.7 or PF.14 interrupt is asserted.
[12]	**EINT4**	**External Interrupt From PA.8, PB.6 or PF.15 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PA.8, PB.6 or PF.15 interrupt is deasserted. 1 = External Interrupt from PA.8, PB.6 or PF.15 interrupt is asserted.
[11]	**EINT3**	**External Interrupt From PB.2 or PC.7 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PB.2 or PC.7 interrupt is deasserted. 1 = External Interrupt from PB.2 or PC.7 interrupt is asserted.
[10]	**EINT2**	**External Interrupt From PB.3 or PC.6 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PB.3 or PC.6 interrupt is deasserted. 1 = External Interrupt from PB.3 or PC.6 interrupt is asserted.
[9]	**EINT1**	**External Interrupt From PA.7, PB.4 or PD.15 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PA.7, PB.4 or PD.15 interrupt is deasserted. 1 = External Interrupt from PA.7, PB.4 or PD.15 interrupt is asserted.
[8]	**EINT0**	**External Interrupt From PA.6 or PB.5 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PA.6 or PB.5 interrupt is deasserted. 1 = External Interrupt from PA.6 or PB.5 interrupt is asserted.

[7:5]	**Reserved**	Reserved.
[4]	**CLKFAIL**	**Clock Fail Detected or IRC Auto Trim Interrupt Flag (Read Only)** 0 = Clock fail detected or IRC Auto Trim interrupt is deasserted. 1 = Clock fail detected or IRC Auto Trim interrupt is asserted.
[3]	**Reserved**	Reserved.
[2]	**PWRWU_INT**	**Power-down Mode Wake-up Interrupt Flag (Read Only)** 0 = Power-down mode wake-up interrupt is deasserted. 1 = Power-down mode wake-up interrupt is asserted.
[1]	**IRC_INT**	**IRC TRIM Interrupt Flag (Read Only)** 0 = HIRC TRIM interrupt is deasserted. 1 = HIRC TRIM interrupt is asserted.
[0]	**BODOUT**	**BOD Interrupt Flag (Read Only)** 0 = BOD interrupt is deasserted. 1 = BOD interrupt is asserted.

6.2.15 System Control Register

The Cortex®-M0 status and operation mode control are managed by System Control Registers. Including CPUID, Cortex®-M0 interrupt priority and Cortex®-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the "*Arm® Cortex®-M0 Technical Reference Manual*" and "*Arm® v6-M Architecture Reference Manual*".

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
SCR Base Address: **SCS_BA = 0xE000_E000**				
ICSR	SCS_BA+0xD04	R/W	Interrupt Control and State Register	0x0000_0000
VTOR	SCS_BA+0xD08	R/W	Vector Table Offset Register	0x0000_0000
AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000
SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000
SHPR1	SCS_BA+0xD18	R/W	System Handler Priority Register 1	0x0000_0000
SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000
SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

Interrupt Control State Register (ICSR)

Register	Offset	R/W	Description	Reset Value
ICSR	SCS_BA+0xD04	R/W	Interrupt Control and State Register	0x0000_0000

31	30	29	28	27	26	25	24
NMIPENDSET	Reserved		PENDSVSET	PENDSVCLR	PENDSTSET	PENDSTCLR	Reserved
23	22	21	20	19	18	17	16
ISRPREEMPT	ISRPENDING	Reserved				VECTPENDING	
15	14	13	12	11	10	9	8
VECTPENDING				RETTOBASE	Reserved		
7	6	5	4	3	2	1	0
Reserved		VECTACTIVE					

Bits	Description	
[31]	**NMIPENDSET**	**NMI Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes NMI exception state to pending. Read Operation: 0 = NMI exception is not pending. 1 = NMI exception is pending. **Note:** Because NMI is the highest-priority exception, normally the processor enters the NMI exception handler as soon as it detects a write of 1 to this bit. Entering the handler then clears this bit to 0. This means a read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.
[30:29]	**Reserved**	Reserved.
[28]	**PENDSVSET**	**PendSV Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes PendSV exception state to pending. Read Operation: 0 = PendSV exception is not pending. 1 = PendSV exception is pending. **Note:** Writing 1 to this bit is the only way to set the PendSV exception state to pending.
[27]	**PENDSVCLR**	**PendSV Clear-pending Bit** Write Operation: 0 = No effect. 1 = Removes the pending state from the PendSV exception. **Note:** This is a write only bit. To clear the PENDSV bit, you must “write 0 to PENDSVSET and write 1 to PENDSVRTC_CAL” at the same time.

[26]	**PENDSTSET**	**SysTick Exception Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes SysTick exception state to pending. Read Operation: 0 = SysTick exception is not pending. 1 = SysTick exception is pending.
[25]	**PENDSTCLR**	**SysTick Exception Clear-pending Bit** Write Operation: 0 = No effect. 1 = Removes the pending state from the SysTick exception. **Note:** This is a write only bit. To clear the PENDST bit, you must "write 0 to PENDSTSET and write 1 to PENDSTRTC_CAL" at the same time.
[24]	**Reserved**	Reserved.
[23]	**ISRPREEMPT**	**Interrupt Preempt Bit (Read Only)** If set, a pending exception will be serviced on exit from the debug halt state.
[22]	**ISRPENDING**	**Interrupt Pending Flag, Excluding NMI and Faults (Read Only)** 0 = Interrupt not pending. 1 = Interrupt pending.
[21:18]	**Reserved**	Reserved.
[17:12]	**VECTPENDING**	**Number of the Highest Pended Exception** Indicate the Exception Number of the Highest Priority Pending Enabled Exception 0 = no pending exceptions. Nonzero = the exception number of the highest priority pending enabled exception. The value indicated by this field includes the effect of the BASEPRI and FAULTMASK registers, but not any effect of the PRIMASK register.
[11]	**RETTOBASE**	**Preempted Active Exceptions Indicator** Indicate whether There are Preempted Active Exceptions 0 = there are preempted active exceptions to execute. 1 = there are no active exceptions, or the currently-executing exception is the only active exception.
[10:6]	**Reserved**	Reserved.
[5:0]	**VECTACTIVE**	**Number of the Current Active Exception** 0 = Thread mode. Non-zero = The exception number of the currently active exception.

Vector Table Offset Register (VTOR)

Register	Offset	R/W	Description	Reset Value
VTOR	SCS_BA+0xD08	R/W	Vector Table Offset Register	0x0000_0000

31	30	29	28	27	26	25	24
TBLOFF							
23	22	21	20	19	18	17	16
TBLOFF							
15	14	13	12	11	10	9	8
TBLOFF							
7	6	5	4	3	2	1	0
TBLOFF	Reserved						

Bits	Description	
[31:7]	TBLOFF	**Table Offset Bits** The vector table address for the selected Security state.
[6:0]	Reserved	Reserved.

Application Interrupt and Reset Control Register (AIRCR)

Register	Offset	R/W	Description	Reset Value
AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000

31	30	29	28	27	26	25	24
VECTORKEY							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VECTORKEY							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENDIANNESS	**Reserved**				**PRIGROUP**		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					**SYSRESETREQ**	**VECTCLRACTIVE**	**VECTRESET**

Bits	Description	
[31:16]	**VECTORKEY**	**Register Access Key** When writing this register, this field should be 0x05FA, otherwise the write action will be unpredictable. The VECTORKEY filed is used to prevent accidental write to this register from resetting the system or clearing of the exception status.
[15]	**ENDIANNESS**	**Data Endianness** 0 = Little-endian. 1 = Big-endian.
[14:11]	**Reserved**	Reserved.
[10:8]	**PRIGROUP**	**Interrupt Priority Grouping** This field determines the Split Of Group priority from subpriority,
[7:3]	**Reserved**	Reserved.
[2]	**SYSRESETREQ**	**System Reset Request** Writing This Bit to 1 Will Cause A Reset Signal To Be Asserted To The Chip And Indicate A Reset Is Requested This bit is write only and self-cleared as part of the reset sequence.
[1]	**VECTCLRACTIVE**	**Exception Active Status Clear Bit** Setting This Bit To 1 Will Clears All Active State Information For Fixed And Configurable Exceptions This bit is write only and can only be written when the core is halted. **Note:** It is the debugger's responsibility to re-initialize the stack.
[0]	**VECTRESET**	Reserved.

PRIGROUP	Binary Point	Group Priority Bits	Subpriority Bits	Number Of Group Priorities	Subpriorities
0b000	bxxxxxxx.y	[7:1]	[0]	128	2
0b001	bxxxxxx.yy	[7:2]	[1:0]	64	4
0b010	bxxxxx.yyy	[7:3]	[2:0]	32	8
0b011	bxxxx.yyyy	[7:4]	[3;0]	16	16
0b100	bxxx.yyyyy	[7:5]	[4:0]	8	32
0b101	bxx.yyyyyy	[7:6]	[5:0]	4	64
0b110	bx.yyyyyyy	[7]	[6:0]	2	128
0b111	b.yyyyyyyy	None	[7:0]	1	256

Table 6.2-12 Priority Grouping

System Control Register (SCR)

Register	Offset	R/W	Description	Reset Value
SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			**SEVONPEND**	**Reserved**	**SLEEPDEEP**	**SLEEPONEXIT**	**Reserved**

Bits	Description	
[31:5]	**Reserved**	Reserved.
[4]	**SEVONPEND**	**Send Event on Pending** 0 = Only enabled interrupts or events can wake up the processor, while disabled interrupts are excluded. 1 = Enabled events and all interrupts, including disabled interrupts, can wake up the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an SEV instruction or an external event.
[3]	**Reserved**	Reserved.
[2]	**SLEEPDEEP**	**Processor Deep Sleep and Sleep Mode Selection** Control Whether the Processor Uses Sleep Or Deep Sleep as its Low Power Mode. 0 = Sleep. 1 = Deep sleep.
[1]	**SLEEPONEXIT**	**Sleep-on-exit Enable Control** This bit indicate Sleep-On-Exit when Returning from Handler Mode to Thread Mode. 0 = Do not sleep when returning to Thread mode. 1 = Enters sleep, or deep sleep, on return from an ISR to Thread mode. Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.
[0]	**Reserved**	Reserved.

System Handler Priority Register 1 (SHPR1)

Register	Offset	R/W	Description	Reset Value
SHPR1	SCS_BA+0xD18	R/W	System Handler Priority Register 1	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_6							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_5							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_4							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:16]	**PRI_6**	Priority of system handler 6, UsageFault
[15:8]	**PRI_5**	Priority of system handler 5, BusFault
[7:0]	**PRI_4**	Priority of system handler 4, MemManage

System Handler Priority Register 2 (SHPR2)

Register	Offset	R/W	Description	Reset Value
SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000

31	30	29	28	27	26	25	24
PRI_11		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:30]	**PRI_11**	**Priority of System Handler 11 – SVCall** "0" denotes the highest priority and "3" denotes the lowest priority.
[29:0]	**Reserved**	Reserved.

System Handler Priority Register 3 (SHPR3)

Register	Offset	R/W	Description	Reset Value
SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

31	30	29	28	27	26	25	24
PRI_15		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_14		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:30]	**PRI_15**	**Priority of System Handler 15 – SysTick** "0" denotes the highest priority and "3" denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_14**	**Priority of System Handler 14 – PendSV** "0" denotes the highest priority and "3" denotes the lowest priority.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M0 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~32 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption

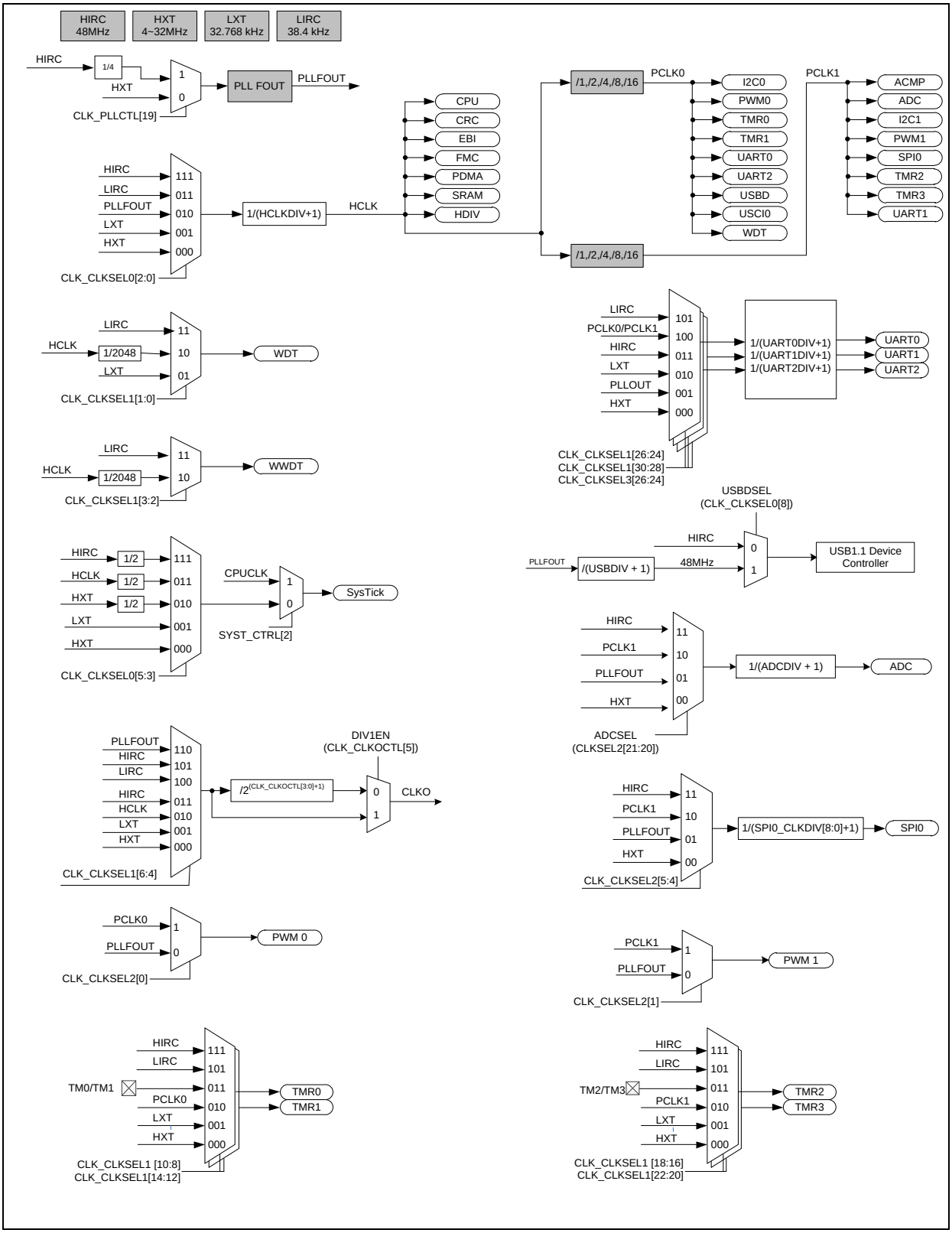


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 6 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~32 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~32 MHz external high speed crystal (HXT) or 48 MHz internal high speed oscillator (HIRC/4)
- 48 MHz internal high speed RC oscillator (HIRC)
- 38.4 kHz internal low speed RC oscillator (LIRC)

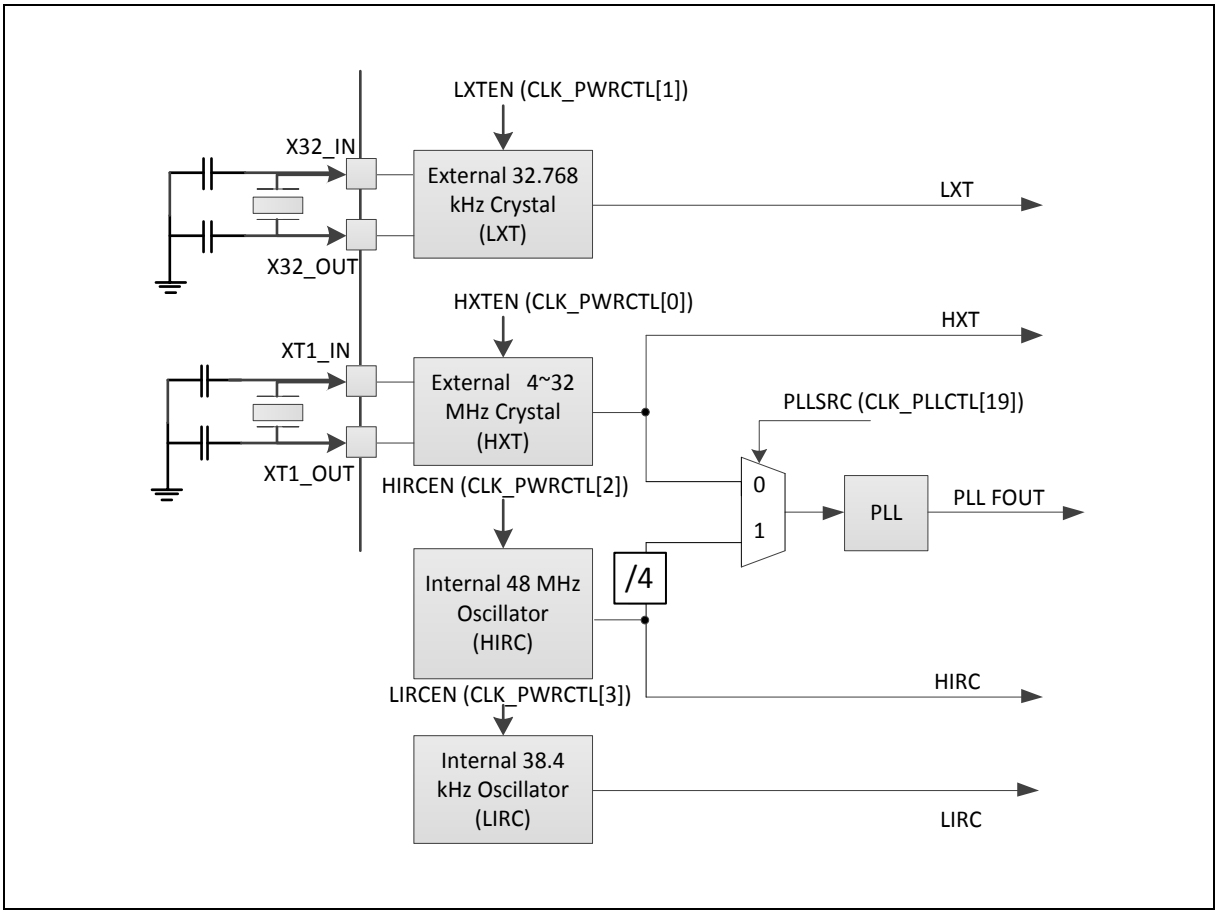


Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3

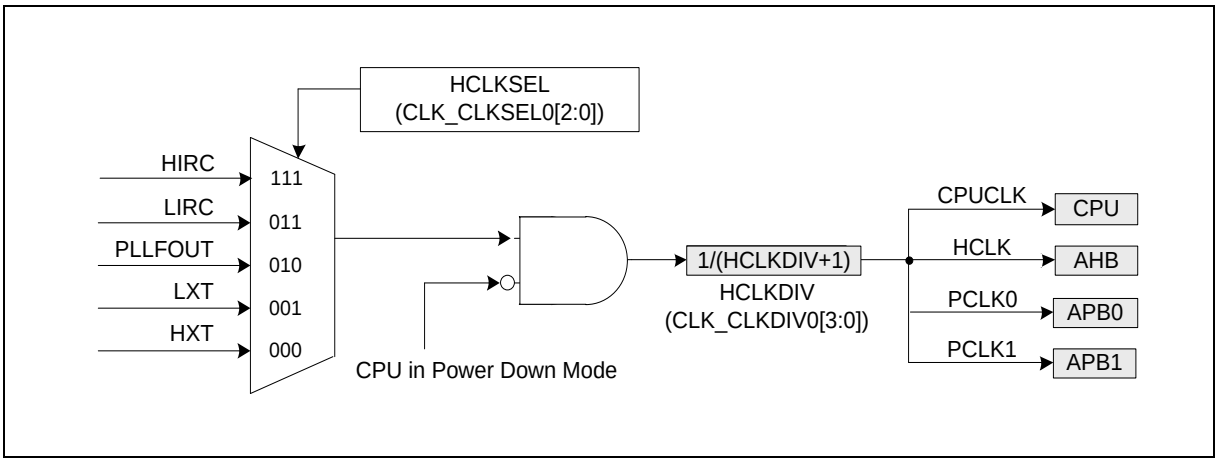


Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6.3-4.

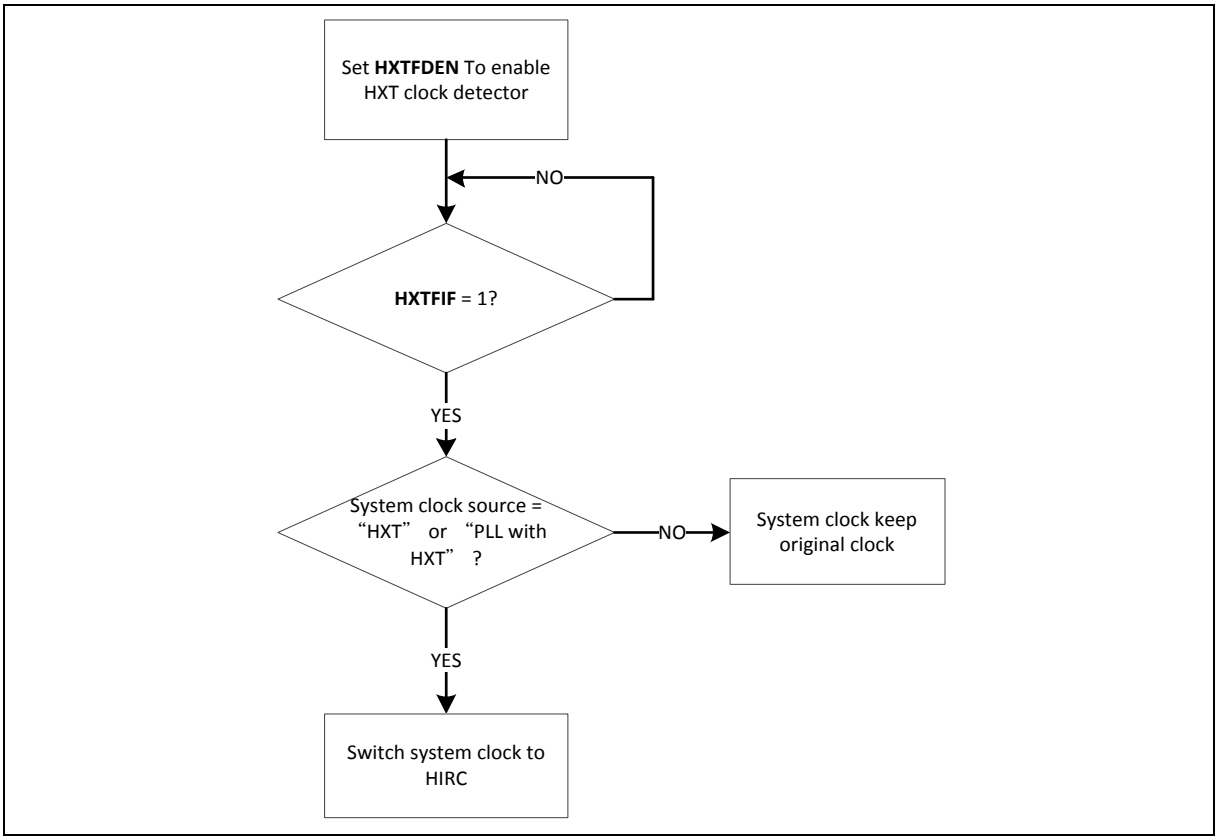


Figure 6.3-4 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

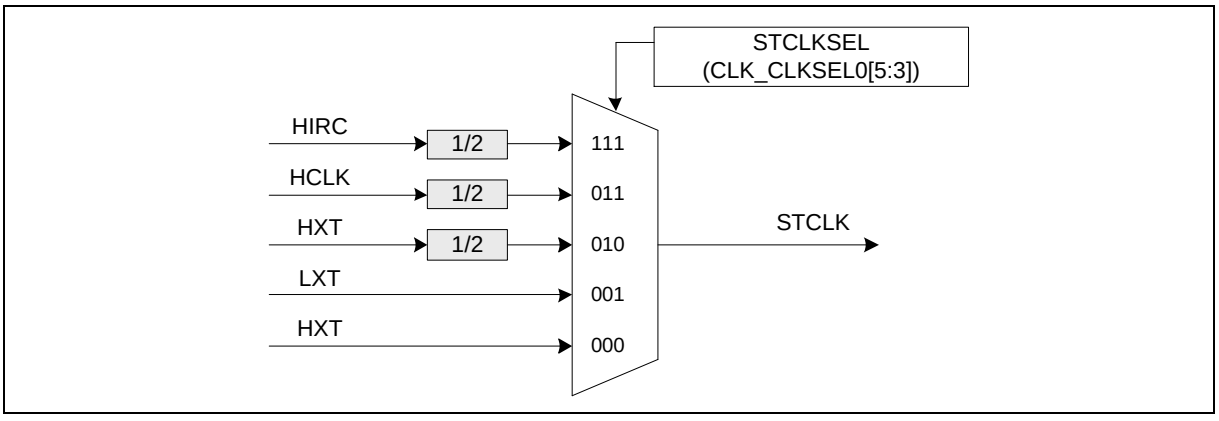


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock has different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSELx register description in 6.3.9.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 38.4 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

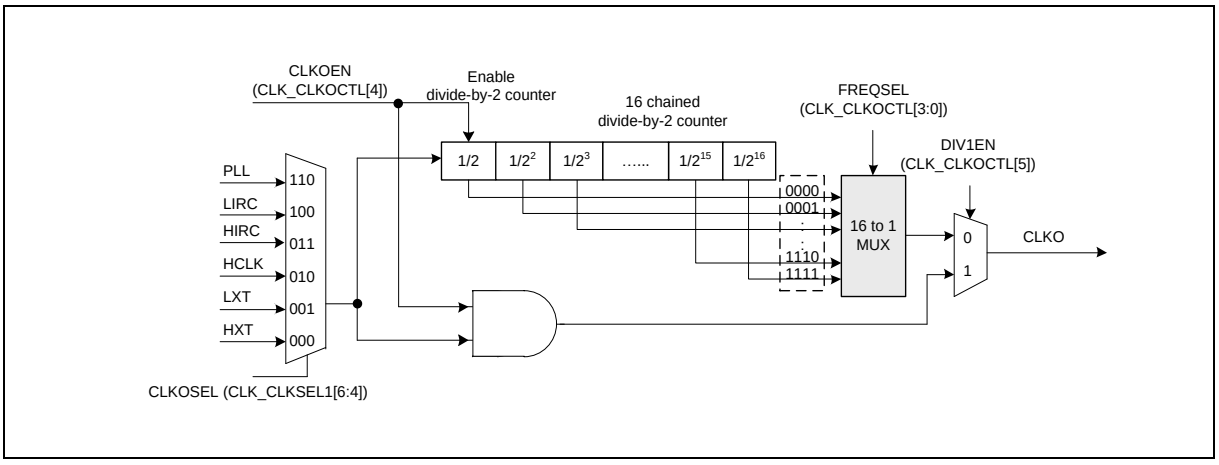


Figure 6.3-6 Clock Output Block Diagram

6.3.7 USB Clock Source

The clock source of USB 1.0 is generated from 48 Mhz HIRC or programmable PLL output. The generated clocks are shown in Figure 6.3-7.

USBDIV is the clock divider output frequency, the output formula is

(PLLFOUT frequency) / (USBDIV + 1).

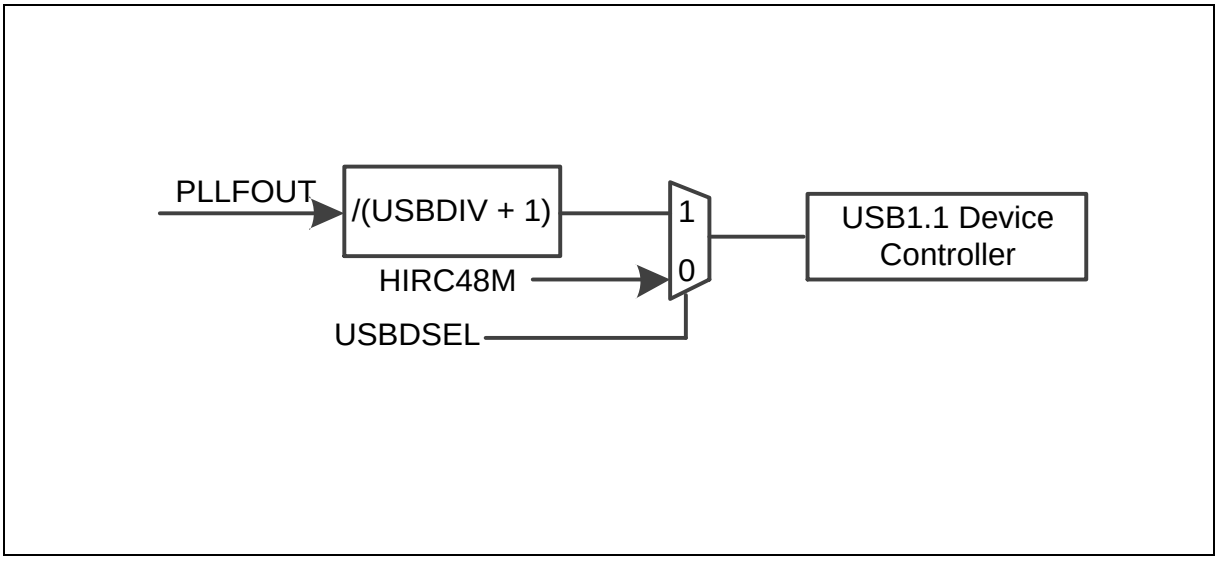


Figure 6.3-7 USB Clock Source

6.3.8 Register Map

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
CLK Base Address: **CLK_BA = 0x4000_0200**				
CLK_PWRCTL	CLK_BA+0x00	R/W	System Power-down Control Register	0x0231_001X
CLK_AHBCLK	CLK_BA+0x04	R/W	AHB Devices Clock Enable Control Register	0x0000_0004
CLK_APBCLK0	CLK_BA+0x08	R/W	APB Devices Clock Enable Control Register 0	0x0000_0001
CLK_APBCLK1	CLK_BA+0x0C	R/W	APB Devices Clock Enable Control Register 1	0x0000_0000
CLK_CLKSEL0	CLK_BA+0x10	R/W	Clock Source Select Control Register 0	0x0000_003F
CLK_CLKSEL1	CLK_BA+0x14	R/W	Clock Source Select Control Register 1	0x4477_773B
CLK_CLKSEL2	CLK_BA+0x18	R/W	Clock Source Select Control Register 2	0x0020_0023
CLK_CLKSEL3	CLK_BA+0x1C	R/W	Clock Source Select Control Register 3	0x0400_0000
CLK_CLKDIV0	CLK_BA+0x20	R/W	Clock Divider Number Register 0	0x0000_0000
CLK_CLKDIV4	CLK_BA+0x30	R/W	Clock Divider Number Register 4	0x0000_0000
CLK_PCLKDIV	CLK_BA+0x34	R/W	APB Clock Divider Register	0x0000_0000
CLK_PLLCTL	CLK_BA+0x40	R/W	PLL Control Register	0x0005_C25E
CLK_STATUS	CLK_BA+0x50	R	Clock Status Monitor Register	0x0000_00XX
CLK_CLKOCTL	CLK_BA+0x60	R/W	Clock Output Control Register	0x0000_0000
CLK_CLKDCTL	CLK_BA+0x70	R/W	Clock Fail Detector Control Register	0x0000_0000
CLK_CLKDSTS	CLK_BA+0x74	R/W	Clock Fail Detector Status Register	0x0000_0000
CLK_CDUPB	CLK_BA+0x78	R/W	Clock Frequency Range Detector Upper Boundary Register	0x0000_0000
CLK_CDLOWB	CLK_BA+0x7c	R/W	Clock Frequency Range Detector Lower Boundary Register	0x0000_0000
CLK_LDOCTL	CLK_BA+0x80	R/W	LDO Control Register	0x0000_0000
CLK_HXTFSEL	CLK_BA+0xB4	R/W	HXT Filter Select Control Register	0x0000_0000

6.3.9 Register Description

System Power-down Control Register (CLK_PWRCTL)

Register	Offset	R/W	Description	Reset Value
CLK_PWRCTL	CLK_BA+0x00	R/W	System Power-down Control Register	0x0231_001X

31	30	29	28	27	26	25	24
Reserved					LXTGAIN		LXTSELXT
23	22	21	20	19	18	17	16
Reserved	HXTGAIN			Reserved			
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
PDEN	PDWKIF	PDWKIEN	PDWKDLY	LIRCEN	HIRCEN	LXTEN	HXTEN

Bits	Description	
[31:27]	**Reserved**	Reserved.
[26:25]	**LXTGAIN**	**LXT Gain Control Bit (Write Protect)** 00 = LXT Crystal ESR = 35K, CL=12.5pF 10 = LXT Crystal ESR = 70K, CL=12.5pF **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[24]	**LXTSELXT**	**LXT Mode Selection** 0 = LXT work as crystal mode. PF.4 and PF.5 are configured as external low speed crystal (LXT) pins. 1 = LXT work as external clock mode. PF.5 is configured as external clock input pin. **Note1:** When LXTSELXT = 1, PF.5 MFP should be setting as GPIO mode. The DC characteristic of X32_IN is the same as GPIO. **Note2:** This bit is write protected. Refer to the SYS_REGLCTL register.
[22:20]	**HXTGAIN**	**HXT Gain Control Bit (Write Protect)** This is a protected register. Please refer to open lock sequence to program it. Gain control is used to enlarge the gain of crystal to make sure crystal work normally. If gain control is enabled, crystal will consume more power than gain control off. 000 = HXT frequency is lower than from 4 MHz. 001 = HXT frequency is from 4 MHz to 8 MHz. 010 = HXT frequency is from 8 MHz to 12 MHz. 011 = HXT frequency is from 12 MHz to 16 MHz. 100 = HXT frequency is from 16 MHz to 24 MHz. 111 = HXT frequency is from 24 MHz to 32 MHz. Others: Reserved **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[19:8]	**Reserved**	Reserved.
[7]	**PDEN**	**System Power-down Enable (Write Protect)**

		When this bit is set to 1, Power-down mode is enabled and chip keeps active till the CPU sleep mode is also active and then the chip enters Power-down mode. When chip wakes up from Power-down mode, this bit is auto cleared. Users need to set this bit again for next Power-down. In Power-down mode, HXT and the HIRC will be disabled in this mode, but LXT and LIRC are not controlled by Power-down mode. In Power-down mode, the PLL and system clock are disabled, and ignored the clock source selection. The clocks of peripheral are not controlled by Power-down mode, if the peripheral clock source is from LXT or LIRC. 0 = Chip operating normally or chip in idle mode because of WFI command. 1 = Chip enters Power-down mode instant or wait CPU sleep command WFI. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[6]	**PDWKIF**	**Power-down Mode Wake-up Interrupt Status** Set by “Power-down wake-up event”, it indicates that resume from Power-down mode” The flag is set if any wake-up source is occurred. Refer Power Modes and Wake-up Sources chapter. **Note1:** Write 1 to clear the bit to 0. **Note2:** This bit works only if PDWKIEN (CLK_PWRCTL[5]) set to 1.
[5]	**PDWKIEN**	**Power-down Mode Wake-up Interrupt Enable Bit (Write Protect)** 0 = Power-down mode wake-up interrupt Disabled. 1 = Power-down mode wake-up interrupt Enabled. **Note1:** The interrupt will occur when both PDWKIF and PDWKIEN are high. **Note2:** This bit is write protected. Refer to the SYS_REGLCTL register.
[4]	**PDWKDLY**	**Enable the Wake-up Delay Counter (Write Protect)** When the chip wakes up from Power-down mode, the clock control will delay certain clock cycles to wait system clock stable. The delayed clock cycle is 4096 clock cycles when chip works at external high speed crystal oscillator (HXT), and 512 clock cycles when chip works at internal high speed RC oscillator (HIRC). 0 = Clock cycles delay Disabled. 1 = Clock cycles delay Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[3]	**LIRCEN**	**LIRC Enable Bit (Write Protect)** 0 = Internal low speed RC oscillator (LIRC) Disabled. 1 = Internal low speed RC oscillator (LIRC) Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[2]	**HIRCEN**	**HIRC Enable Bit (Write Protect)** 0 = Internal high speed RC oscillator (HIRC) Disabled. 1 = Internal high speed RC oscillator (HIRC) Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[1]	**LXTEN**	**LXT Enable Bit (Write Protect)** 0 = External low speed crystal (LXT) Disabled. 1 = External low speed crystal (LXT) Enabled. **Note1** : reset by power on reset **Note2:** This bit is write protected. Refer to the SYS_REGLCTL register.
[0]	**HXTEN**	**HXT Enable Bit (Write Protect)** 0 = Eexternal high speed crystal (HXT) Disabled. 1 = External high speed crystal (HXT) Enabled. **Note1** : reset by power on reset

		Note2: This bit is write protected. Refer to the SYS_REGLCTL register.

AHB Devices Clock Enable Control Register (CLK_AHBCLK)

The bits in this register are used to enable/disable clock for system clock, AHB bus devices clock.

Register	Offset	R/W	Description	Reset Value
CLK_AHBCLK	CLK_BA+0x04	R/W	AHB Devices Clock Enable Control Register	0x0000_0004

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
CRCCKEN	Reserved		HDIV_EN	EBICKEN	ISPCKEN	PDMACKEN	Reserved

Bits	Description	
[31:21]	**Reserved**	Reserved.
[20]	**Reserved**	
[19:8]	**Reserved**	Reserved.
[7]	**CRCCKEN**	**CRC Generator Controller Clock Enable Bit** 0 = CRC peripheral clock Disabled. 1 = CRC peripheral clock Enabled.
[6:5]	**Reserved**	Reserved.
[4]	**HDIV_EN**	**Divider Controller Clock Enable Control** 0 = Divider controller peripheral clock Disabled. 1 = Divider controller peripheral clock Enabled.
[3]	**EBICKEN**	**EBI Controller Clock Enable Bit** 0 = EBI peripheral clock Disabled. 1 = EBI peripheral clock Enabled.
[2]	**ISPCKEN**	**Flash ISP Controller Clock Enable Bit** 0 = Flash ISP peripheral clock Disabled. 1 = Flash ISP peripheral clock Enabled.
[1]	**PDMACKEN**	**PDMA Controller Clock Enable Bit** 0 = PDMA peripheral clock Disabled. 1 = PDMA peripheral clock Enabled.
[0]	**Reserved**	Reserved.

APB Devices Clock Enable Control Register 0 (CLK_APBCLK0)

The bits in this register are used to enable/disable clock for peripheral controller clocks.

Register	Offset	R/W	Description	Reset Value
CLK_APBCLK0	CLK_BA+0x08	R/W	APB Devices Clock Enable Control Register 0	0x0000_0001

31	30	29	28	27	26	25	24
Reserved			ADCCKEN	USBDCKEN	Reserved		
23	22	21	20	19	18	17	16
Reserved					UART2CKEN	UART1CKEN	UART0CKEN
15	14	13	12	11	10	9	8
Reserved		SPI0CKEN	Reserved			I2C1CKEN	I2C0CKEN
7	6	5	4	3	2	1	0
ACMP01CKEN	CLKOCKEN	TMR3CKEN	TMR2CKEN	TMR1CKEN	TMR0CKEN	Reserved	WDTCKEN

Bits	Description	
[31:29]	**Reserved**	Reserved.
[28]	**ADCCKEN**	**Analog-digital-converter (ADC) Clock Enable Bit** 0 = ADC clock Disabled. 1 = ADC clock Enabled.
[27]	**USBDCKEN**	**USB Device Clock Enable Bit** 0 = USB Device clock Disabled. 1 = USB Device clock Enabled.
[26:19]	**Reserved**	Reserved.
[18]	**UART2CKEN**	**UART2 Clock Enable Bit** 0 = UART2 clock Disabled. 1 = UART2 clock Enabled.
[17]	**UART1CKEN**	**UART1 Clock Enable Bit** 0 = UART1 clock Disabled. 1 = UART1 clock Enabled.
[16]	**UART0CKEN**	**UART0 Clock Enable Bit** 0 = UART0 clock Disabled. 1 = UART0 clock Enabled.
[15:14]	**Reserved**	Reserved.
[13]	**SPI0CKEN**	**SPI0 Clock Enable Bit** 0 = SPI0 clock Disabled. 1 = SPI0 clock Enabled.
[12:10]	**Reserved**	Reserved.
[9]	**I2C1CKEN**	**I2C1 Clock Enable Bit**

		0 = I2C1 clock Disabled. 1 = I2C1 clock Enabled.
[8]	**I2C0CKEN**	**I2C0 Clock Enable Bit** 0 = I2C0 clock Disabled. 1 = I2C0 clock Enabled.
[7]	**ACMP01CKEN**	**Analog Comparator 0/1 Clock Enable Bit** 0 = Analog comparator 0/1 clock Disabled. 1 = Analog comparator 0/1 clock Enabled.
[6]	**CLKOCKEN**	**CLKO Clock Enable Bit** 0 = CLKO clock Disabled. 1 = CLKO clock Enabled.
[5]	**TMR3CKEN**	**Timer3 Clock Enable Bit** 0 = Timer3 clock Disabled. 1 = Timer3 clock Enabled.
[4]	**TMR2CKEN**	**Timer2 Clock Enable Bit** 0 = Timer2 clock Disabled. 1 = Timer2 clock Enabled.
[3]	**TMR1CKEN**	**Timer1 Clock Enable Bit** 0 = Timer1 clock Disabled. 1 = Timer1 clock Enabled.
[2]	**TMR0CKEN**	**Timer0 Clock Enable Bit** 0 = Timer0 clock Disabled. 1 = Timer0 clock Enabled.
[1]	**Reserved**	Reserved.
[0]	**WDTCKEN**	**Watchdog Timer Clock Enable Bit (Write Protect)** 0 = Watchdog timer clock Disabled. 1 = Watchdog timer clock Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register. **Note:** This bit is reset by power on reset, Watchdog reset or software chip reset.

APB Devices Clock Enable Control Register 1 (CLK_APBCLK1)

The bits in this register are used to enable/disable clock for peripheral controller clocks.

Register	Offset	R/W	Description	Reset Value
CLK_APBCLK1	CLK_BA+0x0C	R/W	APB Devices Clock Enable Control Register 1	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved						**PWM1CKEN**	**PWM0CKEN**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							**USCI0CKEN**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:18]	**Reserved**	Reserved.
[17]	**PWM1CKEN**	**PWM1 Clock Enable Bit** 0 = PWM1 clock Disabled. 1 = PWM1 clock Enabled.
[16]	**PWM0CKEN**	**PWM0 Clock Enable Bit** 0 = PWM0 clock Disabled. 1 = PWM0 clock Enabled.
[15:9]	**Reserved**	Reserved.
[8]	**USCI0CKEN**	**USCI0 Clock Enable Bit** 0 = USCI0 clock Disabled. 1 = USCI0 clock Enabled.
[7:0]	**Reserved**	Reserved.

Clock Source Select Control Register 0 (CLK_CLKSEL0)

Register	Offset	R/W	Description	Reset Value
CLK_CLKSEL0	CLK_BA+0x10	R/W	Clock Source Select Control Register 0	0x0000_003F

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							USBDSEL
7	6	5	4	3	2	1	0
Reserved		STCLKSEL			HCLKSEL		

Bits	Description	
[31:9]	**Reserved**	Reserved.
[8]	**USBDSEL**	**USB Device Clock Source Selection (Write Protect)** These bits are protected bit. It means programming this bit needs to write “59h”, “16h”, “88h” to address 0x4000_0100 to disable register protection. Refer to the register REGWRPROT at address GCR_BA+0x100. 0 = Clock source from HIRC. 1 = Clock source from PLL divided. **Note:** If the PLL function is not supported, the clock source will be fixed at HIRC. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[7:6]	**Reserved**	Reserved.
[5:3]	**STCLKSEL**	**Cortex®-M0 SysTick Clock Source Selection (Write Protect)** If SYST_CTRL[2]=0, SysTick uses listed clock source below. 000 = Clock source from HXT. 001 = Clock source from LXT. 010 = Clock source from HXT/2. 011 = Clock source from HCLK/2. 111 = Clock source from HIRC/2. Other = Reserved. **Note:** if SysTick clock source is not from HCLK (i.e. SYST_CTRL[2] = 0), SysTick clock source must less than or equal to HCLK/2. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[2:0]	**HCLKSEL**	**HCLK Clock Source Selection (Write Protect)** Before clock switching, the related clock sources (both pre-select and new-select) must be turned on. 000 = Clock source from HXT. 001 = Clock source from LXT.

		010 = Clock source from PLL. 011 = Clock source from LIRC. 111= Clock source from HIRC. Other = Reserved. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register. **Note :** reset by power on reset **Note:** If the PLL function is not supported, the clock source will be fixed at HIRC. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information. **Note:** If the LXT function is not supported, the clock source will be kept previous clock selection. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.

Clock Source Select Control Register 1 (CLK_CLKSEL1)

Before clock switching, the related clock sources (pre-selected and newly-selected) must be turned on.

Register	Offset	R/W	Description	Reset Value
CLK_CLKSEL1	CLK_BA+0x14	R/W	Clock Source Select Control Register 1	0x4477_773B

31	30	29	28	27	26	25	24
Reserved	UART1SEL			Reserved	UART0SEL		
23	22	21	20	19	18	17	16
Reserved	TMR3SEL			Reserved	TMR2SEL		
15	14	13	12	11	10	9	8
Reserved	TMR1SEL			Reserved	TMR0SEL		
7	6	5	4	3	2	1	0
Reserved	CLKOSEL			WWDTSEL		WDTSEL	

Bits	Description	
[31]	**Reserved**	Reserved.
[30:28]	**UART1SEL**	**UART1 Clock Source Selection** 000 = Clock source from external high speed crystal oscillator (HXT). 001 = Clock source from PLL. 010 = Clock source from external low speed crystal oscillator (LXT). 011 = Clock source from internal high speed RC oscillator (HIRC). 100 = Clock source from PCLK1. 101 = Clock source from internal low speed RC oscillator (LIRC). Other = Reserved. **Note:** If the PLL function is not supported, the clock source will be fixed at PCLK1. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[27]	**Reserved**	Reserved.
[26:24]	**UART0SEL**	**UART0 Clock Source Selection** 000 = Clock source from external high speed crystal oscillator (HXT). 001 = Clock source from PLL. 010 = Clock source from external low speed crystal oscillator (LXT). 011 = Clock source from internal high speed RC oscillator (HIRC). 100 = Clock source from PCLK0. 101 = Clock source from internal low speed RC oscillator (LIRC). Other = Reserved. **Note:** If the PLL function is not supported, the clock source will be fixed at PCLK0. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.

[23]	**Reserved**	Reserved.
[22:20]	**TMR3SEL**	**TIMER3 Clock Source Selection** 000 = Clock source from external high speed crystal oscillator (HXT). 001 = Clock source from external low speed crystal oscillator (LXT). 010 = Clock source from PCLK1. 011 = Clock source from external clock T3 pin. 101 = Clock source from internal low speed RC oscillator (LIRC). 111 = Clock source from internal high speed RC oscillator (HIRC). Others = Reserved. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[19]	**Reserved**	Reserved.
[18:16]	**TMR2SEL**	**TIMER2 Clock Source Selection** 000 = Clock source from external high speed crystal oscillator (HXT). 001 = Clock source from external low speed crystal oscillator (LXT). 010 = Clock source from PCLK1. 011 = Clock source from external clock T2 pin. 101 = Clock source from internal low speed RC oscillator (LIRC). 111 = Clock source from internal high speed RC oscillator (HIRC). Others = Reserved. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[15]	**Reserved**	Reserved.
[14:12]	**TMR1SEL**	**TIMER1 Clock Source Selection** 000 = Clock source from external high speed crystal oscillator (HXT). 001 = Clock source from external low speed crystal oscillator (LXT). 010 = Clock source from PCLK0. 011 = Clock source from external clock T1 pin. 101 = Clock source from internal low speed RC oscillator (LIRC). 111 = Clock source from internal high speed RC oscillator (HIRC). Others = Reserved. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[11]	**Reserved**	Reserved.
[10:8]	**TMR0SEL**	**TIMER0 Clock Source Selection** 000 = Clock source from external high speed crystal oscillator (HXT). 001 = Clock source from external low speed crystal oscillator (LXT). 010 = Clock source from PCLK0. 011 = Clock source from external clock T0 pin. 101 = Clock source from internal low speed RC oscillator (LIRC). 111 = Clock source from internal high speed RC oscillator (HIRC). Others = Reserved. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[7]	**Reserved**	Reserved.
[6:4]	**CLKOSEL**	**Clock Divider Clock Source Selection**

		000 = Clock source from external high speed crystal oscillator (HXT). 001 = Clock source from external low speed crystal oscillator (LXT). 010 = Clock source from HCLK. 011 = Clock source from internal high speed RC oscillator (HIRC). 100 = Clock source from internal low speed RC oscillator (LIRC). 101 = Clock source from internal high speed RC oscillator (HIRC). 110 = Clock source from PLL. 111 = Clock source from USB SOF. **Note:** If the PLL function is not supported, the clock source will be fixed at HIRC. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[3:2]	**WWDTSEL**	**Window Watchdog Timer Clock Source Selection (Write Protect)** 10 = Clock source from HCLK/2048. 11 = Clock source from internal low speed RC oscillator (LIRC). Others = Reserved.
[1:0]	**WDTSEL**	**Watchdog Timer Clock Source Selection (Write Protect)** 00 = Reserved. 01 = Clock source from external low speed crystal oscillator (LXT). 10 = Clock source from HCLK/2048. 11 = Clock source from internal low speed RC oscillator (LIRC). **Note:** This bit is write protected. Refer to the SYS_REGLCTL register. 2. Will be forced to 11 when CONFIG0[31], CONFIG0[4], CONFIG0[3] are all ones. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.

Clock Source Select Control Register 2 (CLK_CLKSEL2)

Before clock switching, the related clock sources (pre-select and new-select) must be turned on.

Register	Offset	R/W	Description	Reset Value
CLK_CLKSEL2	CLK_BA+0x18	R/W	Clock Source Select Control Register 2	0x0020_0023

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved		ADCSEL		Reserved			
15	14	13	12	11	10	9	8
Reserved		Reserved		Reserved			
7	6	5	4	3	2	1	0
Reserved		SPI0SEL		Reserved		PWM1SEL	PWM0SEL

Bits	Description	
[31]	**Reserved**	Reserved.
[21:20]	**ADCSEL**	**ADC Clock Source Selection** 00 = Clock source from external high speed crystal oscillator (HXT) clock. 01 = Clock source from PLL. 10 = Clock source from PCLK1. 11 = Clock source from internal high speed RC oscillator (HIRC) clock. **Note:** If the PLL function is not supported, the clock source will be fixed at PCLK1. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[5:4]	**SPI0SEL**	**SPI0 Clock Source Selection** 00 = Clock source from external high speed crystal oscillator (HXT). 01 = Clock source from PLL. 10 = Clock source from PCLK1. 11 = Clock source from internal high speed RC oscillator (HIRC). **Note:** If the PLL function is not supported, the clock source will be fixed at PCLK1. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[3:2]	**Reserved**	Reserved.
[1]	**PWM1SEL**	**PWM1 Clock Source Selection** The peripheral clock source of PWM1 is defined by PWM1SEL. 0 = Clock source from PLL. 1 = Clock source from PCLK1. **Note:** If the PLL function is not supported, the clock source will be fixed at PCLK1. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[0]	**PWM0SEL**	**PWM0 Clock Source Selection** The peripheral clock source of PWM0 is defined by PWM0SEL. 0 = Clock source from PLL. 1 = Clock source from PCLK0. **Note:** If the PLL function is not supported, the clock source will be fixed at PCLK0. Please

		refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.

Clock Source Select Control Register 3 (CLK_CLKSEL3)

Before clock switching, the related clock sources (pre-select and new-select) must be turned on.

Register	Offset	R/W	Description	Reset Value
CLK_CLKSEL3	CLK_BA+0x1C	R/W	Clock Source Select Control Register 3	0x0400_0000

31	30	29	28	27	26	25	24
Reserved					**UART2SEL**		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:27]	**Reserved**	Reserved.
[26:24]	**UART2SEL**	**UART2 Clock Source Selection** 000 = Clock source from external high speed crystal oscillator (HXT). 001 = Clock source from PLL. 010 = Clock source from external low speed crystal oscillator (LXT). 011 = Clock source from internal high speed RC oscillator (HIRC). 100 = Clock source from PCLK0. 101 = Clock source from internal low speed RC oscillator (LIRC). Other = Reserved. **Note:** If the PLL function is not supported, the clock source will be fixed at PCLK0. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information. **Note:** If the LXT function is not supported, the clock source will be stopped. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[23:0]	**Reserved**	Reserved.

Clock Divider Number Register 0 (CLK_CLKDIV0)

Register	Offset	R/W	Description	Reset Value
CLK_CLKDIV0	CLK_BA+0x20	R/W	Clock Divider Number Register 0	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADCDIV							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UART1DIV				**UART0DIV**			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
USBDIV				**HCLKDIV**			

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:16]	**ADCDIV**	**ADC Clock Divide Number From ADC Clock Source** ADC clock frequency = (ADC clock source frequency) / (ADCDIV + 1).
[15:12]	**UART1DIV**	**UART1 Clock Divide Number From UART1 Clock Source** UART1 clock frequency = (UART1 clock source frequency) / (UART1DIV + 1).
[11:8]	**UART0DIV**	**UART0 Clock Divide Number From UART0 Clock Source** UART0 clock frequency = (UART0 clock source frequency) / (UART0DIV + 1).
[7:4]	**USBDIV**	**USB Clock Divide Number From PLL Clock** USB clock frequency = (PLL frequency) / (USBDIV + 1).
[3:0]	**HCLKDIV**	**HCLK Clock Divide Number From HCLK Clock Source** HCLK clock frequency = (HCLK clock source frequency) / (HCLKDIV + 1).

Clock Divider Number Register 4 (CLK_CLKDIV4)

Register	Offset	R/W	Description	Reset Value
CLK_CLKDIV4	CLK_BA+0x30	R/W	Clock Divider Number Register 4	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				**UART2DIV**			

Bits	Description	
[31:4]	**Reserved**	Reserved.
[3:0]	**UART2DIV**	**UART2 Clock Divide Number From UART2 Clock Source** UART2 clock frequency = (UART2 clock source frequency) / (UART2DIV + 1).

APB Clock Divider Register (CLK_PCLKDIV)

Register	Offset	R/W	Description	Reset Value
CLK_PCLKDIV	CLK_BA+0x34	R/W	APB Clock Divider Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved	APB1DIV			Reserved	APB0DIV		

Bits	Description	
[31:7]	**Reserved**	Reserved.
[6:4]	**APB1DIV**	**APB1 Clock DIvider** APB1 clock can be divided from HCLK 000: PCLK1 = HCLK. 001: PCLK1 = 1/2 HCLK. 010: PCLK1 = 1/4 HCLK. 011: PCLK1 = 1/8 HCLK. 100: PCLK1 = 1/16 HCLK. Others: Reserved.
[3]	**Reserved**	Reserved.
[2:0]	**APB0DIV**	**APB0 Clock DIvider** APB0 clock can be divided from HCLK 000: PCLK0 = HCLK. 001: PCLK0 = 1/2 HCLK. 010: PCLK0 = 1/4 HCLK. 011: PCLK0 = 1/8 HCLK. 100: PCLK0 = 1/16 HCLK. Others: Reserved.

PLL Control Register (CLK_PLLCTL)

The PLL reference clock input is from the 4~32 MHz external high speed crystal oscillator (HXT) clock input or from the 48 MHz internal high speed oscillator (HIRC/4). This register is used to control the PLL output frequency and PLL operation mode.

Programming these bits needs to write “59h”, “16h”, “88h” to address 0x4000_0100 to disable register protection. Refer to the register SYS_REGLCTL at address SYS_BA+0x100.

Register	Offset	R/W	Description	Reset Value
CLK_PLLCTL	CLK_BA+0x40	R/W	PLL Control Register	0x0005_C25E

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
STBSEL	**Reserved**			**PLLSRC**	**OE**	**BP**	**PD**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTDIV		**INDIV**					**FBDIV**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FBDIV							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23]	**STBSEL**	**PLL Stable Counter Selection (Write Protect)** 0 = PLL stable time is 6144 PLL source clock (suitable for source clock is equal to or less than 12 MHz). 1 = PLL stable time is 16128 PLL source clock (suitable for source clock is larger than 12 MHz). **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[22:20]	**Reserved**	Reserved.
[19]	**PLLSRC**	**PLL Source Clock Selection (Write Protect)** 0 = PLL source clock from external high-speed crystal oscillator (HXT). 1 = PLL source clock from 48 MHz internal high-speed oscillator (HIRC/4). **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[18]	**OE**	**PLL OE (FOUT Enable) Pin Control (Write Protect)** 0 = PLL FOUT Enabled. 1 = PLL FOUT is fixed low. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[17]	**BP**	**PLL Bypass Control (Write Protect)** 0 = PLL is in normal mode (default). 1 = PLL clock output is same as PLL input clock FIN. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

[16]	**PD**	**Power-down Mode (Write Protect)** If set the PDEN bit to 1 in CLK_PWRCTL register, the PLL will enter Power-down mode, too. 0 = PLL is in normal mode. 1 = PLL is in Power-down mode (default). **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[15:14]	**OUTDIV**	**PLL Output Divider Control (Write Protect)** Refer to the formulas below the table. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[13:9]	**INDIV**	**PLL Input Divider Control (Write Protect)** Refer to the formulas below the table. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[8:0]	**FBDIV**	**PLL Feedback Divider Control (Write Protect)** Refer to the formulas below the table. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

Output Clock Frequency Setting

$$FOUT = FIN \times \frac{NF}{NR} \times \frac{1}{NO}$$

Constraint:

1. $3.2MHz < FIN < 150MHz$
2. $800kHz < \frac{FIN}{2 * NR} < 8MHz$
3. $200MHz < FCO = FIN * \frac{NF}{NR} < 500MHz,$
   $FCO > 250MHz \ \ is \ \ preferred$

Symbol	Description
FOUT	Output Clock Frequency
FIN	Input (Reference) Clock Frequency
NR	Input Divider (INDIV + 2)
NF	Feedback Divider (FBDIV + 2)
NO	OUTDIV = “00” : NO = 1 OUTDIV = “01” : NO = 2 OUTDIV = “10” : NO = 2 OUTDIV = “11” : NO = 4

Table 6.3-1 Symbol Definition of PLL Output Frequency Formula

Clock Status Monitor Register (CLK_STATUS)

The bits in this register are used to monitor if the chip clock source is stable or not, and whether the clock switch is failed.

Register	Offset	R/W	Description	Reset Value
CLK_STATUS	CLK_BA+0x50	R	Clock Status Monitor Register	0x0000_00XX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
CLKSFAIL	Reserved		HIRCSTB	LIRCSTB	PLLSTB	LXTSTB	HXTSTB

Bits	Description	
[31:8]	**Reserved**	Reserved.
[7]	**CLKSFAIL**	**Clock Switching Fail Flag (Read Only)** This bit is updated when software switches system clock source. If switch target clock is stable, this bit will be set to 0. If switch target clock is not stable, this bit will be set to 1. 0 = Clock switching success. 1 = Clock switching failure. **Note:** Write 1 to clear the bit to 0.
[6:5]	**Reserved**	Reserved.
[4]	**HIRCSTB**	**HIRC Clock Source Stable Flag (Read Only)** 0 = Internal high speed RC oscillator (HIRC) clock is not stable or disabled. 1 = Internal high speed RC oscillator (HIRC) clock is stable and enabled.
[3]	**LIRCSTB**	**LIRC Clock Source Stable Flag (Read Only)** 0 = Internal low speed RC oscillator (LIRC) clock is not stable or disabled. 1 = Internal low speed RC oscillator (LIRC) clock is stable and enabled.
[2]	**PLLSTB**	**Internal PLL Clock Source Stable Flag (Read Only)** 0 = Internal PLL clock is not stable or disabled. 1 = Internal PLL clock is stable and enabled. **Note:** If the PLL function is not supported, this bit field will become invalid. Please refer to section 4.3 NuMicro® M031/M032 Series Selection Guide for detailed information.
[1]	**LXTSTB**	**LXT Clock Source Stable Flag (Read Only)** 0 = External low speed crystal oscillator (LXT) clock is not stable or disabled. 1 = External low speed crystal oscillator (LXT) clock is stabled and enabled.
[0]	**HXTSTB**	**HXT Clock Source Stable Flag (Read Only)** 0 = External high speed crystal oscillator (HXT) clock is not stable or disabled.

		1 = External high speed crystal oscillator (HXT) clock is stable and enabled.

Clock Output Control Register (CLK_CLKOCTL)

Register	Offset	R/W	Description	Reset Value
CLK_CLKOCTL	CLK_BA+0x60	R/W	Clock Output Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		DIV1EN	CLKOEN	FREQSEL			

Bits	Description	
[31:6]	**Reserved**	Reserved.
[5]	**DIV1EN**	**Clock Output Divide One Enable Bit** 0 = Clock Output will output clock with source frequency divided by FREQSEL. 1 = Clock Output will output clock with source frequency.
[4]	**CLKOEN**	**Clock Output Enable Bit** 0 = Clock Output function Disabled. 1 = Clock Output function Enabled.
[3:0]	**FREQSEL**	**Clock Output Frequency Selection** The formula of output frequency is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$. F_{in} is the input clock frequency. F_{out} is the frequency of divider output clock. N is the 4-bit value of FREQSEL[3:0].

Clock Fail Detector Control Register (CLK_CLKDCTL)

Register	Offset	R/W	Description	Reset Value
CLK_CLKDCTL	CLK_BA+0x70	R/W	Clock Fail Detector Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						HXTFQIEN	HXTFQDEN
15	14	13	12	11	10	9	8
Reserved		LXTFIEN	LXTFDEN	Reserved			
7	6	5	4	3	2	1	0
Reserved		HXTFIEN	HXTFDEN	Reserved			

Bits	Description	
[31:18]	**Reserved**	Reserved.
[17]	**HXTFQIEN**	**HXT Clock Frequency Range Detector Interrupt Enable Bit** 0 = External high speed crystal oscillator (HXT) clock frequency range detector fail interrupt Disabled. 1 = External high speed crystal oscillator (HXT) clock frequency range detector fail interrupt Enabled.
[16]	**HXTFQDEN**	**HXT Clock Frequency Range Detector Enable Bit** 0 = External high speed crystal oscillator (HXT) clock frequency range detector Disabled. 1 = External high speed crystal oscillator (HXT) clock frequency range detector Enabled.
[15:14]	**Reserved**	Reserved.
[13]	**LXTFIEN**	**LXT Clock Fail Interrupt Enable Bit** 0 = External low speed crystal oscillator (LXT) clock fail interrupt Disabled. 1 = External low speed crystal oscillator (LXT) clock fail interrupt Enabled.
[12]	**LXTFDEN**	**LXT Clock Fail Detector Enable Bit** 0 = External low speed crystal oscillator (LXT) clock fail detector Disabled. 1 = External low speed crystal oscillator (LXT) clock fail detector Enabled.
[11:6]	**Reserved**	Reserved.
[5]	**HXTFIEN**	**HXT Clock Fail Interrupt Enable Bit** 0 = External high speed crystal oscillator (HXT) clock fail interrupt Disabled. 1 = External high speed crystal oscillator (HXT) clock fail interrupt Enabled.
[4]	**HXTFDEN**	**HXT Clock Fail Detector Enable Bit** 0 = External high speed crystal oscillator (HXT) clock fail detector Disabled. 1 = External high speed crystal oscillator (HXT) clock fail detector Enabled.
[3:0]	**Reserved**	Reserved.

Clock Fail Detector Status Register (CLK_CLKDSTS)

Register	Offset	R/W	Description	Reset Value
CLK_CLKDSTS	CLK_BA+0x74	R/W	Clock Fail Detector Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							HXTFQIF
7	6	5	4	3	2	1	0
Reserved						LXTFIF	HXTFIF

Bits	Description	
[31:9]	**Reserved**	Reserved.
[8]	**HXTFQIF**	**HXT Clock Frequency Range Detector Interrupt Flag (Write Protect)** 0 = External high speed crystal oscillator (HXT) clock frequency is normal. 1 = External high speed crystal oscillator (HXT) clock frequency is abnormal. **Note:** Write 1 to clear the bit to 0.
[7:2]	**Reserved**	Reserved.
[1]	**LXTFIF**	**LXT Clock Fail Interrupt Flag (Write Protect)** 0 = External low speed crystal oscillator (LXT) clock is normal. 1 = External low speed crystal oscillator (LXT) stops. **Note:** Write 1 to clear the bit to 0.
[0]	**HXTFIF**	**HXT Clock Fail Interrupt Flag (Write Protect)** 0 = External high speed crystal oscillator (HXT) clock is normal. 1 = External high speed crystal oscillator (HXT) clock stops. **Note:** Write 1 to clear the bit to 0.

Clock Frequency Range Detector Upper Boundary Register (CLK_CDUPB)

Register	Offset	R/W	Description	Reset Value
CLK_CDUPB	CLK_BA+0x78	R/W	Clock Frequency Range Detector Upper Boundary Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						UPERBD	
7	6	5	4	3	2	1	0
UPERBD							

Bits	Description	
[31:10]	**Reserved**	Reserved.
[9:0]	**UPERBD**	**HXT Clock Frequency Range Detector Upper Boundary Value** The bits define the maximum value of frequency range detector window. When HXT frequency is higher than this maximum frequency value, the HXT Clock Frequency Range Detector Interrupt Flag will be set to 1.

Clock Frequency Range Detector Lower Boundary Register (CLK_CDLOWB)

Register	Offset	R/W	Description	Reset Value
CLK_CDLOWB	CLK_BA+0x7c	R/W	Clock Frequency Range Detector Lower Boundary Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						LOWERBD	
7	6	5	4	3	2	1	0
LOWERBD							

Bits	Description	
[31:10]	**Reserved**	Reserved.
[9:0]	**LOWERBD**	**HXT Clock Frequency Range Detector Lower Boundary Value** The bits define the minimum value of frequency range detector window. When HXT frequency lower than this minimum frequency value, the HXT Clock Frequency Range Detector Interrupt Flag will set to 1.

Frequency out of range will be asserted when HIRC_period*1024> HXT_period*CLK_DUPB or HIRC_period*1024 < HXT_period*CLK_CDLOWB

HXT Filter Select Control Register (CLK_HXTFSEL)

Register	Offset	R/W	Description	Reset Value
CLK_HXTFSEL	CLK_BA+0xB4	R/W	HXT Filter Select Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							**HXTFSEL**

Bits	Description	
[31:1]	**Reserved**	Reserved.
[0]	**HXTFSEL**	**HXT Filter Select** 0 = HXT frequency is greater than12 MHz. 1 = HXT frequency is less than or equal to 12 MHz. **Note:** This bit should not be changed during HXT running.

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

This chip is equipped with 16/32/64/128 Kbytes on-chip embedded Flash for application and Data Flash to store some application dependent data. A User Configuration block provides for system initialization. A 2/4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function with 128 Kbytes Flash and 2 Kbytes LDROM for other size Flash. A 512 bytes security protection ROM (SPROM) can conceal user program. This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded Flash updated.

6.4.2 Features

- Supports16/32/64/128 Kbytes application ROM (APROM).
- Supports 2/4 Kbytes loader ROM (LDROM).
- Supports configurable Data Flash size to share with APROM.
- Supports 512 bytes security protection ROM (SPROM) to conceal user program.
- Supports 12 bytes User Configuration block to control system initialization.
- Supports 512 bytes page erase for all embedded Flash.
- Supports CRC-32 checksum calculation function.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 55 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 55 pins are arranged in 5 ports named as PA, PB, PC, PD and PF. PA and PB has 16 pins on port. PC has 9 pins on port. PD has 5 pins on port. PF has 9 pins on port. Each of the 55 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]).

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- Schmitt trigger input
- I/O pin can be configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function
- Supports input 5V tolerance, except analog pin (PA.10 ~ 11; PB.0 ~ 15; PF.2 ~ 5; all USB pin and nRESET pin).

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 5 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports 5 independently configurable channels
- Selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and I^2C, SPI/I^2S, UART, USCI, ADC, PWM and TIMER request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

6.7.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- Supports event counting source from internal USB SOF signal
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports internal capture triggered while internal ACMP output signal and LIRC transition
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, ADC, PDMA function
- Supports Inter-Timer trigger mode

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.8.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 416us ~ 27.3 s if WDT_CLK = 38.4 kHz (LIRC).
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT.

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.9.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.10 PWM Generator and Capture Timer (PWM)

6.10.1 Overview

The chip provides two PWM generators — PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.10.2 Features

6.10.2.1 PWM Function Features

- Supports maximum clock frequency up to 96 MHz
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up-down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM counter matches 0, period value or compared value

6.10.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution

- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for PWM all channels

6.11 UART Interface Controller (UART)

6.11.1 Overview

The chip provides three channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.11.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Support Single-wire function mode.
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function (Only UART0 /UART1 with Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function)
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT. (Only UART0 /UART1 with this feature)
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function

UART Feature	UART0/ UART1	UART2		USCI-UART

FIFO	16 Bytes	1 Bytes		TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√		√
IrDA	√	√		-
LIN	-	-		-
RS-485 Function Mode	√	√		√
nCTS Wake-up	√	√		√
Imcoming Data Wake-up	√	√		√
Received Data FIFO reached threshold Wake-up	√	-		-
RS-485 Address Match (AAD mode) Wake-up	√	-		-
Auto-Baud Rate Measurement	√	√		√
STOP Bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit		1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits		6~13 bits
Even / Odd Parity	√	√		√
Stick Bit	√	√		-
Note: √= Supported				

Table 6.11-1 NuMicro® M031 Series UART Features

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one set of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I^2S mode to connect external audio CODEC.

6.12.2 Features

- SPI Mode
  - Supports one set of SPI controller
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers which depended on SPI setting of data width
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Master mode up to 24 MHz and Slave mode up to 16 MHz (when chip works at V_{DD} = 1.8~3.6V)
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
  - Supports PDMA transfer
- I^2S Mode
  - Supports one set of I^2S by SPI controller
  - Interface with external audio CODEC
  - Supports Master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports two PDMA requests, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary

6.13 I²C Serial Interface Controller (I²C)

6.13.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers which support Power-down wake-up function.

6.13.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps) and Fast mode (400 kbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports two-level buffer function
- Supports setup/hold time programmable

6.14 USCI - Universal Serial Control Interface Controller (USCI)

6.14.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.14.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.15 USCI – UART Mode

6.15.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system.

6.15.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wakeup Only)

6.16 USCI - SPI Mode

6.16.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as Master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in Master and Slave mode are shown below.

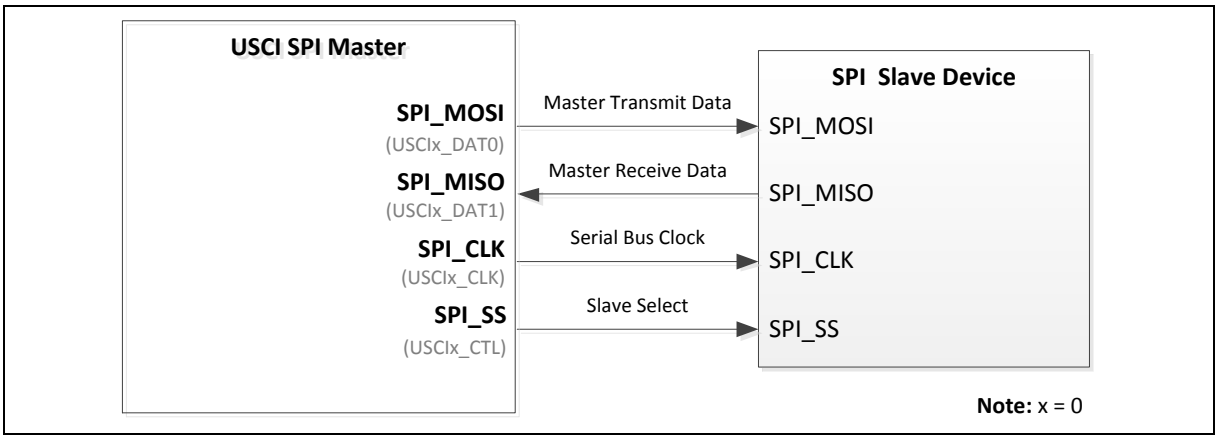


Figure 6.16-1 SPI Master Mode Application Block Diagram

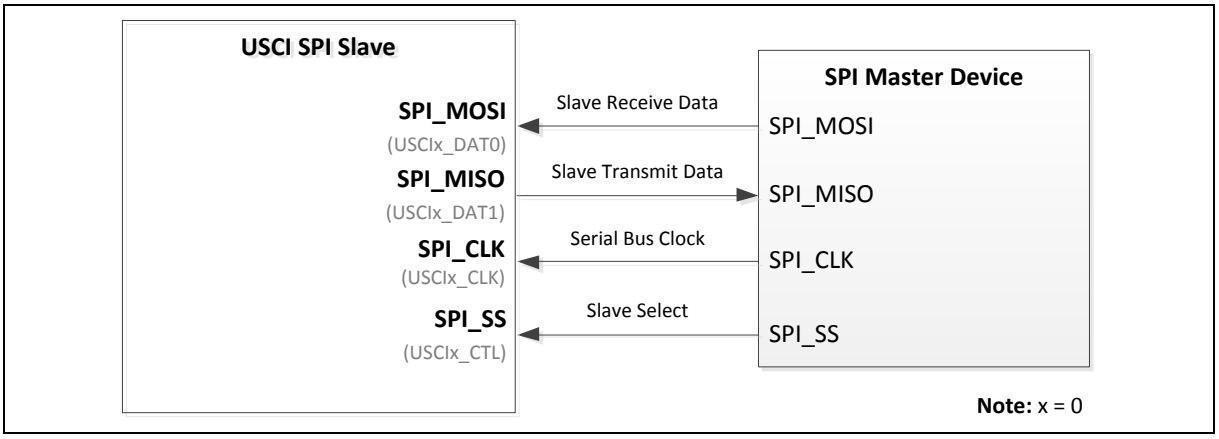


Figure 6.16-2 SPI Slave Mode Application Block Diagram

6.16.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence

- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.17 USCI - I²C Mode

6.17.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.17-1 for more detailed I²C BUS Timing.

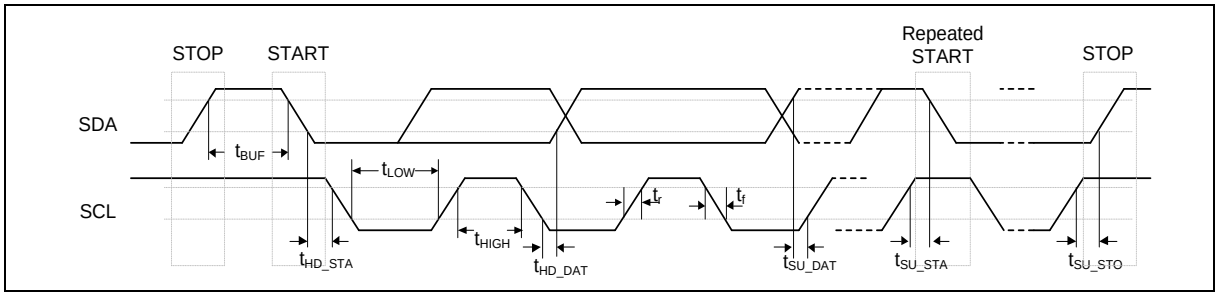


Figure 6.17-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode .

6.17.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.18 External Bus Interface (EBI)

6.18.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.18.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports Address/Data multiplexed Mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)

6.19 USB Device Controller (USBD)

6.19.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 Bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 8 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register USBD_EPSTS0 to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.19.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (SOF, NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 8 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 byte buffer size
- Provides remote wake-up capability

6.20 CRC Controller (CRC)

6.20.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.20.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.21 Hardware Divider (HDIV)

6.21.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.21.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Write divisor to trigger calculation
- Waiting for calculation ready automatically when reading quotient and remainder

6.22 Analog-to-Digital Converter (ADC)

6.22.1 Overview

The ADC contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 16 input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC/PF.5), timer0~3 overflow pulse trigger and PWM trigger.

6.22.2 Features

- Operating voltage: 1.8V~3.6V.
- Analog input voltage: 0 ~ AV_{DD}.
- Supports external reference voltage from VREF pin.
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 16 single-end analog input channels or 8 differential analog input channels.
- Maximum ADC peripheral clock frequency is 48 MHz.
- Up to 2 MSPS sampling rate.
- Scan on enabled channels
- Threshold voltage detection
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit.
  - External pin (STADC).
  - Timer 0~3 overflow pulse trigger.
  - PWM trigger.
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Supports extend sample time function (0~255 ADC clock).
- One internal channel from band-gap voltage (VBG).
- Supports PDMA transfer mode.
- Supports Calibration mode.

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300 k SPS.

Note3: The ADC Clock frequency must be slower than or equal to PCLK.

6.23 Analog Comparator Controller (ACMP)

6.23.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.23.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 3 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 3 negative sources:
    - ACMP1_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for PWM
- Supports window compare mode and window latch mode

6.24 Peripherals Interconnection

6.24.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interaction without CPU saves CPU resources, reduces power consumption, and allows for operation with no software latency and fast responds.

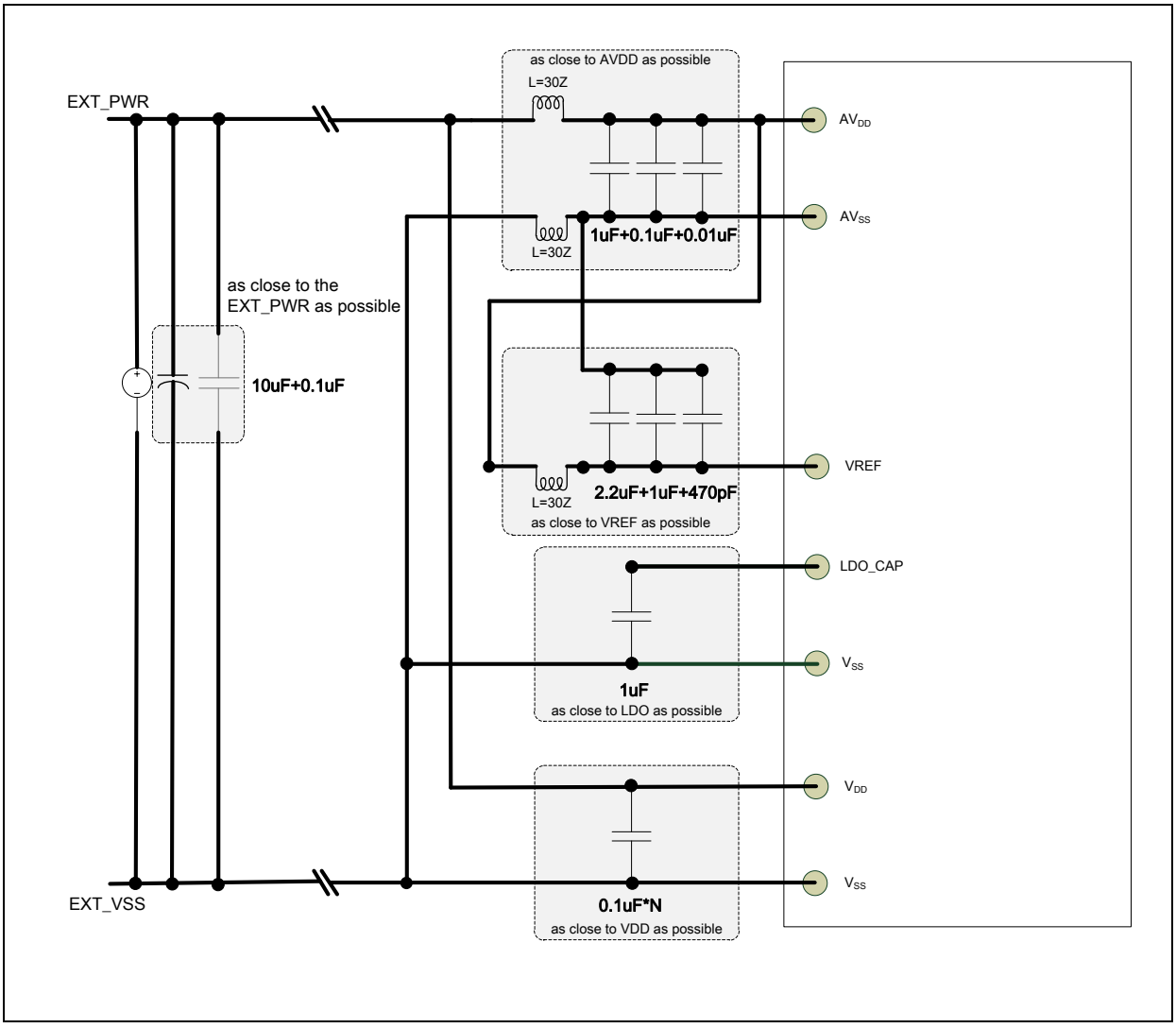
6.24.2 Peripherals Interconnect Matrix Table

Source	Destination				
	ADC	HIRC TRIM	PWM	Timer	UART/USCI
ACMP	-	-	3	6	-
BOD	-	-	3	-	-
Clock Fail	-	-	3	-	-
CPU Lockup	-	-	3	-	-
LIRC	-	-	-	6	-
HXT	-	-	-	-	
LXT	-	2	-	-	
PWM	1	-	4	-	8
Timer	1	-	5	7	-
USB 1.1 Device	-	2	-		-

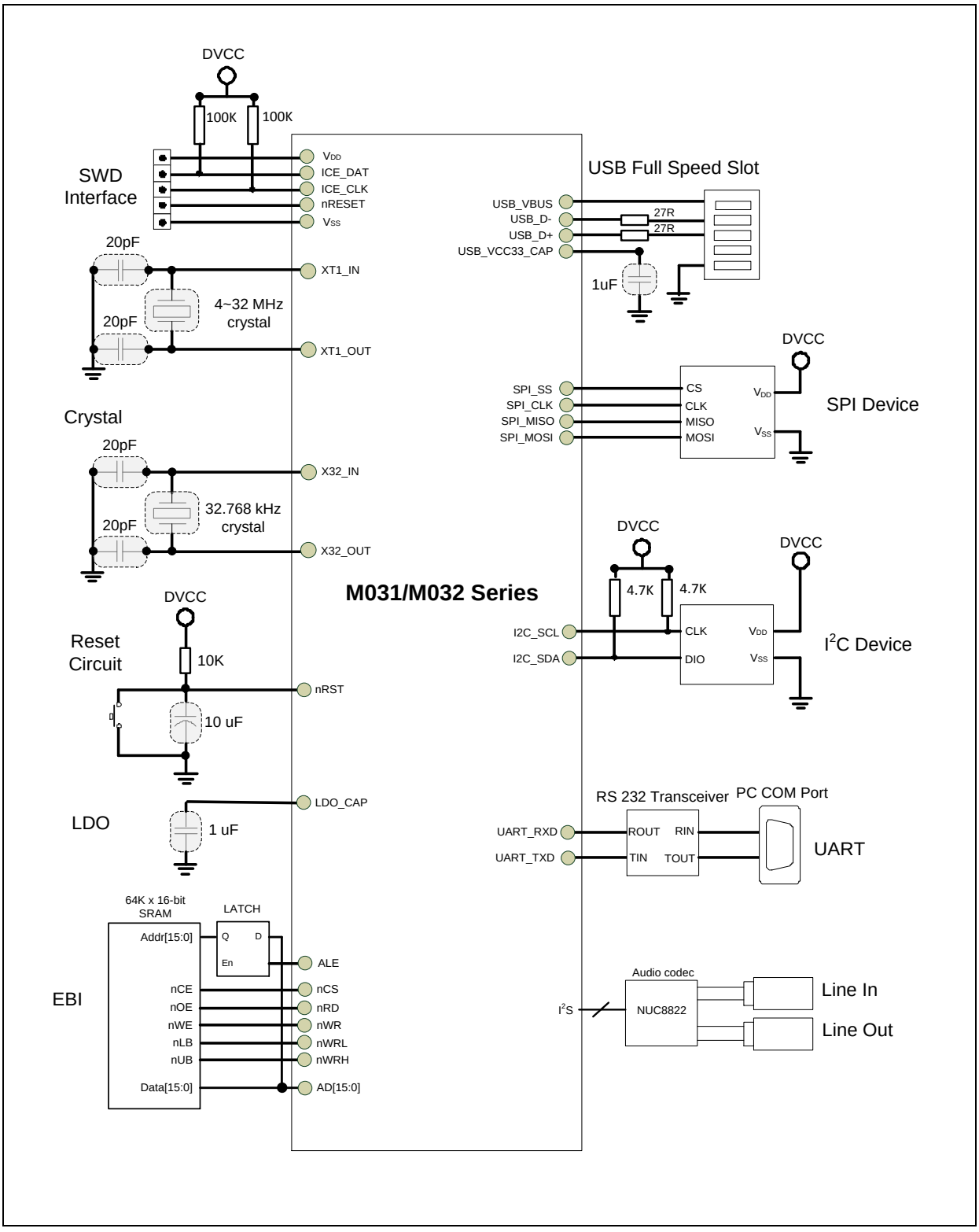
Table 6.24-1 Peripherals Interconnect Matrix Table

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



7.2 Peripheral Application Scheme



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	4.0	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on 5V-tolerance I/O	V_{SS}-0.3	5.5	V
	Input voltage on any other pin[*2]	V_{SS}-0.3	4.0	V

Note:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Non 5V-tolerance I/O includes PA.10 ~ 11; PB.0 ~ 15; PF.2, 3, 4, 5; all USB pin and nRESET pin. V_{IN} maximum value must be respected to avoid permanent damage. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	150	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$[*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$[*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>A_{VDD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA} [*1]	Thermal resistance junction-ambient 20-pin TSSOP(4.4x6.5 mm)	-	38	-	°C/Watt
	Thermal resistance junction-ambient 28-pin TSSOP(4.4x9.7 mm)	-	30	-	°C/Watt
	Thermal resistance junction-ambient 33-pin QFN(4x4 mm)	-	28	-	°C/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	°C/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	°C/Watt
	Thermal resistance junction-ambient 128-pin LQFP(14x14 mm)	-	38.5	-	°C/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-6000	-	+6000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[*3]	-400	-	+400	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.1-4 EMC Characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
20-pin TSSOP(4.4x6.5 mm) [*1]	MSL 3
28-pin TSSOP(4.4x9.7 mm) [*1]	MSL 3
33-pin QFN(4x4 mm) [*1]	MSL 3
48-pin LQFP(7x7 mm) [*1]	MSL 3
64-pin LQFP(7x7 mm) [*1]	MSL 3
128-pin LQFP(14x14 mm) [*1]	MSL 3
Note: 1. Determined according to IPC/JEDEC J-STD-020	

Table 8.1-5 Package Moisture Sensitivity (MSL)

8.1.6 Soldering Profile

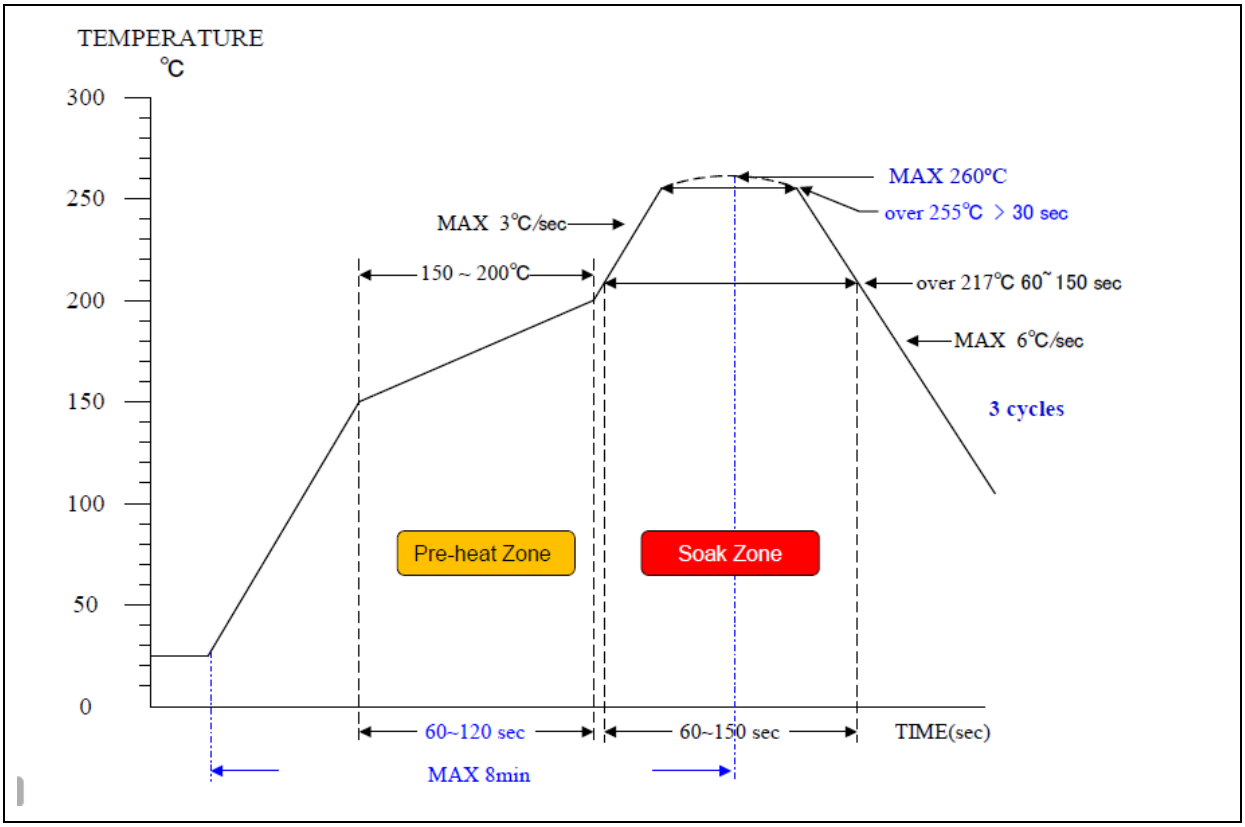


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260°C
Ramp-down rate	6°C/sec ax.
Time 25°C to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 1.8 ~ 3.6V, T_A = 25°C, HCLK = 48 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz	
V_{DD}	Operation voltage	1.8	-	3.6	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	1.8	-	AV_{DD}		$AV_{DD} - V_{REF} < 1.2$ V
V_{LDO}	LDO output voltage	-	1.8	-		
V_{BG}[*4]	Band-gap voltage	1.14	1.2	1.26		
C_{LDO}[*2]	LDO output capacitor on each pin	1				
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	0.1	-	10	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	150	-	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	2.25	-	µC	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 150 mA for 15 us

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1. 8V ~ 3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	48 MHz	8.5	9.78	TBD	TBD	mA
		32 MHz	5.6	6.44	TBD	TBD	
		24 MHz	5	5.75	TBD	TBD	
		12 MHz	3.6	4.14	TBD	TBD	
		4 MHz	2.4	TBD	TBD	TBD	
		38.4 kHz	0.095	0.119	TBD	TBD	
		32.768 kHz	0.095	0.119	TBD	TBD	
	Normal run mode, executed from Flash, all peripherals enable	48 MHz	17.5	20.2	TBD	TBD	
		32 MHz	11.5	13.1	TBD	TBD	
		24 MHz	9.5	10.9	TBD	TBD	
		12 MHz	5.6	6.4	TBD	TBD	
		4 MHz	2.9	TBD	TBD	TBD	
		38.4 kHz	0.103	0.128	TBD	TBD	
		32.768 kHz	0.103	0.128	TBD	TBD	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ	Max[*1] [*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable	48 MHz	3.3	3.8	TBD	TBD	mA
		32 MHz	2.2	2.5	TBD	TBD	
		24 MHz	2.35	2.7	TBD	TBD	
		12 MHz	1.83	2.1	TBD	TBD	
		4 MHz	1.51	TBD	TBD	TBD	
		38.4 kHz	0.093	0.117	TBD	TBD	
		32.768 kHz	0.093	0.117	TBD	TBD	
	Idle mode, all peripherals enable	48 MHz	12.8	14.7	TBD	TBD	
		32 MHz	8.3	9.55	TBD	TBD	
		24 MHz	7.2	8.28	TBD	TBD	
		12 MHz	4.3	4.95	TBD	TBD	
		4 MHz	2.43	TBD	TBD	TBD	
		38.4 kHz	0.099	0.124	TBD	TBD	
		32.768 kHz	0.099	0.124	TBD	TBD	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current Consumption in Idle Mode

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 38.4 kHz	Typ[*2]	Max[*3][*4]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	12	TBD [*5]	TBD	TBD [*5]	µA
	Power-down mode, WDT/Timer/UART enable	V	-	13.5	TBD	TBD	TBD	
	Power-down mode, WDT/Timer/UART enable	-	V	12.5	TBD	TBD	TBD	
	Power-down mode, WDT use LIRC, UART/Timer use LXT	V	V	14	TBD	TBD	TBD	

Note:

1. Crystal used: AURUM XF66RU000032C0 with a CL of 20 pF for typical values
2. V_{DD} = AV_{DD} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption in Power-down Mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 48 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
ADC[*2]	TBD	mA
ACMP01[*3]	TBD	
PWM0	1.23	
PWM1	1.23	
WDT/WWDT	0.12	
SPI/I2S	TBD	
UART0	0.56	
UART1	0.56	
UART2	0.56	
I2C0	TBD	
I2C1	TBD	
USCI0	0.60	
EBI	TBD	
TMR0	0.28	
TMR1	0.27	
TMR2	0.28	
TMR3	0.27	
USB FS Device	TBD	
CRC	TBD	
EBI	TBD	
PDMA	TBD	
ADC[*2]	TBD	

Note:
1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	5	6	cycles
t_{WU_NPD}[*1][*2]	Wakeup from normal power down mode	TBD	TBD	μs

Note:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

Table 8.3-5 Low-power Mode Wakeup Timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} except 5V-tolenece I/O should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	NA		Injected current on any other 5V-tolerance I/O

Table 8.3-6 I/O Current Injection Characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	0	-	$0.3*V_{DD}$	V	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1		1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5$ V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1] [*3]	Pull up resistor	-	45	-	kΩ	V_{DD} = 3.3 V, Quasi mode
		-	120	-		V_{DD} = 1.8 V, Quasi mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 8.3-7 I/O Input Characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-25.5	-28	-31	μA	V_{DD} = 3.3 V V_{IN}=(V_{DD}-0.4) V
		-19	-22	-24	μA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
		-10.5	-13	-16	μA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	-8.5	-10	-11	mA	V_{DD} = 3.3 V V_{IN}=(V_{DD}-0.4) V
		-7	-8	-9	mA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
		-4.4	-5.5	-6.5	mA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2]	Sink current for push-pull mode and low level	8	9.5	11	mA	V_{DD} = 3.3 V V_{IN}= 0.4 V
		7	7.5	9	mA	V_{DD} = 2.5 V V_{IN}= 0.4 V
		4.3	5	6.3	mA	V_{DD} = 1.8 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O Output Characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	-	45	-	KΩ	V_{DD} = 3.3 V
		-	120	-		V_{DD} = 1.8 V
t_{FR}[*1]	nRESET input filtered pulse time	-	32	-	μs	Normal run and Idle mode
		75	-	155		Power down mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

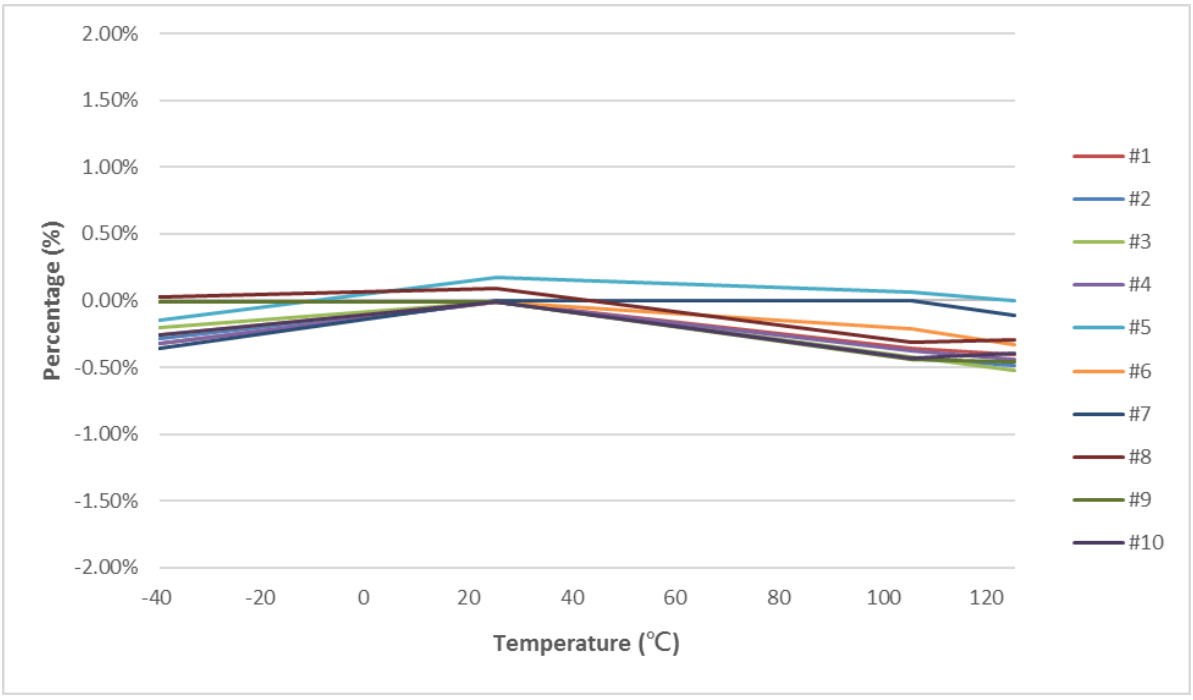
The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[*1]	-	2[*1]	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.8 ~ 3.6V
I_{HRC}[*1]	Operating current	-	TBD	-	µA	
T_S[*2]	Stable time	-	11	15	µs	T_A = -40°C ~ +105 °C, V_{DD} = 1.8 ~ 3.6V

Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-148 MHz Internal High Speed RC Oscillator(HIRC) Characteristics



Note: Test condition V_{DD}=3.3V, Temp = -40~125°C

Figure 8.4-1 HIRC vs. Temperature

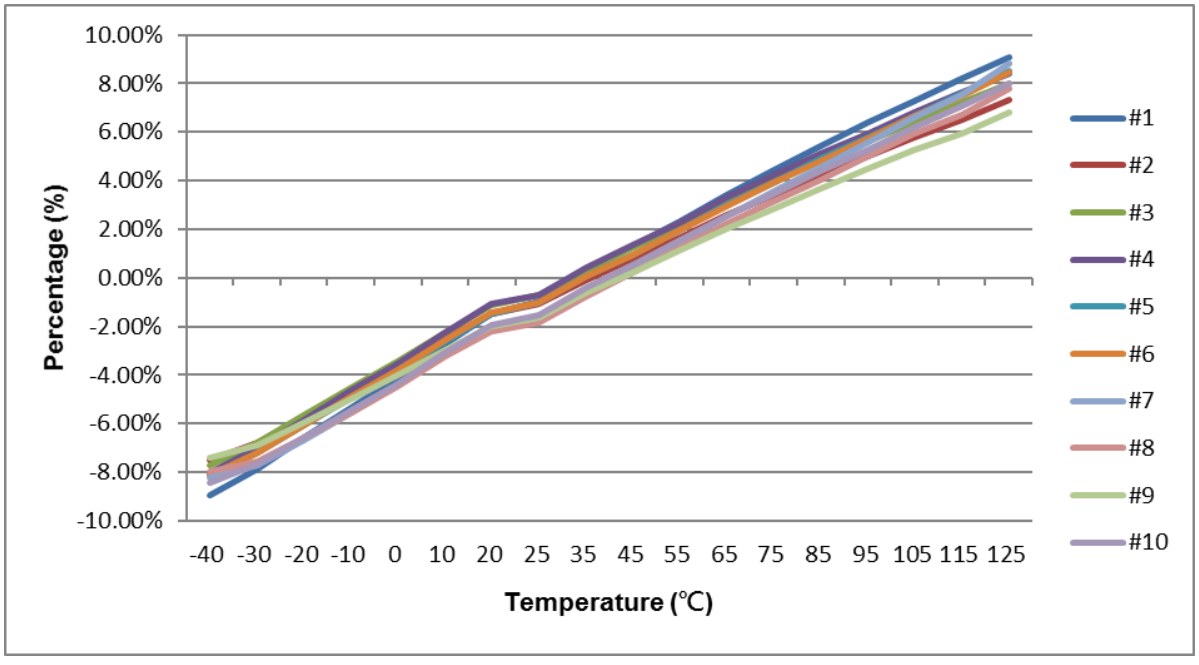
8.4.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
F_{LRC} [*2]	Oscillator frequnecy	38.016	38.4	38.784	kHz	
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-15	-	15	%	T_A=-40~105 °C V_{DD}=1.8V~3.6V Without software calibration
I_{LRC}	Operating current	-	0.85	1	µA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	µs	T_A=-40~105 °C V_{DD}=1.8V~3.6V

Note:

1. Guaranteed by characterization, not tested in production.
2. The 38.4 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

Table 8.4-238.4 kHz Internal Low Speed RC Oscillator(LIRC) characteristics



Note: Test condition V_{DD}=3.3V, Temp = -40~125°C

Figure 8.4-2 LIRC vs. Temperature

8.4.3 External 4~32 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
R_f	Internal feedback resister	-	200	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	32	MHz	
I_{HXT}	Current consumption	-	120	200	μA	4 MHz, Gain = L0
			170	300		8 MHz, Gain = L1
		-	250	450		12 MHz, Gain = L2
		-	350	600		16 Mhz, Gain = L3
			500	850		24 MHz, Gain = L4
		-	650	1100		32 MHz, Gain = L7
T_S	Stable time	-	1700	2200	μs	4 MHz, Gain = L0
			900	1100		8 MHz, Gain = L1
		-	600	740		12 MHz, Gain = L2
		-	450	650		16 Mhz, Gain = L3
		-	400	600		24 MHz, Gain = L4
		-	350	550		32 MHz, Gain = L7
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	-	1	-	V	

Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-3 External 4~32 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	TBD	-	Ω	Crystal @4 MHz
		-	TBD	-		Crystal @12 MHz
		-	TBD	-		Crystal @16 MHz
		-	TBD	-		Crystal @24 MHz
		-	TBD	-		Crystal @32 MHz

Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-4 External 4~32 MHz High Speed Crystal Characteristics

8.4.3.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 32 MHz	10 ~ 25 pF	10 ~ 25 pF	without

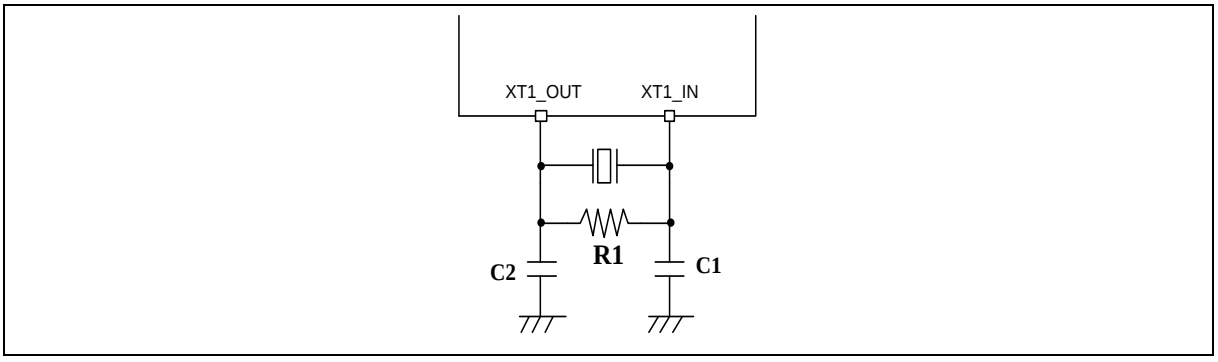
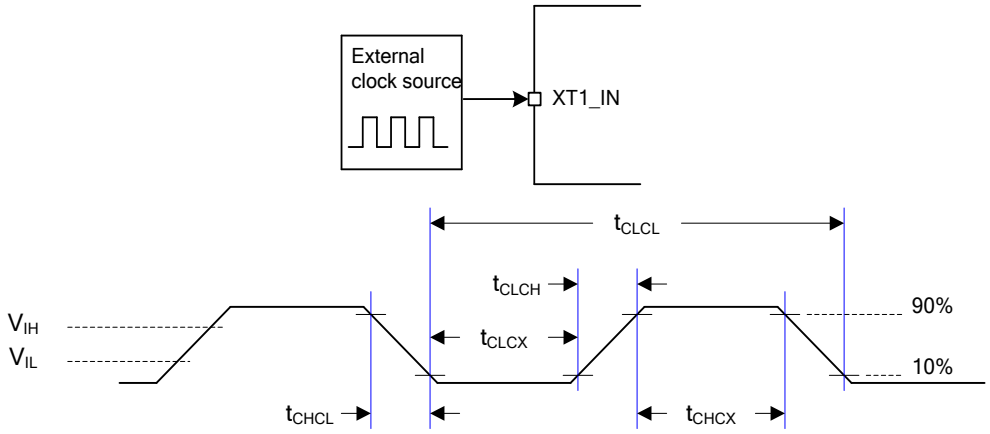


Figure 8.4-3 Typical Crystal Application Circuit

8.4.4 External 4~32 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	32	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~32 MHz High Speed Clock Input Signal

8.4.5 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	1.8	-	3.6	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	15	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	1.5	6	μA	ESR=35 kΩ, Gain = L1
		-	2	6		ESR=70 kΩ, Gain = L2
Ts_{LXT}	Stable time	-	500	900	ms	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	-	TBD	-	V	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-6 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 8.4-7 External 32.768 kHz Low Speed Crystal Characteristics

8.4.5.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	20 pF	20 pF	without

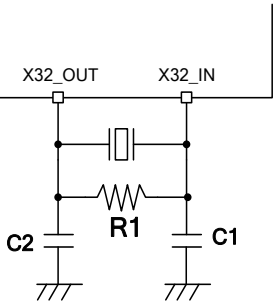
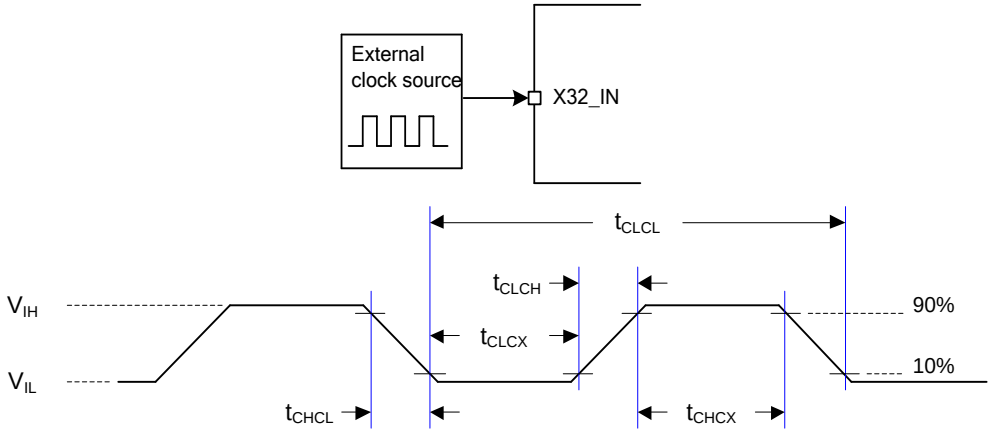


Figure 8.4-4 Typical 32.768 kHz Crystal Application Circuit

8.4.6 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LSE_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	ns	
t_{CLCX}	Clock low time	450	-	-	ns	
t_{CLCH}	Clock rise time	-	-	50	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	ns	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	40	-	60	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by design, not tested in production

Table 8.4-8 External 32.768 kHz Low Speed Clock Input Signal

8.4.7 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	3.2	-	32	MHz	
f_{PLL_OUT}	PLL multiplier output clock	50	-	96	MHz	
f_{PLL_REF}	PLL reference clock	0.8	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	200	-	500	MHz	
T_L	PLL locking time	-	-	500	µs	
Jitter[*2]	Cycle-to-cycle Jitter	-	200	350	ps	
I_{DD}	Power consumption	-	3.1	5	mA	V_{DD} =3.3V @ f_{PLL_OUT} = 96 MHz

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-9 PLL Characteristics

8.4.8 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time	-	5.5	ns	C_L = 30 pF, V_{DD} >= 2.7 V
		-	3		C_L = 10 pF, V_{DD} >= 2.7 V
		-	8.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	4.5		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time	-	5.5	ns	C_L = 30 pF, V_{DD} >= 2.7 V
		-	3		C_L = 10 pF, V_{DD} >= 2.7 V
		-	8.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	4.5		C_L = 10 pF, V_{DD} >= 1.8 V
$f_{max(IO)out}$[*3]	I/O maximum frequency	-	60	MHz	C_L = 30 pF, V_{DD} >= 2.7 V
		-	110		C_L = 10 pF, V_{DD} >= 2.7 V
		-	40		C_L = 30 pF, V_{DD} >= 1.8 V
		-	75		C_L = 10 pF, V_{DD} >= 1.8 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Note:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-10 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	1.8	-	3.6	V	
V_{LDO}	Output voltage	-	1.8	-	V	
T_A	Temperature	-40	-	105	°C	

Note

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest VSS pin of the device.
2. For ensuring power stability, a 1μF capacitor must be connected between LDO_CAP pin and the closest VSS pin of the device.

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	20	30	μA	AV_{DD} = 3.6V
I_{LVR}[*1]	LVR operating current	-	2	TBD		AV_{DD} = 3.6V
I_{BOD}[*1]	BOD operating current	-	3	TBD		AV_{DD} = 3.6V
V_{POR}	POR reset voltage	1.35	1.5	1.65	V	-
V_{LVR}	LVR reset voltage	1.6	1.7	1.8		
V_{BOD}	BOD brown-out detect voltage	1.8	2.0	2.2		BODVL = 0
		2.3	2.5	2.7		BODVL = 1
T_{LVR_SU}[*1]	LVR startup time	-	TBD	-	μs	-
T_{LVR_RE}[*1]	LVR respond time	-	TBD	-		-
T_{BOD_SU}[*1]	BOD startup time	-	TBD	-		-
T_{BOD_RE}[*1]	BOD respond time	-	TBD	-		-
R_{VDDR}[*1]	V_{DD} rise time rate	10	-	-	μs/V	POR Enabled
R_{VDDF}[*1]	V_{DD} fall time rate	10	-	-		POR Enabled
		TBD	-	-		LVR Enabled
		TBD	-	-		BOD 2.0V Enabled
		TBD	-	-		BOD 2.5V Enabled

Note:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and Power Control Unit

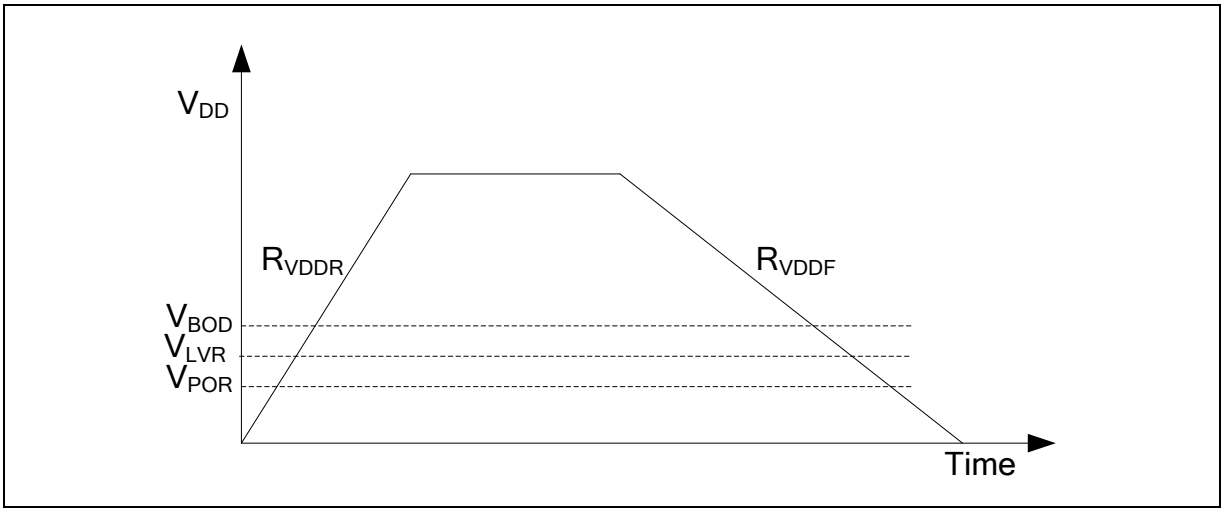


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR ADC

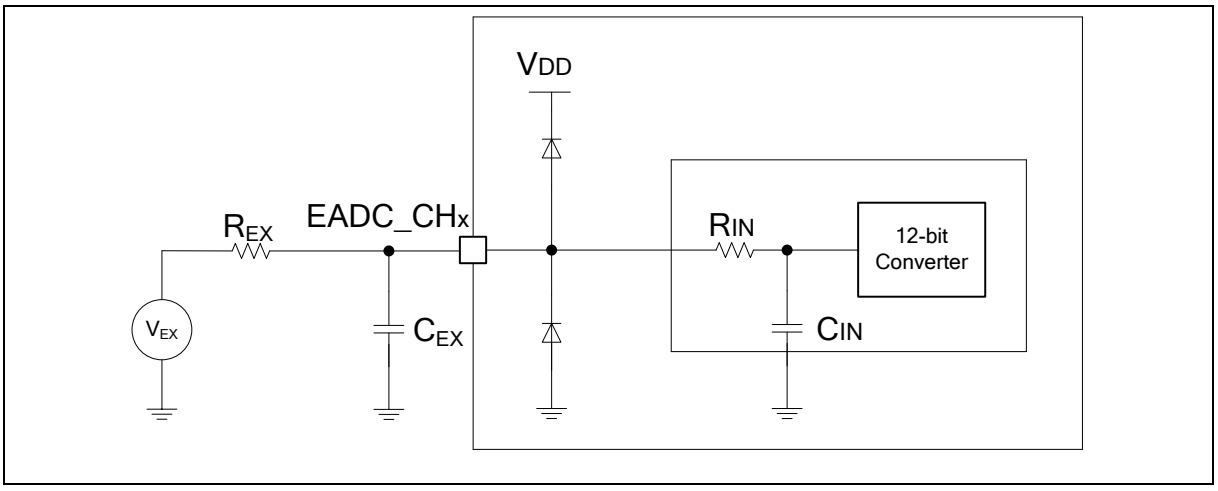
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog operating voltage	1.8	-	3.6	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.8	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
V_{CM}	Common-Mode Input Range	$V_{REF}/2$			V	Full differential input
I_{ADC}[*1]	Operating current (AV_{DD} + V_{REF} current)	-	-	355	µA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 34 MHz $T_{CONV} = 17 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	4	-	34	MHz	
T_{SMP}	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(ADC_ESMPCTL[7:0]) + 1) * T_{ADC}
T_{CONV}	Conversion time	17	-	272	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 16 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	0.236	-	2	MSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
T_{EN}	Enable to ready time	20	-	-	µs	
INL[*1]	Integral Non-Linearity Error	-2	-	+2	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28
		-4		+4	LSB	$V_{REF} = AV_{DD}$ TSSOP20 and TSSOP28
DNL[*1]	Differential Non-Linearity Error	-1	-	+2	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28
		-1		+4	LSB	$V_{REF} = AV_{DD}$ TSSOP20 and TSSOP28
E_G[*1]	Gain error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28
		-10		+4	LSB	$V_{REF} = AV_{DD}$ TSSOP20 and TSSOP28
E_O[*1]$_T$	Offset error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28
		-4		+10	LSB	$V_{REF} = AV_{DD}$ TSSOP20 and TSSOP28
E_A[*1]	Absolute Error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
		-8		+8	LSB	V_{REF} = AV_{DD} TSSOP20 and TSSOP28
ENOB[*1]	Effective number of bits	-	-	TBD	bits	F_{ADC} = 34 MHz AV_{DD} = V_{DD} = V_{REF} = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	-	TBD	dB	
SNR[*1]	Signal-to-noise ratio	-	-	TBD		
THD[*1]	Total harmonic distortion	-	-	TBD		
C_{IN}[*1]	Internal Capacitance	-	2.9	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	-	2	kΩ	
R_{EX}[*1]	External input impedance	-	-	50	kΩ	

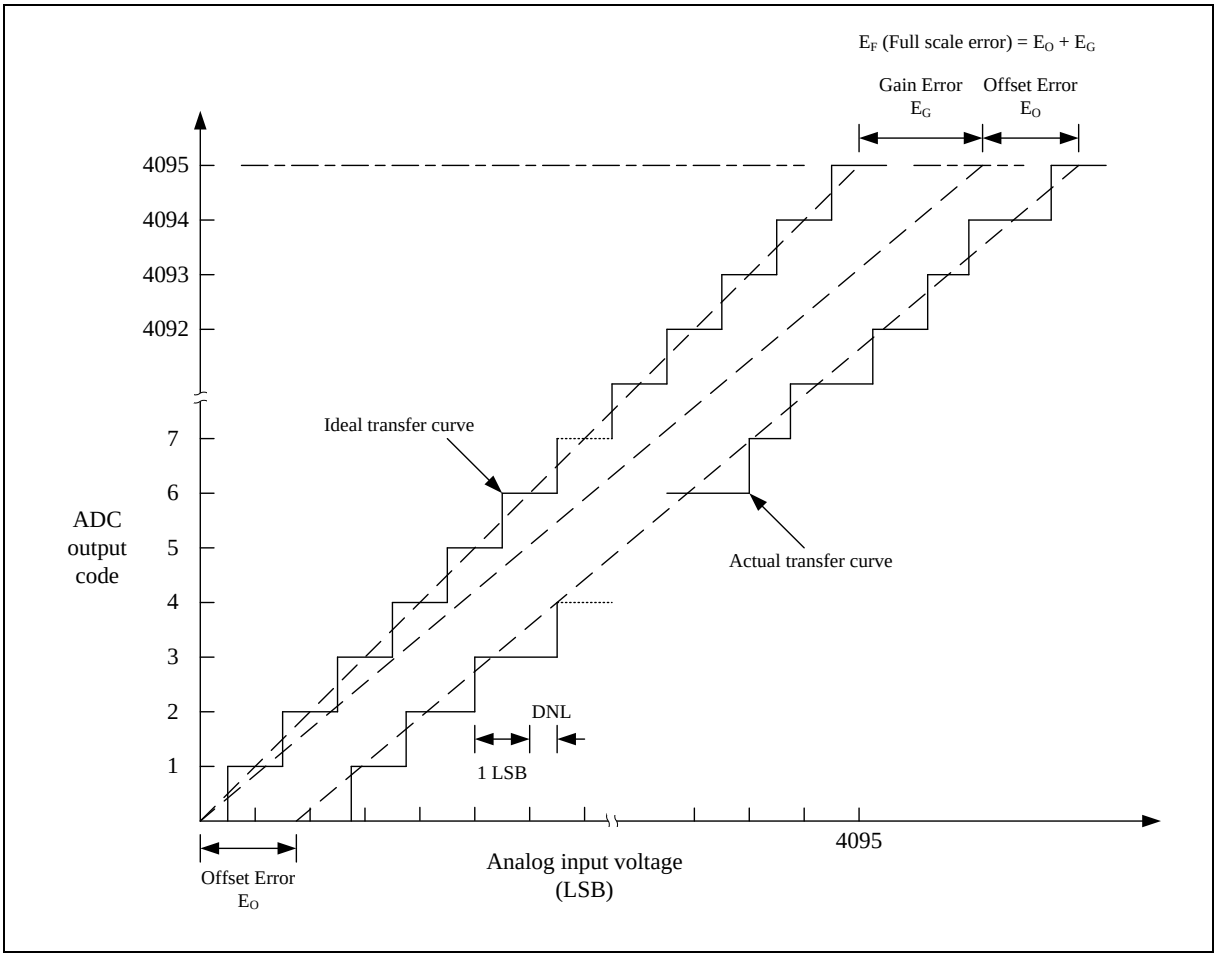
Note:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	2.2	-	3.6	V	$V_{DD} = AV_{DD}$
T_A	Temperature	-40	-	105	˚C	
I_{DD}	Operating current	-	30	45	μA	
V_{CM}[*2]	Input common mode voltage range	0.35	1/2 AV_{DD}	AV_{DD} -0.3		
V_{DI}[*2]	Differential input voltage sensitivity	10	20	-	mV	Hysteresis disable
V_{offset}[*2]	Input offset voltage	-	10	20	mV	Hysteresis disable,
V_{hys}[*2]	Hysteresis window	-	60	140	mV	
A_v[*1]	DC voltage Gain	45	65	75	dB	
T_d[*2]	Propagation delay	-	-	400	nS	
T_{Setup}[*2]	Setup time	-	-	350	uS	
A_{CRV}[*2]	CRV output voltage	-5	-	5	%	AV_{DD} x (1/6+CRVCTL/24)
R_{CRV}[*2]	Unit resistor value	-	4.2	-	kΩ	
T_{SETUP_CRV}[*2]	Setup time	-	-	350	μS	CRV output voltage settle to ±5%
I_{DD_CRV}[*2]	Operating current	-	30	45	μA	

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-2 ACMP Characteristics

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	24	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	24		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	8.5	ns	1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-1 SPI Master Mode Characteristics

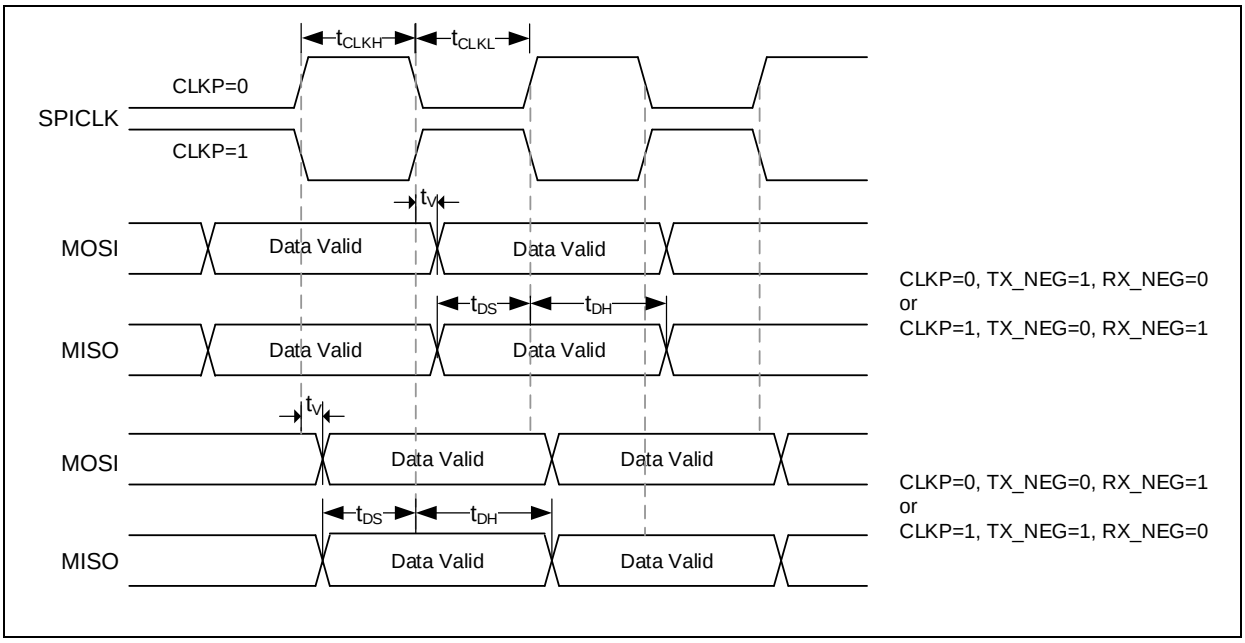


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	16	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
		-	-	16		1.8 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
		1 T_{SPICLK} + 3ns	-	-		1.8 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	1.5	-	-	ns	
t_{DH}	Data input hold time	3.5	-	-	ns	
t_V	Data output valid time	-	-	17.5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
		-	-	25		1.8 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-2 SPI Slave Mode Characteristics

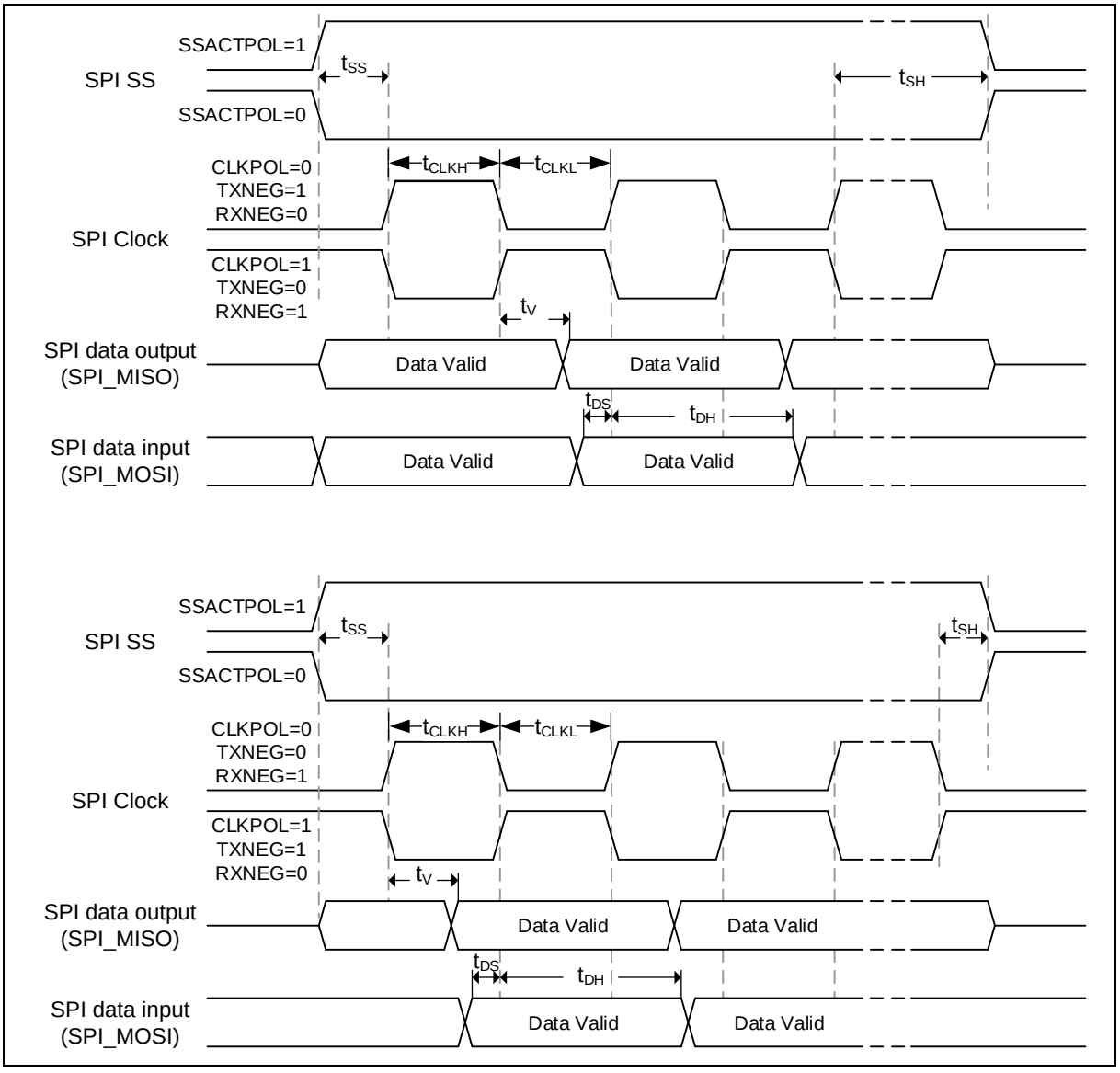


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [*1]	Max [*1]	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	80	-	ns	Master f_{PCLK} = 48 MHz, data: 24 bits, audio frequency = 128 kHz
$t_{w(CKL)}$	I²S clock low time	80	-		
$t_{v(WS)}$	WS valid time	2	6		Master mode
$t_{h(WS)}$	WS hold time	2	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	25		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design.

Table 8.6-3 I²S Characteristics

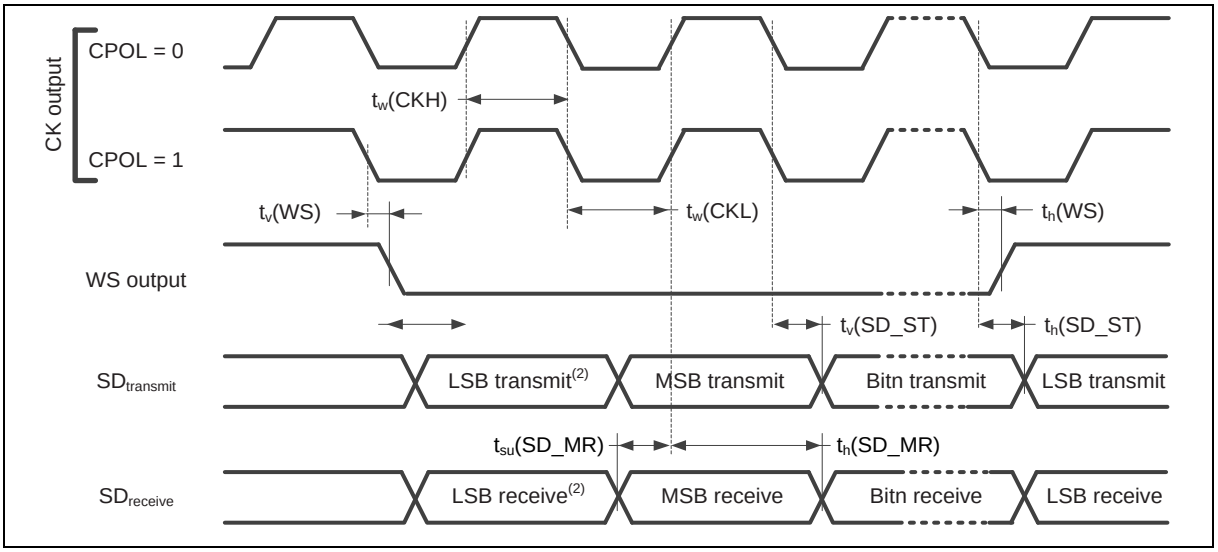


Figure 8.6-3 I2S Master Mode Timing Diagram

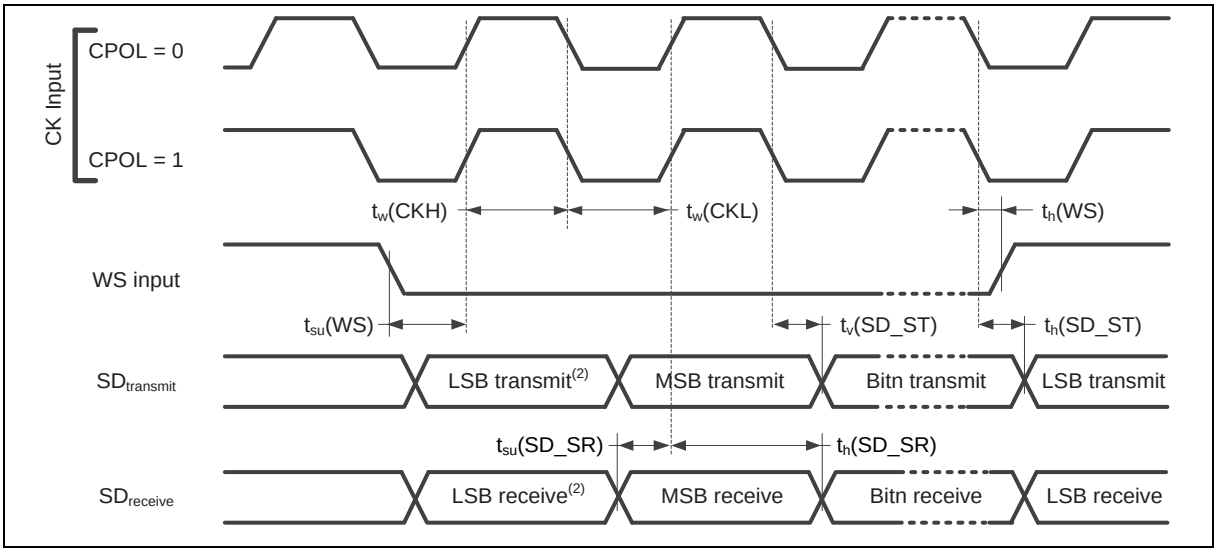


Figure 8.6-4 I^2S Slave Mode Timing Diagram

8.6.3 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μs
t_{HIGH}	SCL high period	4	-	0.6	-	μs
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	0.6	-	μs
$t_{HD;STA}$	START condition hold time	4	-	0.6	-	μs
$t_{SU;STO}$	STOP condition setup time	4	-	0.6	-	μs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-4 I²C Characteristics

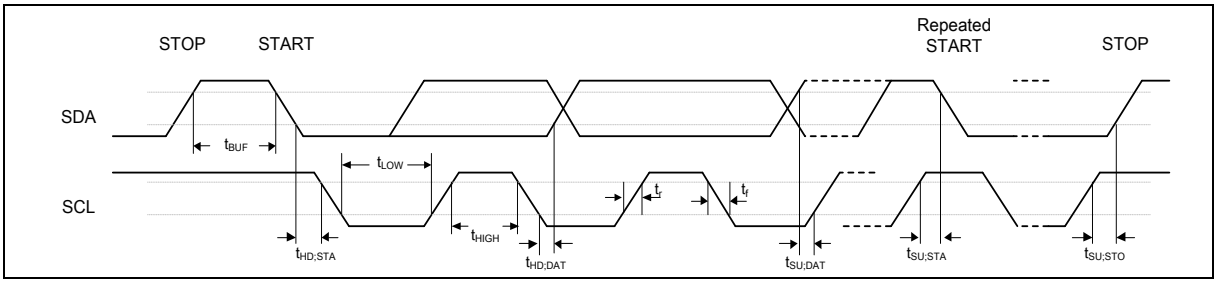


Figure 8.6-5 I²C Timing Diagram

8.6.4 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	24	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	24		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	8.5	ns	1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-5 USCI-SPI Master Mode Characteristics

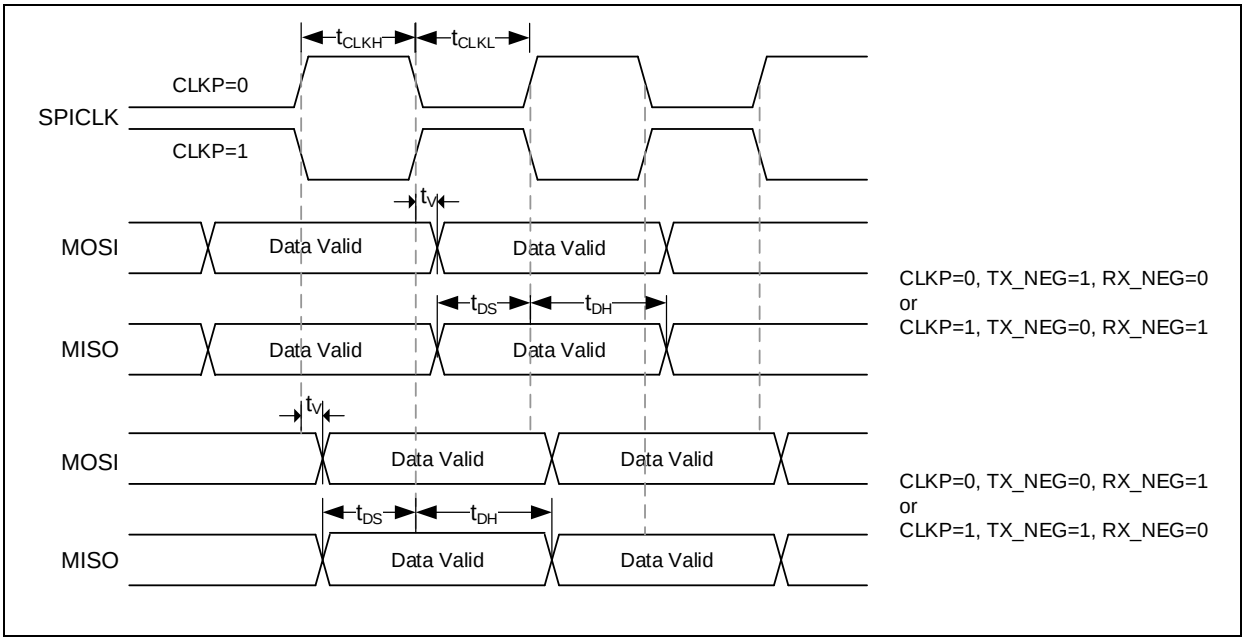


Figure 8.6-6 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	7	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	7		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		1 T_{SPICLK} + 3ns	-	-		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	65	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	70		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-6 USCI-SPI Slave Mode Characteristics

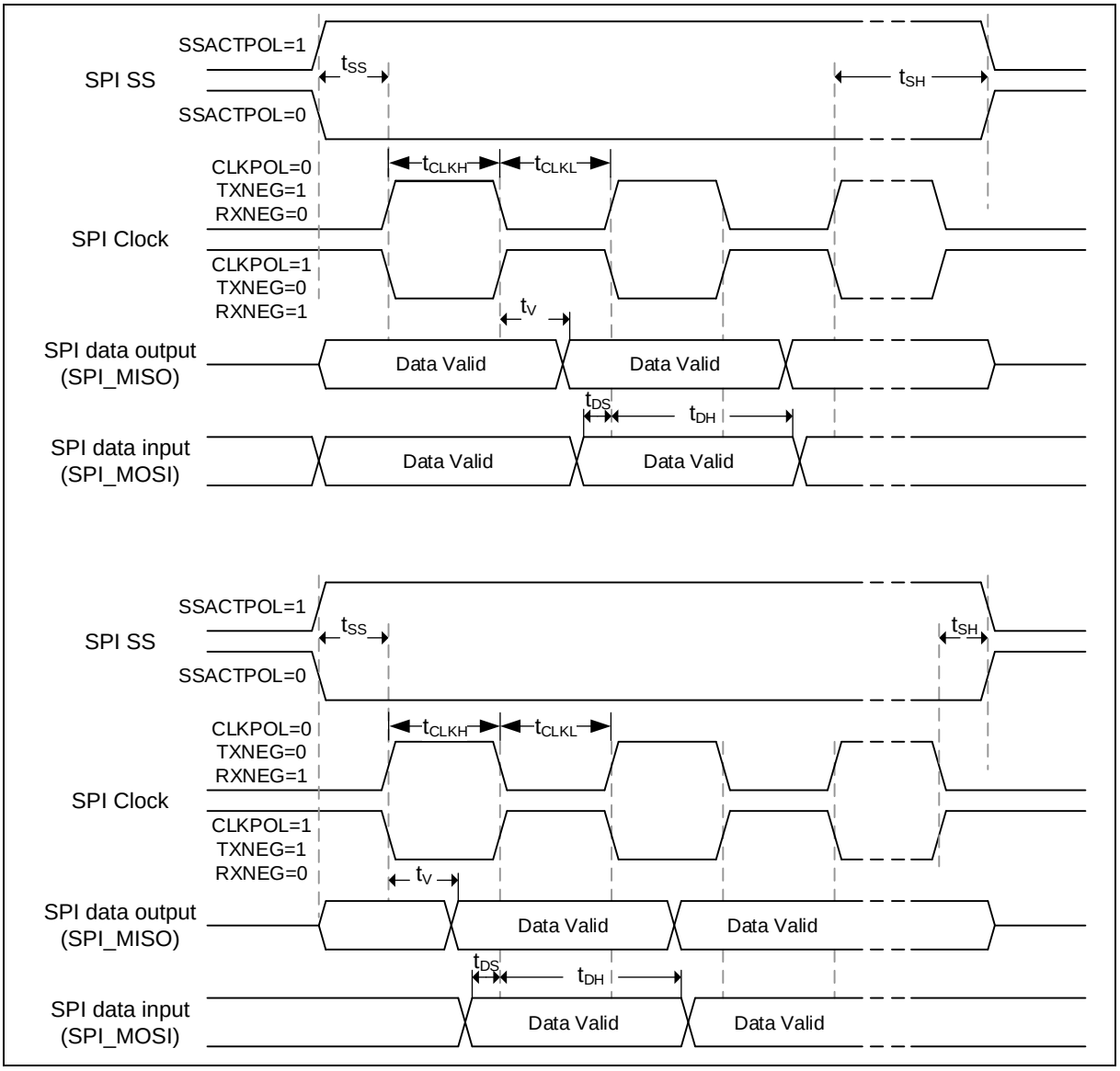


Figure 8.6-7 USCI-SPI Slave Mode Timing Diagram

8.6.5 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μs
t_{HIGH}	SCL high period	4	-	0.6	-	μs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-7 USCI-I²C Characteristics

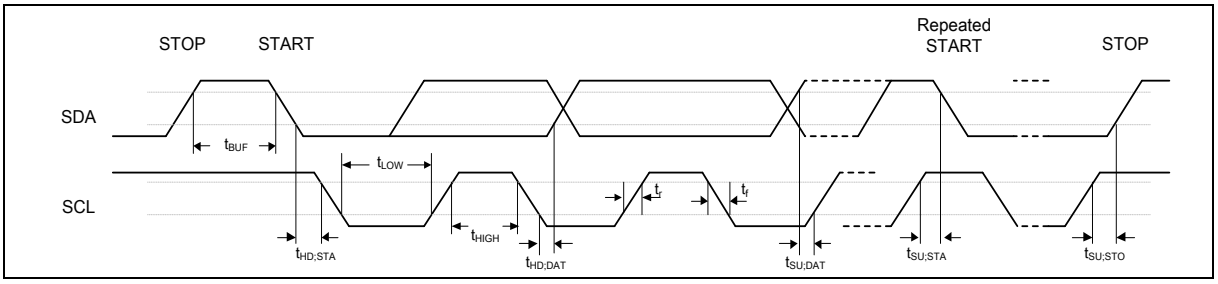


Figure 8.6-8 USCI-I²C Timing Diagram

8.6.6 USB Characteristics

8.6.6.1 USB Full-Speed Characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BUS}	USB full speed transceiver operating voltage	4.4		5.25	V	
V_{DD33} [*2]	USB Internal power regulator output	3.0	3.3	3.6	V	
V_{IH}	Input high (driven)	2.0	-	-	V	-
V_{IL}	Input low	-	-	0.8	V	-
V_{DI}	Differential input sensitivity	0.2	-	-	V	|(USB_D+) - (USB_D-)|
V_{CM}	Differential common-mode range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended receiver threshold	0.8	-	2.0	V	-
	Receiver hysteresis	-	200	-	mV	-
V_{OL}	Output low (driven)	0	-	0.3	V	-
V_{OH}	Output high (driven)	2.8	-	3.6	V	-
V_{CRS}	Output signal cross voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up resistor	1.19	-	1.9	kΩ	-
V_{TRM}	Termination voltage for upstream port pull-up (RPU)	3.0	-	3.6	V	
Z_{DRV} [*3]	Driver output resistance	-	10	-	Ω	Steady state drive
C_{IN}	Transceiver capacitance	-	-	26	pF	Pin to GND

Note:

1. Guaranteed by characterization result, not tested in production.
2. To ensure stability, an external 1 μF output capacitor, 1uF external capacitor must be connected between the USB_VDD33_CAP pin and the closest GND pin of the device.
3. USB_D+ and USB_D- must be connected with series resistors to fit USB Full-speed spec request (28 ~ 44Ω).

Table 8.6-8 USB Full-Speed Characteristics

8.6.6.2 USB Full-Speed PHY characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_{FR}	rise time	4	-	20	ns	C_L=50 pF
T_{FF}	fall time	4	-	20	ns	C_L=50 pF
T_{FRFF}	rise and fall time matching	90	-	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-9 USB Full-Speed PHY Characteristics

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

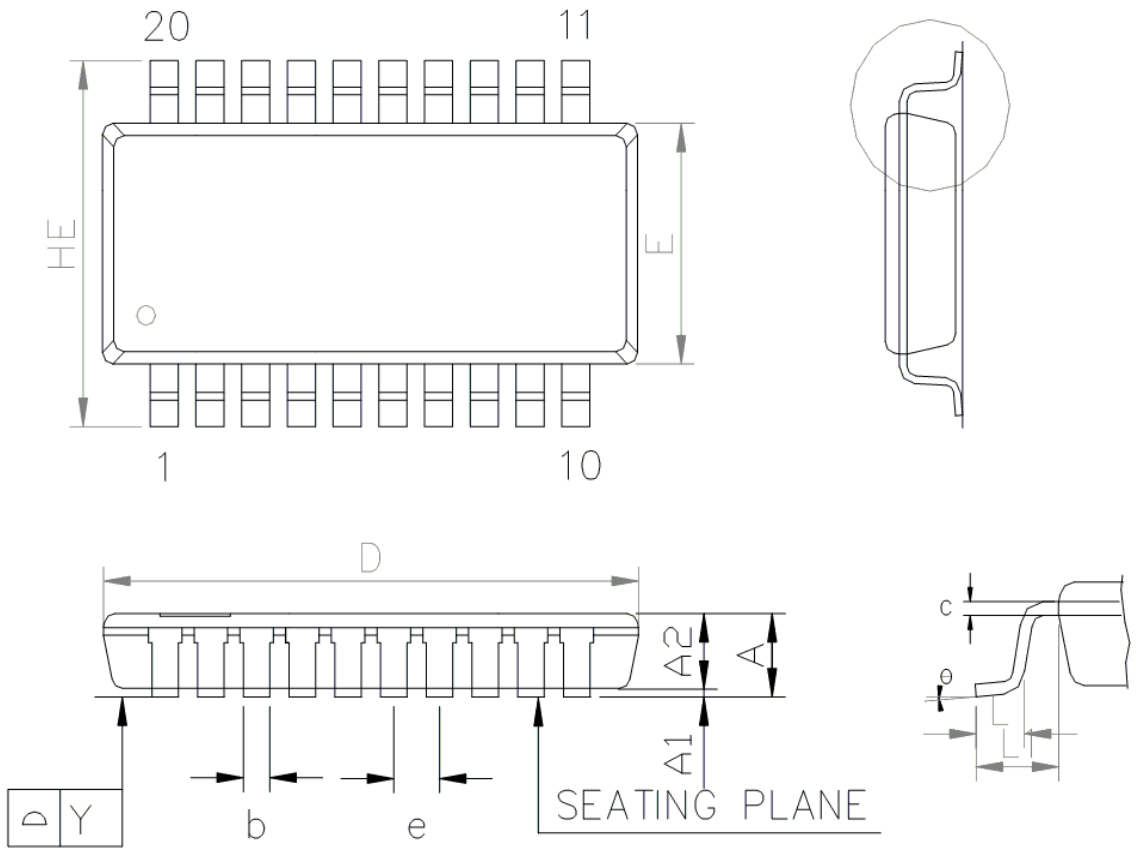
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.62	1.8	1.98	V	T_A = 25°C
T_{ERASE}	Page erase time	-	20	-	ms	
T_{PROG}	Program time	-	60	-	µs	
I_{DD1}	Read current	-	7	-	mA	
I_{DD2}	Program current	-	8	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	20,000	-		cycles[2]	T_J = -40°C~125°C
T_{RET}	Data retention	65	-	-	year	20 kcycle[3] T_A = 55°C
		10	-	-	year	20 kcycle[3] T_A = 85°C
		4	-	-	year	20 kcycle[3] T_A = 125°C

Note:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

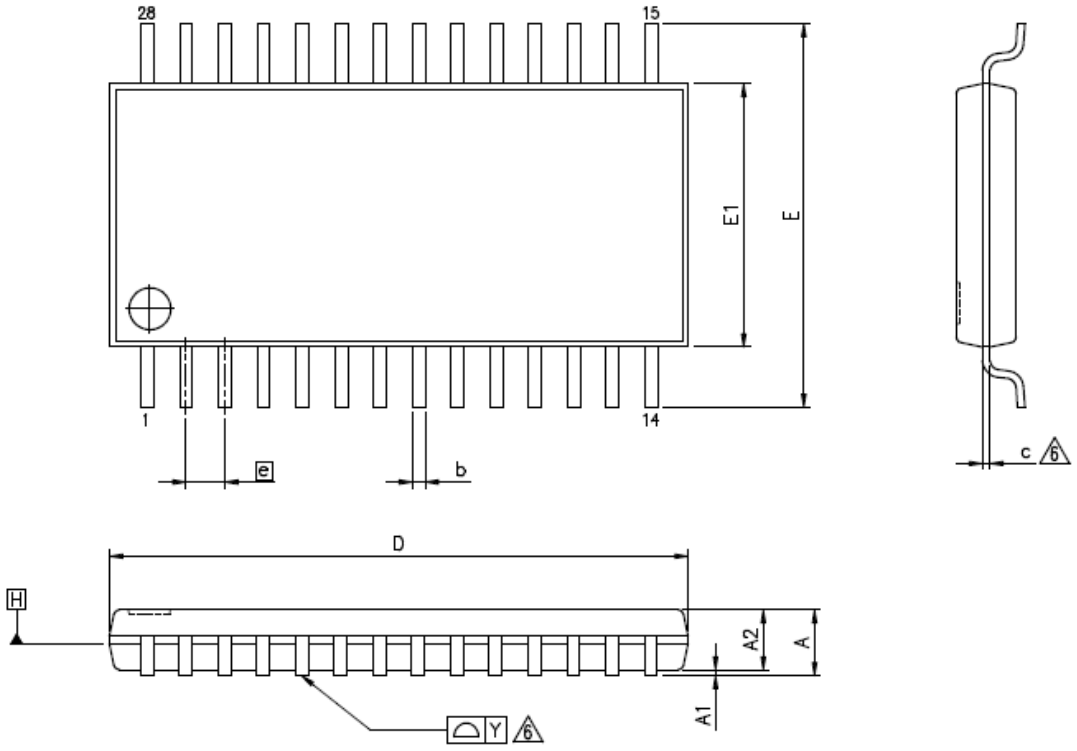
9 PACKAGE DIMENSIONS

9.1 TSSOP 20 (4.4x6.5x0.9 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE		6.40 BSC			0.252 BSC	
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1		1.00 REF			0.039 REF	
b	0.19	-	0.30	0.007	-	0.012
e		0.65 BSC			0.026 BSC	
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y		0.10 BASIC			0.004 BASIC	

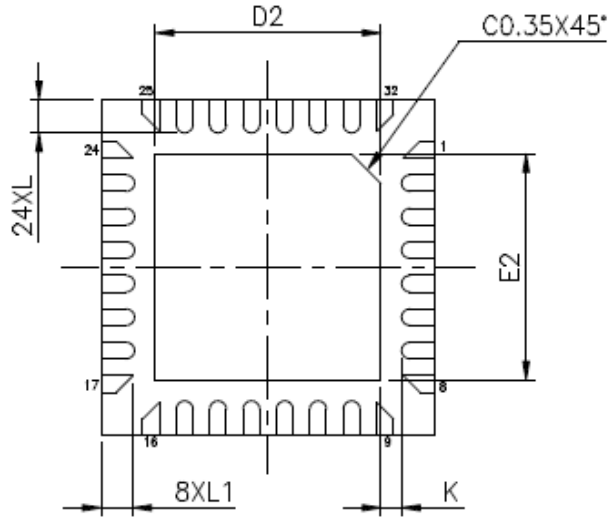
9.2 TSSOP 28 (4.4x9.7x1.0 mm)

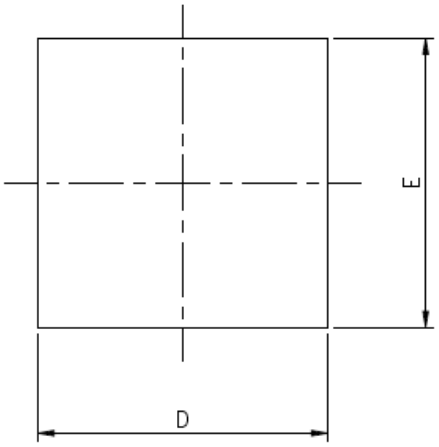


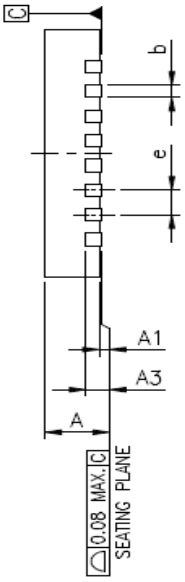
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

9.3 QFN 33L (4X4x0.8 mm Pitch:0.40 mm)



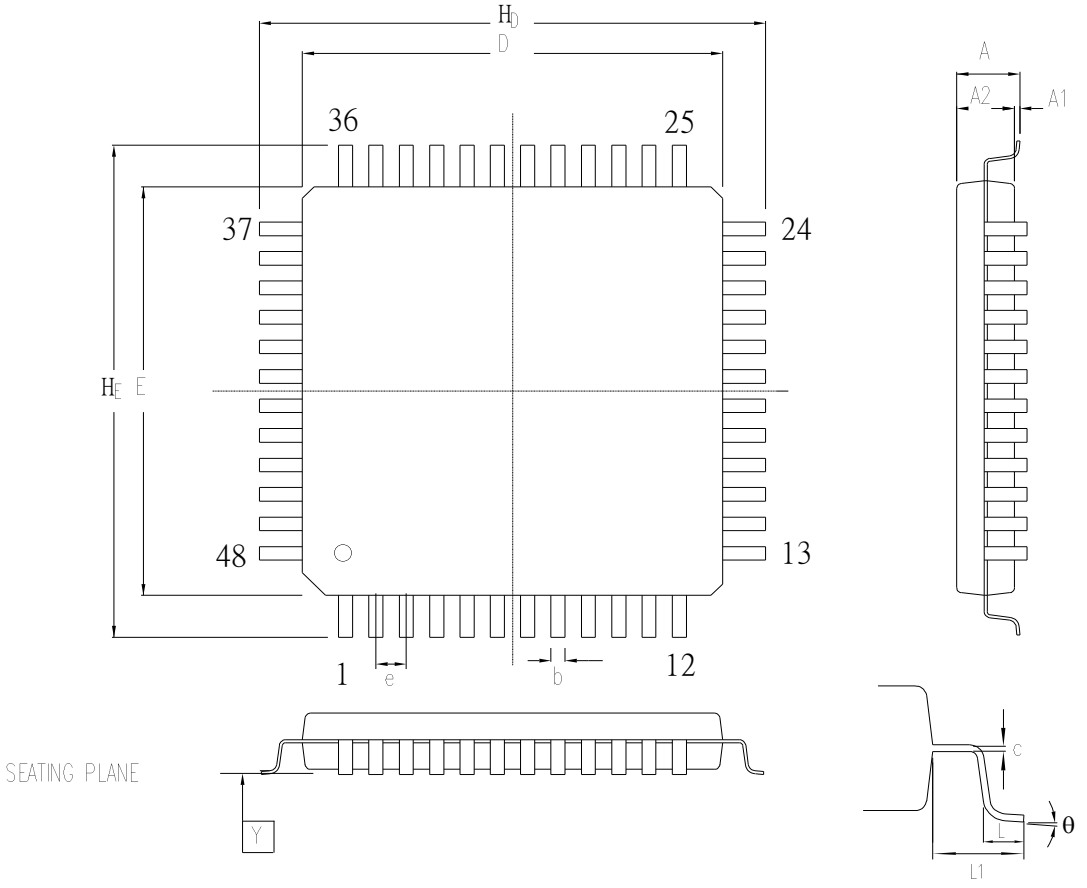




	Symbol	Min	Nom	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0.0	0.02	0.05
L/F Thickness	A3		0.2 REF.	
Lead Width	b	0.15	0.20	0.25
Body Size	D		4.00 BSC	
	E		4.00 BSC	
Lead Pitch	e		0.40 BSC	
Lead Length	L	0.35	0.4	0.45
	K	0.2	--	--

Symbol	L/F SIZE	Dimension in mm		
		MIN.	NOR.	MAX.
D2	114X114 mm	2.6	2.7	2.75
E2		2.6	2.7	2.75

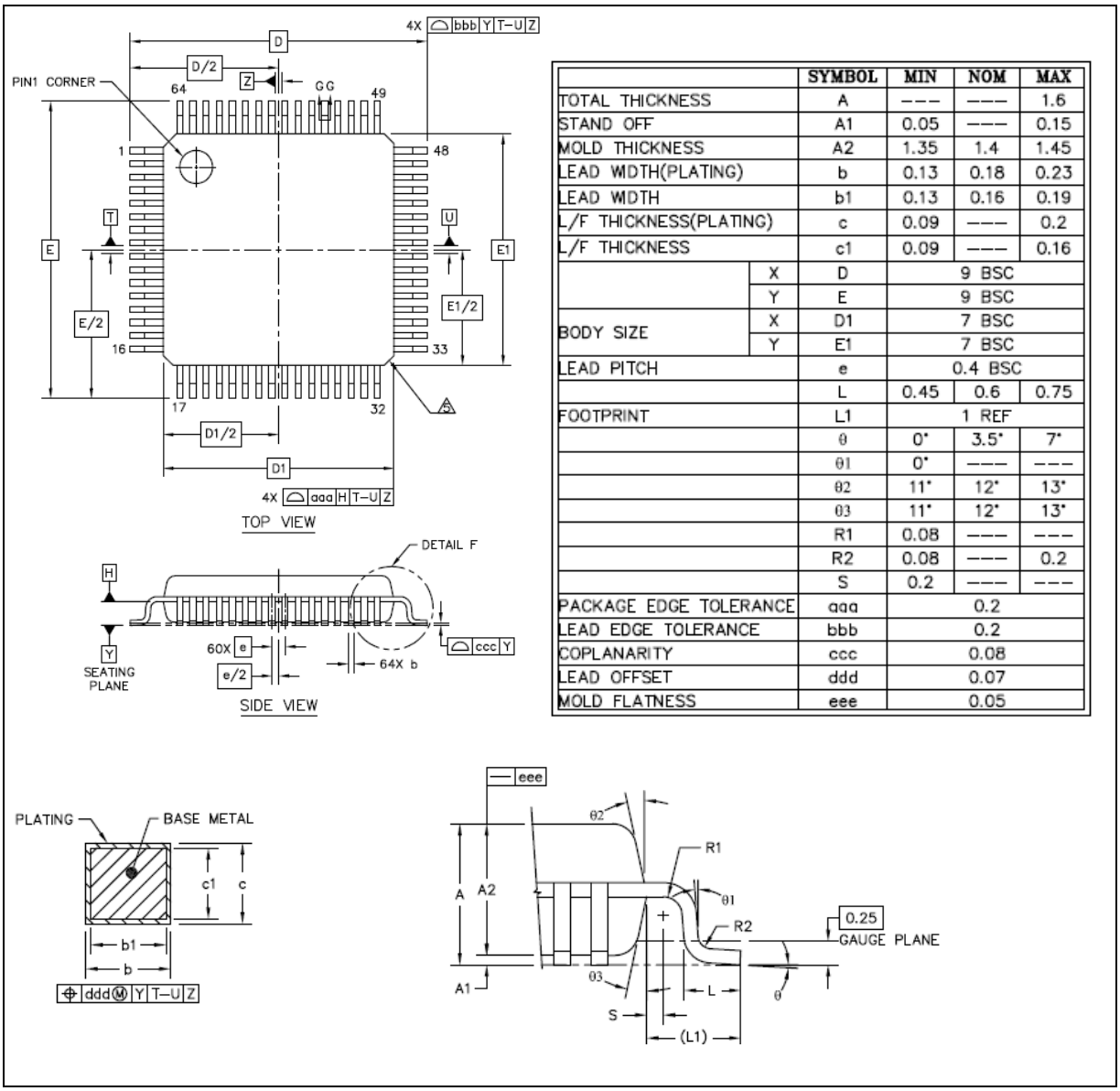
9.4 LQFP 48L (7x7x1.4 mm Footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

9.5 LQFP 64L (7x7x1.4 mm Footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
ADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~32 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	38.4 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2018.12.24	1.00	Initial version.
2019.02.25	1.01	1. Modified ISP ROM size in section 3.3.1 and section 3.3.2 2. Modified HIRC trim reference clock in section 6.2.8 and section 6.24.2.

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