ARM® Cortex®-M
32-bit Microcontroller

NuMicro® NUC100 Series
NUC100/120xxxDN
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® NUC100 series 32-bit microcontroller (MCU) is embedded with the ARM® Cortex®-M0 core with the cost equivalent to traditional 8-bit MCU. The NUC100 series can be used in consumer electronics, industrial control and applications which requiring rich communication interfaces such as industrial automation, alarm system, energy system and power system.

The NuMicro® NUC100 Advanced Line and NUC120 USB Line are embedded with the Cortex®-M0 core running up to 50 MHz and features 32/64/128 Kbytes Flash, 4/8/16 Kbytes embedded SRAM and 4 Kbytes loader ROM for the ISP. It operates at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40℃ ~ +85℃. The NUC100 series is also provided with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I^2C, I^2S, PWM Timer, GPIO, PS/2, EBI, Smart Card Host, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector. Additionally, the NUC120 USB Line is equipped with a USB 2.0 Full-speed Device. These peripherals have been incorporated into the NUC100 series to reduce component count, board space and system cost.

The NUC100 series is equipped with ISP (In-System Programming), IAP (In-Application-Programming) and ICP (In-Circuit Programming) functions, which allows the user to update the program under software control through the on-chip connectivity interface, such as SWD, UART and USB.

Product Line	UART	SPI	I^2C	USB	PS/2	I^2S	SC
NUC100xxxDN	3	4	2	-	1	1	3
NUC120xxxDN	3	4	2	1	1	1	3

Table 1-1 NuMicro® NUC100 Series Connectivity Support Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro® NUC100 Features – Advanced Line

- ARM® Cortex®-M0 core
  - Runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 32/64/128 Kbytes Flash for program code
  - 4 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Configurable Data Flash address and size for 128 KB system, fixed 4 KB Data Flash for the 32 KB and 64 KB system
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 4/8/16 Kbytes embedded SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ±3 % at -40 ℃ ~ +85 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL, up to 50 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function
- Supports input capture function

- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports wake-up function
- PWM/Capture
  - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to three UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports PDMA mode
- SPI
  - Up to four sets of SPI controllers
  - SPI clock rate of Master can be up to 36 MHz (chip working at 5V); SPI clock rate of Slave can be up to 18 MHz (chip working at 5V)
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
  - Supports Byte Suspend mode in 32-bit transmission
  - Supports PDMA mode

- Supports three wire, no slave select signal, bi-direction interface

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- I^2S
  - Interface with external audio CODEC
  - Operate as either Master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - Software override bus
- EBI (External bus interface)
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8-/16-bit data width
  - Supports byte write in 16-bit data width mode
- ADC
  - 12-bit SAR ADC with 760 kSPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion started by software programming or external input
  - Supports PDMA mode
- Analog Comparator
  - Up to two analog comparators
  - External input or internal Band-gap voltage selectable at negative node
  - Interrupt when compare results change
  - Supports Power-down wake-up
- Smart Card Host (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to three ISO-7816-3 ports

  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detecting the card is removal
- 96-bit unique ID (UID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40℃ ~ 85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin
  - LQFP 64-pin
  - LQFP 48-pin

2.2 NuMicro® NUC120 Features – USB Line

- ARM® Cortex®-M0 core
  - Runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32/64/128 Kbytes Flash for program code
  - 4 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Configurable Data Flash address and size for 128 KB system, fixed 4 KB Data Flash for the 32 KB and 64 KB system
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 4/8/16 Kbytes embedded SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ±3 % at -40 ℃ ~ +85 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL, up to 50 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer

- Provides one-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function
- Supports input capture function

- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports wake-up function
- PWM/Capture
  - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to three UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports PDMA mode
- SPI
  - Up to four sets of SPI controllers
  - The maximum SPI clock rate of Master can up to 36 MHz (chip working at 5V)
  - The maximum SPI clock rate of Slave can up to 18 MHz (chip working at 5V)
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
  - Supports Byte Suspend mode in 32-bit transmission
  - Supports PDMA mode
  - Supports three wire, no slave select signal, bi-direction interface

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- I^2S
  - Interface with external audio CODEC
  - Operate as either Master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - Software override bus
- EBI (External bus interface)
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8-/16-bit data width
  - Supports byte write in 16-bit data width mode
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12 Mbps
  - On-chip USB Transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 6 programmable endpoints
  - Includes 512 Bytes internal SRAM as USB buffer
  - Provides remote wake-up capability
- ADC
  - 12-bit SAR ADC with 760 kSPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion started by software programming or external input
  - Supports PDMA mode

- Analog Comparator
  - Up to two analog comparators
  - External input or internal Band-gap voltage selectable at negative node
  - Interrupt when compare results change
  - Supports Power-down wake-up
- Smart Card Host (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to three ISO-7816-3 ports
  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detecting the card removal
- 96-bit unique ID (UID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40℃ ~ 85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin
  - LQFP 64-pin
  - LQFP48-pin

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® NUC100/120xxxDN Selection Guide

4.1.1 NuMicro® NUC100 Advanced Line Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I²S	SC	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I²C	USB	LIN	CAN									
NUC100LC1DN	32 KB	4 KB	4 KB	4 KB	up to 37	4x32-bit	2	1	2	-	-	-	1	3	1	6	8x12-bit	v	-	v	LQFP48
NUC100LD2DN	64 KB	8 KB	4 KB	4 KB	up to 37	4x32-bit	2	1	2	-	-	-	1	3	1	6	8x12-bit	v	-	v	LQFP48
NUC100LE3DN	128 KB	16 KB	Definable	4 KB	up to 37	4x32-bit	2	1	2	-	-	-	1	3	1	6	8x12-bit	v	-	v	LQFP48
NUC100RC1DN	32 KB	4 KB	4 KB	4 KB	up to 51	4x32-bit	3	2	2	-	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC100RD1DN	64 KB	4 KB	4 KB	4 KB	up to 51	4x32-bit	3	2	2	-	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC100RD2DN	64 KB	8 KB	4 KB	4 KB	up to 51	4x32-bit	3	2	2	-	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC100RE3DN	128 KB	16 KB	Definable	4 KB	up to 51	4x32-bit	3	2	2	-	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC100VE3DN	128 KB	16 KB	Definable	4 KB	up to 84	4x32-bit	3	4	2	-	-	-	1	3	2	8	8x12-bit	v	v	v	LQFP100

4.1.2 NuMicro® NUC120 USB Line Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I²S	SC	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I²C	USB	LIN	CAN									
NUC120LC1DN	32 KB	4 KB	4 KB	4 KB	up to 33	4x32-bit	2	1	2	1	-	-	1	3	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD2DN	64 KB	8 KB	4 KB	4 KB	up to 33	4x32-bit	2	1	2	1	-	-	1	3	1	4	8x12-bit	v	-	v	LQFP48
NUC120LE3DN	128 KB	16 KB	Definable	4 KB	up to 33	4x32-bit	2	1	2	1	-	-	1	3	1	4	8x12-bit	v	-	v	LQFP48
NUC120RC1DN	32 KB	4 KB	4 KB	4 KB	up to 47	4x32-bit	2	2	2	1	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC120RD1DN	64 KB	4 KB	4 KB	4 KB	up to 47	4x32-bit	2	2	2	1	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC120RD2DN	64 KB	8 KB	4 KB	4 KB	up to 47	4x32-bit	2	2	2	1	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC120RE3DN	128 KB	16 KB	Definable	4 KB	up to 47	4x32-bit	2	2	2	1	-	-	1	3	2	6	8x12-bit	v	v	v	LQFP64
NUC120VE3DN	128 KB	16 KB	Definable	4 KB	up to 80	4x32-bit	3	4	2	1	-	-	1	3	2	8	8x12-bit	v	v	v	LQFP100

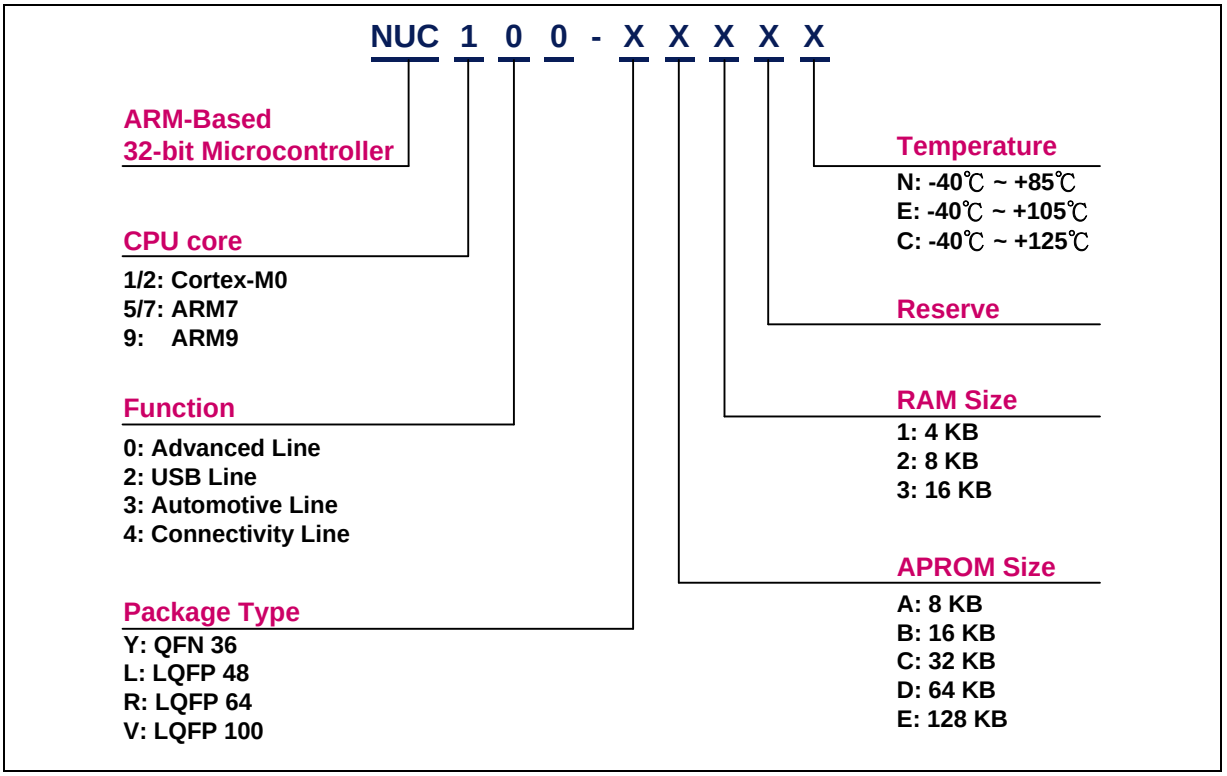


Figure 4-1 NuMicro® NUC100 Series Selection Code

4.2 Pin Configuration

4.2.1 NuMicro® NUC100 Pin Diagram

4.2.1.1 NuMicro® NUC100VxxDN LQFP 100 pin

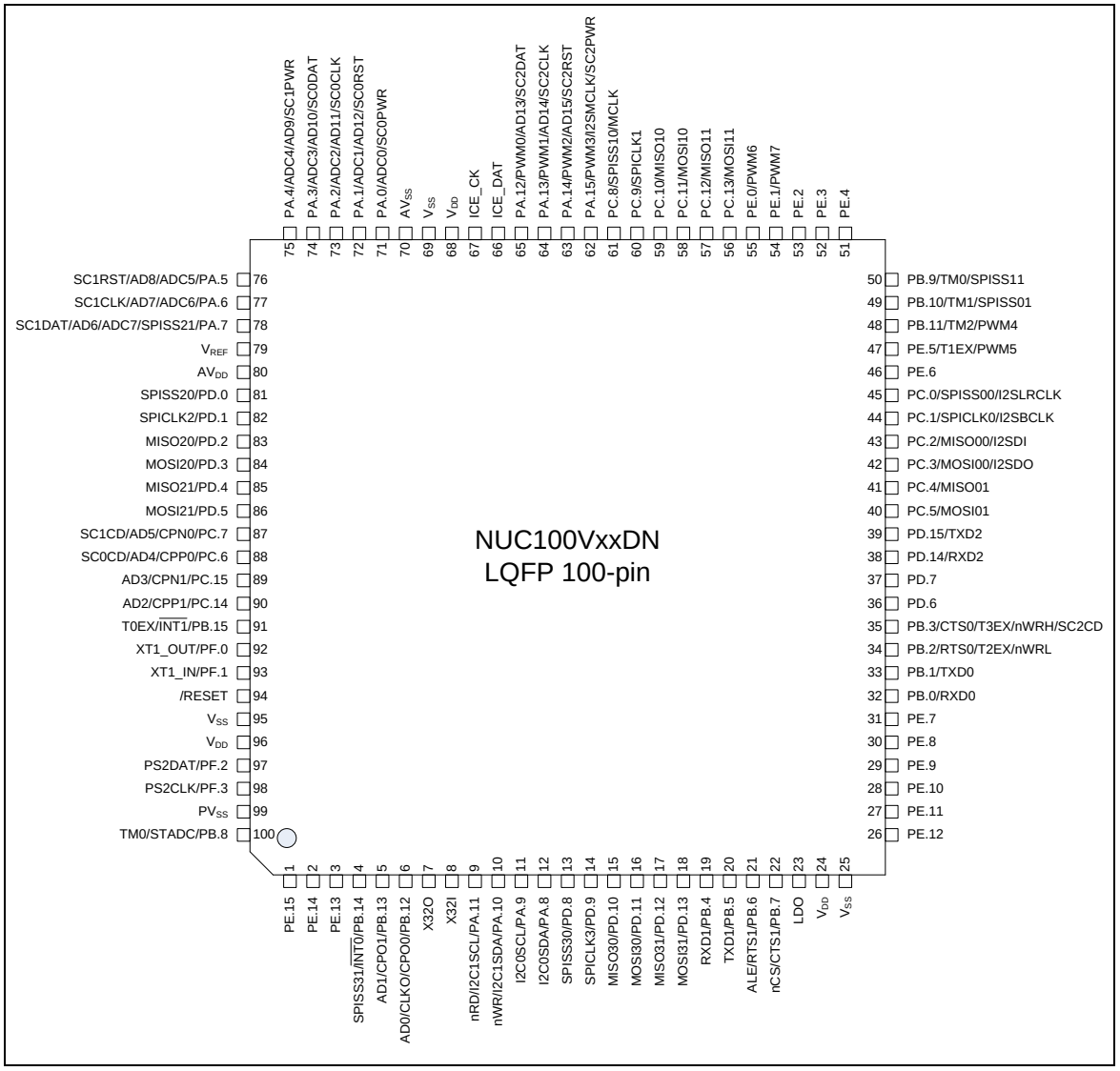


Figure 4-2 NuMicro® NUC100VxxDN LQFP 100-pin Diagram

4.2.1.2 NuMicro® NUC100RxxDN LQFP 64 pin

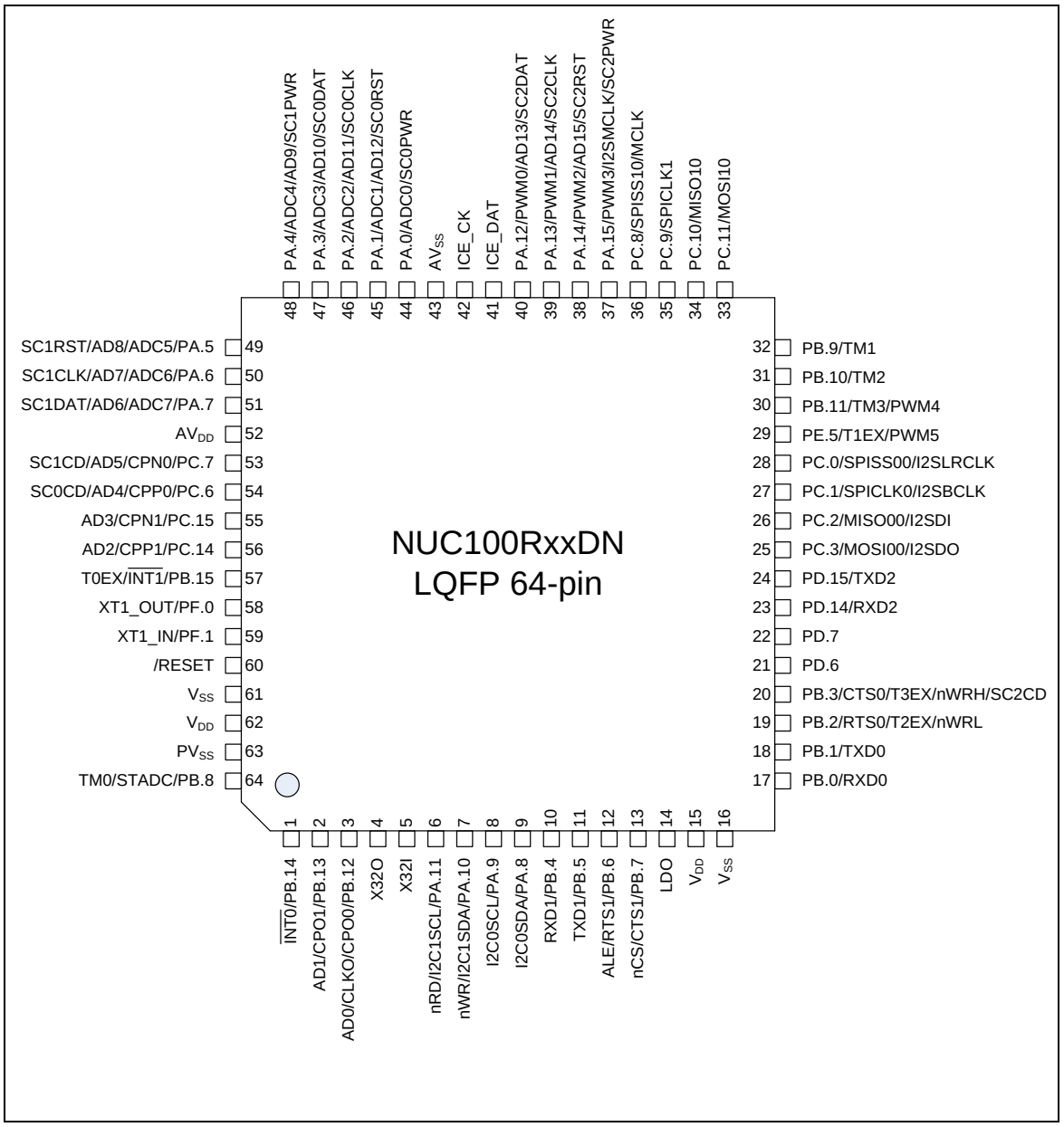


Figure 4-3 NuMicro® NUC100RxxDN LQFP 64-pin Diagram

4.2.1.3 NuMicro® NUC100LxxDN LQFP 48 pin

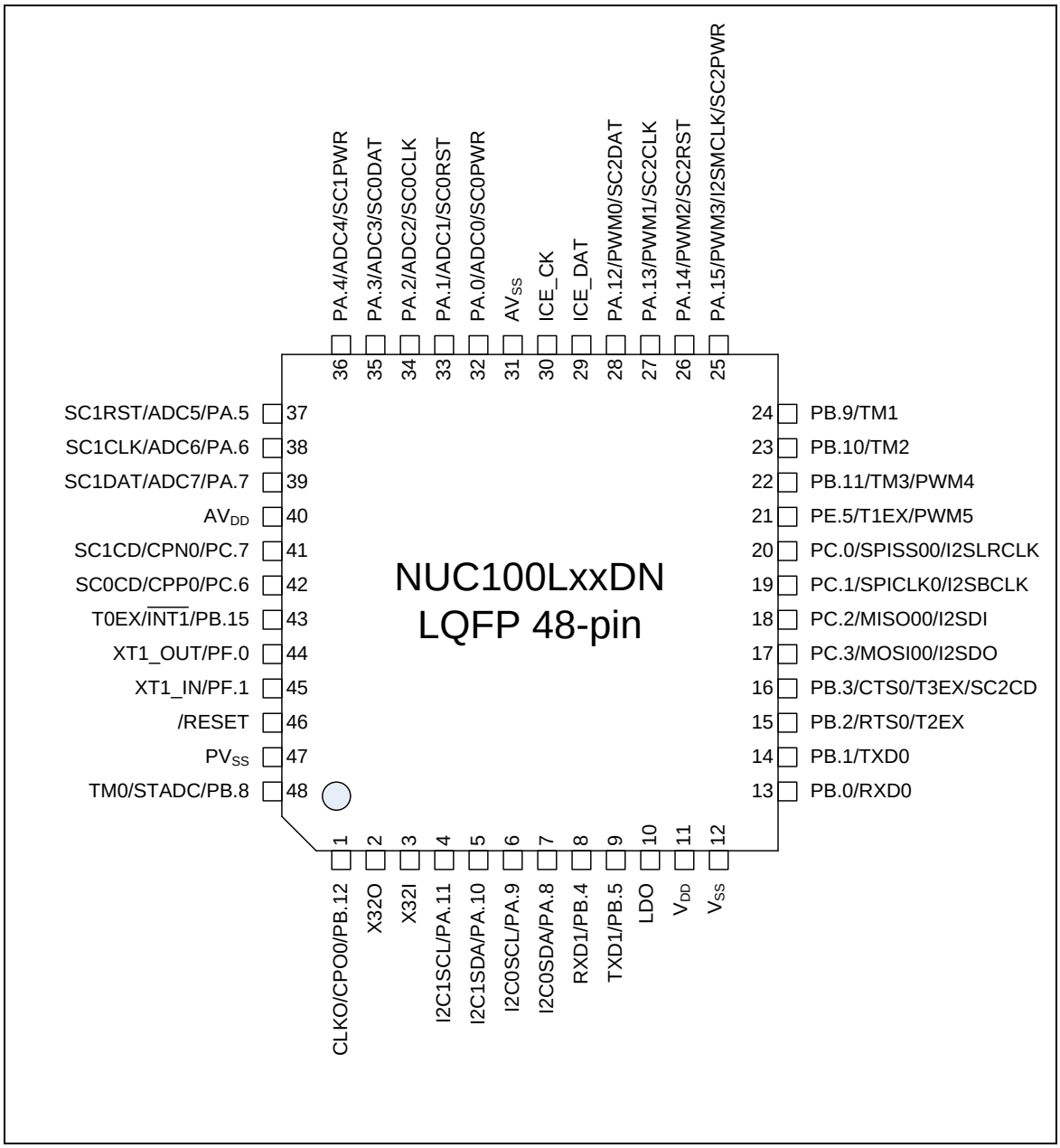


Figure 4-4 NuMicro® NUC100LxxDN LQFP 48-pin Diagram

4.2.2 NuMicro® NUC120 Pin Diagram

4.2.2.1 NuMicro® NUC120VxxDN LQFP 100 pin

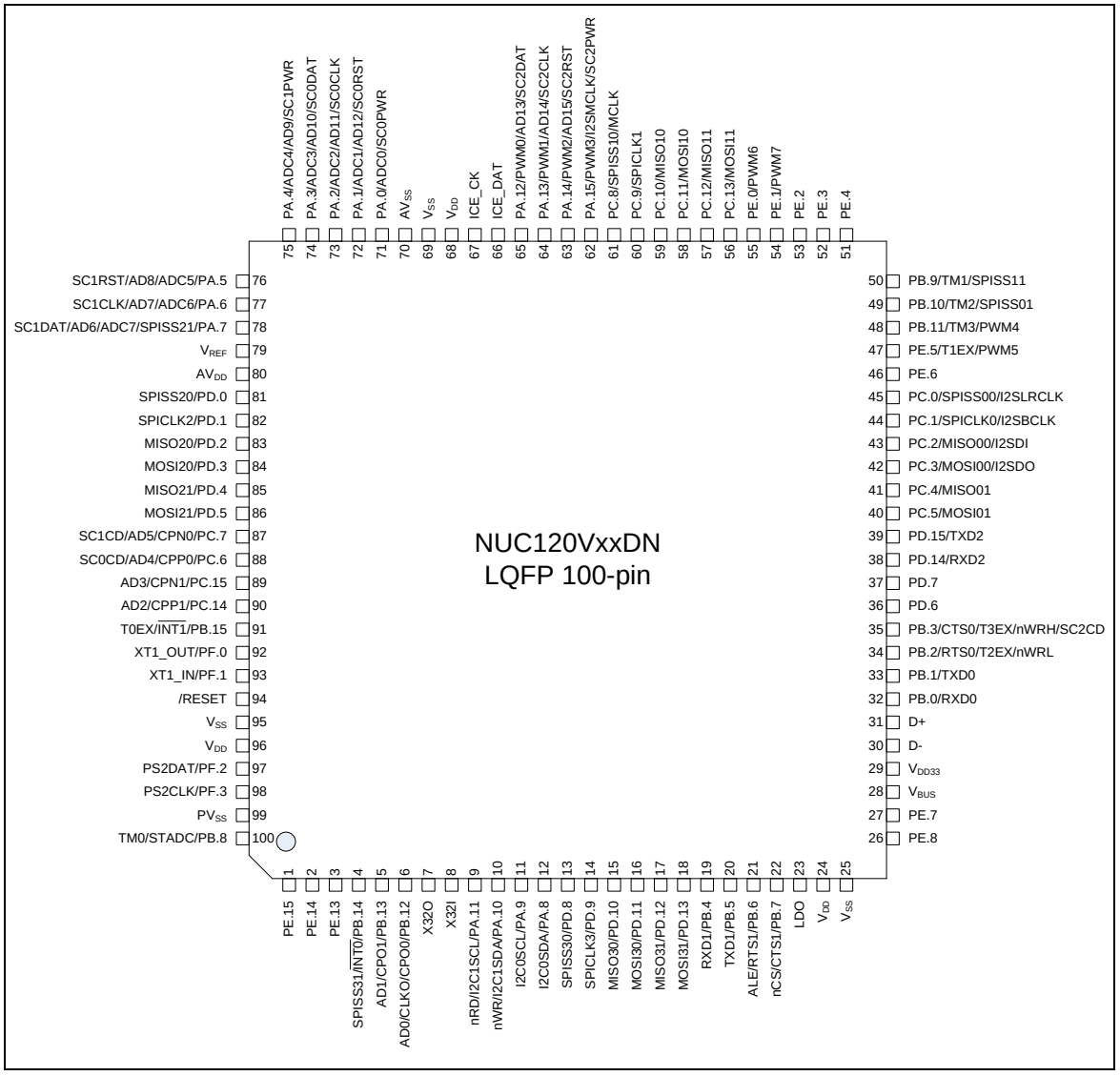


Figure 4-5 NuMicro® NUC120VxxDN LQFP 100-pin Diagram

4.2.2.2 NuMicro® NUC120RxxDN LQFP 64 pin

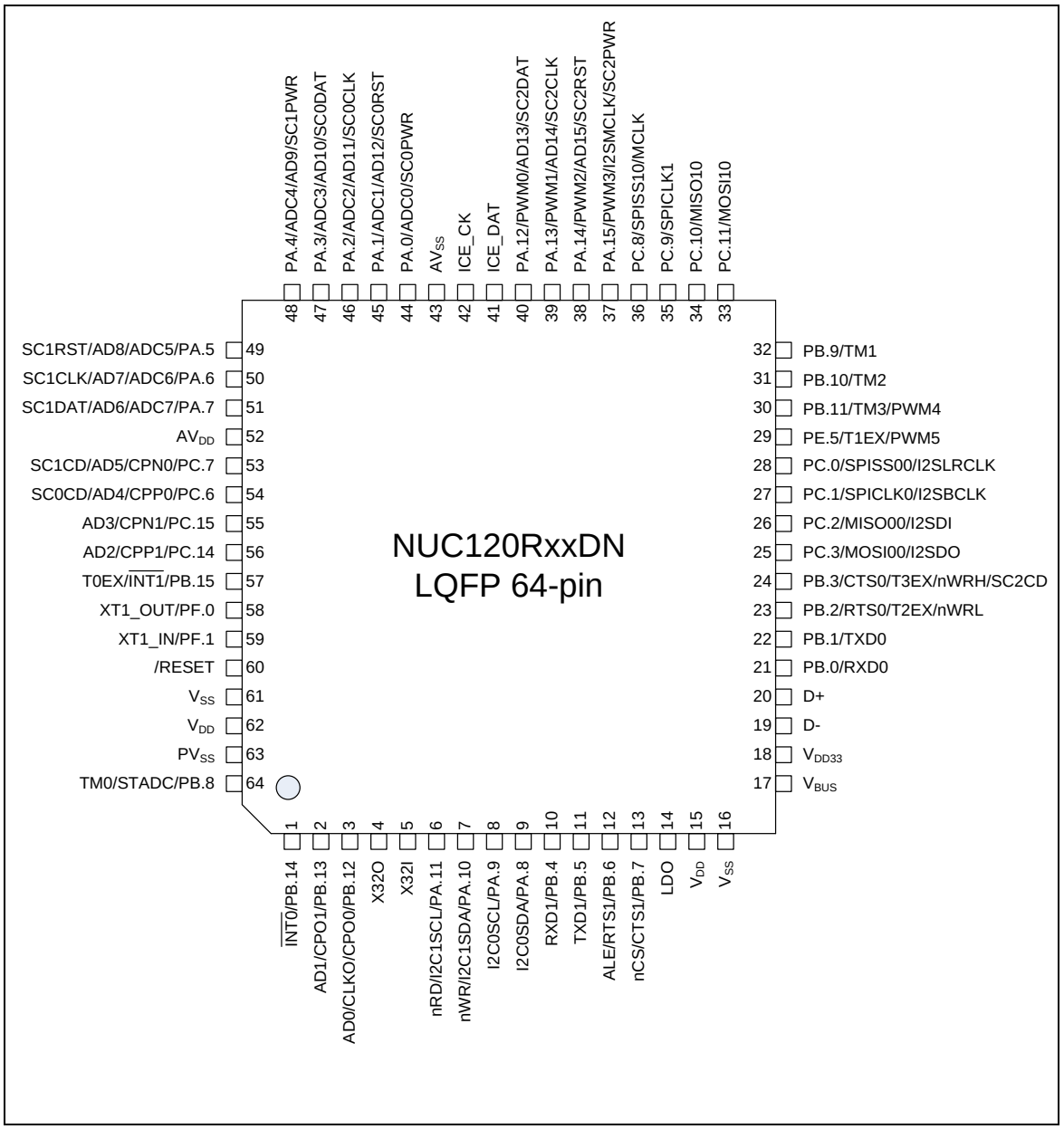


Figure 4-6 NuMicro® NUC120RxxDN LQFP 64-pin Diagram

4.2.2.3 NuMicro® NUC120LxxDN LQFP 48 pin

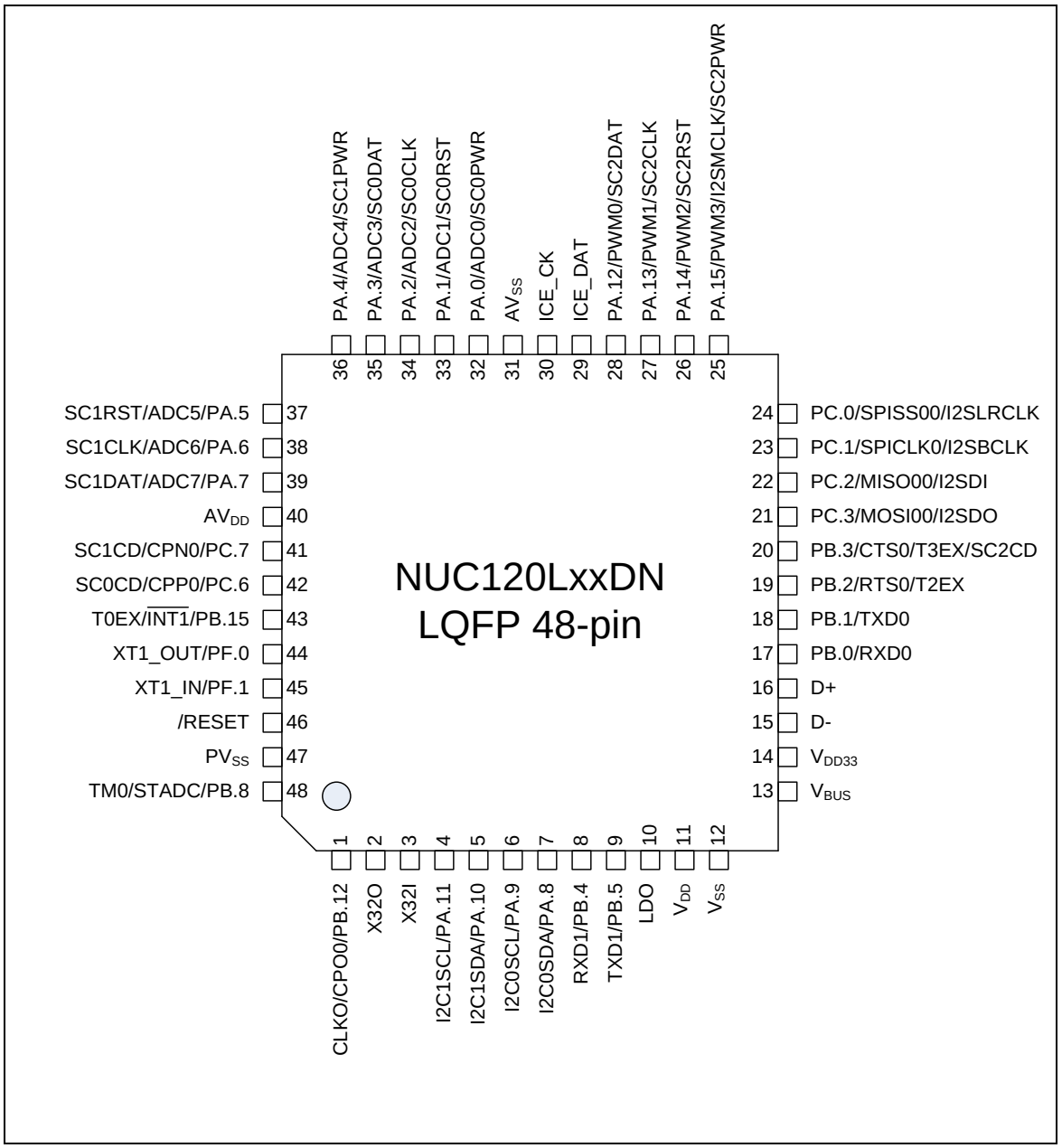


Figure 4-7 NuMicro® NUC120LxxDN LQFP 48-pin Diagram

4.3 Pin Description

4.3.1 NuMicro® NUC100 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	**I/O**	General purpose digital I/O pin.
2			PE.14	**I/O**	General purpose digital I/O pin.
3			PE.13	**I/O**	General purpose digital I/O pin.
4	1		PB.14	**I/O**	General purpose digital I/O pin.
			/INT0	**I**	External interrupt0 input pin.
			SPISS31	**I/O**	2nd SPI3 slave select pin.
5	2		PB.13	**I/O**	General purpose digital I/O pin.
			CPO1	**O**	Comparator1 output pin.
			AD1	**I/O**	EBI Address/Data bus bit1
6	3	1	PB.12	**I/O**	General purpose digital I/O pin.
			CPO0	**O**	Comparator0 output pin
			CLKO	**O**	Frequency Divider output pin
			AD0	**I/O**	EBI Address/Data bus bit0
7	4	2	X32O	**O**	External 32.768 kHz low speed crystal output pin
8	5	3	X32I	**I**	External 32.768 kHz low speed crystal input pin
9	6	4	PA.11	**I/O**	General purpose digital I/O pin.
			I2C1SCL	**I/O**	I2C1 clock pin.
			nRD	**O**	EBI read enable output pin
10	7	5	PA.10	**I/O**	General purpose digital I/O pin.
			I2C1SDA	**I/O**	I2C1 data input/output pin.
			nWR	**O**	EBI write enable output pin
11	8	6	PA.9	**I/O**	General purpose digital I/O pin.
			I2C0SCL	**I/O**	I2C0 clock pin.
12	9	7	PA.8	**I/O**	General purpose digital I/O pin.
			I2C0SDA	**I/O**	I2C0 data input/output pin.
13			PD.8	**I/O**	General purpose digital I/O pin.
			SPISS30	**I/O**	1st SPI3 slave select pin.
14			PD.9	**I/O**	General purpose digital I/O pin.
			SPICLK3	**I/O**	SPI3 serial clock pin.
15			PD.10	**I/O**	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			MISO30	**I/O**	1st SPI3 MISO (Master In, Slave Out) pin.
16			PD.11	**I/O**	General purpose digital I/O pin.
			MOSI30	**I/O**	1st SPI3 MOSI (Master Out, Slave In) pin.
17			PD.12	**I/O**	General purpose digital I/O pin.
			MISO31	**I/O**	2nd SPI3 MISO (Master In, Slave Out) pin.
18			PD.13	**I/O**	General purpose digital I/O pin.
			MOSI31	**I/O**	2nd SPI3 MOSI (Master Out, Slave In) pin.
19	10	8	PB.4	**I/O**	General purpose digital I/O pin.
			RXD1	**I**	Data receiver input pin for UART1.
20	11	9	PB.5	**I/O**	General purpose digital I/O pin.
			TXD1	**O**	Data transmitter output pin for UART1.
21	12		PB.6	**I/O**	General purpose digital I/O pin.
			RTS1	**O**	Request to Send output pin for UART1.
			ALE	**O**	EBI address latch enable output pin
22	13		PB.7	**I/O**	General purpose digital I/O pin.
			CTS1	**I**	Clear to Send input pin for UART1.
			nCS	**O**	EBI chip select enable output pin
23	14	10	LDO	**P**	LDO output pin
24	15	11	V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
25	16	12	V_{SS}	**P**	Ground pin for digital circuit.
26			PE.12	**I/O**	General purpose digital I/O pin.
27			PE.11	**I/O**	General purpose digital I/O pin.
28			PE.10	**I/O**	General purpose digital I/O pin.
29			PE.9	**I/O**	General purpose digital I/O pin.
30			PE.8	**I/O**	General purpose digital I/O pin.
31			PE.7	**I/O**	General purpose digital I/O pin.
32	17	13	PB.0	**I/O**	General purpose digital I/O pin.
			RXD0	**I**	Data receiver input pin for UART0.
33	18	14	PB.1	**I/O**	General purpose digital I/O pin.
			TXD0	**O**	Data transmitter output pin for UART0.
34	19	15	PB.2	**I/O**	General purpose digital I/O pin.
			RTS0	**O**	Request to Send output pin for UART0.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			T2EX	I	Timer2 external capture input pin.
			nWRL	O	EBI low byte write enable output pin
35	20	16	PB.3	I/O	General purpose digital I/O pin.
			CTS0	I	Clear to Send input pin for UART0.
			T3EX	I	Timer3 external capture input pin.
			SC2CD	I	SmartCard2 card detect pin.
			nWRH	O	EBI high byte write enable output pin
36	21		PD.6	I/O	General purpose digital I/O pin.
37	22		PD.7	I/O	General purpose digital I/O pin.
38	23		PD.14	I/O	General purpose digital I/O pin.
			RXD2	I	Data receiver input pin for UART2.
39	24		PD.15	I/O	General purpose digital I/O pin.
			TXD2	O	Data transmitter output pin for UART2.
40			PC.5	I/O	General purpose digital I/O pin.
			MOSI01	I/O	2nd SPI0 MOSI (Master Out, Slave In) pin.
41			PC.4	I/O	General purpose digital I/O pin.
			MISO01	I/O	2nd SPI0 MISO (Master In, Slave Out) pin.
42	25	17	PC.3	I/O	General purpose digital I/O pin.
			MOSI00	I/O	1st SPI0 MOSI (Master Out, Slave In) pin.
			I2SDO	O	I2S data output.
43	26	18	PC.2	I/O	General purpose digital I/O pin.
			MISO00	I/O	1st SPI0 MISO (Master In, Slave Out) pin.
			I2SDI	I	I2S data input.
44	27	19	PC.1	I/O	General purpose digital I/O pin.
			SPICLK0	I/O	SPI0 serial clock pin.
			I2SBCLK	I/O	I2S bit clock pin.
45	28	20	PC.0	I/O	General purpose digital I/O pin.
			SPISS00	I/O	1st SPI0 slave select pin.
			I2SLRCLK	I/O	I2S left right channel clock.
46			PE.6	I/O	General purpose digital I/O pin.
47	29	21	PE.5	I/O	General purpose digital I/O pin.
			PWM5	I/O	PWM5 output/Capture input.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			T1EX	I	Timer1 external capture input pin.
48	30	22	PB.11	I/O	General purpose digital I/O pin.
			TM3	I/O	Timer3 event counter input / toggle output.
			PWM4	I/O	PWM4 output/Capture input.
49	31	23	PB.10	I/O	General purpose digital I/O pin.
			TM2	I/O	Timer2 event counter input / toggle output.
			SPISS01	I/O	2nd SPI0 slave select pin.
50	32	24	PB.9	I/O	General purpose digital I/O pin.
			TM1	I/O	Timer1 event counter input / toggle output.
			SPISS11	I/O	2nd SPI1 slave select pin.
51			PE.4	I/O	General purpose digital I/O pin.
52			PE.3	I/O	General purpose digital I/O pin.
53			PE.2	I/O	General purpose digital I/O pin.
54			PE.1	I/O	General purpose digital I/O pin.
			PWM7	I/O	PWM7 output/Capture input.
55			PE.0	I/O	General purpose digital I/O pin.
			PWM6	I/O	PWM6 output/Capture input.
56			PC.13	I/O	General purpose digital I/O pin.
			MOSI11	I/O	2nd SPI1 MOSI (Master Out, Slave In) pin.
57			PC.12	I/O	General purpose digital I/O pin.
			MISO11	I/O	2nd SPI1 MISO (Master In, Slave Out) pin.
58	33		PC.11	I/O	General purpose digital I/O pin.
			MOSI10	I/O	1st SPI1 MOSI (Master Out, Slave In) pin.
59	34		PC.10	I/O	General purpose digital I/O pin.
			MISO10	I/O	1st SPI1 MISO (Master In, Slave Out) pin.
60	35		PC.9	I/O	General purpose digital I/O pin.
			SPICLK1	I/O	SPI1 serial clock pin.
61	36		PC.8	I/O	General purpose digital I/O pin.
			SPISS10	I/O	1st SPI1 slave select pin.
			MCLK	O	EBI external clock output pin
62	37	25	PA.15	I/O	General purpose digital I/O pin.
			PWM3	I/O	PWM output/Capture input.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			I2SMCLK	**O**	I^2S master clock output pin.
			SC2PWR	**O**	SmartCard2 power pin.
63	38	26	PA.14	**I/O**	General purpose digital I/O pin.
			PWM2	**I/O**	PWM2 output/Capture input.
			SC2RST	**O**	SmartCard2 reset pin.
			AD15	**I/O**	EBI Address/Data bus bit15
64	39	27	PA.13	**I/O**	General purpose digital I/O pin.
			PWM1	**I/O**	PWM1 output/Capture input.
			SC2CLK	**O**	SmartCard2 clock pin.
			AD14	**I/O**	EBI Address/Data bus bit14
65	40	28	PA.12	**I/O**	General purpose digital I/O pin.
			PWM0	**I/O**	PWM0 output/Capture input.
			SC2DAT	**O**	SmartCard2 data pin.
			AD13	**I/O**	EBI Address/Data bus bit13
66	41	29	ICE_DAT	**I/O**	Serial wire debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin
67	42	30	ICE_CLK	**I**	Serial wire debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin
68			V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V_{SS}	**P**	Ground pin for digital circuit.
70	43	31	AV_{SS}	**AP**	Ground pin for analog circuit.
71	44	32	PA.0	**I/O**	General purpose digital I/O pin.
			ADC0	**AI**	ADC0 analog input.
			SC0PWR	**O**	SmartCard0 power pin.
72	45	33	PA.1	**I/O**	General purpose digital I/O pin.
			ADC1	**AI**	ADC1 analog input.
			SC0RST	**O**	SmartCard0 reset pin.
			AD12	**I/O**	EBI Address/Data bus bit12
73	46	34	PA.2	**I/O**	General purpose digital I/O pin.
			ADC2	**AI**	ADC2 analog input.
			SC0CLK	**O**	SmartCard0 clock pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			AD11	I/O	EBI Address/Data bus bit11
74	47	35	PA.3	I/O	General purpose digital I/O pin.
			ADC3	AI	ADC3 analog input.
			SC0DAT	O	SmartCard0 data pin.
			AD10	I/O	EBI Address/Data bus bit10
75	48	36	PA.4	I/O	General purpose digital I/O pin.
			ADC4	AI	ADC4 analog input.
			SC1PWR	O	SmartCard1 power pin.
			AD9	I/O	EBI Address/Data bus bit9
76	49	37	PA.5	I/O	General purpose digital I/O pin.
			ADC5	AI	ADC5 analog input.
			SC1RST	O	SmartCard1 reset pin.
			AD8	I/O	EBI Address/Data bus bit8
77	50	38	PA.6	I/O	General purpose digital I/O pin.
			ADC6	AI	ADC6 analog input.
			SC1CLK	I/O	SmartCard1 clock pin.
			AD7	I/O	EBI Address/Data bus bit7
78	51	39	PA.7	I/O	General purpose digital I/O pin.
			ADC7	AI	ADC7 analog input.
			SC1DAT	O	SmartCard1 data pin.
			SPISS21	I/O	2nd SPI2 slave select pin.
			AD6	I/O	EBI Address/Data bus bit6
79			V_{REF}	AP	Voltage reference input for ADC.
80	52	40	AV_{DD}	AP	Power supply for internal analog circuit.
81			PD.0	I/O	General purpose digital I/O pin.
			SPISS20	I/O	1st SPI2 slave select pin.
82			PD.1	I/O	General purpose digital I/O pin.
			SPICLK2	I/O	SPI2 serial clock pin.
83			PD.2	I/O	General purpose digital I/O pin.
			MISO20	I/O	1st SPI2 MISO (Master In, Slave Out) pin.
84			PD.3	I/O	General purpose digital I/O pin.
			MOSI20	I/O	1st SPI2 MOSI (Master Out, Slave In) pin.
85			PD.4	I/O	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			MISO21	**I/O**	2nd SPI2 MISO (Master In, Slave Out) pin.
86			PD.5	**I/O**	General purpose digital I/O pin.
			MOSI21	**I/O**	2nd SPI2 MOSI (Master Out, Slave In) pin.
87	53	41	PC.7	**I/O**	General purpose digital I/O pin.
			CPN0	**AI**	Comparator0 negative input pin.
			SC1CD	**I**	SmartCard1 card detect pin.
			AD5	**I/O**	EBI Address/Data bus bit5
88	54	42	PC.6	**I/O**	General purpose digital I/O pin.
			CPP0	**AI**	Comparator0 positive input pin.
			SC0CD	**I**	SmartCard0 card detect pin.
			AD4	**I/O**	EBI Address/Data bus bit4
89	55		PC.15	**I/O**	General purpose digital I/O pin.
			CPN1	**AI**	Comparator1 negative input pin.
			AD3	**I/O**	EBI Address/Data bus bit3
90	56		PC.14	**I/O**	General purpose digital I/O pin.
			CPP1	**AI**	Comparator1 positive input pin.
			AD2	**I/O**	EBI Address/Data bus bit2
91	57	43	PB.15	**I/O**	General purpose digital I/O pin.
			/INT1	**I**	External interrupt1 input pin.
			T0EX	**I**	Timer0 external capture input pin.
92	58	44	PF.0	**I/O**	General purpose digital I/O pin.
			XT1_OUT	**O**	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	**I/O**	General purpose digital I/O pin.
			XT1_IN	**I**	External 4~24 MHz (high speed) crystal input pin.
94	60	46	/RESET	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
95	61		V_{SS}	**P**	Ground pin for digital circuit.
96	62		V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	**I/O**	General purpose digital I/O pin.
			PS2DAT	**I/O**	PS/2 data pin.
98			PF.3	**I/O**	General purpose digital I/O pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			PS2CLK	**I/O**	PS/2 clock pin.
99	63	47	PV_{SS}	**P**	PLL ground.
100	64	48	PB.8	**I/O**	General purpose digital I/O pin.
			STADC	**I**	ADC external trigger input.
			TM0	**I/O**	Timer0 event counter input / toggle output.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

4.3.2 NuMicro® NUC120 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.15	I/O	General purpose digital I/O pin.
2			PE.14	I/O	General purpose digital I/O pin.
3			PE.13	I/O	General purpose digital I/O pin.
4	1		PB.14	I/O	General purpose digital I/O pin.
			/INT0	I	External interrupt0 input pin.
			SPISS31	I/O	2nd SPI3 slave select pin.
5	2		PB.13	I/O	General purpose digital I/O pin.
			CPO1	O	Comparator1 output pin.
			AD1	I/O	EBI Address/Data bus bit1
6	3	1	PB.12	I/O	General purpose digital I/O pin.
			CPO0	O	Comparator0 output pin
			CLKO	O	Frequency Divider output pin
			AD0	I/O	EBI Address/Data bus bit0
7	4	2	X32O	O	External 32.768 kHz low speed crystal output pin
8	5	3	X32I	I	External 32.768 kHz low speed crystal input pin
9	6	4	PA.11	I/O	General purpose digital I/O pin.
			I2C1SCL	I/O	I2C1 clock pin.
			nRD	O	EBI read enable output pin
10	7	5	PA.10	I/O	General purpose digital I/O pin.
			I2C1SDA	I/O	I2C1 data input/output pin.
			nWR	O	EBI write enable output pin
11	8	6	PA.9	I/O	General purpose digital I/O pin.
			I2C0SCL	I/O	I2C0 clock pin.
12	9	7	PA.8	I/O	General purpose digital I/O pin.
			I2C0SDA	I/O	I2C0 data input/output pin.
13			PD.8	I/O	General purpose digital I/O pin.
			SPISS30	I/O	1st SPI3 slave select pin.
14			PD.9	I/O	General purpose digital I/O pin.
			SPICLK3	I/O	SPI3 serial clock pin.
15			PD.10	I/O	General purpose digital I/O pin.
			MISO30	I/O	1st SPI3 MISO (Master In, Slave Out) pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
16			PD.11	**I/O**	General purpose digital I/O pin.
			MOSI30	**I/O**	1st SPI3 MOSI (Master Out, Slave In) pin.
17			PD.12	**I/O**	General purpose digital I/O pin.
			MISO31	**I/O**	2nd SPI3 MISO (Master In, Slave Out) pin.
18			PD.13	**I/O**	General purpose digital I/O pin.
			MOSI31	**I/O**	2nd SPI3 MOSI (Master Out, Slave In) pin.
19	10	8	PB.4	**I/O**	General purpose digital I/O pin.
			RXD1	**I**	Data receiver input pin for UART1.
20	11	9	PB.5	**I/O**	General purpose digital I/O pin.
			TXD1	**O**	Data transmitter output pin for UART1.
21	12		PB.6	**I/O**	General purpose digital I/O pin.
			RTS1	**O**	Request to Send output pin for UART1.
			ALE	**O**	EBI address latch enable output pin
22	13		PB.7	**I/O**	General purpose digital I/O pin.
			CTS1	**I**	Clear to Send input pin for UART1.
			nCS	**O**	EBI chip select enable output pin
23	14	10	LDO	**P**	LDO output pin
24	15	11	V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
25	16	12	V_{SS}	**P**	Ground pin for digital circuit.
26			PE.8	**I/O**	General purpose digital I/O pin.
27			PE.7	**I/O**	General purpose digital I/O pin.
28	17	13	VBUS	**USB**	Power supply from USB host or HUB.
29	18	14	V_{DD33}	**USB**	Internal power regulator output 3.3V decoupling pin.
30	19	15	D-	**USB**	USB differential signal D-.
31	20	16	D+	**USB**	USB differential signal D+.
32	21	17	PB.0	**I/O**	General purpose digital I/O pin.
			RXD0	**I**	Data receiver input pin for UART0.
33	22	18	PB.1	**I/O**	General purpose digital I/O pin.
			TXD0	**O**	Data transmitter output pin for UART0.
34	23	29	PB.2	**I/O**	General purpose digital I/O pin.
			RTS0	**O**	Request to Send output pin for UART0.
			T2EX	**I**	Timer2 external capture input pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			nWRL	O	EBI low byte write enable output pin
35	24	20	PB.3	I/O	General purpose digital I/O pin.
			CTS0	I	Clear to Send input pin for UART0.
			T3EX	I	Timer3 external capture input pin.
			SC2CD	I	SmartCard2 card detect pin.
			nWRH	O	EBI high byte write enable output pin
36			PD.6	I/O	General purpose digital I/O pin.
37			PD.7	I/O	General purpose digital I/O pin.
38			PD.14	I/O	General purpose digital I/O pin.
			RXD2	I	Data receiver input pin for UART2.
39			PD.15	I/O	General purpose digital I/O pin.
			TXD2	O	Data transmitter output pin for UART2.
40			PC.5	I/O	General purpose digital I/O pin.
			MOSI01	I/O	2nd SPI0 MOSI (Master Out, Slave In) pin.
41			PC.4	I/O	General purpose digital I/O pin.
			MISO01	I/O	2nd SPI0 MISO (Master In, Slave Out) pin.
42	25	21	PC.3	I/O	General purpose digital I/O pin.
			MOSI00	I/O	1st SPI0 MOSI (Master Out, Slave In) pin.
			I2SDO	O	I2S data output.
43	26	22	PC.2	I/O	General purpose digital I/O pin.
			MISO00	I/O	1st SPI0 MISO (Master In, Slave Out) pin.
			I2SDI	I	I2S data input.
44	27	23	PC.1	I/O	General purpose digital I/O pin.
			SPICLK0	I/O	SPI0 serial clock pin.
			I2SBCLK	I/O	I2S bit clock pin.
45	28	24	PC.0	I/O	General purpose digital I/O pin.
			SPISS00	I/O	1st SPI0 slave select pin.
			I2SLRCLK	I/O	I2S left right channel clock.
46			PE.6	I/O	General purpose digital I/O pin.
47	29		PE.5	I/O	General purpose digital I/O pin.
			PWM5	I/O	PWM5 output/Capture input.
			T1EX	I	Timer1 external capture input pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
48	30		PB.11	I/O	General purpose digital I/O pin.
			TM3	I/O	Timer3 event counter input / toggle output.
			PWM4	I/O	PWM4 output/Capture input.
49	31		PB.10	I/O	General purpose digital I/O pin.
			TM2	I/O	Timer2 event counter input / toggle output.
			SPISS01	I/O	2nd SPI0 slave select pin.
50	32		PB.9	I/O	General purpose digital I/O pin.
			TM1	I/O	Timer1 event counter input / toggle output.
			SPISS11	I/O	2nd SPI1 slave select pin.
51			PE.4	I/O	General purpose digital I/O pin.
52			PE.3	I/O	General purpose digital I/O pin.
53			PE.2	I/O	General purpose digital I/O pin.
54			PE.1	I/O	General purpose digital I/O pin.
			PWM7	I/O	PWM7 output/Capture input.
55			PE.0	I/O	General purpose digital I/O pin.
			PWM6	I/O	PWM6 output/Capture input.
56			PC.13	I/O	General purpose digital I/O pin.
			MOSI11	I/O	2nd SPI1 MOSI (Master Out, Slave In) pin.
57			PC.12	I/O	General purpose digital I/O pin.
			MISO11	I/O	2nd SPI1 MISO (Master In, Slave Out) pin.
58	33		PC.11	I/O	General purpose digital I/O pin.
			MOSI10	I/O	1st SPI1 MOSI (Master Out, Slave In) pin.
59	34		PC.10	I/O	General purpose digital I/O pin.
			MISO10	I/O	1st SPI1 MISO (Master In, Slave Out) pin.
60	35		PC.9	I/O	General purpose digital I/O pin.
			SPICLK1	I/O	SPI1 serial clock pin.
61	36		PC.8	I/O	General purpose digital I/O pin.
			SPISS10	I/O	1st SPI1 slave select pin.
			MCLK	O	EBI external clock output pin
62	37	25	PA.15	I/O	General purpose digital I/O pin.
			PWM3	I/O	PWM output/Capture input.
			I2SMCLK	O	I^2S master clock output pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
			SC2PWR	**O**	SmartCard2 power pin.
63	38	26	PA.14	**I/O**	General purpose digital I/O pin.
			PWM2	**I/O**	PWM2 output/Capture input.
			SC2RST	**O**	SmartCard2 reset pin.
			AD15	**I/O**	EBI Address/Data bus bit15
64	39	27	PA.13	**I/O**	General purpose digital I/O pin.
			PWM1	**I/O**	PWM1 output/Capture input.
			SC2CLK	**O**	SmartCard2 clock pin.
			AD14	**I/O**	EBI Address/Data bus bit14
65	40	28	PA.12	**I/O**	General purpose digital I/O pin.
			PWM0	**I/O**	PWM0 output/Capture input.
			SC2DAT	**O**	SmartCard2 data pin.
			AD13	**I/O**	EBI Address/Data bus bit13
66	41	29	ICE_DAT	**I/O**	Serial wire debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin
67	42	30	ICE_CLK	**I**	Serial wire debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin
68			V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
69			V_{SS}	**P**	Ground pin for digital circuit.
70	43	31	AV_{SS}	**AP**	Ground pin for analog circuit.
71	44	32	PA.0	**I/O**	General purpose digital I/O pin.
			ADC0	**AI**	ADC0 analog input.
			SC0PWR	**O**	SmartCard0 power pin.
72	45	33	PA.1	**I/O**	General purpose digital I/O pin.
			ADC1	**AI**	ADC1 analog input.
			SC0RST	**O**	SmartCard0 reset pin.
			AD12	**I/O**	EBI Address/Data bus bit12
73	46	34	PA.2	**I/O**	General purpose digital I/O pin.
			ADC2	**AI**	ADC2 analog input.
			SC0CLK	**O**	SmartCard0 clock pin.
			AD11	**I/O**	EBI Address/Data bus bit11

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
74	47	35	PA.3	I/O	General purpose digital I/O pin.
			ADC3	AI	ADC3 analog input.
			SC0DAT	O	SmartCard0 data pin.
			AD10	I/O	EBI Address/Data bus bit10
75	48	36	PA.4	I/O	General purpose digital I/O pin.
			ADC4	AI	ADC4 analog input.
			SC1PWR	O	SmartCard1 power pin.
			AD9	I/O	EBI Address/Data bus bit9
76	49	37	PA.5	I/O	General purpose digital I/O pin.
			ADC5	AI	ADC5 analog input.
			SC1RST	O	SmartCard1 reset pin.
			AD8	I/O	EBI Address/Data bus bit8
77	50	38	PA.6	I/O	General purpose digital I/O pin.
			ADC6	AI	ADC6 analog input.
			SC1CLK	I/O	SmartCard1 clock pin.
			AD7	I/O	EBI Address/Data bus bit7
78	51	39	PA.7	I/O	General purpose digital I/O pin.
			ADC7	AI	ADC7 analog input.
			SC1DAT	O	SmartCard1 data pin.
			SPISS21	I/O	2nd SPI2 slave select pin.
			AD6	I/O	EBI Address/Data bus bit6
79			V_{REF}	AP	Voltage reference input for ADC.
80	52	40	AV_{DD}	AP	Power supply for internal analog circuit.
81			PD.0	I/O	General purpose digital I/O pin.
			SPISS20	I/O	1st SPI2 slave select pin.
82			PD.1	I/O	General purpose digital I/O pin.
			SPICLK2	I/O	SPI2 serial clock pin.
83			PD.2	I/O	General purpose digital I/O pin.
			MISO20	I/O	1st SPI2 MISO (Master In, Slave Out) pin.
84			PD.3	I/O	General purpose digital I/O pin.
			MOSI20	I/O	1st SPI2 MOSI (Master Out, Slave In) pin.
85			PD.4	I/O	General purpose digital I/O pin.
			MISO21	I/O	2nd SPI2 MISO (Master In, Slave Out) pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
86			PD.5	**I/O**	General purpose digital I/O pin.
			MOSI21	**I/O**	2nd SPI2 MOSI (Master Out, Slave In) pin.
87	53	41	PC.7	**I/O**	General purpose digital I/O pin.
			CPN0	**AI**	Comparator0 negative input pin.
			SC1CD	**I**	SmartCard1 card detect pin.
			AD5	**I/O**	EBI Address/Data bus bit5
88	54	42	PC.6	**I/O**	General purpose digital I/O pin.
			CPP0	**AI**	Comparator0 positive input pin.
			SC0CD	**I**	SmartCard0 card detect pin.
			AD4	**I/O**	EBI Address/Data bus bit4
89	55		PC.15	**I/O**	General purpose digital I/O pin.
			CPN1	**AI**	Comparator1 negative input pin.
			AD3	**I/O**	EBI Address/Data bus bit3
90	56		PC.14	**I/O**	General purpose digital I/O pin.
			CPP1	**AI**	Comparator1 positive input pin.
			AD2	**I/O**	EBI Address/Data bus bit2
91	57	43	PB.15	**I/O**	General purpose digital I/O pin.
			/INT1	**I**	External interrupt1 input pin.
			T0EX	**I**	Timer0 external capture input pin.
92	58	44	PF.0	**I/O**	General purpose digital I/O pin.
			XT1_OUT	**O**	External 4~24 MHz (high speed) crystal output pin.
93	59	45	PF.1	**I/O**	General purpose digital I/O pin.
			XT1_IN	**I**	External 4~24 MHz (high speed) crystal input pin.
94	60	46	/RESET	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
95	61		V_{SS}	**P**	Ground pin for digital circuit.
96	62		V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
97			PF.2	**I/O**	General purpose digital I/O pin.
			PS2DAT	**I/O**	PS/2 data pin.
98			PF.3	**I/O**	General purpose digital I/O pin.
			PS2CLK	**I/O**	PS/2 clock pin.

Pin No.			Pin Name	Pin Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin			
99	63	47	PV_{SS}	**P**	PLL ground.
100	64	48	PB.8	**I/O**	General purpose digital I/O pin.
			STADC	**I**	ADC external trigger input.
			TM0	**I/O**	Timer0 event counter input / toggle output.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

5.1 NuMicro® NUC100 Block Diagram

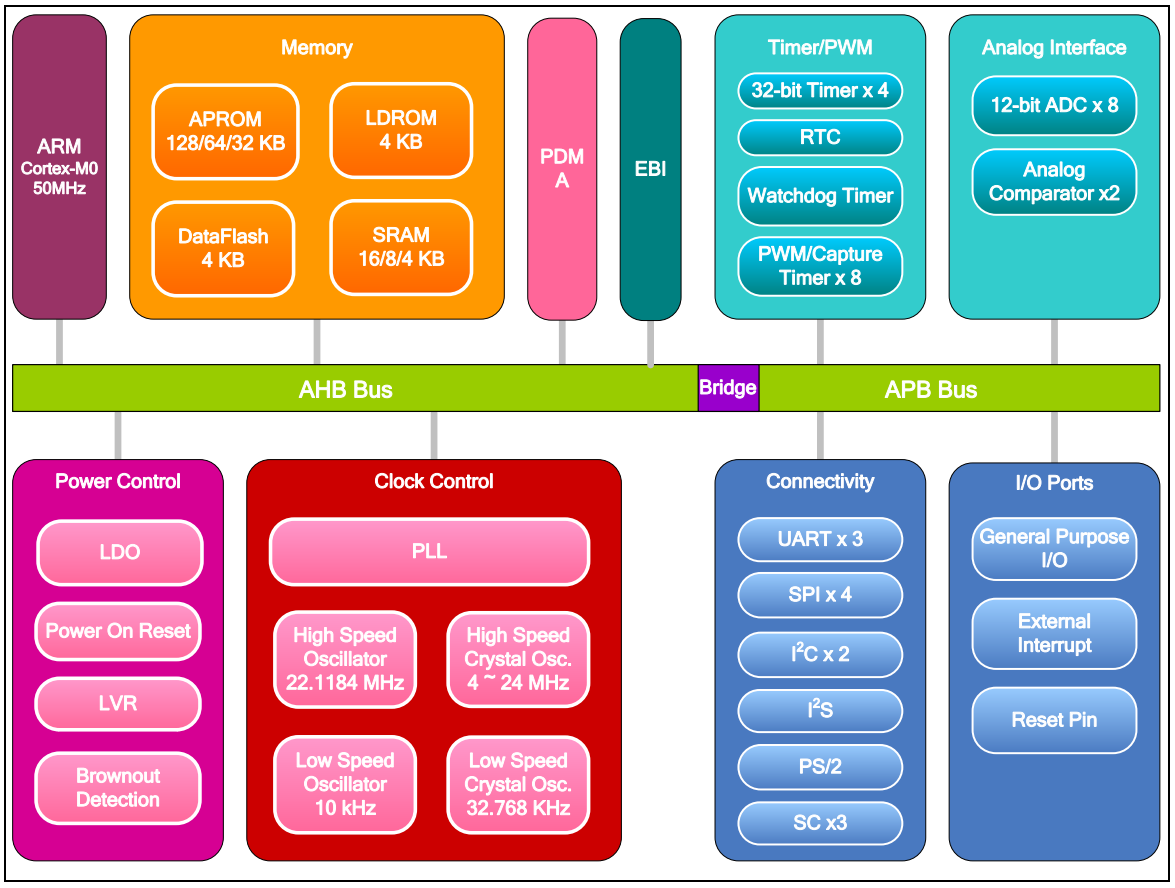


Figure 5-1 NuMicro® NUC100 Block Diagram

5.2 NuMicro® NUC120 Block Diagram

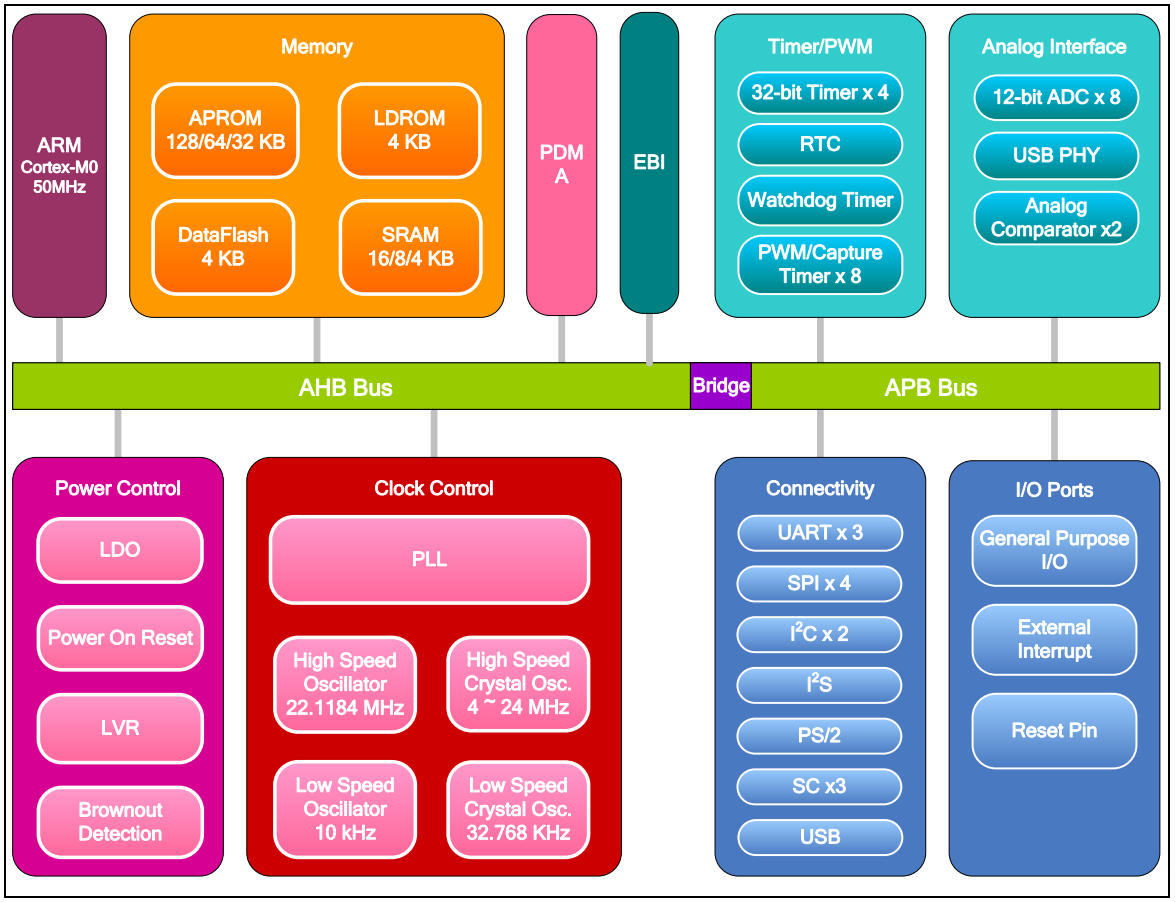


Figure 5-2 NuMicro® NUC120 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6-1 shows the functional controller of processor.

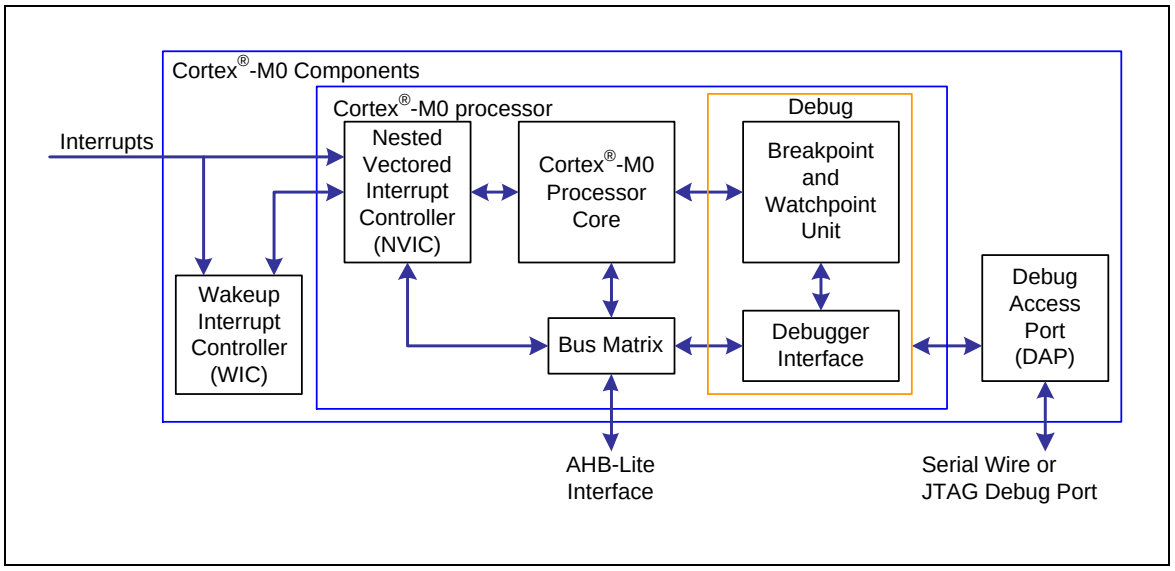


Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC:

  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from RSTSRC register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIP_RST (IPRSTC1[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPU_RST (IPRSTC1[1])

Power-on Reset or CHIP_RST (IPRSTC1[0]) reset the whole chip including all peripherals, external crystal circuit and BS (ISPCON[1]) bit.

SYSRESETREQ (AIRCR[2]) reset the whole chip including all peripherals, but does not reset external crystal circuit and BS (ISPCON[1]) bit.

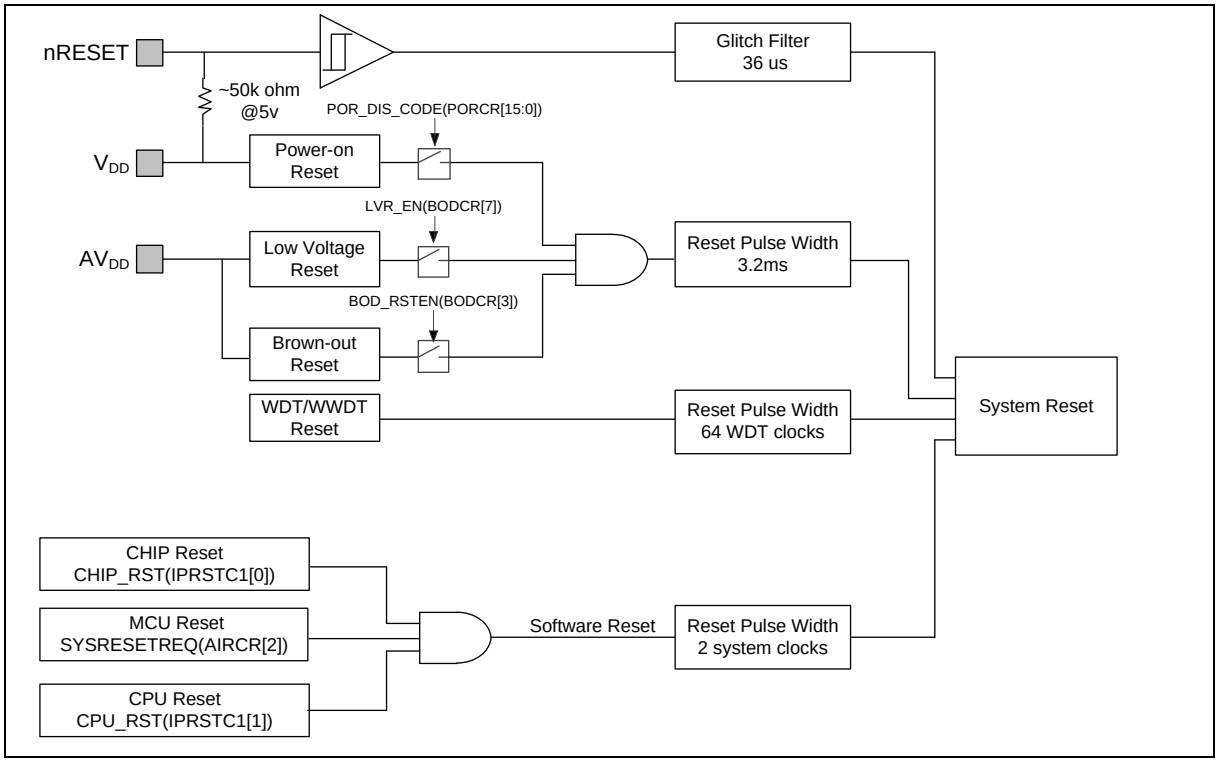


Figure 6-2 System Reset Resources

There are a total of 8 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6-1.

Reset Sources / Register	POR	nRESET	WDT	LVR	BOD	CHIP	MCU	CPU
RSTSRC	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIP_RST (IPRSTC1[0])	0x0	-	-	-	-	-	-	-
BOD_EN (BODCR[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	-
BOD_VL (BODCR[2:1])								
BOD_RSTEN (BODCR[3])								
XTL12M_EN (PWRCON[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDT_EN (APBCLK[0])	0x1	-	0x1	-	-	0x1	-	-
HCLK_S (CLKSEL0[2:0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDT_S	0x3	0x3	-	-	-	-	-	-

(CLKSEL1[1:0])								
XTL12M_STB (CLKSTATUS[0])	0x0	-	-	-	-	-	-	-
XTL32K_STB (CLKSTATUS[1])	0x0	-	-	-	-	-	-	-
PLL_STB (CLKSTATUS[2])	0x0	-	-	-	-	-	-	-
OSC10K_STB (CLKSTATUS[3])	0x0	-	-	-	-	-	-	-
OSC22M_STB (CLKSTATUS[4])	0x0	-	-	-	-	-	-	-
CLK_SW_FAIL (CLKSTATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
WTE (WTCR[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
WTCR	0x0700	0x0700	0x0700	0x0700	0x0700	0x0700	-	-
WTCRALT	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTRLD	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTCR	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	-
WWDTSR	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTCVR	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	-	-
BS (ISPCON[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
DFBADR	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	-
CBS (ISPSTA[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
VECMAP (ISPSTA[20:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value							-
FMC Registers	Reset Value							
Note: '-' means that the value of register keeps original setting.								

Table 6-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 36 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 36 us (glitch filter). The RSTS_RESET (RSTSRC[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6-3 shows the nRESET reset waveform.

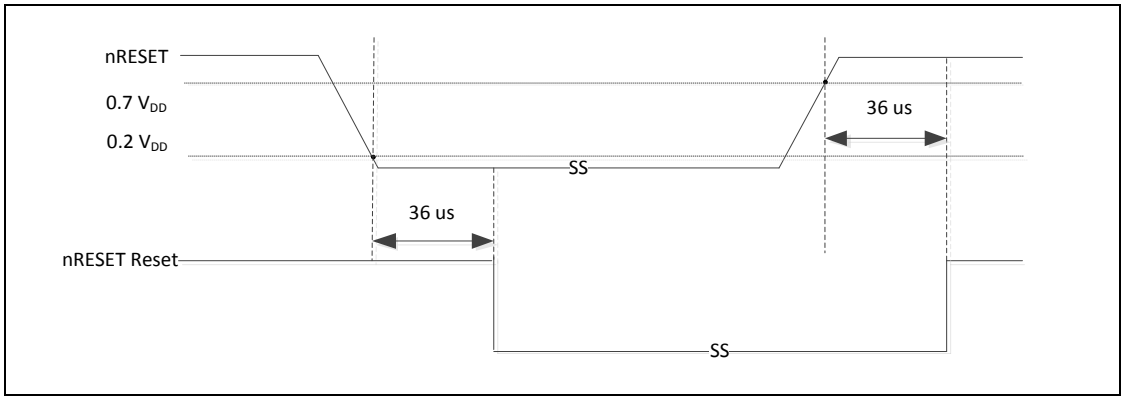


Figure 6-3 nRESET Reset Waveform

6.2.2.2 Power-On Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the RSTS_POR (RSTSRC[0]) will be set to 1 to indicate there is a POR reset event. The RSTS_POR (RSTSRC[0]) bit can be cleared by writing 1 to it. Figure 6-4 shows the waveform of Power-On reset.

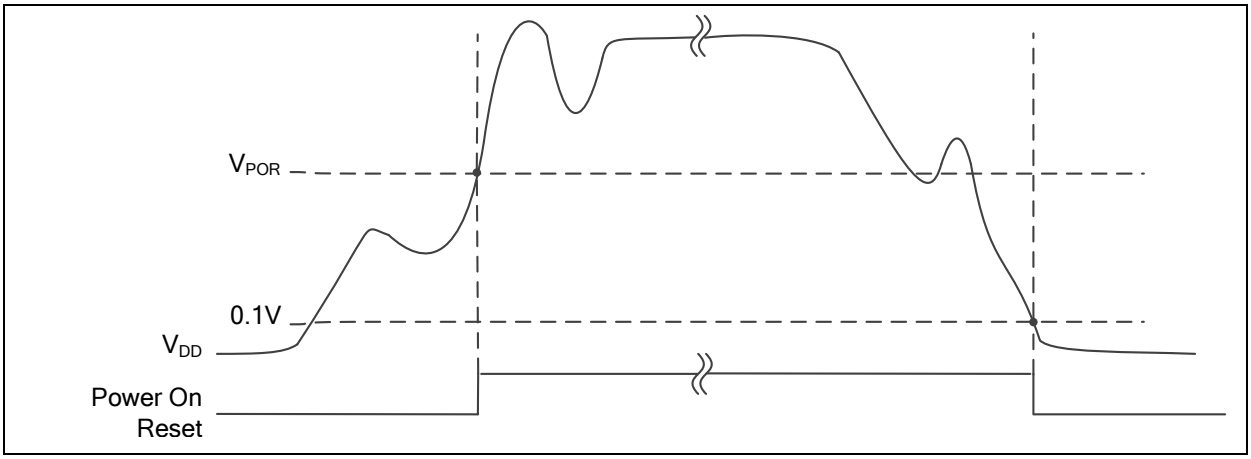


Figure 6-4 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVR_EN (BODCR[7]) to 1, after 100us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the

AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time (16*HCLK cycles), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time. The RSTS_RESET (RSTSRC[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6-5 shows the Low Voltage Reset waveform.

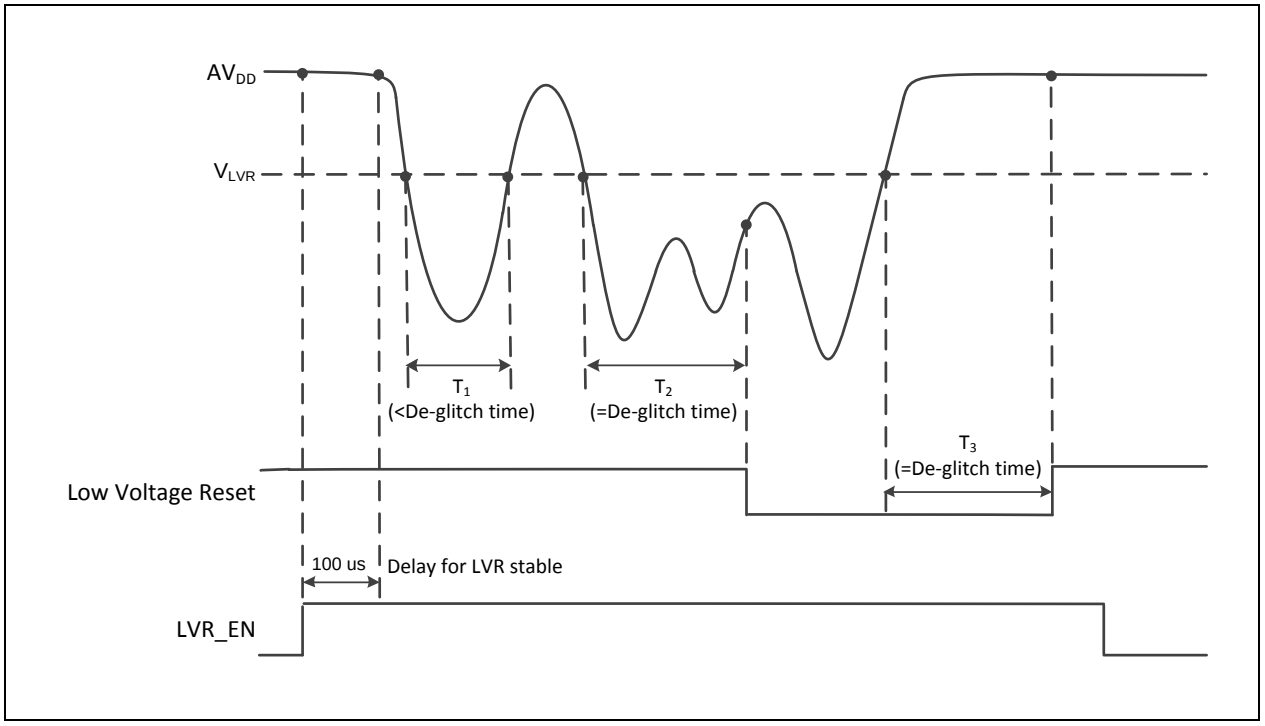


Figure 6-5 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BOD_EN (BODCR[0]), Brown-Out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BOD_EN (BODCR[0]) and BOD_VL (BODCR[2:1]) and the state keeps longer than De-glitch time (Max(20*HCLK cycles, 1*LIRC cycle)), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time. The default value of BOD_EN, BOD_VL and BOD_RSTEN is set by flash controller user configuration register CBODEN (CONFIG0[23]), CBOV1-0 (CONFIG0[22:21]) and CBORST (CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6-6 shows the Brown-Out Detector waveform.

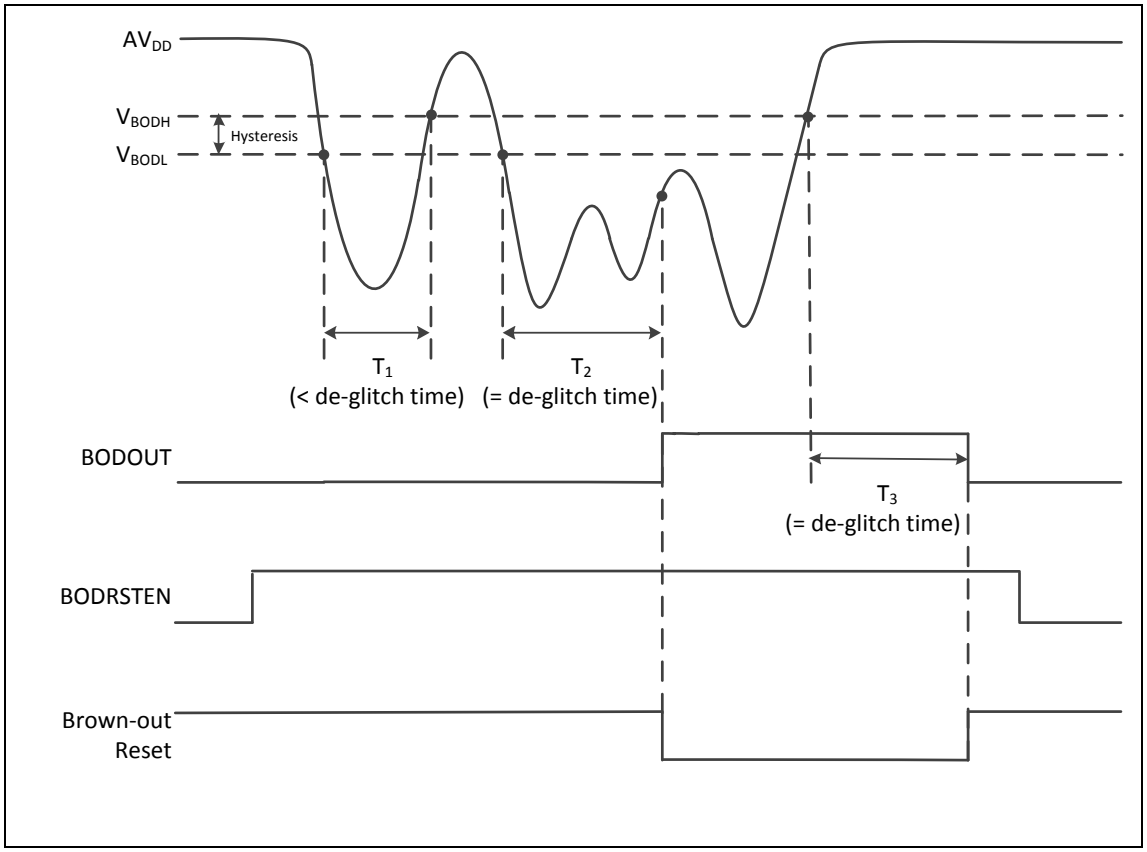


Figure 6-6 Brown-Out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer (WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking RSTS_WDT (RSTSRC[2]).

6.2.2.6 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPU Reset CPU_RST (IPRSTC1[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-On Reset. The CPU and all peripherals are reset and BS (ISPCON[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIP Reset CHIP_RST (IPRSTC1[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS (ISPCON[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the MCU Reset SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, BOD, USB and GPIO
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6-2 Power Mode Difference Table

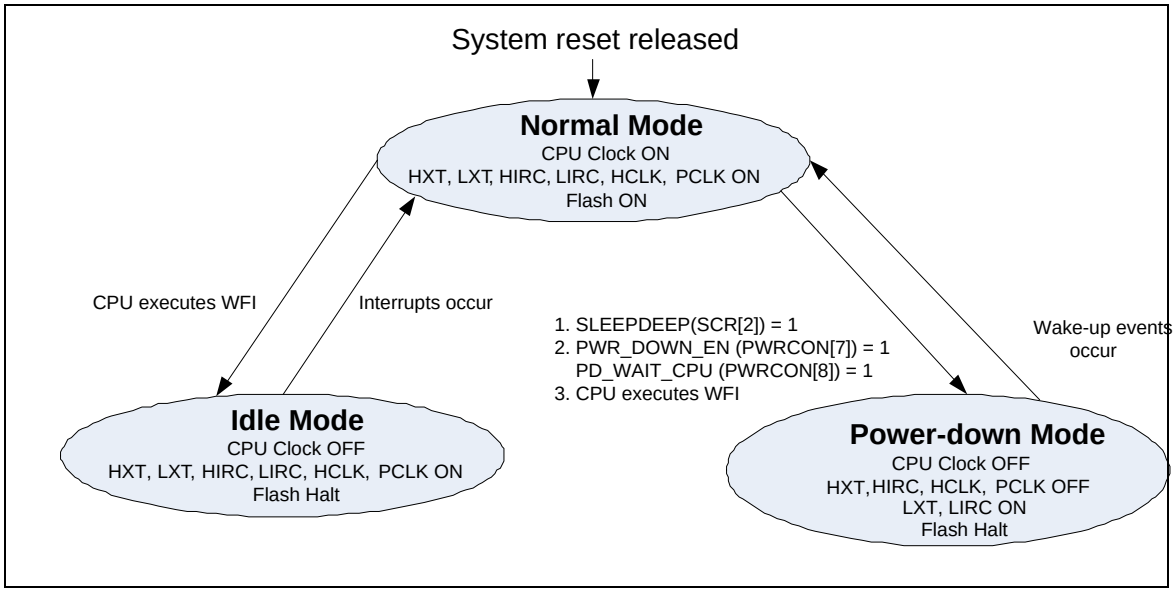


Figure 6-7 Power Mode State Machine

1. LXT (32 kHz XTL) ON or OFF depends on S/W setting in run mode.
2. LIRC (10 kHz OSC) ON or OFF depends on S/W setting in run mode.

3. If TIMER clock source is selected as LXT/LIRC and LXT/LIRC is on.
4. If PWM clock source is selected as LXT and LXT is on.
5. If WDT clock source is selected as LXT/LIRC and LXT/LIRC is on.
6. If RTC clock source LXT is on.

	Normal Mode	Idle Mode	Power-down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (12/16 MHz OSC)	ON	ON	Halt
LXT (32 kHz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
EBI	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	ON/OFF[4]
WDT	ON	ON	ON/OFF[5]
WWDT	ON	ON	Halt
RTC	ON	ON	ON/OFF[6]
UART	ON	ON	Halt
SC	ON	ON	Halt
PS/2	ON	ON	Halt
I^2C	ON	ON	Halt
SPI	ON	ON	Halt
I^2S	ON	ON	Halt
USB	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt

Table 6-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, RTC, UART, BOD, GPIO and USB

After chip enters power down, the following wake-up sources can wake chip up to normal mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear BOD_INTF (BODCR[4]).
GPIO	GPIO Interrupt	After software write 1 to clear the ISRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWF (TISRx[1]) and TIF (TISRx[0]).
WDT	WDT Interrupt	After software writes 1 to clear WTWKF (WTCR[5]) (Write Protect).
RTC	Alarm Interrupt	After software writes 1 to clear AIF (RIIR[0]).
	Time Tick Interrupt	After software writes 1 to clear TIF (RIIR[1]).
UART	nCTS wake-up	After software writes 1 to clear DCTSF (UA_MSR[0]).
I^2C	Addressing I^2C device	After software writes 1 to clear WKUPIF (I2CWKUPSTS[0]).
USB	Remote Wake-up	After software writes 1 to clear BUS_STS (USBD_INTSTS[0]).

*User needs to wait this condition before setting PWR_DOWN_EN (PWRCON[7]) and execute WFI to enter Power-down mode.

Table 6-4*User needs to wait this condition before setting PWR_DOWN_EN (PWRCON[7]) and execute WFI to enter Power-down mode.

Table 6-4 lists the condition about how to enter Power-down mode again for each peripheral.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear BOD_INTF (BODCR[4]).
GPIO	GPIO Interrupt	After software write 1 to clear the ISRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWF (TISRx[1]) and TIF (TISRx[0]).
WDT	WDT Interrupt	After software writes 1 to clear WTWKF (WTCR[5]) (Write Protect).
RTC	Alarm Interrupt	After software writes 1 to clear AIF (RIIR[0]).
	Time Tick Interrupt	After software writes 1 to clear TIF (RIIR[1]).
UART	nCTS wake-up	After software writes 1 to clear DCTSF (UA_MSR[0]).
I^2C	Addressing I^2C device	After software writes 1 to clear WKUPIF (I2CWKUPSTS[0]).
USB	Remote Wake-up	After software writes 1 to clear BUS_STS (USBD_INTSTS[0]).

*User needs to wait this condition before setting PWR_DOWN_EN (PWRCON[7]) and execute WFI to enter Power-down mode.

Table 6-4 Condition of Entering Power-down Mode Again

6.2.4 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.

- USB transceiver power from V_{BUS} offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and V_{DD33}, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6-8 shows the power distribution of NuMicro® NUC100. Figure 6-9 shows the power distribution of NuMicro® NUC120.

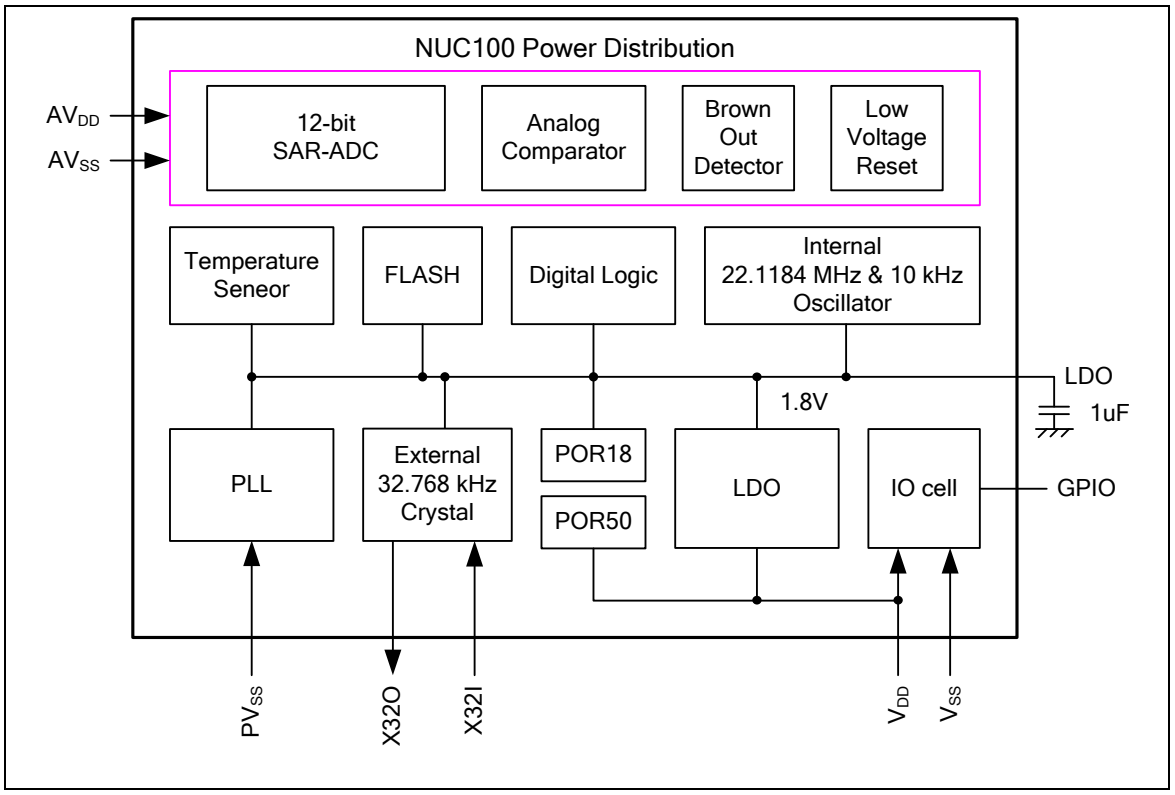


Figure 6-8 NuMicro® NUC100 Power Distribution Diagram

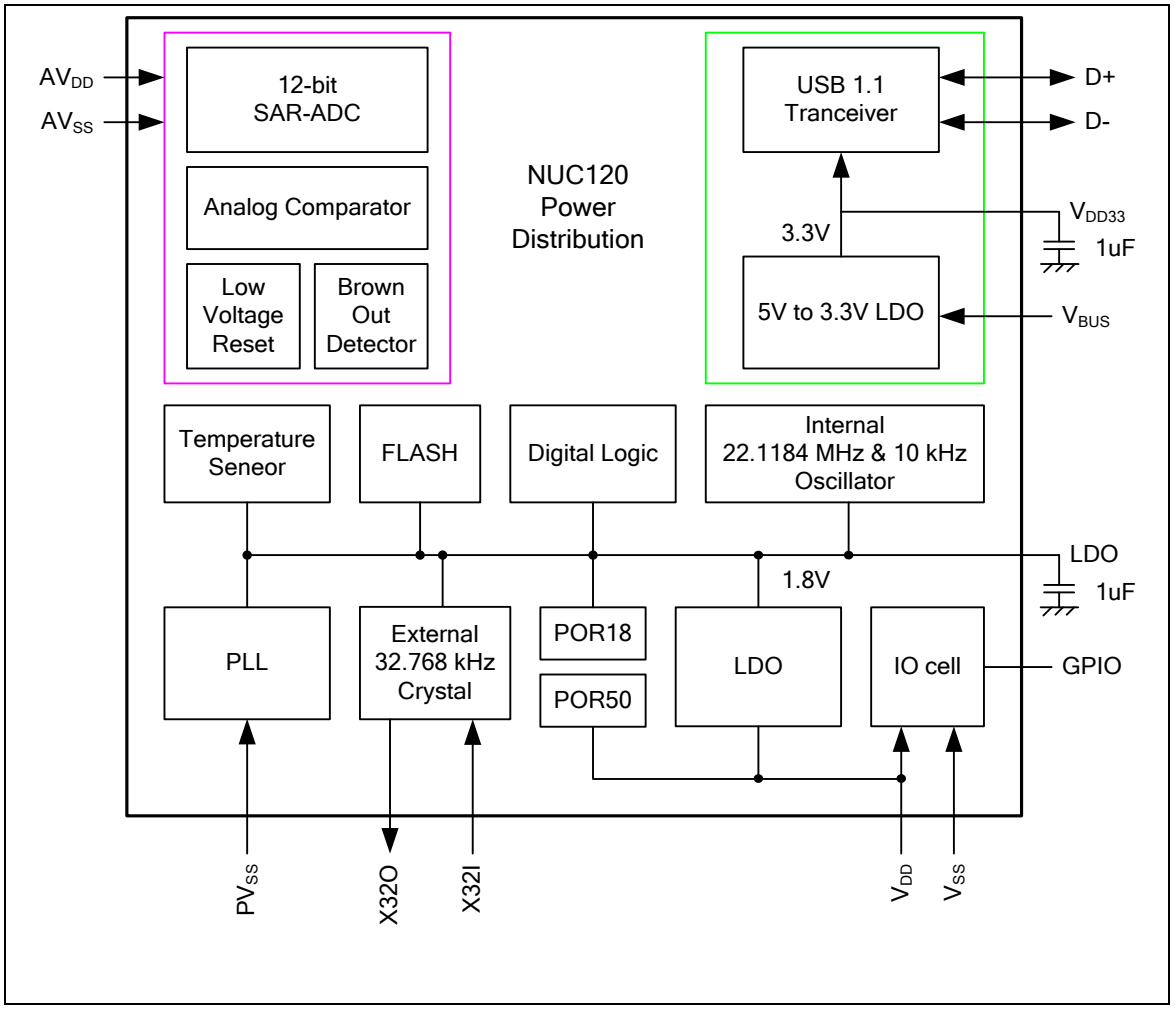


Figure 6-9 NuMicro® NUC120 Power Distribution Diagram

6.2.5 System Memory Map

The NuMicro® NUC100 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripheral. The NuMicro® NUC100 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers
0x4013_4000 – 0x4013_7FFF	SPI3_BA	SPI3 with master/slave function Control Registers
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers

0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
0x4019_0000 – 0x4019_3FFF	SC0_BA	SC0 Control Registers
0x4019_4000 – 0x4019_7FFF	SC1_BA	SC1 Control Registers
0x4019_8000 – 0x4019_BFFF	SC2_BA	SC2 Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I^2S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6-5 Address Space Assignments for On-Chip Controllers

6.2.6 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.7 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator to reduce the overall system power consumption.

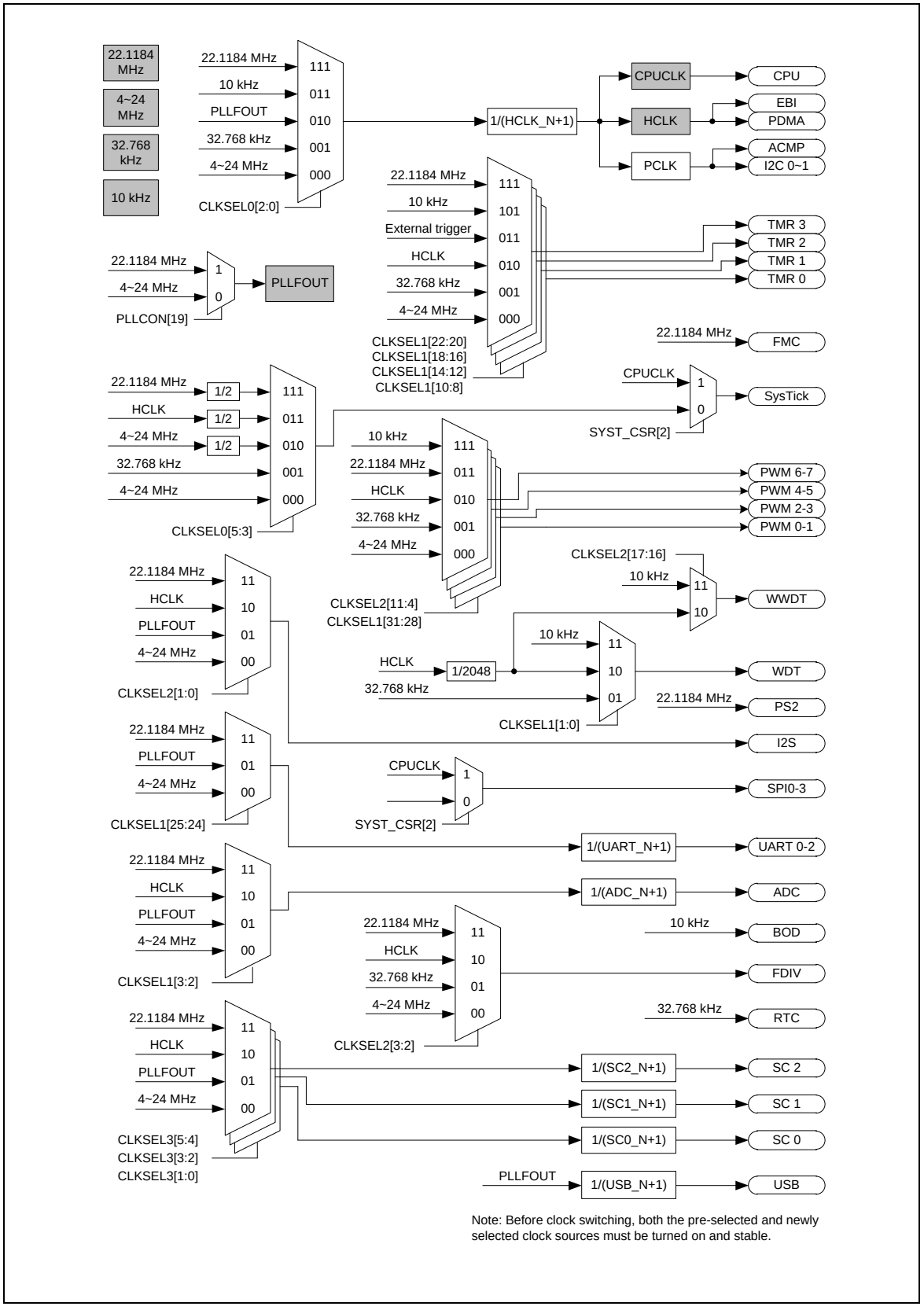


Figure 6-10 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 5 clock sources as listed below:

- One external 32.768 kHz low speed crystal
- One external 4~24 MHz high speed crystal
- One programmable PLL FOUT (PLL source consists of external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator)
- One internal 22.1184 MHz high speed oscillator
- One internal 10 kHz low speed oscillator

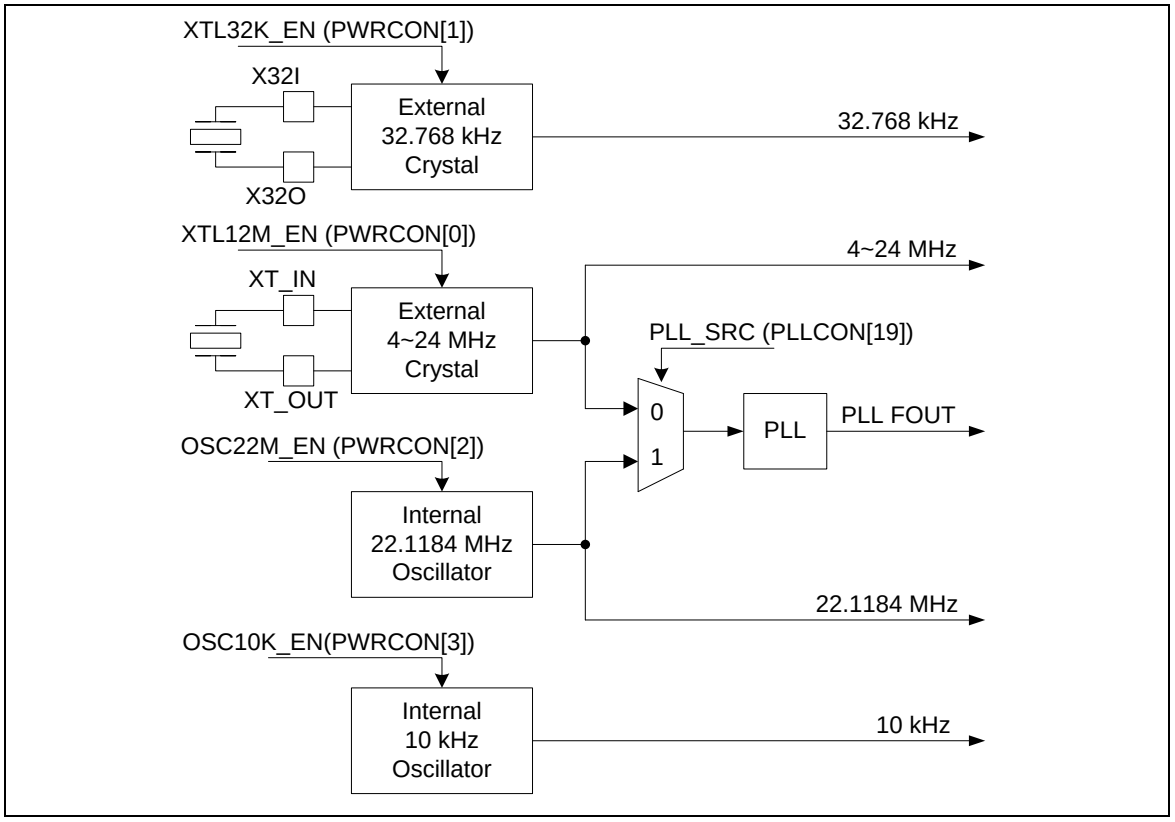


Figure 6-11 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6-12.

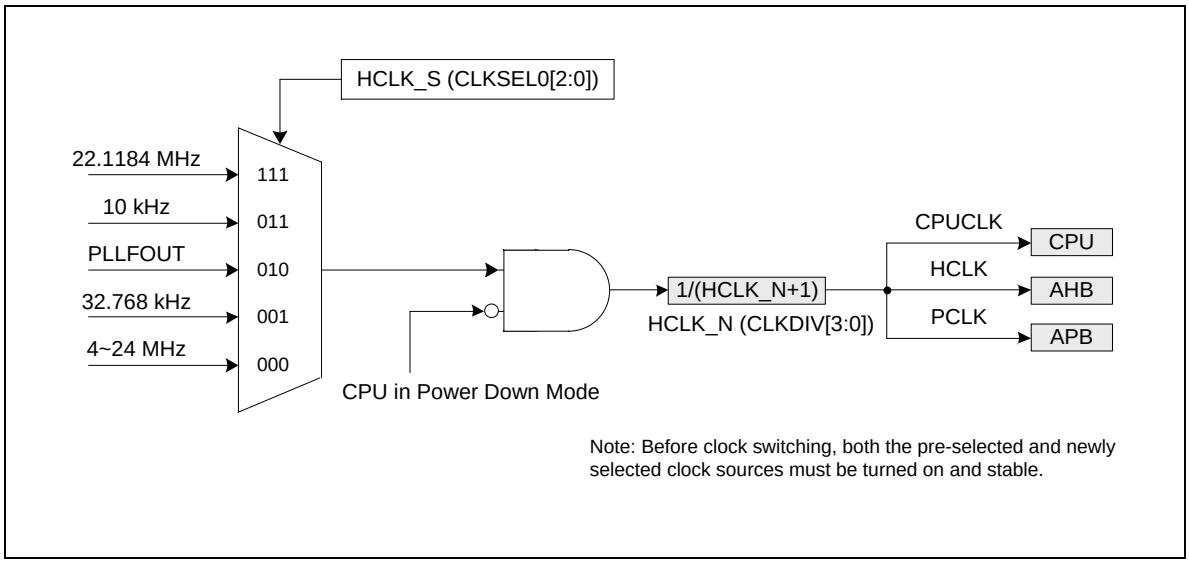


Figure 6-12 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6-13.

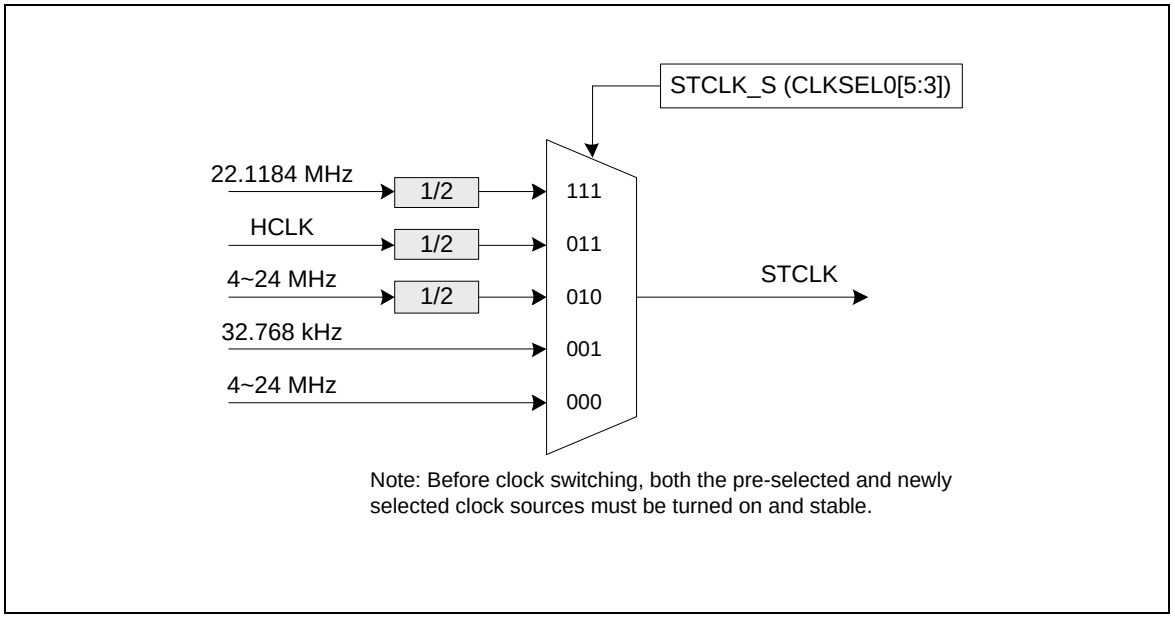


Figure 6-13 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock can be selected as different clock source depends on the clock source select control registers (CLKSEL1, CLKSEL2 and CLKSEL3).

6.3.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
  - Internal 10 kHz low speed oscillator clock
  - External 32.768 kHz low speed crystal clock
- Peripherals Clock (when IP adopt external 32.768 kHz low speed crystal oscillator or 10 kHz low speed oscillator as clock source)

6.3.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^{1}$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

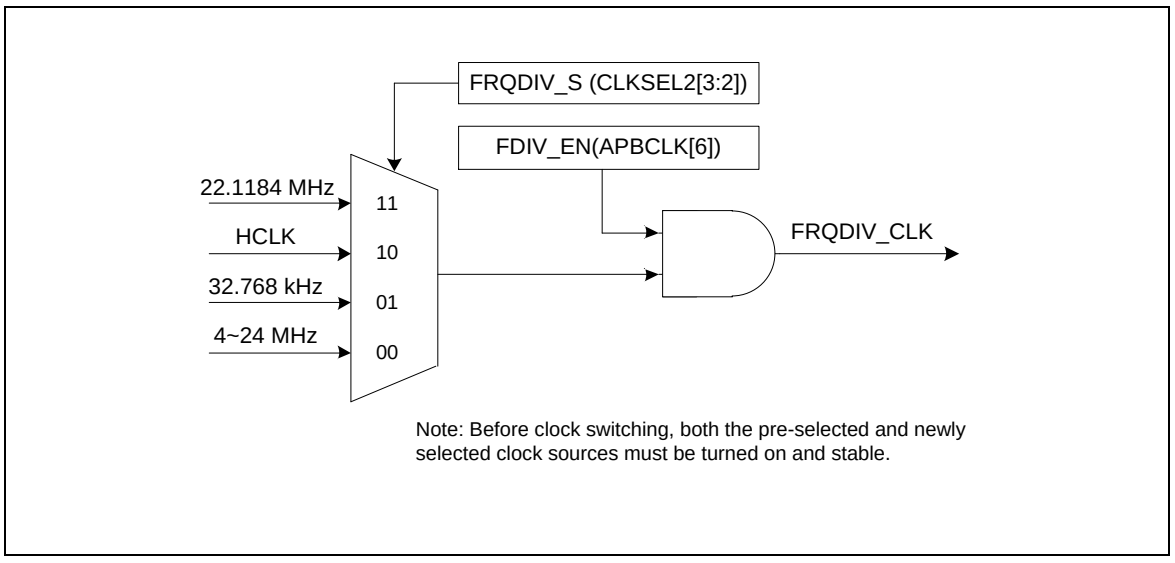


Figure 6-14 Clock Source of Frequency Divider

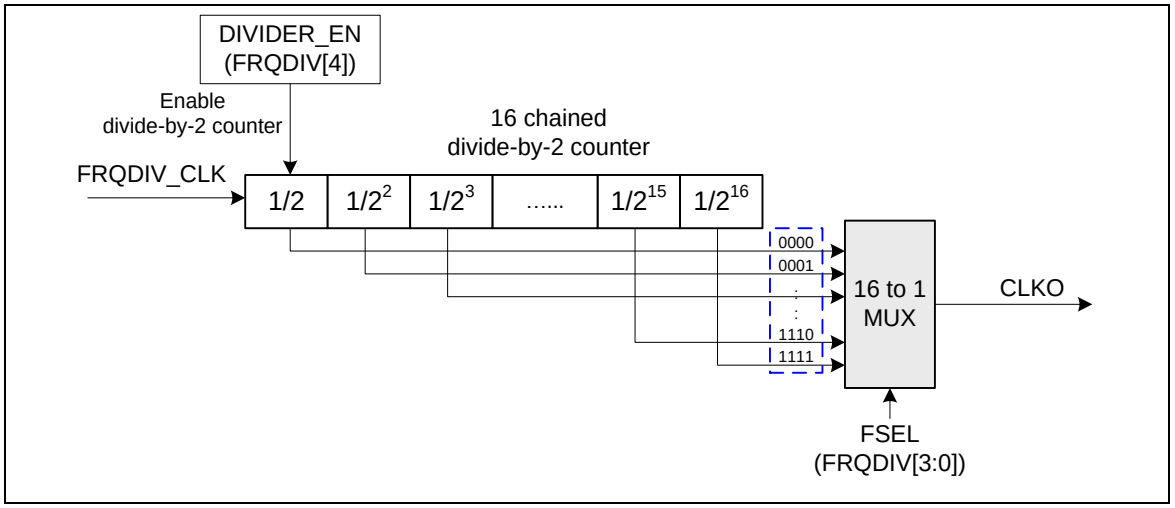


Figure 6-15 Frequency Divider Block Diagram

6.4 FLASH MEMORY CONTROLLER (FMC)

6.4.1 Overview

The NuMicro® NUC100 series has 128/64/32 Kbytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, the NuMicro® NUC100 series also provides additional DATA Flash for user to store some application dependent data. For 128 Kbytes APROM device, the Data Flash is shared with original 128K program memory and its start address is configurable in Config1. For 64/32 Kbytes APROM device, the Data Flash is fixed at 4K.

6.4.2 Features

- Runs up to 50 MHz with zero wait state for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 128/64/32 KB application program memory (APROM)
- 4 KB In-System-Programming (ISP) loader program memory (LDROM)
- 4KB Data Flash for 64/32 KB APROM device
- Configurable Data Flash size for 128KB APROM device
- Configurable or fixed 4 KB Data Flash with 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

6.5 External Bus Interface (EBI)

6.5.1 Overview

The NuMicro® NUC100 series LQFP-64 and LQFP-100 package is equipped with an external bus interface (EBI) for accessing an external device.

To save the connections between external device and this chip, EBI supports address bus and data bus multiplex mode. And, address latch enable (ALE) signal is used to differentiate the address and data cycle.

6.5.2 Features

External Bus Interface has the following functions:

- Supports external devices with max. 64 KB size (8-bit data width)/128 KB (16-bit data width)
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports 8-bit or 16-bit data width
- Supports variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD)
- Supports address bus and data bus multiplex mode to save the address pins
- Supports configurable idle cycle for different access condition: Write command finish (W2X), Read-to-Read (R2R)

6.6 General Purpose I/O (GPIO)

6.6.1 Overview

The NuMicro® NUC100 series has up to 84 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 84 pins are arranged in 6 ports named as GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. The GPIOA/B/C/D/E port has the maximum of 16 pins and GPIOF port has the maximum of 4 pins. Each of the 84 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} is from 5.0 V to 2.5 V.

6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function.

6.7 PDMA Controller (PDMA)

6.7.1 Overview

The NuMicro® NUC100 series DMA contains nine-channel peripheral direct memory access (PDMA) controller and a cyclic redundancy check (CRC) generator.

The PDMA that transfers data to and from memory or transfer data to and from APB devices. For PDMA channel (PDMA CH0~CH8), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. Software can stop the PDMA operation by disable PDMA PDMA_CSRx[PDMACEN]. The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The PDMA controller can increase source or destination address or fixed them as well.

The DMA controller contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU PIO mode and DMA transfer mode.

6.7.2 Features

- Supports nine PDMA channels and one CRC channel. Each PDMA channel can support a unidirectional transfer
- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Hardware round robin priority scheme. DMA channel 0 has the highest priority and channel 8 has the lowest priority
- PDMA operation
  - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
  - Supports word/half-word/byte transfer data width from/to peripheral
  - Supports address direction: increment, fixed.
- Cyclic Redundancy Check (CRC)
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8: $X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$
    - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
  - Supports programmable CRC seed value.
  - Supports programmable order reverse setting for input data and CRC checksum.
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports CPU PIO mode or DMA transfer mode.
  - Supports the follows write data length in CPU PIO mode
    - 8-bit write mode (byte): 1-AHB clock cycle operation.
    - 16-bit write mode (half-word): 2-AHB clock cycle operation.
    - 32-bit write mode (word): 4-AHB clock cycle operation.
  - Supports byte alignment transfer data length and word alignment transfer source address in CRC DMA mode.

6.8 Timer Controller (TMR)

6.8.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, event counting, interval measurement, clock generation, and delay timing. The timer can generate an interrupt signal upon time-out, or provide the current value during operation.

6.8.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin
- Supports external pin capture function for interval measurement
- Supports external pin capture function for reset timer counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated (TIF set to 1)

6.9 PWM Generator and Capture Timer (PWM)

6.9.1 Overview

The NuMicro® NUC100 series has 2 sets of PWM groups supporting a total of 4 sets of PWM generators that can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 4 sets of PWM generators provide eight independent PWM interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will be 1/900ns = 1000 kHz

6.9.2 Features

6.9.2.1 PWM Function:

- Up to 2 PWM groups (PWMA/PWMB) to support 8 PWM channels or 4 complementary PWM paired channels
- Each PWM group has two PWM generators with each PWM generator supporting one 8-bit prescaler, two clock divider, two PWM-timers, one Dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Edge-aligned type or Center-aligned type option

6.9.2.2 Capture Function:

- Timing control logic shared with PWM Generators
- Supports 8 Capture input channels shared with 8 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

6.10 Watchdog Timer (WDT)

6.10.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.10.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable Watchdog Timer reset delay period, it includes (1024+2)、(128+2) 、(16+2) or (1+2) WDT_CLK reset delay period.
- Supports force Watchdog Timer enabled after chip powered on or reset while CWDTEN (Config0[31] watchdog enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function when WDT clock source is selected to 10 kHz low speed oscillator.

6.11 Window Watchdog Timer (WWDT)

6.11.1 Overview

The purpose of Window Watchdog Timer is to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.11.2 Features

- 6-bit down counter (WWDTVAL[5:0]) and 6-bit compare value (WWDTCR[21:16] – WINCMP value) to make the window period flexible
- Selectable maximum 11-bit WWDT clock prescale (WWDTCR[11:8] – PERIODSEL value) to make WWDT time-out interval variable

6.13 Real Time Clock (RTC)

6.13.1 Overview

The Real Time Clock (RTC) controller provides user with the real time and calendar message. The clock source of RTC controller is from an external 32.768 kHz low speed crystal which connected at pins X32I and X32O (refer to pin Description) or from an external 32.768 kHz low speed oscillator output fed at pin X32I. The RTC controller provides the real time message (hour, minute, second) in TLR (RTC Time Loading Register) as well as calendar message (year, month, day) in CLR (RTC Calendar Loading Register). It also offers RTC alarm function that user can preset the alarm time in TAR (RTC Time Alarm Register) and alarm calendar in CAR (RTC Calendar Alarm Register). The data format of RTC time and calendar message are all expressed in BCD format.

The RTC controller supports periodic RTC Time Tick and Alarm Match interrupts. The periodic RTC Time Tick interrupt has 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0] Time Tick Register). When real time and calendar message in TLR and CLR are equal to alarm time and calendar settings in TAR and CAR, the AIF (RIIR [0] RTC Alarm Interrupt Flag) is set to 1 and the RTC alarm interrupt signal is generated if the AIER (RIER [0] Alarm Interrupt Enable) is enabled.

Both RTC Time Tick and Alarm Match interrupt signal can cause chip to wake-up from Idle or Power-down mode if the correlate interrupt enable bit (AIER or TIER) is set to 1 before chip enters Idle or Power-down mode.

6.13.2 Features

- Supports real time counter in TLR (hour, minute, second) and calendar counter in CLR (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in TAR and CAR
- Selectable 12-hour or 24-hour time scale in TSSR register
- Supports Leap Year indication in LIR register
- Supports Day of the Week counter in DWR register
- Frequency of RTC clock source compensate by FCR register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated

6.14 UART Interface Controller (UART)

The NuMicro® NUC100 series provides up to three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UART. Besides, only UART0 and UART1 support the flow control function.

6.14.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR, LIN master/slave mode and RS-485 mode functions. Each UART channel supports seven types of interrupts including:

- Transmitter FIFO empty interrupt (INT_THRE)
- Receiver threshold level reached interrupt (INT_RDA),
- Line status interrupt (parity error or frame error or break interrupt) (INT_RLS),
- Receiver buffer time-out interrupt (INT_TOUT),
- MODEM/Wake-up status interrupt (INT_MODEM),
- Buffer error interrupt (INT_BUF_ERR)
- LIN interrupt (INT_LIN)

Interrupts of UART0 and UART2 share the interrupt number 12 (vector number is 28); Interrupt number 13 (vector number is 29) only supports UART1 interrupt. Refer to the Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0 is built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU. The UART1~2 are equipped with 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, frame error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 6-6 lists the equations in the various conditions and Table 6-7 lists the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud Rate Equation
0	0	0	Don't care	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	UART_CLK / (A+2), A must >=3

Table 6-6 UART Baud Rate Equation

System Clock = Internal 22.1184 MHz High Speed Oscillator						
Baud Rate	Mode 0		Mode 1		Mode 2	
	Parameter	Register	Parameter	Register	Parameter	Register
921600	x	x	A=0,B=11	0x2B00_0000	A=22	0x3000_0016

460800	A=1	0x0000_0001	A=1,B=15 A=2,B=11	0x2F00_0001 0x2B00_0002	A=46	0x3000_002E
230400	A=4	0x0000_0004	A=4,B=15 A=6,B=11	0x2F00_0004 0x2B00_0006	A=94	0x3000_005E
115200	A=10	0x0000_000A	A=10,B=15 A=14,B=11	0x2F00_000A 0x2B00_000E	A=190	0x3000_00BE
57600	A=22	0x0000_0016	A=22,B=15 A=30,B=11	0x2F00_0016 0x2B00_001E	A=382	0x3000_017E
38400	A=34	0x0000_0022	A=62,B=8 A=46,B=11 A=34,B=15	0x2800_003E 0x2B00_002E 0x2F00_0022	A=574	0x3000_023E
19200	A=70	0x0000_0046	A=126,B=8 A=94,B=11 A=70,B=15	0x2800_007E 0x2B00_005E 0x2F00_0046	A=1150	0x3000_047E
9600	A=142	0x0000_008E	A=254,B=8 A=190,B=11 A=142,B=15	0x2800_00FE 0x2B00_00BE 0x2F00_008E	A=2302	0x3000_08FE
4800	A=286	0x0000_011E	A=510,B=8 A=382,B=11 A=286,B=15	0x2800_01FE 0x2B00_017E 0x2F00_011E	A=4606	0x3000_11FE

Table 6-7 UART Baud Rate Setting Table

The UART0 and UART1 controllers support the auto-flow control function that uses two low-level signals, /CTS (clear-to-send) and /RTS (request-to-send), to control the flow of data transfer between the chip and external devices (e.g. Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts /RTS to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR [19:16]), the /RTS is de-asserted. The UART sends data out when UART controller detects /CTS is asserted from external device. If a valid asserted /CTS is not detected the UART controller will not send data out.

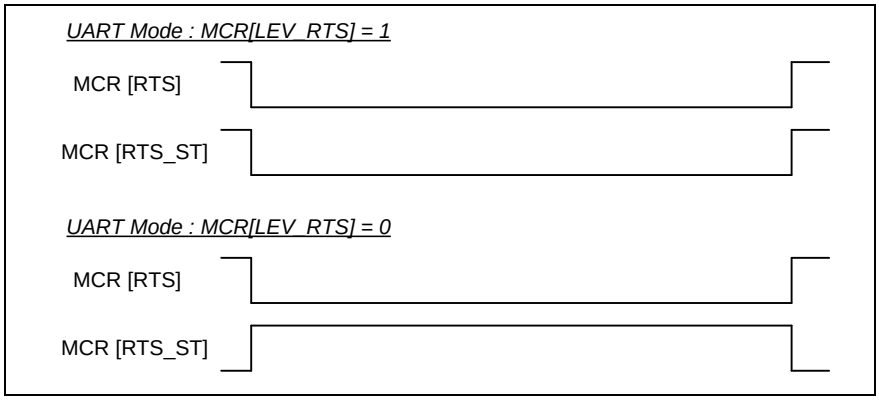


Figure 6-16 UART nRTS Auto-Flow Control Trigger Level

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UA_FUN_SEL [1]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with 1 start bit, 8 data bits, and 1 stop bit. The maximum data rate supports up to 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA

SIR Protocol encoder/decoder. The IrDA SIR Protocol encoder/decoder is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception, and this delay feature must be implemented by software.

The alternate function of UART controllers is LIN (Local Interconnect Network) function. The LIN mode is selected by setting the UA_FUN_SEL[1:0] to '01'. In LIN mode, 1 start bit and 8 data bits format with 1 stop bit are required in accordance with the LIN standard.

For NuMicro® NUC100 series, another alternate function of UART controllers is RS-485 9-bit mode, and direction control provided by /RTS pin or can program GPIO (PB.2 for UART0_nRTS and PB.6 for UART1_nRTS) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 transceiver control is implemented using the /RTS control signal from an asynchronous serial port to enable the RS-485 transceiver. In RS-485 mode, many characteristics of the receiving and transmitting are same as UART.

6.14.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 64/16/16 bytes (UART0/UART1/UART2) entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0 and UART1 support)
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0 and UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- UART0/UART1 can through DMA channels to receive/transmit data
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3-/16-bit duration for normal mode
- LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode.

- Supports RS-485 9-bit mode
- Supports hardware or software direct enable control provided by RTS pin

6.15 Smart Card Host Interface (SC)

6.15.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.15.2 Features

- ISO7816-3 T=0, T=1 compliant
- EMV2000 compliant
- Supports up to three ISO7816-3 ports
- Separates receive/ transmit 4 byte entry buffer for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 266 ETU)
- One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
- Supports auto inverse convention function
- Supports transmitter and receiver error retry and error retry number limitation function
- Supports hardware activation sequence process
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detecting the card removal

6.16 PS/2 Device Controller (PS2D)

6.16.1 Overview

The PS/2 device controller provides a basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the receive/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a “Request to Send” state, but host has ultimate control over communication. Data of DATA line sent from the host to the device is read on the rising edge and sent from the device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. Software can select 1 to 16 bytes for a continuous transmission.

6.16.2 Features

- Host communication inhibit and Request to Send state detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- Software override bus

6.17 I²C Serial Interface Controller (I²C)

6.17.1 Overview

I²C is a two-wire, bidirectional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6-17 for more detailed I²C BUS Timing.

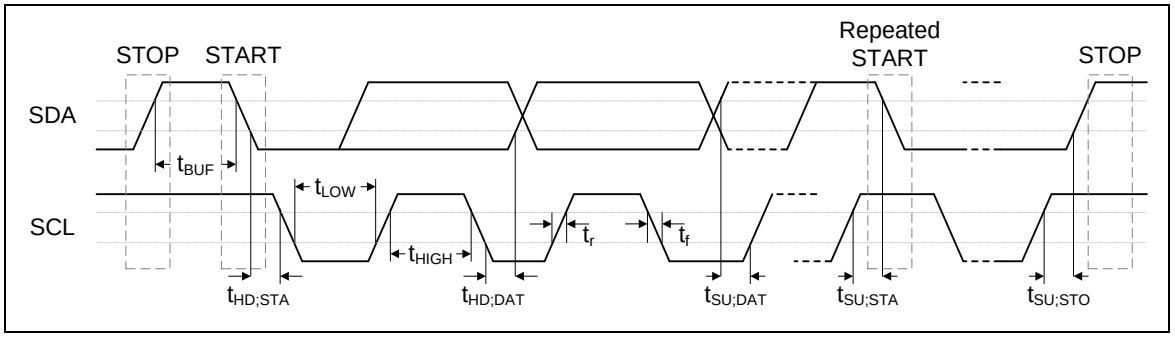


Figure 6-17 I²C Bus Timing

The device's on-chip I²C logic provides a serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C hardware interfaces to the I²C bus via two pins: SDA and SCL. Pull-up resistor is needed for I²C operation as the SDA and SCL are open drain pins. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

6.17.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- A built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- External pull-up resistors needed for high output
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave addresses with mask option)

6.18 Serial Peripheral Interface (SPI)

6.18.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro® NUC100 series contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a master or a slave device.

The SPI controller supports the variable serial clock function for special applications and 2-bit Transfer mode to connect 2 off-chip slave devices at the same time. This controller also supports the PDMA function to access the data buffer and also supports Dual I/O Transfer mode.

6.18.2 Features

- Up to four sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual I/O Transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Two slave select lines in Master mode
- Supports the byte reorder function
- Supports Byte or Word Suspend mode
- Variable output serial clock frequency in Master mode
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface

6.19 I²S Controller (I²S)

6.19.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 8-word deep FIFO for read path and write path respectively and is capable of handling 8-, 16-, 24- and 32-bit word sizes. PDMA controller handles the data movement between FIFO and memory.

6.19.2 Features

- Operated as either Master or Slave
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Supports Mono and stereo audio data
- Supports I²S and MSB justified data format
- Provides two 8-word FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Two PDMA requests, one for transmitting and the other for receiving

6.20 USB Device Controller (USB)

6.20.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through “buffer segmentation register (USB_BUFSEGx)”.

There are 6 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of ENDPOINT CONTROL is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the wake-up function, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disable function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables DRVSE0 bit (USB_DRVSE0), the USB controller will force the output of USB_DP and USB_DM to level low and its function is disabled. After disable the DRVSE0 bit, host will enumerate the USB device again.

Please refer to *Universal Serial Bus Specification Revision 1.1*

6.20.2 Features

This Universal Serial Bus (USB) performs a serial interface with a single connector type for attaching all USB peripherals to the host system. Following is the feature list of this USB.

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Provides 6 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provides remote wake-up capability

6.21 Analog-to-Digital Converter (ADC)

6.21.1 Overview

The NuMicro® NUC100 series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converter can be started by software, PWM Center-aligned trigger and external STADC pin.

6.21.2 Features

- Analog input voltage range: 0~V_{REF}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels
- Up to 760 kSPS conversion rate as ADC clock frequency is 16 MHz (chip working at 5V)
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by:
  - Writing 1 to ADST bit through software
  - PWM Center-aligned trigger
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 3 input sources: external analog voltage, internal Band-gap voltage, and internal temperature sensor output

6.22 Analog Comparator (ACMP)

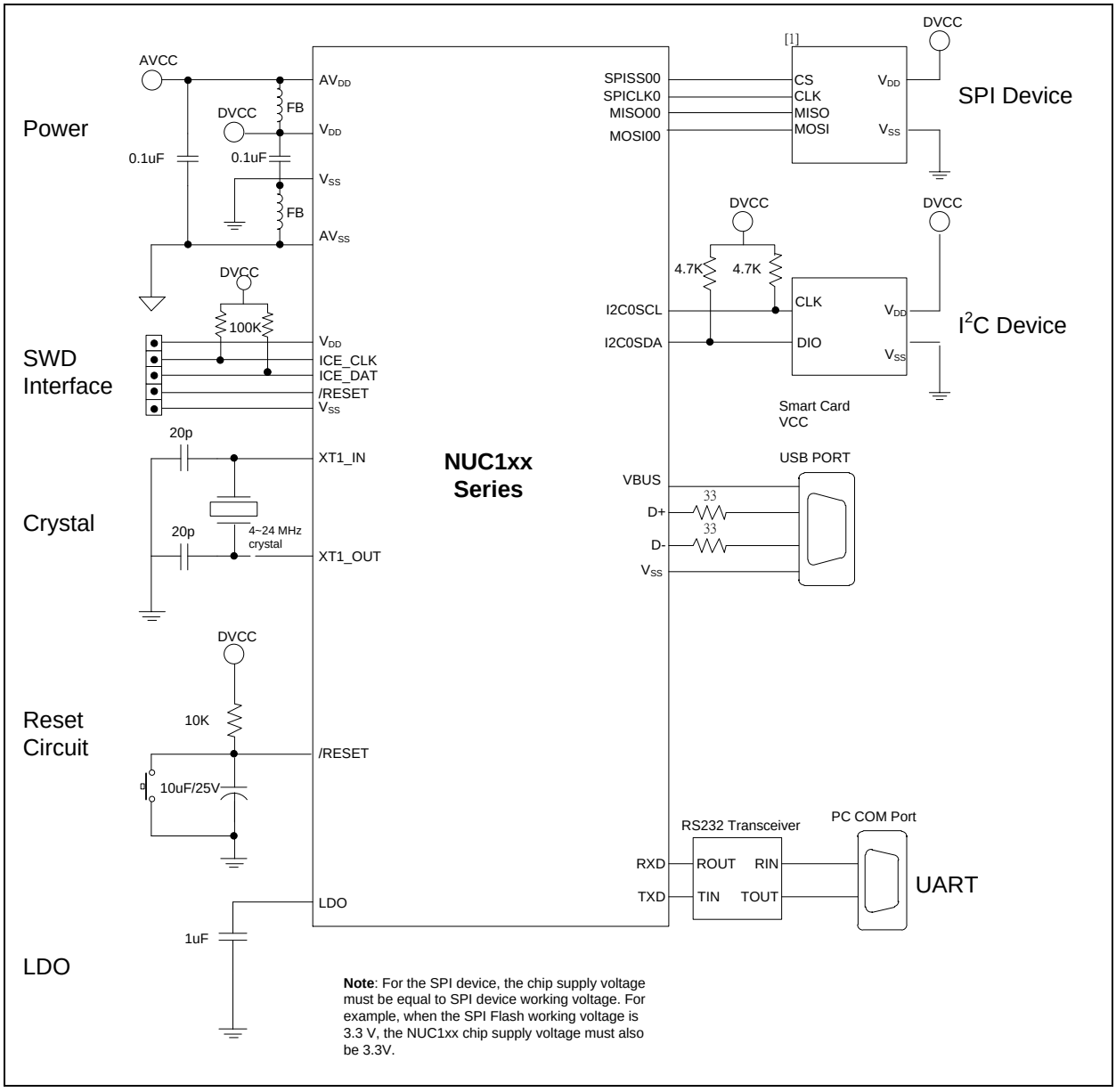
6.22.1 Overview

The NuMicro® NUC100 series contains two comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input voltage is greater than negative input voltage; otherwise the output is logic 0. Each comparator can be configured to cause an interrupt when the comparator output value changes.

6.22.2 Features

- Analog input voltage range: 0~ V_{DDA}
- Supports Hysteresis function
- Supports optional internal reference voltage input at negative end for each comparator

7 APPLICATION CIRCUIT



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

8.2 DC Electrical Characteristics

(V_{DD}-V_{SS}=5.5 V, T_A = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS			
		MIN.	TYP.	MAX.	UNIT				
Operation Voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5V ~ 5.5V up to 50 MHz			
Power Ground	V_{SS} AV_{SS}	-0.3			V				
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} > 2.5V			
Analog Operating Voltage	AV_{DD}		V_{DD}		V	When system used analog function, please refer to chapter 8.4 for corresponding analog operating voltage			
Operating Current Normal Run Mode at 50 MHz	I_{DD1}		34		mA	V_{DD}	XTAL	PLL	All IP
						5.5V	12 MHz	V	V
	I_{DD2}		15		mA	5.5V	12 MHz	V	X
	I_{DD3}		32		mA	3.3V	12 MHz	V	V
	I_{DD4}		14		mA	3.3V	12 MHz	V	X
Operating Current Normal Run Mode at 12 MHz	I_{DD5}		8.5		mA	V_{DD}	XTAL	PLL	All IP
						5.5V	12 MHz	X	V
	I_{DD6}		3.6		mA	5.5V	12 MHz	X	X
	I_{DD7}		7.5		mA	3.3V	12 MHz	X	V
	I_{DD8}		2.6		mA	3.3V	12 MHz	X	X
Operating Current Normal Run Mode at 4 MHz	I_{DD9}		3.6		mA	V_{DD}	XTAL	PLL	All IP
						5.5V	4 MHz	X	V
	I_{DD10}		2		mA	5.5V	4 MHz	X	X
	I_{DD11}		2.8		mA	3.3V	4 MHz	X	V
	I_{DD12}		1.2		mA	3.3V	4 MHz	X	X
Operating Current Normal Run Mode at 32.768 kHz	I_{DD13}		141		µA	V_{DD}	XTAL	PLL	All IP
						5.5V	32.768 kHz	X	V
	I_{DD14}		129		µA	5.5V	32.768 kHz	X	X
	I_{DD15}		138		µA	3.3V	32.768 kHz	X	V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS			
		MIN.	TYP.	MAX.	UNIT				
	I_{DD16}		125		μA	3.3V	32.768 kHz	X	X
Operating Current Normal Run Mode at 10 kHz	I_{DD17}		125		μA	V_{DD}	LIRC	PLL	All IP
						5.5V	10 kHz	X	V
	I_{DD18}		120		μA	5.5V	10 kHz	X	X
	I_{DD19}		125		μA	3.3V	10 kHz	X	V
	I_{DD20}		120		μA	3.3V	10 kHz	X	X
Operating Current Idle Mode at 50 MHz	I_{IDLE1}		28		mA	V_{DD}	XTAL	PLL	All IP
						5.5V	12 MHz	V	V
	I_{IDLE2}		10		mA	5.5V	12 MHz	V	X
	I_{IDLE3}		27		mA	3.3V	12 MHz	V	V
	I_{IDLE4}		9		mA	3.3V	12 MHz	V	X
Operating Current Idle Mode at 12 MHz	I_{IDLE5}		7.5		mA	V_{DD}	XTAL	PLL	All IP
						5.5V	12 MHz	X	V
	I_{IDLE6}		2.4		mA	5.5V	12 MHz	X	X
	I_{IDLE7}		6.5		mA	3.3V	12 MHz	X	V
	I_{IDLE8}		1.5		mA	3.3V	12 MHz	X	X
Operating Current Idle Mode at 4 MHz	I_{IDLE9}		3.3		mA	V_{DD}	XTAL	PLL	All IP
						5.5V	4 MHz	X	V
	I_{IDLE10}		1.7		mA	5.5V	4 MHz	X	X
	I_{IDLE11}		2.4		mA	3.3V	4 MHz	X	V
	I_{IDLE12}		0.8		mA	3.3V	4 MHz	X	X
Operating Current Idle Mode at 32.768 kHz	I_{IDLE13}		133		μA	V_{DD}	XTAL	PLL	All IP
						5.5V	32.768 kHz	X	V
	I_{IDLE14}		120		μA	5.5V	32.768 kHz	X	X
	I_{IDLE15}		133		μA	3.3V	32.768 kHz	X	V
	I_{IDLE16}		120		μA	3.3V	32.768 kHz	X	X
Operating Current	I_{IDLE13}		122		μA	V_{DD}	LIRC	PLL	All IP

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS			
		MIN.	TYP.	MAX.	UNIT				
Idle Mode at 10 kHz						5.5V	10 kHz	X	V
	I_{IDLE14}		118		μA	5.5V	10 kHz	X	X
	I_{IDLE15}		122		μA	3.3V	10 kHz	X	V
	I_{IDLE16}		118		μA	3.3V	10 kHz	X	X
Standby Current Power-down Mode (Deep Sleep Mode)	I_{PWD1}		15		μA	V_{DD}	RTC	BOD function	
						5.5V	X	X	
	I_{PWD2}		15		μA	5.5V	X	X	
	I_{PWD3}		17		μA	3.3V	X	X	
	I_{PWD4}		17		μA	3.3V	X	X	
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}		-50	-60	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}			
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V			
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}			
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN}<2.0V			
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V			
		-0.3	-	0.6		V_{DD} = 2.5V			
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V			
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V			
Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IL2}	-0.3	-	0.3V_{DD}	V				
Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IH2}	0.7V_{DD}	-	V_{DD} +0.2	V				
Hysteresis voltage of PA, PB, PC, PD,PE, PF (Schmitt input)	V_{HY}		0.2V_{DD}		V				
Input Low Voltage XT1_IN[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V			
		0	-	0.4		V_{DD} = 3.0V			
Input High Voltage XT1_IN[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V			
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V			

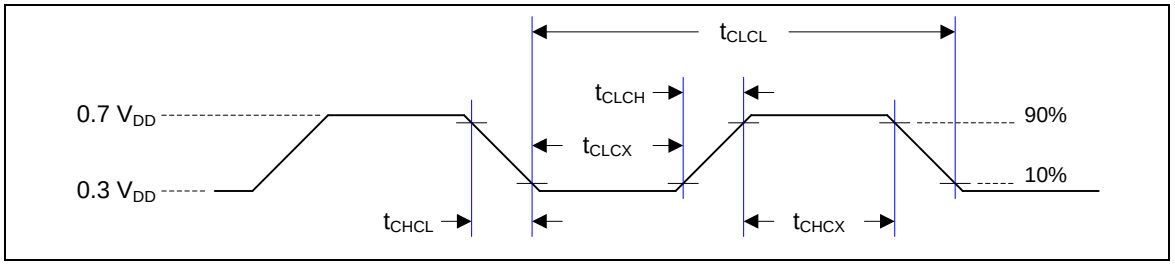
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	v	
Input High Voltage X32I[*2]	V_{IH4}	1.2		1.8	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	$0.2V_{DD}$ -0.2	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	$0.7V_{DD}$	-	V_{DD} +0.5	V	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	µA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	µA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	µA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-24	-28	-32	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brown-out Voltage with BOD_VL [1:0] = 00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-out Voltage with BOD_VL [1:0] = 01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-out voltage with BOD_VL [1:0] = 10b	$V_{BO3.7}$	3.5	3.7	3.9	V	
Brown-out Voltage with BOD_VL [1:0] = 11b	$V_{BO4.4}$	4.2	4.4	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V~5.5V
Band-gap voltage	V_{BG}	1.175	1.20	1.225	V	V_{DD} = 2.5V - 5.5V

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD, PE and PF can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD} = 5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

8.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Temperature	-	-40	-	85	℃
Operating Current	12 MHz at V_{DD} = 5V	-	1	-	mA
Clock Frequency	External crystal	4		24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

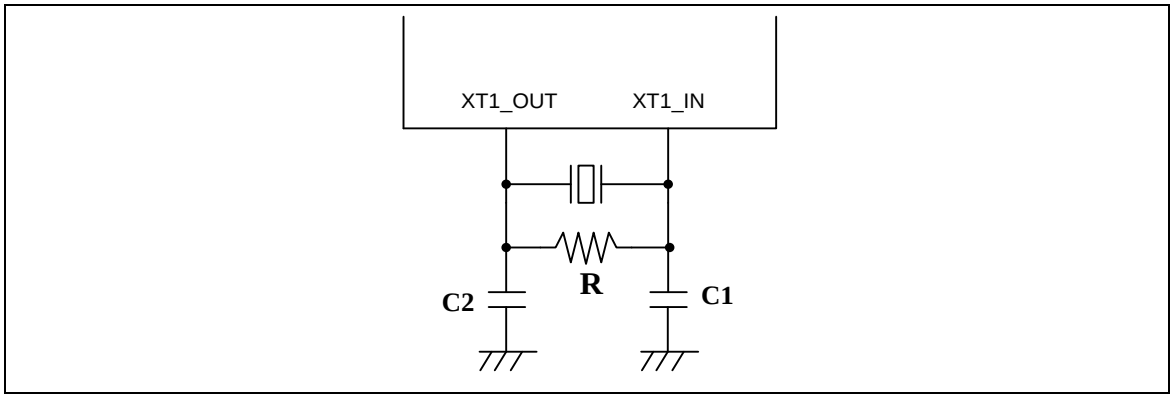


Figure 8-1 Typical Crystal Application Circuit

8.3.3 External 32.768 kHz Low Speed Crystal Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Operation Temperature	-	-40	-	85	℃
Operation Current	32.768KHz at V_{DD}=5V		1.5		μA
Clock Frequency	External crystal	-	32.768	-	kHz

8.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-1	-	+1	%
	-40℃~+85℃; V_{DD}=2.5 V~5.5 V	-3	-	+3	%
Operation Current	V_{DD} =5 V	-	500	-	uA

8.3.5 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-30	-	+30	%

	-40℃~+85℃; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

8.4 Analog Characteristics

8.4.1 12-bit SARADC Specification

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	12	Bit
DNL	Differential nonlinearity error	-	-1~2	-1~4	LSB
INL	Integral nonlinearity error	-	±2	±4	LSB
EO	Offset error	-	±1	10	LSB
EG	Gain error (Transfer gain)	-	1	1.005	-
-	Monotonic	Guaranteed			
F_{ADC}	ADC clock frequency (AV_{DD} = 5V/3V)	-	-	16/8	MHz
F_S	Sample rate	-	-	760	kSPS
V_{DDA}	Supply voltage	3	-	5.5	V
I_{DD}	Supply current (Avg.)	-	0.5	-	mA
I_{DDA}		-	1.5	-	mA
V_{REF}	Reference voltage	3		V_{DDA}	V
I_{REF}	Reference current (Avg.)	-	1	-	mA
V_{IN}	Input voltage	0	-	V_{REF}	V

8.4.2 LDO and Power Management Specification

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage V_{DD}	2.5		5.5	V	V_{DD} input voltage
Output Voltage	1.62	1.8	1.98	V	V_{DD} > 2.5 V
Operating Temperature	-40	25	85	℃	
C_{bp}	-	1	-	μF	R_{ESR} = 1 Ω

Note:

1. It is recommended that a 10 uF or higher capacitor and a 100 nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.

2. To ensure power stability, a 1 μF must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

8.4.3 Low Voltage Reset Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Quiescent Current	V_{DD}=5.5 V	-	1	5	μA
Operation Temperature	-	-40	25	85	℃
Threshold Voltage	Temperature=-40~85℃	1.7	2.0	2.3	V
Hysteresis	-	0	0	0	V

8.4.4 Brown-out Detector Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Temperature	-	-40	25	85	℃
Quiescent Current	AV_{DD}=5.5 V	-	-	125	μA
Brown-out Voltage	BOD_VL[1:0]=11	4.2	4.4	4.6	V
	BOD_VL [1:0]=10	3.5	3.7	3.9	V
	BOD_VL [1:0]=01	2.6	2.7	2.8	V
	BOD_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

8.4.5 Power-on Reset Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Temperature	-	-40	25	85	℃
Reset Voltage	V+	-	2	-	V
Quiescent Current	Vin > reset voltage	-	1	-	nA

8.4.6 Temperature Sensor Specification

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operation Voltage[1]		2.5	-	5.5	V
Operation Temperature		-40	-	85	℃
Current Consumption		6.4	-	10.5	μA
Gain			-1.76		mV/℃
Offset Voltage	Temp=0 ℃		720		mV

Note: Internal operation voltage comes from internal LDO.

8.4.7 Comparator Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage AV_{DD}	-	2.5		5.5	V
Operation Temperature	-	-40	25	85	℃
Operation Current	V_{DD}=3.0 V	-	20	40	μA
Input Offset Voltage	-	-	5	15	mV
Output Swing	-	0.1	-	V_{DD}-0.1	V
Input Common Mode Range	-	0.1	-	V_{DD}-0.1	V
DC Gain	-	-	70	-	dB
Propagation Delay	VCM=1.2 V and VDIFF=0.1 V	-	200	-	ns
Comparison Voltage	20 mV at VCM=1 V 50 mV at VCM=0.1 V 50 mV at VCM=V_{DD}-1.2 10 mV for non-hysteresis	10	20	-	mV
Hysteresis	VCM=0.4 V ~ V_{DD}-1.2 V	-	±10	-	mV
Stable Time	CINP=1.3 V CINN=1.2 V	-	-	2	μs

8.4.8 USB PHY Specification

8.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High (driven)		2.0			V
V_{IL}	Input Low				0.8	V
V_{DI}	Differential Input Sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential Common-mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
V_{OL}	Output Low (driven)		0		0.3	V
V_{OH}	Output High (driven)		2.8		3.6	V
V_{CRS}	Output Signal Cross Voltage		1.3		2.0	V
R_{PU}	Pull-up Resistor		1.425		1.575	kΩ
V_{TRM}	Termination Voltage for Upstream Port Pull-up (RPU)		3.0		3.6	V
Z_{DRV}	Driver Output Resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver Capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

8.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and Fall Time Matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

8.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VBUS}	VBUS Current (Steady State)	Standby		50		μA

8.4.8.4 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V_{DD33}	LDO Output Voltage		3.0	3.3	3.6	V
C_{bp}	External Bypass Capacitor			1.0	-	uF

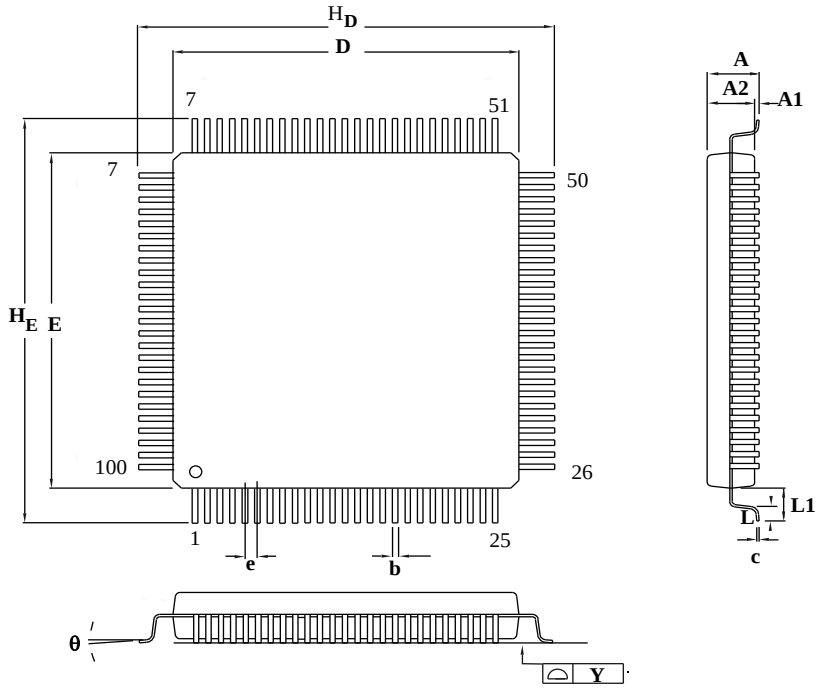
8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		1.62	1.8	1.98	V[1]
T_{RET}	Data Retention	At 85℃	10			year
T_{ERASE}	Page Erase Time			2		ms
T_{MER}	Mass Erase Time			10		ms
T_{PROG}	Program Time			20		μs
I_{DD1}	Read Current		-	0.15	0.5	mA/MHz
I_{DD2}	Program/Erase Current				7	mA
I_{PD}	Power Down Current		-	1	20	μA

1. V_{DD} is source from chip LDO output voltage.
2. This table is guaranteed by design, not test in production.

9 PACKAGE DIMENSIONS

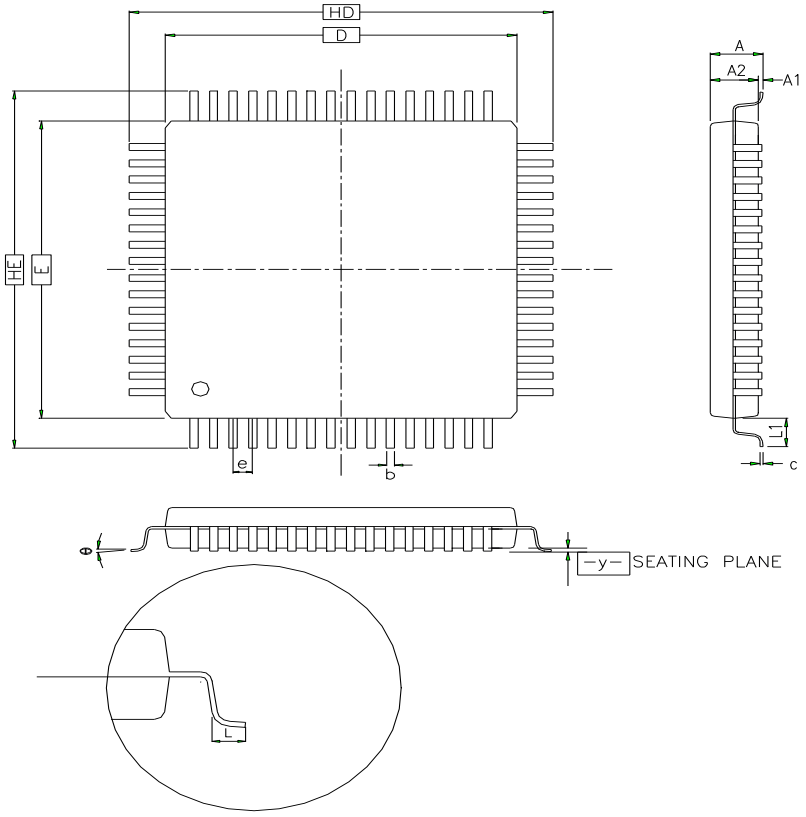
9.1 100-pin LQFP (14x14x1.4 mm footprint 2.0 mm)



Controlling Dimension : Millimeters

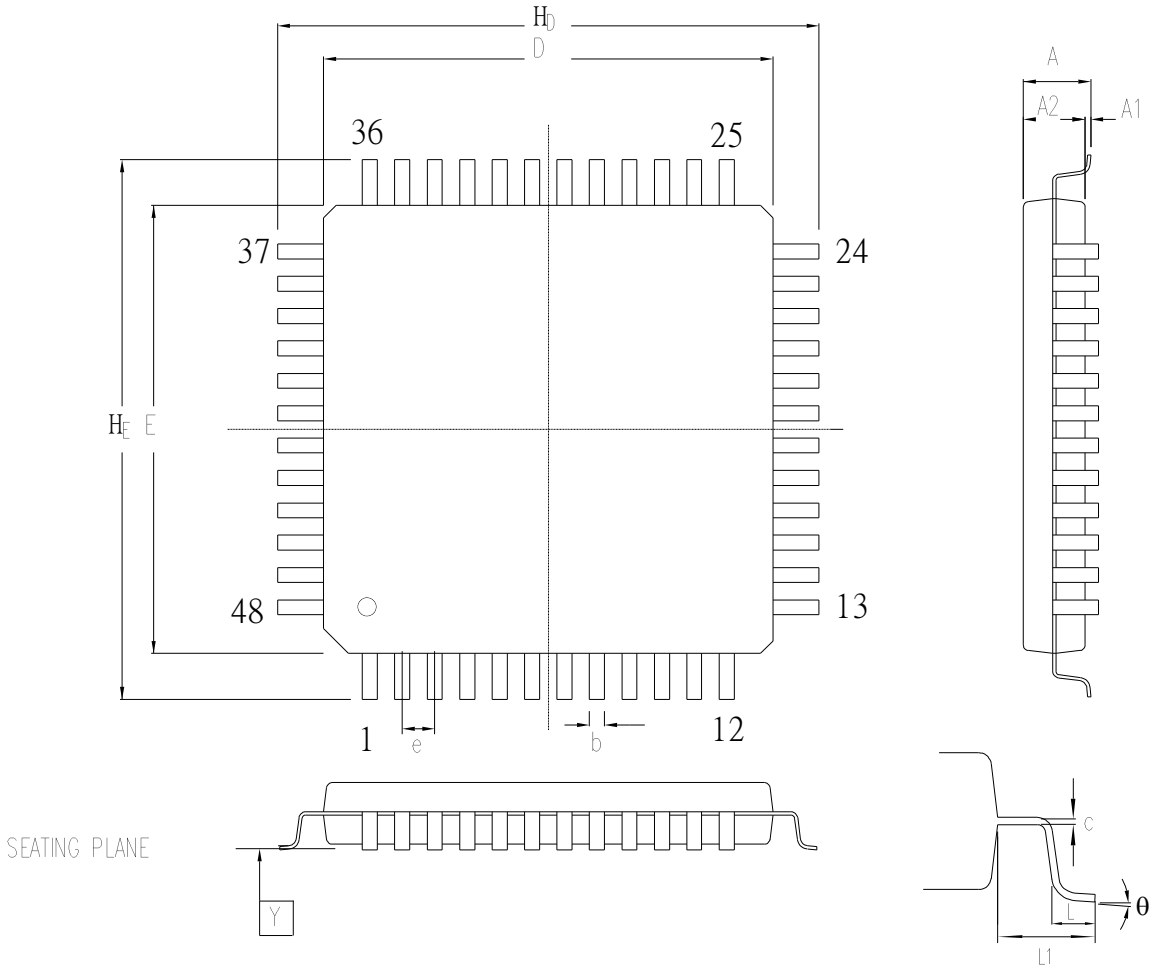
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

9.2 64-pin LQFP (10x10x1.4 mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0	3.5	7	0	3.5	7

9.3 48-pin LQFP (7x7x1.4 mm footprint 2.0 mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

10 REVISION HISTORY

Date	Revision	Description
2014.05.13	1.00	1. Preliminary version.
2015.08.31	1.01	1. Reorganized the chapter sequence. 2. Added a note in all clock source block diagrams of all peripheral sections that “Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.” 3. Revised package size of 64-pin LQFP (10x10x1.4 mm footprint 2.0 mm) in section 9.2.
2017.03.02	1.02	1. Updated section 4.1 NuMicro® NUC100/120xxxDN Selection Guide. 2. Updated Low Voltage Reset Specification in section 8.4.3. 3. Updated Comparator Specification in section 8.4.7.
2019.03.21	1.03	1. Updated external capacitor value for LDO Specification note in section 8.4.7
2020.04.08	1.04	1. Added notes about the hardware reference design for ICE_DAT, ICE_CLK and nRESET pins in section 4.3 and chapter 7.

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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