

INA143 INA2143

For most current data sheet and other product information, visit www.burr-brown.com

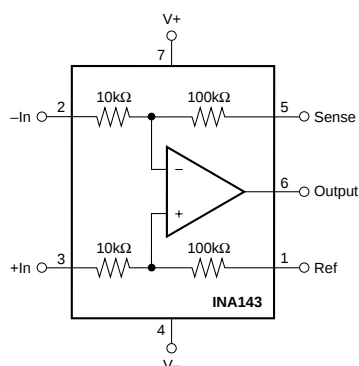
High-Speed, Precision, $G = 10$ or $G = 0.1$ DIFFERENCE AMPLIFIERS

FEATURES

- DESIGNED FOR LOW COST
- $G = 10V/V$ or $G = 0.1V/V$
- SINGLE, DUAL VERSIONS
- LOW OFFSET VOLTAGE:
 $\pm 250\mu V$ max, $\pm 3\mu V/^\circ C$ max
- LOW GAIN ERROR: 0.01%
- HIGH SLEW RATE: $5V/\mu s$
- FAST SETTLING TIME: $9\mu s$ to 0.01%
- LOW QUIESCENT CURRENT: $950\mu A$
- WIDE SUPPLY RANGE: $\pm 2.25V$ to $\pm 18V$
- SO-8 and SO-14 PACKAGES

DESCRIPTION

The INA143 and INA2143 are high slew rate, gain of $10V/V$ or $0.1V/V$ difference amplifiers consisting of a precision op amp with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistor maintains gain accuracy and common-mode rejection over temperature. They operate over a wide supply range, $\pm 2.25V$ to $\pm 18V$ ($+4.5V$ to $+36V$ single supply), and input common-mode voltage range extends beyond the positive and negative supply rails.

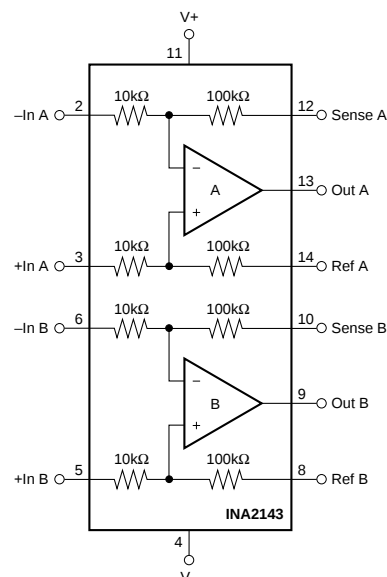


APPLICATIONS

- DIFFERENTIAL INPUT AMPLIFIER BUILDING BLOCK
- DIFF IN/DIFF OUT AMPLIFIER
- GAIN = -10 INVERTING AMPLIFIER
- GAIN = $+10$ NON-INVERTING AMPLIFIER
- GAIN = $+11$ NON-INVERTING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT/DIFFERENTIAL LINE RECEIVER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- BATTERY POWERED SYSTEMS
- LOW COST AUTOMOTIVE

The differential amplifier is the foundation of many commonly used circuits. The low cost INA143 and INA2143 provide this precision circuit function without using an expensive precision network.

The single version, INA143, package is the SO-8 surface mount. The dual version, INA2143, package is the SO-14 surface mount. Both are specified for operation over the extended industrial temperature range, $-40^\circ C$ to $+85^\circ C$. Operation is from $-55^\circ C$ to $+125^\circ C$.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS: $V_S = \pm 15V$

At $T_A = +25^\circ C$, $V_S = \pm 15V$, $G = 10$, $R_L = 10k\Omega$ connected to ground, and reference pin connected to ground, unless otherwise noted.

PARAMETER	CONDITIONS	INA143U INA2143U			INA143UA INA2143UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE⁽¹⁾ Initial ⁽¹⁾ vs Temperature vs Power Supply vs Time Channel Separation (dual)	RTI $V_{CM} = 0V$ $V_S = \pm 2.25V$ to $\pm 18V$ dc		± 100 ± 1 ± 5 0.2 140	± 250 ± 3 ± 20		* See Typical Curve * *	± 500 ± 30	μV $\mu V/^\circ C$ $\mu V/V$ $\mu V/\sqrt{mo}$ dB
INPUT IMPEDANCE⁽³⁾ Differential Common-Mode			20 55			* *		k Ω k Ω
INPUT VOLTAGE RANGE Common-Mode Voltage Range Positive Negative Common-Mode Rejection Ratio	RTI $V_O = 0V$ $V_O = 0V$ $V_{CM} = -14.85V$ to $14.85V$, $R_S = 0\Omega$	1.1[(V+)-1.5] 1.1[(V-)+1.5] 86	1.1[(V+)-1] 1.1[(V-)+1] 96		* * 80	* * *		V V dB
OUTPUT VOLTAGE NOISE⁽³⁾ f = 0.1Hz to 10Hz f = 10Hz f = 100Hz f = 1kHz	RTI		1 45 30 27			* * * *		$\mu Vp-p$ nV/ $\sqrt{Hz}$ nV/ $\sqrt{Hz}$ nV/ $\sqrt{Hz}$
GAIN Initial Error vs Temperature Nonlinearity	$V_O = -14V$ to $+13.5V$ $V_O = -14V$ to $+13.5V$		10 ± 0.01 ± 1 ± 0.0001	± 0.05 ± 10 ± 0.001		* * * *	± 0.1 * ± 0.002	V/V % ppm/ $^\circ C$ % of FS
OUTPUT Voltage Output Positive Negative Positive Negative Current Limit Capacitive Load (stable operation)	Gain Error < 0.1% $R_L = 10k\Omega$ to Ground $R_L = 10k\Omega$ to Ground $R_L = 100k\Omega$ to Ground $R_L = 100k\Omega$ to Ground Continuous-to-Common	(V+) -1.5 (V-) +1	(V+) -1.3 (V-) +0.8 (V+) -0.8 (V-) +0.3 -25, +32 1000		* *	* * * * * *		V V V V mA pF
FREQUENCY RESPONSE Small-Signal Bandwidth Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time	-3dB $V_O = 10V$ Step, $C_L = 100pF$ $V_O = 10V$ Step, $C_L = 100pF$ 50% Overdrive		0.15 5 6 9 6			* * * * *		MHz V/ μs μs μs μs
POWER SUPPLY Rated Voltage Operating Voltage Range Dual Supplies Single Supply Quiescent Current (per amplifier)	$I_O = 0$	± 2.25 +4.5	± 15 ± 0.95	± 18 +36 ± 1.2	* *	* *	* *	V V V mA
TEMPERATURE RANGE Specification Operation Storage Thermal Resistance SO-8 Surface Mount SO-14 Surface Mount	θ_{JA}	-40 -55 -55		+85 +125 +125	* * *		* * *	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$

* Specifications the same as INA143U, INA2143U.

NOTES: (1) Includes the effects of amplifier's input bias and offset currents. (2) Internal resistors are ratio matched but have $\pm 20\%$ absolute value. (3) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATIONS: $V_S = \pm 5V$

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5V$, $G = 10$, $R_L = 10\text{k}\Omega$ connected to ground, and reference pin connected to ground, unless otherwise noted.

PARAMETER	CONDITIONS	INA143U INA2143U			INA143UA INA2143UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE⁽¹⁾ Initial ⁽¹⁾ vs Temperature	RTI $V_{CM} = 0V$		± 200 ± 1	± 500		*	± 750	μV $\mu V/^\circ\text{C}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Positive Negative Common-Mode Rejection Ratio	RTI $V_O = 0V$ $V_O = 0V$ $V_{CM} = -3.85V$ to $+3.85V$, $R_S = 0\Omega$	$1.1[(V+) - 1.5]$ $1.1[(V-) + 1.5]$ 86	$1.1[(V+) - 1]$ $1.1[(V-) + 1]$ 96		*	*		V V dB
GAIN Initial Gain Error Nonlinearity	$V_O = -4V$ to $+3.5V$ $V_O = -4V$ to $+3.5V$		10 ± 0.01 ± 0.0001	± 0.05 ± 0.001		*	± 0.1 ± 0.002	V/V % % of FS
OUTPUT Voltage Output Positive Negative Positive Negative	Gain Error < 0.1% $R_L = 10\text{k}\Omega$ to Ground $R_L = 10\text{k}\Omega$ to Ground $R_L = 100\text{k}\Omega$ to Ground $R_L = 100\text{k}\Omega$ to Ground	(V+) -1.5 (V-) +1	(V+) -1.3 (V-) +0.8 (V+) -0.8 (V-) +0.3		*	*		V V V V
POWER SUPPLY Rated Voltage Operating Voltage Range Dual Supplies Single Supply Quiescent Current (per amplifier)	$I_O = 0$		+5			*		V
		± 2.25 +4.5		± 18 +36	*	*	*	V V mA
			± 0.92	± 1.2		*	*	

* Specifications the same as INA143U, INA2143U.

NOTES: (1) Includes the effects of amplifier's input bias and offset currents.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, $V+$ to $V-$	36V
Input Signal ($G = 10$), Voltage	$1.1 \cdot V_S$
Current	0.5mA
Input Signal ($G = 0.1$), Voltage	$11 \cdot V_S$
Current	0.5mA
Output Short-Circuit (to ground) ⁽²⁾	Continuous
Operating Temperature	-55°C to $+125^\circ\text{C}$
Storage Temperature	-55°C to $+125^\circ\text{C}$
Junction Temperature	$+150^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) One channel per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

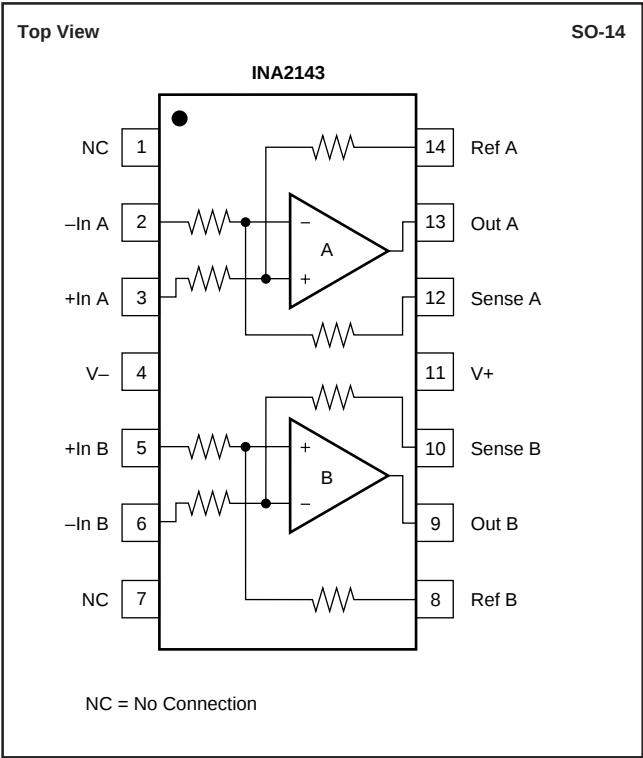
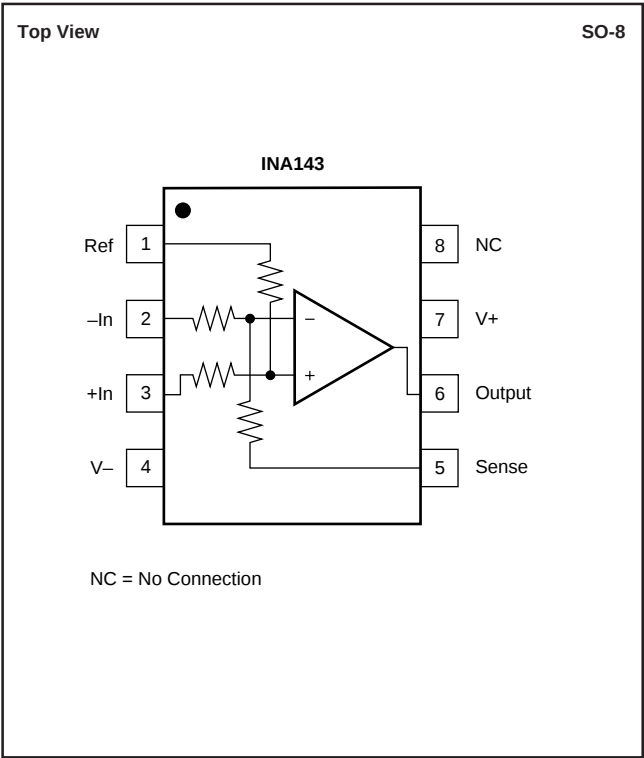
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽²⁾	TRANSPORT MEDIA
Single						
INA143U	SO-8 Surface Mount	182	-40°C to $+85^\circ\text{C}$	INA143U	INA143U	Rails
"	"	"	"	"	INA143U/2K5	Tape and Reel
INA143UA	SO-8 Surface Mount	182	-40°C to $+85^\circ\text{C}$	INA143UA	INA143UA	Rails
"	"	"	"	"	INA143UA/2K5	Tape and Reel
Dual						
INA2143U	SO-14 Surface Mount	235	-40°C to $+85^\circ\text{C}$	INA2143U	INA2143U	Rails
"	"	"	"	"	INA2143U/2K5	Tape and Reel
INA2143UA	SO-14 Surface Mount	235	-40°C to $+85^\circ\text{C}$	INA2143UA	INA2143UA	Rails
"	"	"	"	"	INA2143UA/2K5	Tape and Reel

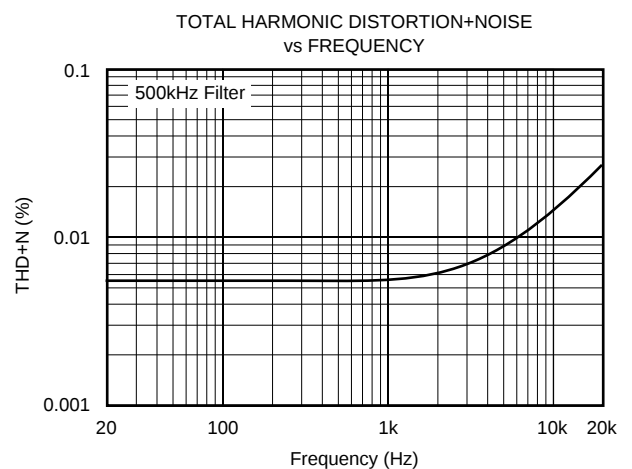
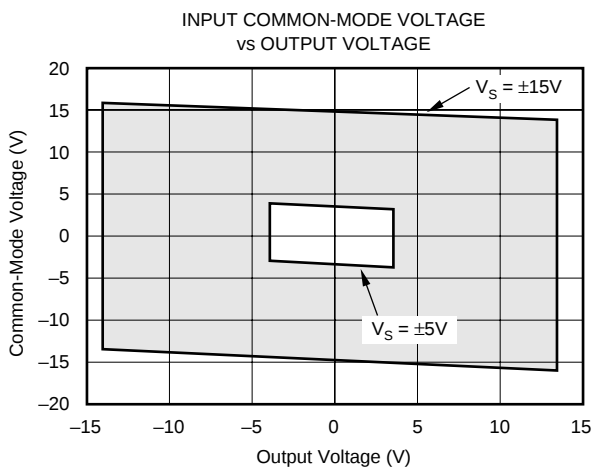
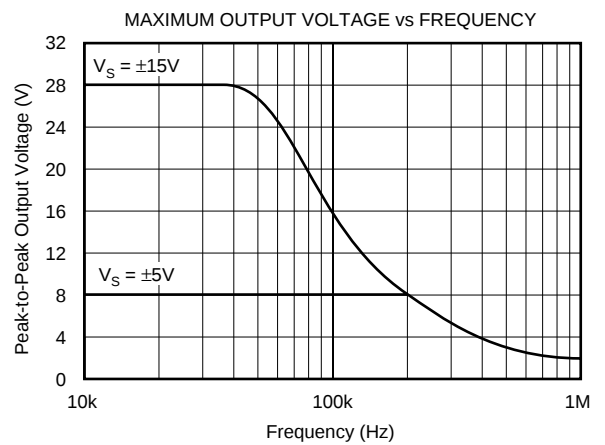
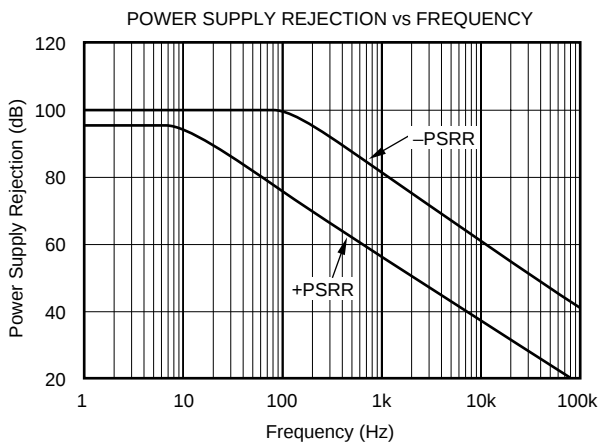
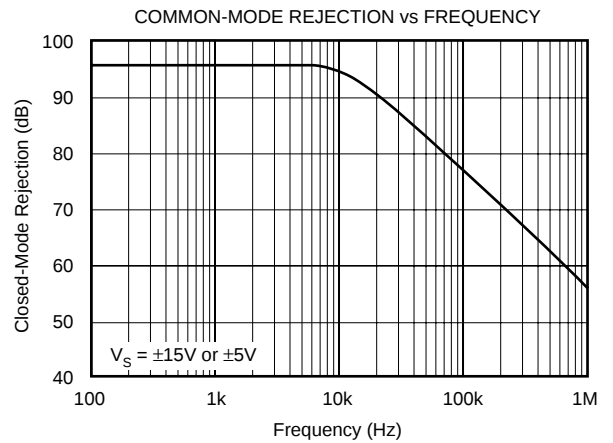
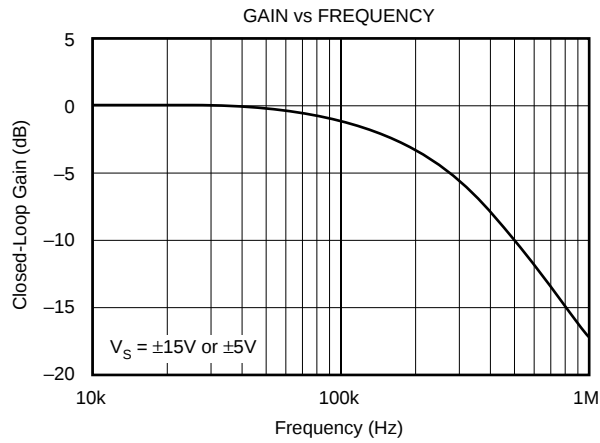
NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA143UA/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

PIN CONFIGURATIONS



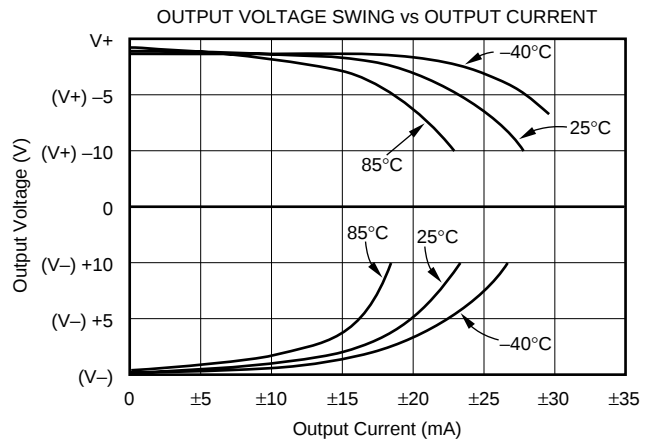
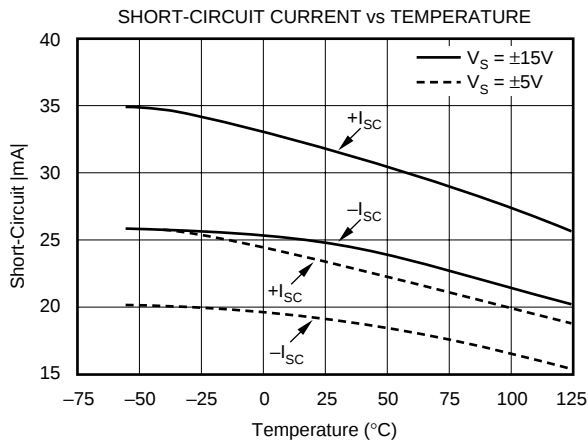
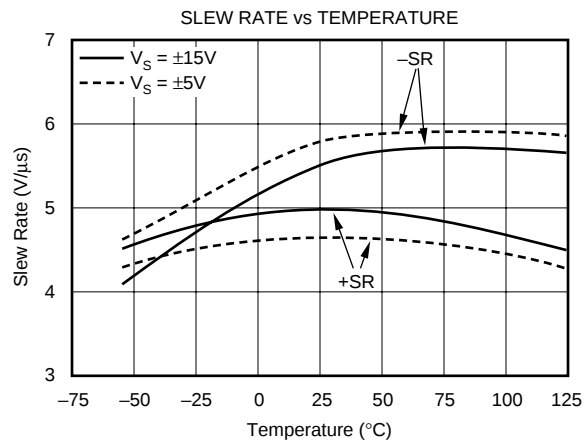
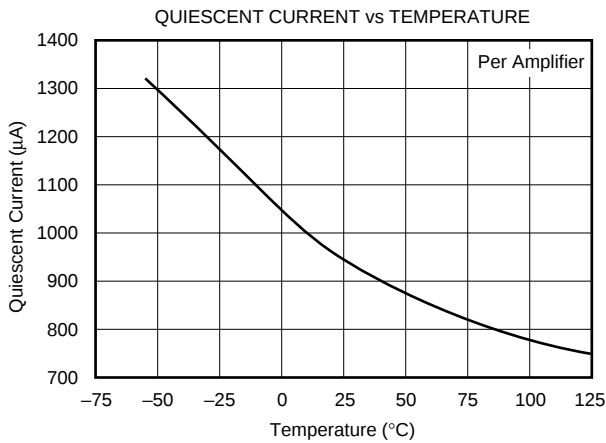
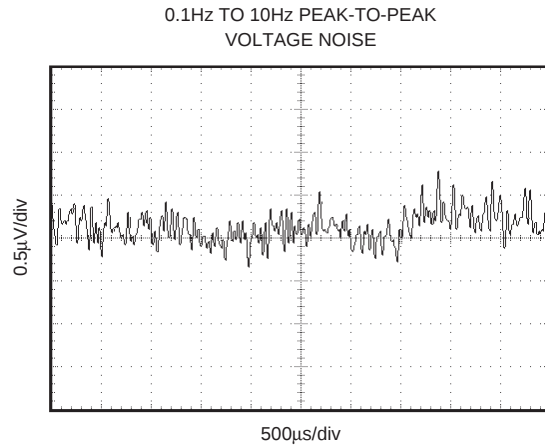
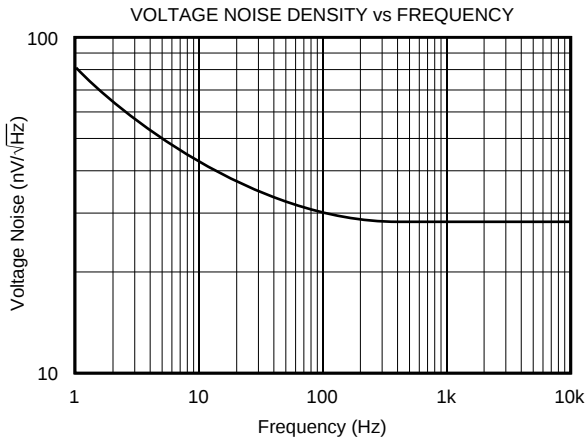
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 10$, $R_L = 10\text{k}\Omega$ connected to ground, and reference pin connected to ground, unless otherwise noted.



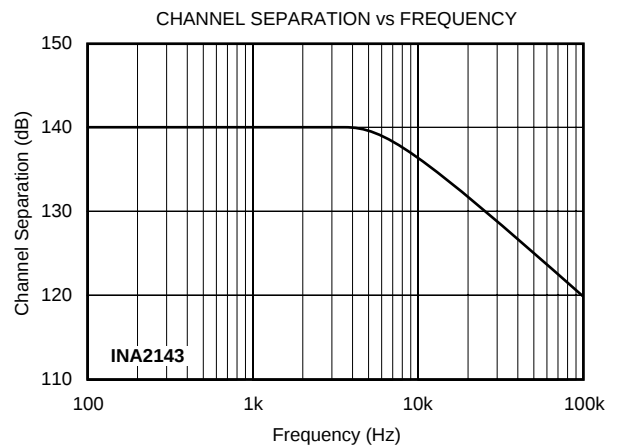
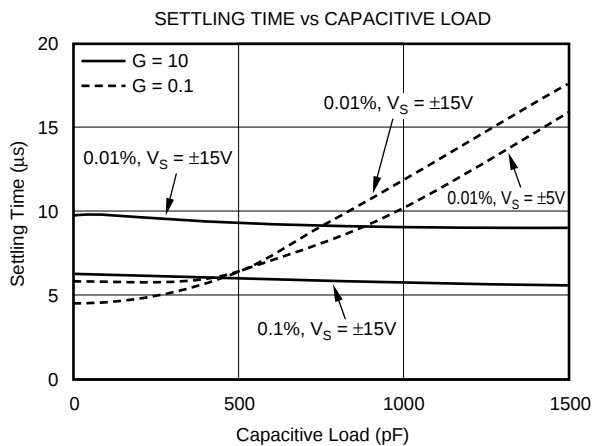
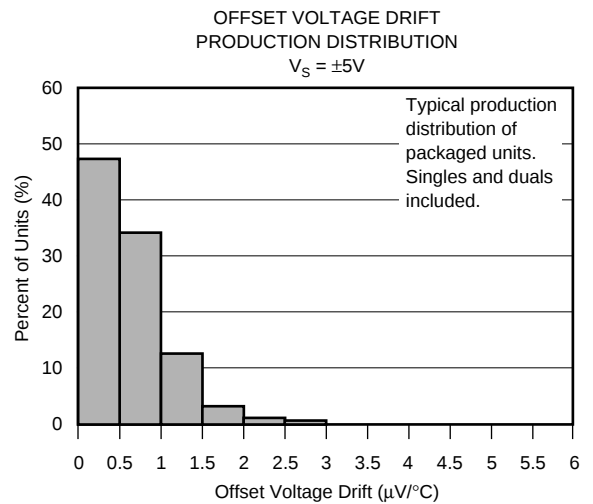
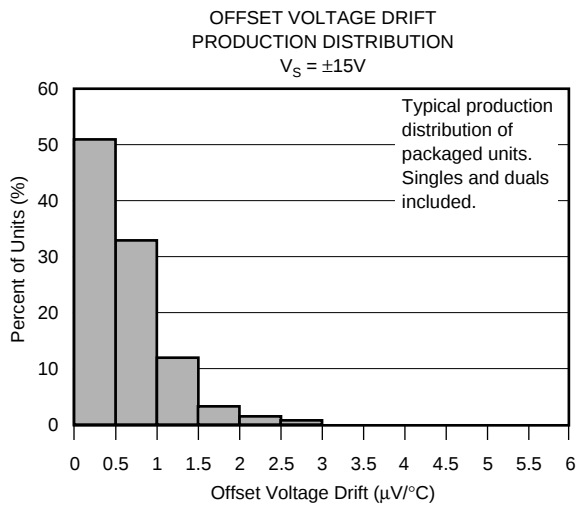
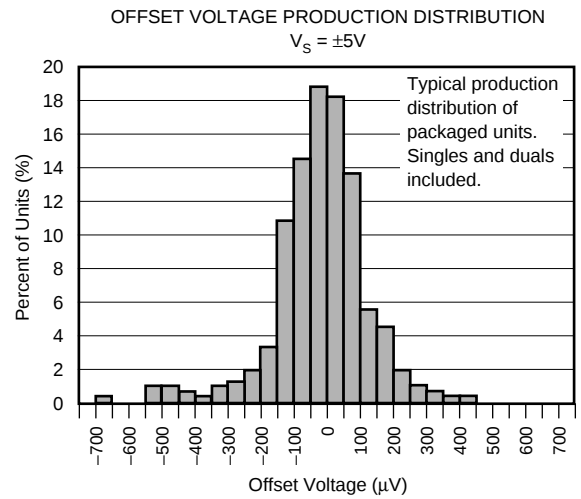
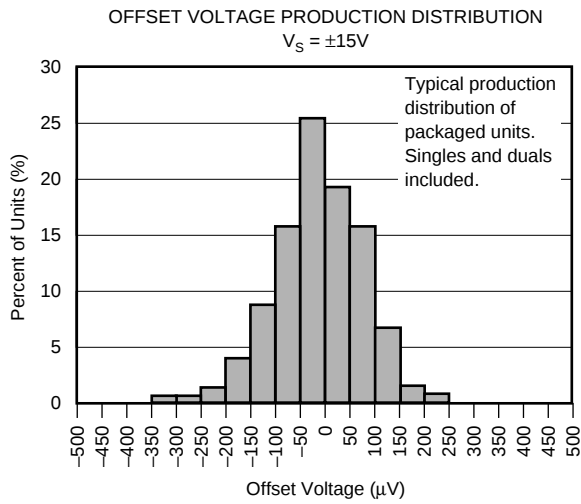
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 10$, $R_L = 10\text{k}\Omega$ connected to ground, and reference pin connected to ground, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

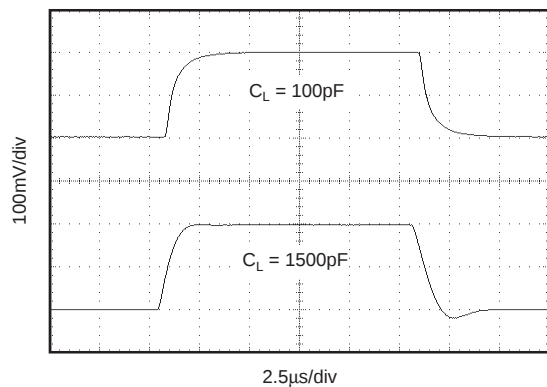
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 10$, $R_L = 10\text{k}\Omega$ connected to ground, and reference pin connected to ground, unless otherwise noted.



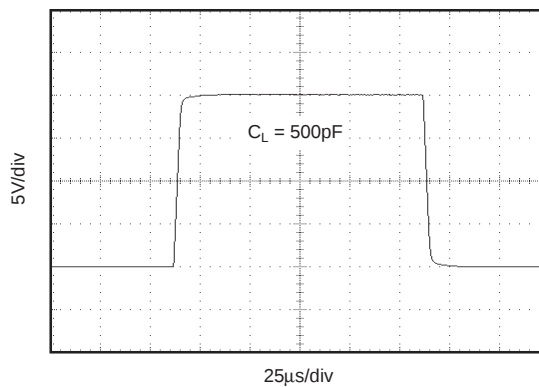
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 10$, $R_L = 10\text{k}\Omega$ connected to ground, and reference pin connected to ground, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE



LARGE-SIGNAL STEP RESPONSE



APPLICATIONS INFORMATION

The INA143 and INA2143 are high-speed difference amplifiers suitable for a wide range of general-purpose applications. Figure 1 shows the basic $G = 10$ configuration. The input and feedback resistors can be reversed to achieve $G = 0.1$, as shown in Figure 2. For applications requiring $G = 1$, the INA133 and INA2133 are recommended.

Decoupling capacitors are strongly recommended for applications with noisy or high impedance power supplies. The capacitors should be placed close to the device pins as shown in Figure 1. All circuitry is completely independent in the dual version assuring lowest crosstalk and normal behavior when one amplifier is overdriven or short-circuited.

As shown in Figure 1, the differential input signal is connected to pins 2 and 3. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. A 5Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 86dB (RTI). If the source has a known impedance mismatch, an additional resistor in series with the opposite input can be used to preserve good common-mode rejection.

The INA143's internal resistors are accurately ratio trimmed to match. That is, R_1/R_2 and R_3/R_4 are trimmed to equal 0.1. However, the absolute values may not be equal ($R_1 + R_2$ may be slightly different than $R_3 + R_4$). Thus, large series resistors on the input (greater than 100Ω), even if well matched, will degrade common-mode rejection.

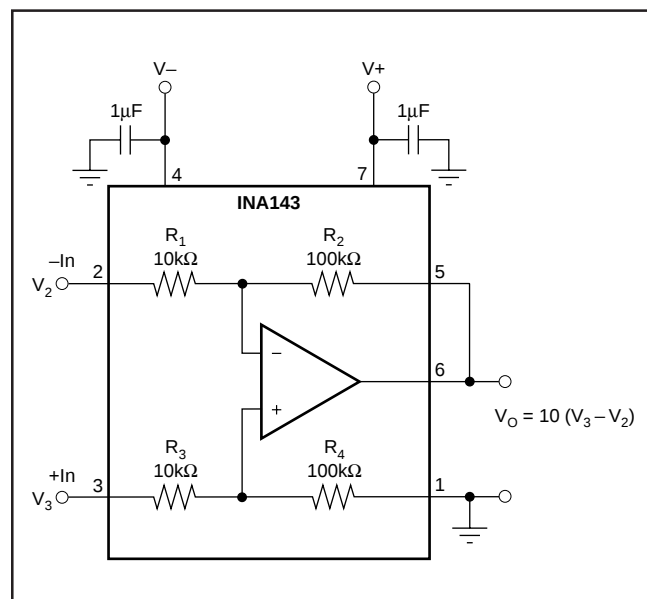


FIGURE 1. $G = 10$ Basic Power Supply and Signal Connections.

OPERATING VOLTAGE

The INA143 and INA2143 operate from single (+4.5V to +36V) or dual ($\pm 2.25V$ to $\pm 18V$) supplies with excellent performance. Specifications are production tested with $\pm 5V$ and $\pm 15V$ supplies. Most behavior remains unchanged

throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Performance Curves.

OFFSET VOLTAGE TRIM

The INA143 and INA2143 are laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 3 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 3. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

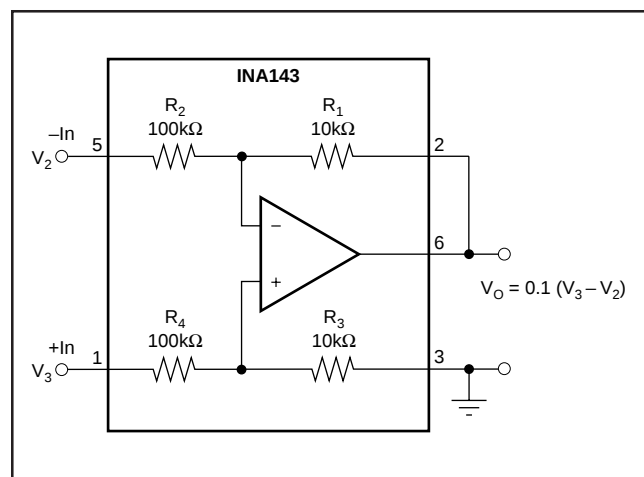


FIGURE 2. $G = 0.1$ Difference Amplifier.

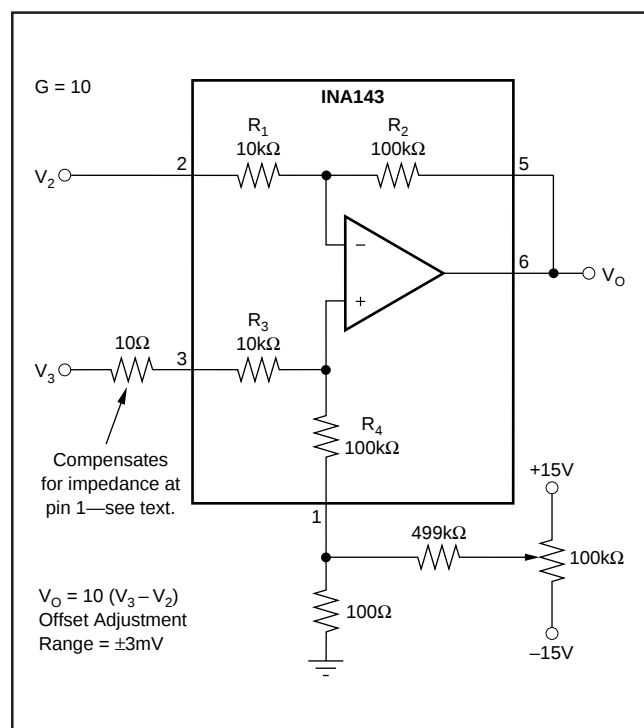


FIGURE 3. Offset Adjustment.

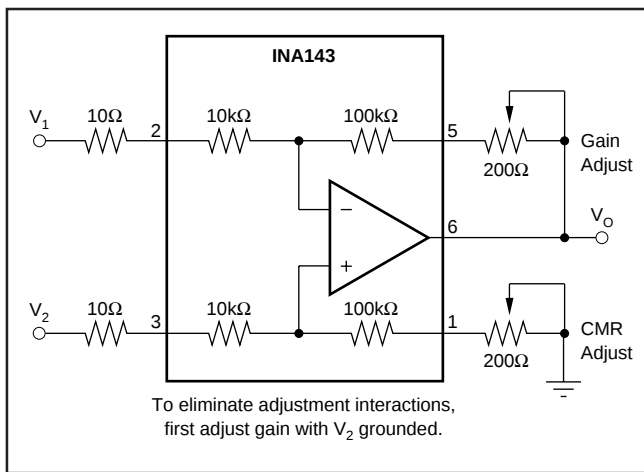


FIGURE 4. Difference Amplifier with Gain and CMR Adjust.

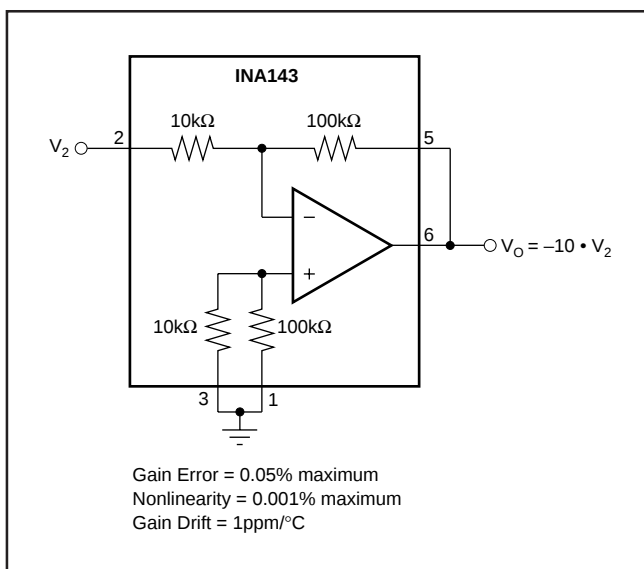


FIGURE 5. Precision $G = -10$ Inverting Amplifier.

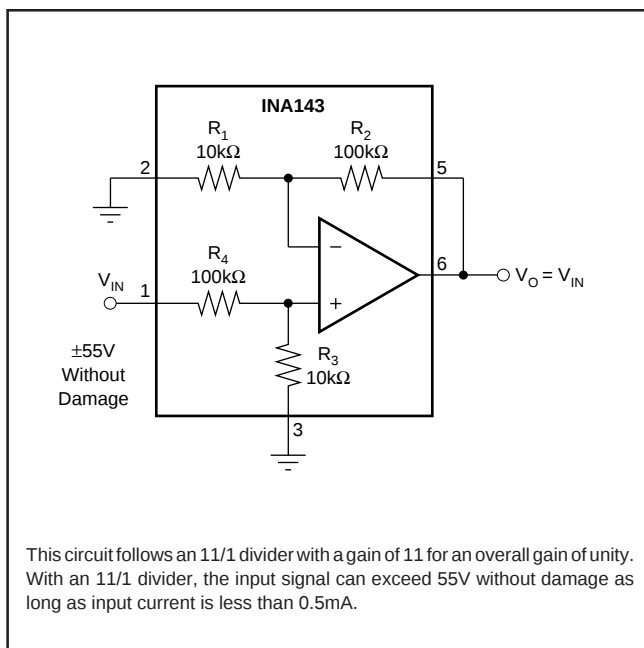
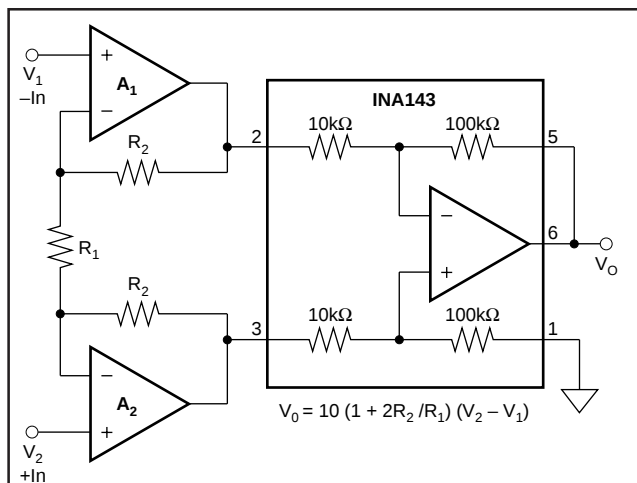


FIGURE 6. Voltage Follower with Input Protection.



The INA143 can be combined with op amps to form a complete instrumentation amplifier with specialized performance characteristics. Burr-Brown offers many complete high performance IAs. Products with related performances are shown at the right in the table below.

A_1, A_2	FEATURE	SIMILAR COMPLETE BURR-BROWN IA
OPA2227	Low Noise	INA103
OPA129	Ultra Low Bias Current (fA)	INA116
OPA2277	Low Offset Drift, Low Noise	INA114, INA128
OPA2130	Low Power, FET-Input (pA)	INA121
OPA2234	Single Supply, Precision, Low Power	INA122, INA118
OPA2237	Single Supply, Low Power, MSOP-8	INA122, INA126

FIGURE 7. Precision Instrumentation Amplifier.

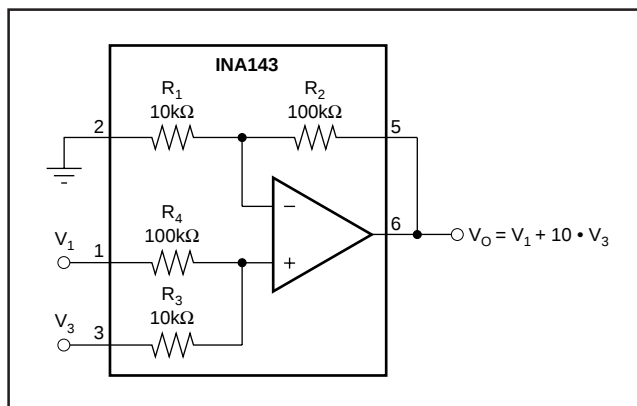


FIGURE 8. Precision Summing Amplifier.

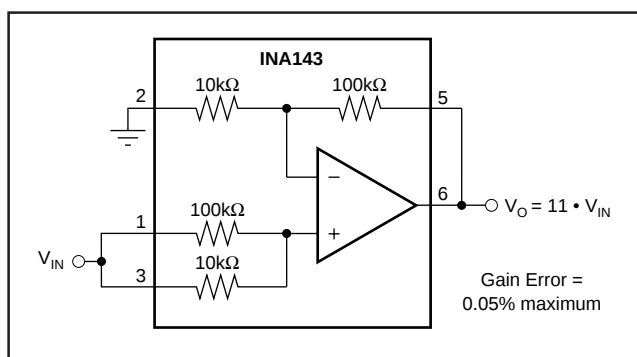


FIGURE 9. Precision $G = 11$ Buffer.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA143U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA 143U	Samples
INA143U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 143U	Samples
INA143UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 143U A	Samples
INA143UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		INA 143U A	Samples
INA2143U	ACTIVE	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-55 to 125	INA2143U A	Samples
INA2143UA	ACTIVE	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-55 to 125	INA2143U A	Samples
INA2143UAE4	ACTIVE	SOIC	D	14	50	RoHS & Green	Call TI	Level-3-260C-168 HR	-55 to 125	INA2143U A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

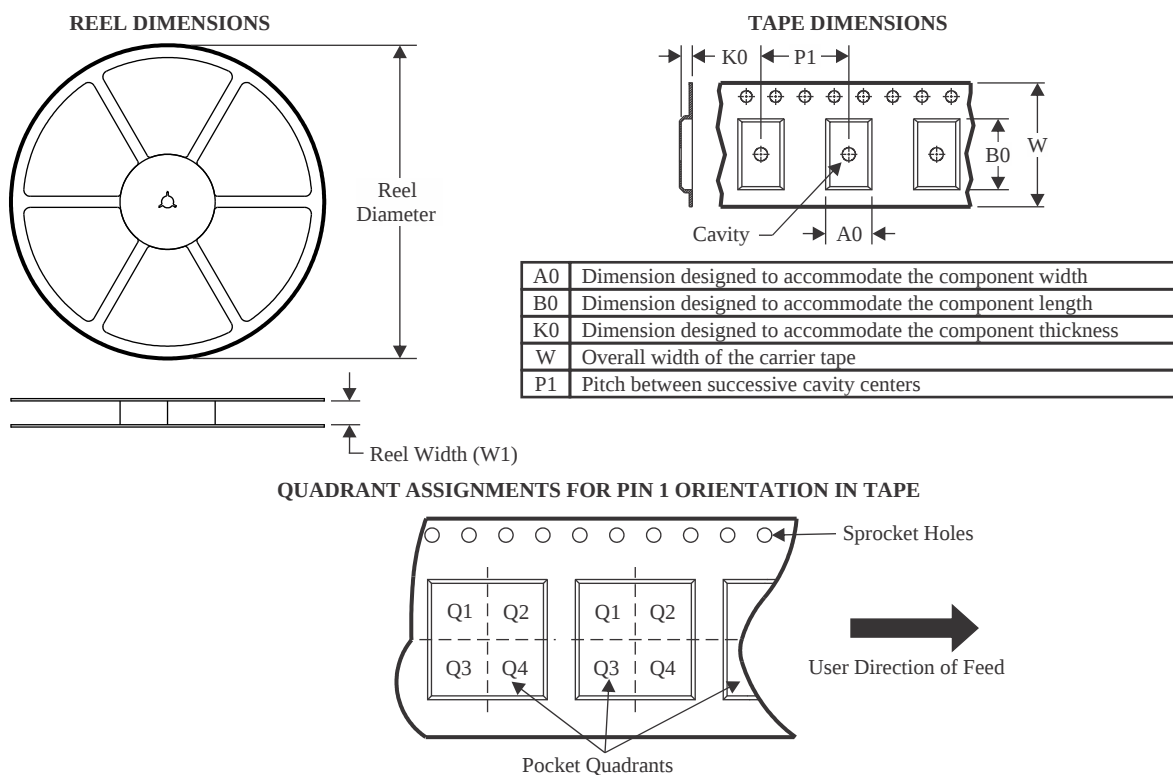
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

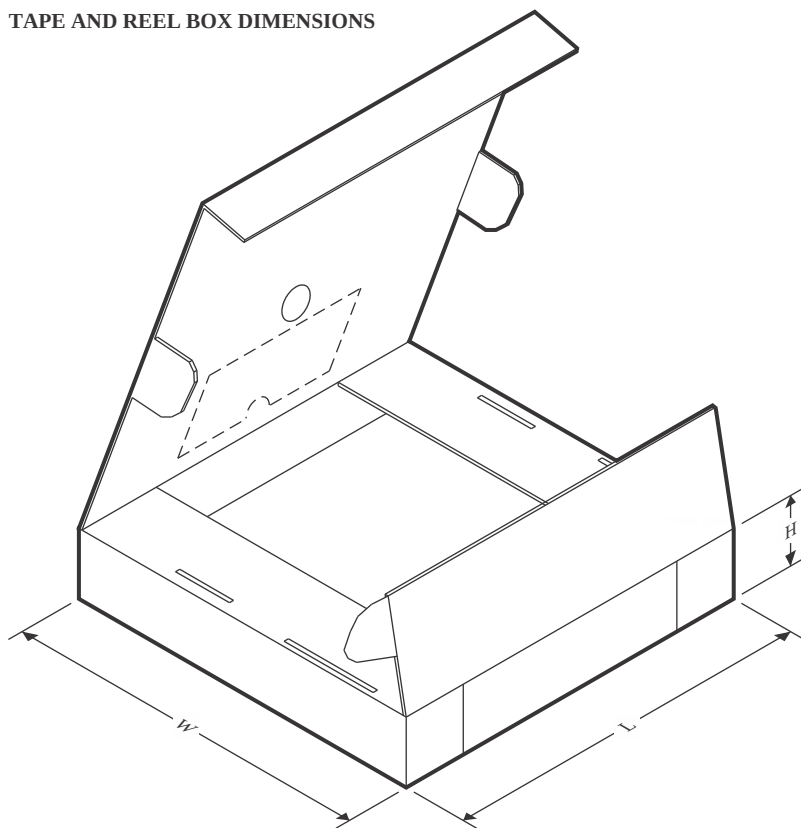
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA143U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA143UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

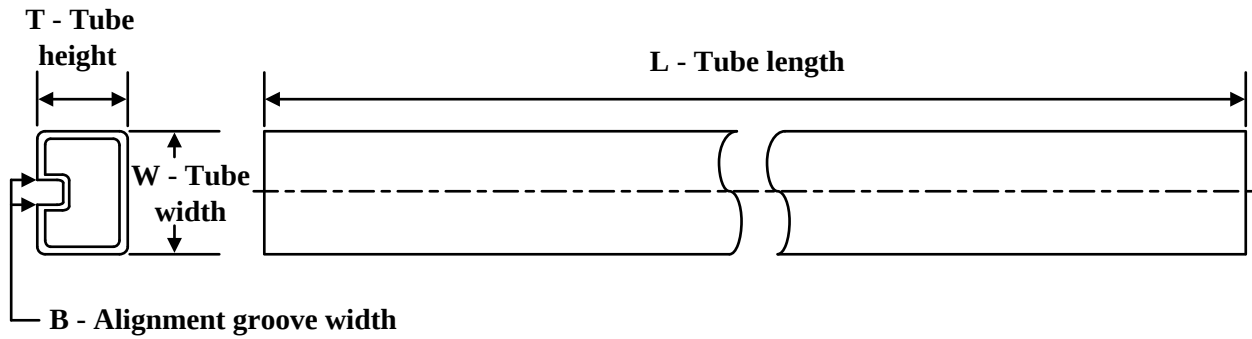
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA143U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA143UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE

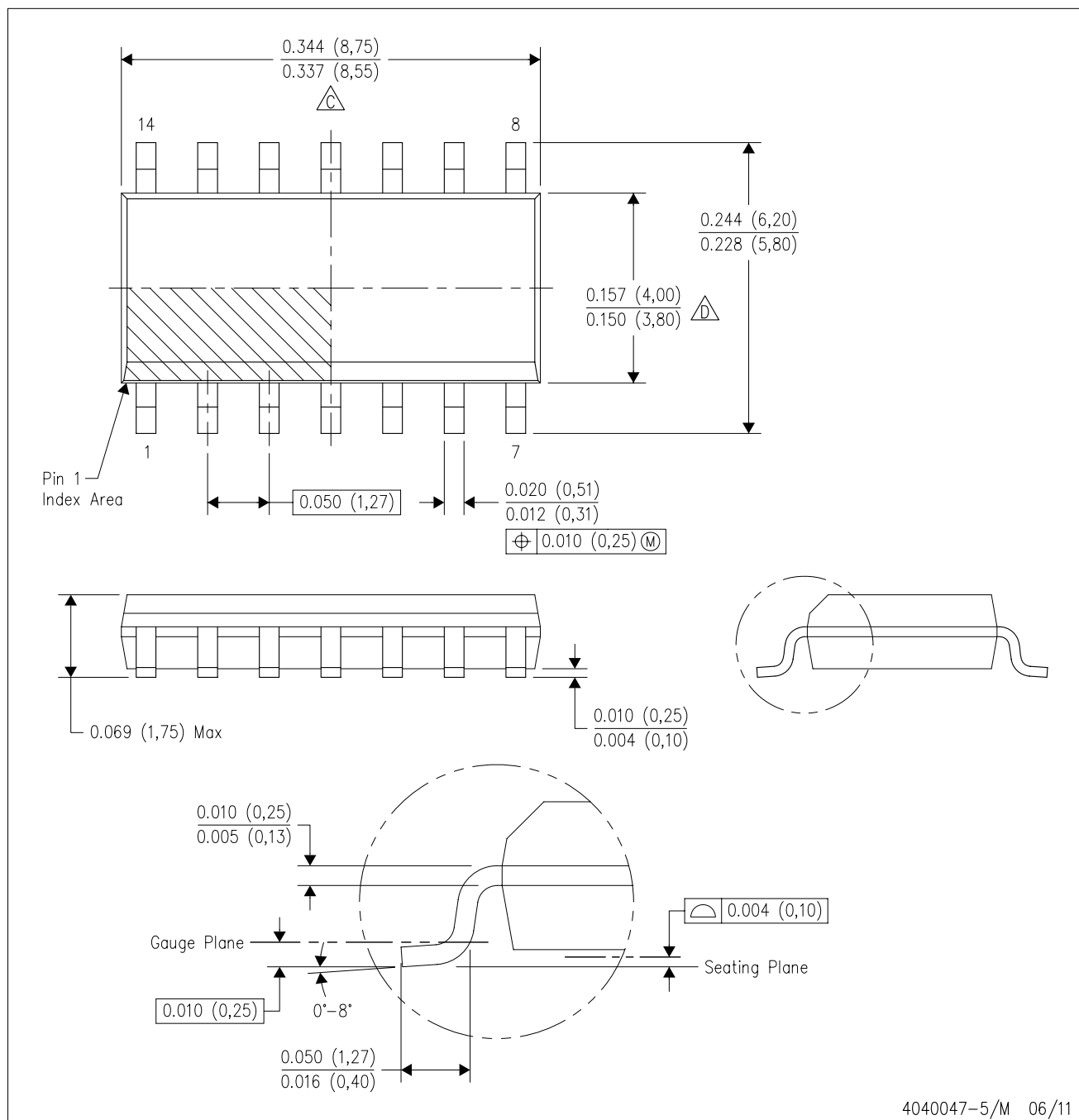


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA143U	D	SOIC	8	75	506.6	8	3940	4.32
INA143UA	D	SOIC	8	75	506.6	8	3940	4.32
INA2143U	D	SOIC	14	50	506.6	8	3940	4.32
INA2143UA	D	SOIC	14	50	506.6	8	3940	4.32
INA2143UAE4	D	SOIC	14	50	506.6	8	3940	4.32

D (R-PDSO-G14)

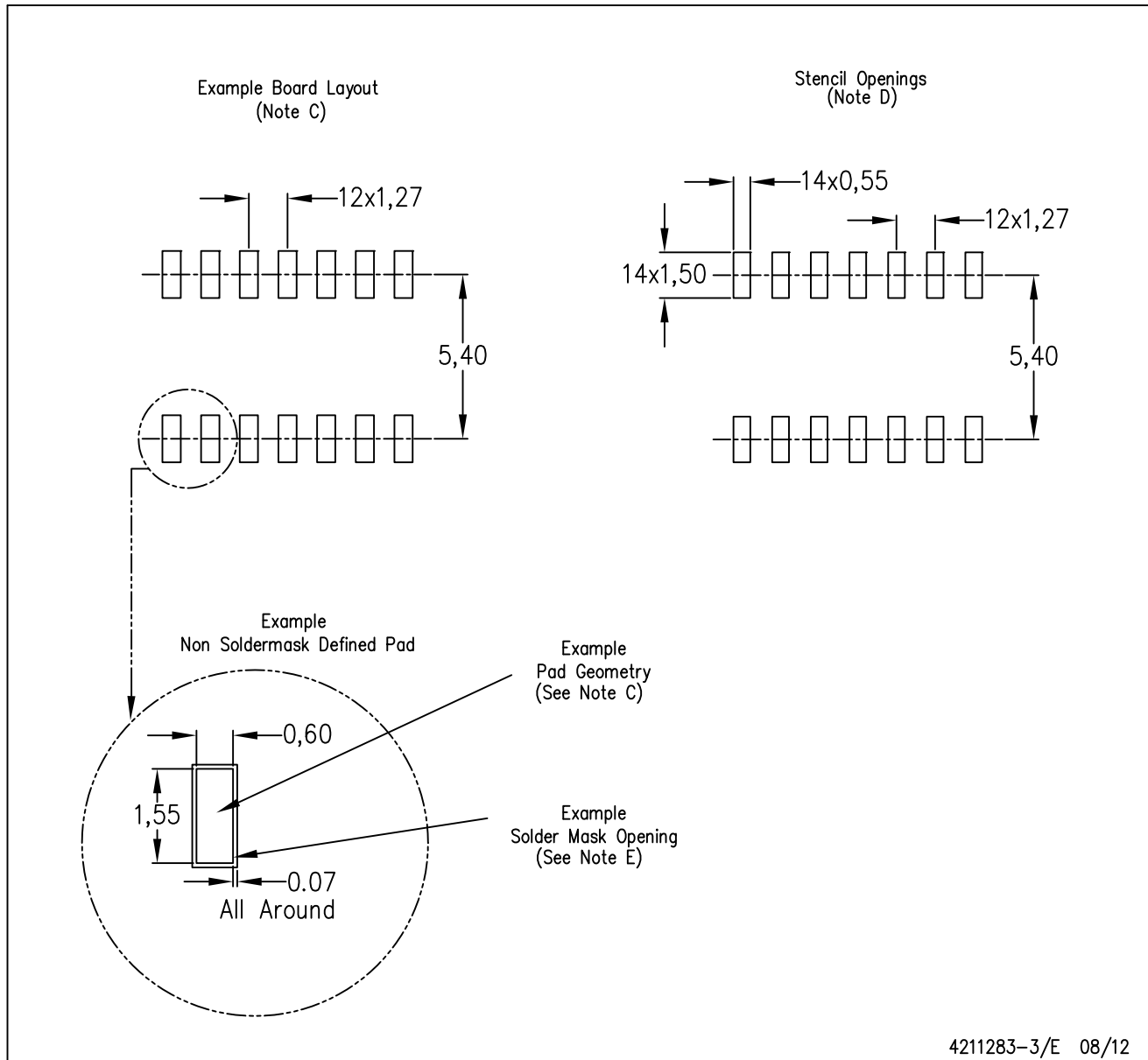
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



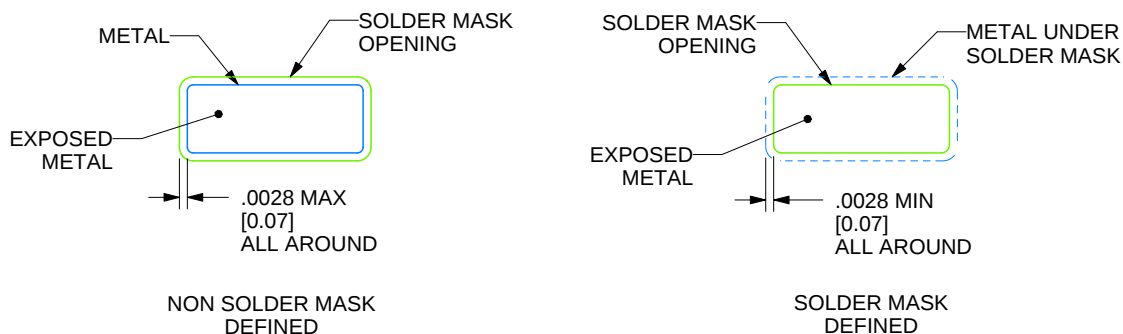
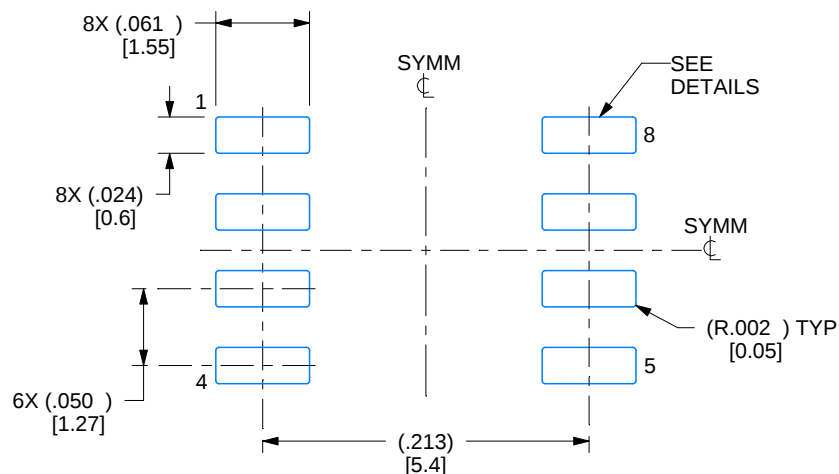
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

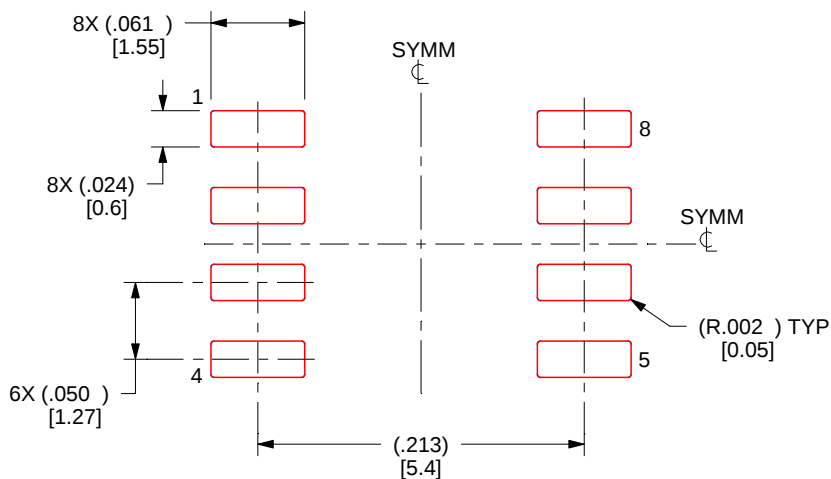
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated