CSD13302W 12 V N Channel NexFET™ Power MOSFET

1 Features

- Ultra Low On Resistance
- Low Q_g and Q_{gd}
- Small Footprint 1 mm × 1 mm
- Low Profile 0.62 mm Height
- Pb Free
- RoHS Compliant
- Halogen Free

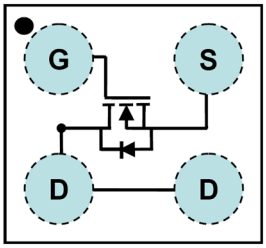
2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

This 14.6 mΩ, 12 V, N-Channel device is designed to deliver the lowest on resistance and gate charge in a small 1 x 1 mm outline with excellent thermal characteristics and an ultra low profile.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	6.0		nC
Q_{gd}	Gate Charge Gate-to-Drain	2.1		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V	21.2	mΩ
		V_{GS} = 4.5 V	14.6	mΩ
$V_{GS(th)}$	Threshold Voltage	1.0		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD13302W	3000	7-Inch Reel	1.0 mm × 1.0 mm Wafer Level Package	Tape and Reel
CSD13302WT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

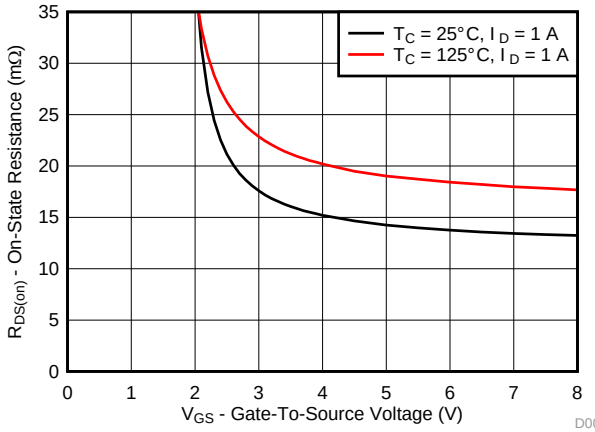
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_D	Continuous Drain Current (1)	1.6	A
I_{DM}	Pulsed Drain Current (2)	29	A
P_D	Power Dissipation (3)	1.8	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Device Operating at a temperature of 105ºC

(2) Min Cu Typ $R_{\theta JA}$ = 275ºC/W, Pulse width ≤100 µs, duty cycle ≤1%

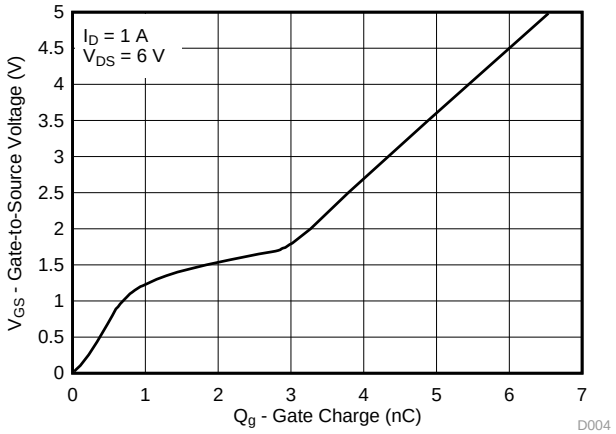
(3) Max Cu Typ $R_{\theta JA}$ = 70ºC/W

$R_{DS(on)}$ vs V_{GS}



D007

Gate Charge



D004

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

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5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C)

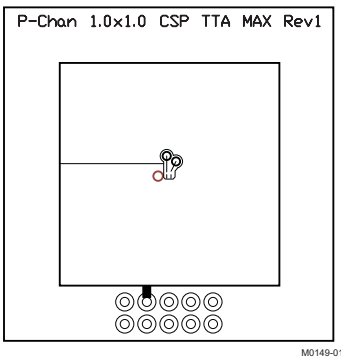
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 , I_D = 250 µA	12			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 9.6 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 10 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.7	1.0	1.3	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V, I_D = 1 A		21.2	25.8	mΩ
		V_{GS} = 4.5 V, I_D = 1 A		14.6	17.1	
g_{fs}	Transconductance	V_{DS} = 1.2 V, I_D = 1 A		10		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz		663	862	pF
C_{OSS}	Output Capacitance			211	274	pF
C_{RSS}	Reverse Transfer Capacitance			151	196	pF
R_g	Series Gate Resistance			3.6	7.2	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 6 V, I_D = 1 A		6.0	7.8	nC
Q_{gd}	Gate Charge Gate-to-Drain			2.1		nC
Q_{gs}	Gate Charge Gate-to-Source			0.7		nC
$Q_{g(th)}$	Gate Charge at Vth			0.7		nC
Q_{OSS}	Output Charge	V_{DS} = 6 V, V_{GS} = 0 V		1.3		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 1 A R_G = 0 Ω		6		ns
t_r	Rise Time			7		ns
$t_{d(off)}$	Turn Off Delay Time			17		ns
t_f	Fall Time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = 1 A, V_{GS} = 0 V		0.7	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 6 V, I_S = 1 A, di/dt = 200 A/µs		11.6		nC
t_{rr}	Reverse Recovery Time			19.6		ns

5.2 Thermal Information

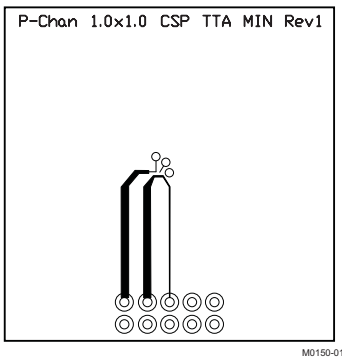
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)		275		°C/W
	Junction-to-Ambient Thermal Resistance(2)		70		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Typical $R_{\theta JA}$ = 70°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Typical $R_{\theta JA}$ = 275°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

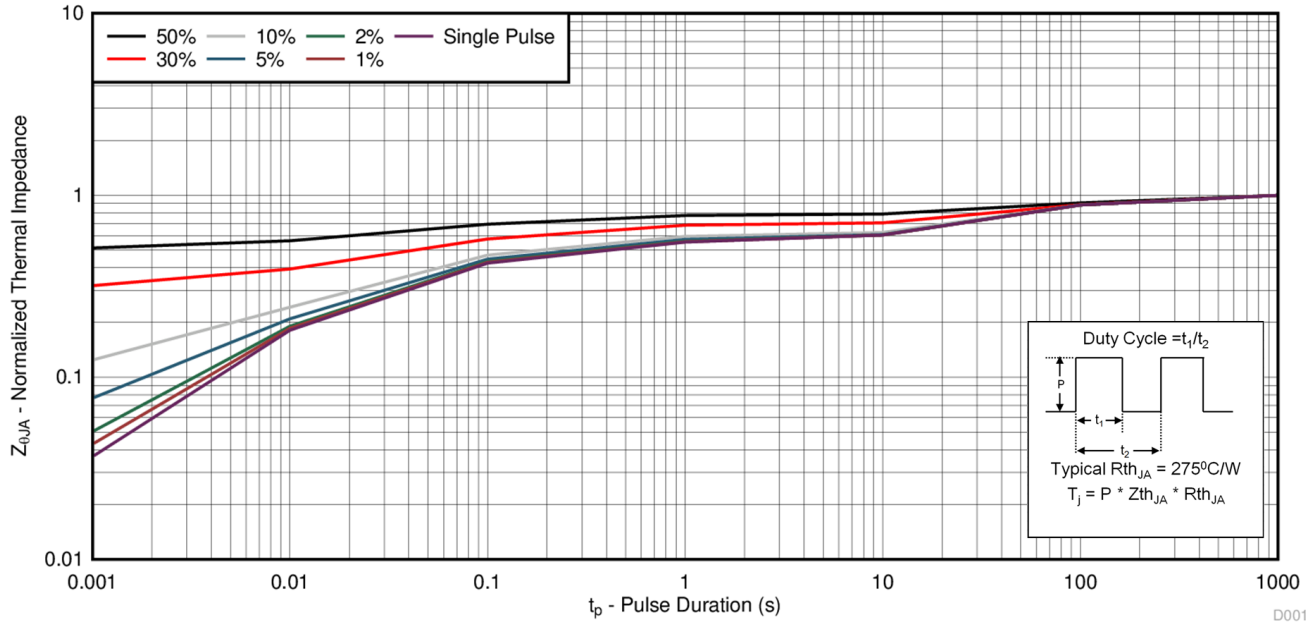


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

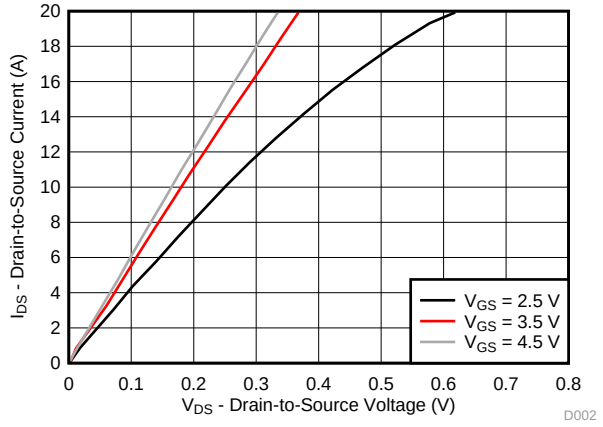


Figure 2. Saturation Characteristics

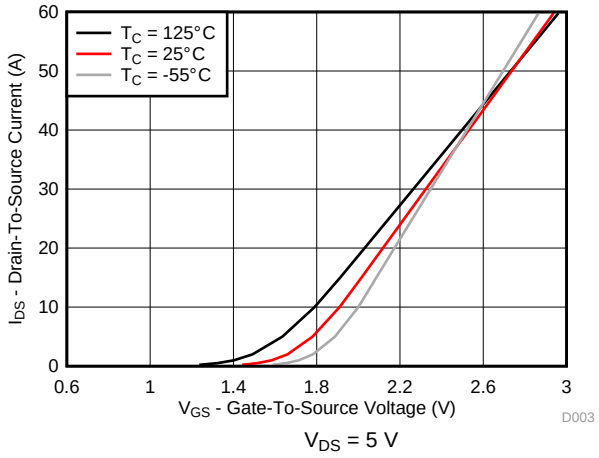


Figure 3. Transfer Characteristics

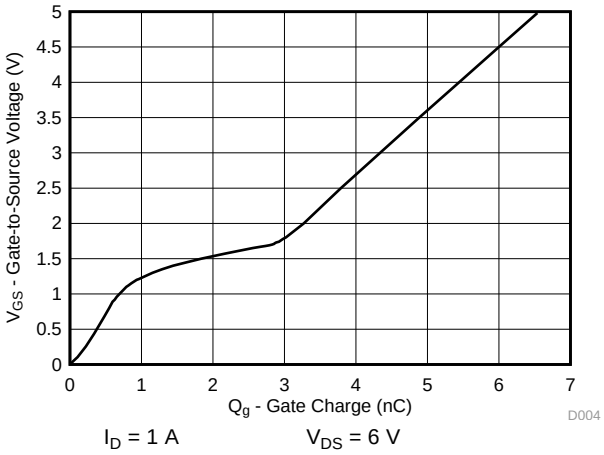


Figure 4. Gate Charge

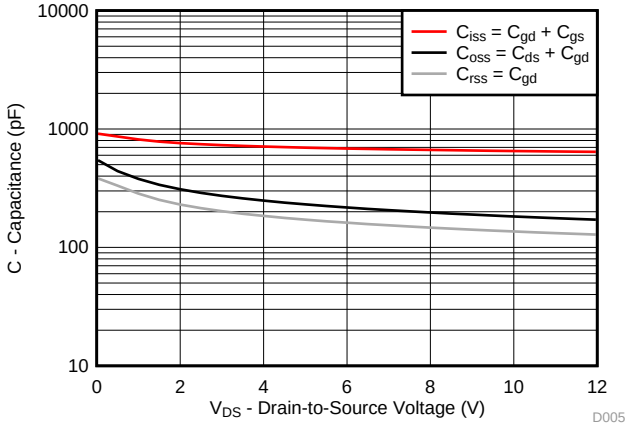


Figure 5. Capacitance

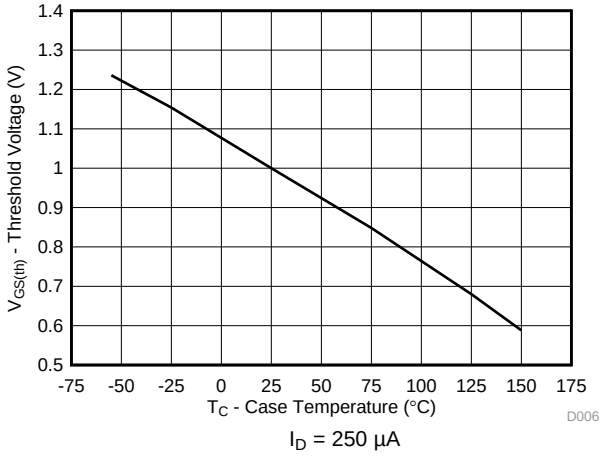


Figure 6. Threshold Voltage vs Temperature

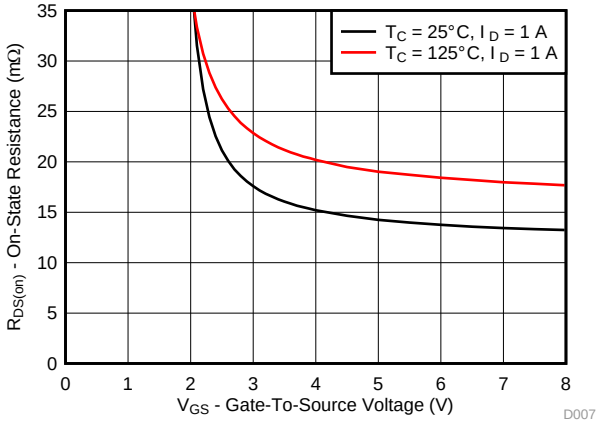


Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

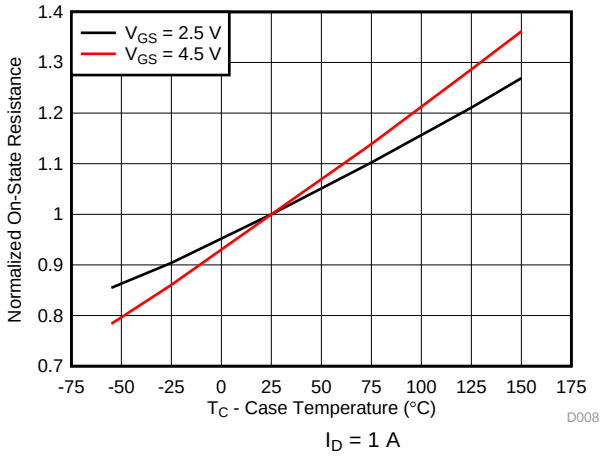


Figure 8. Normalized On-State Resistance vs Temperature

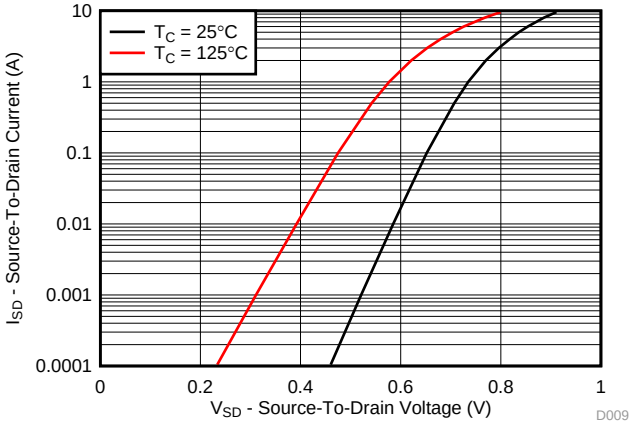


Figure 9. Typical Diode Forward Voltage

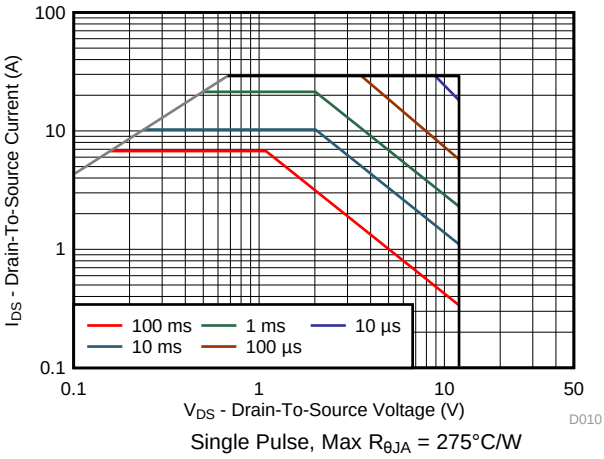


Figure 10. Maximum Safe Operating Area

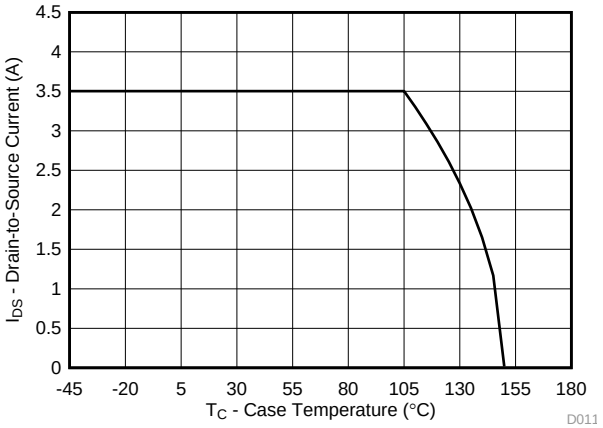


Figure 11. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

SLYZ022 — *TI Glossary*.

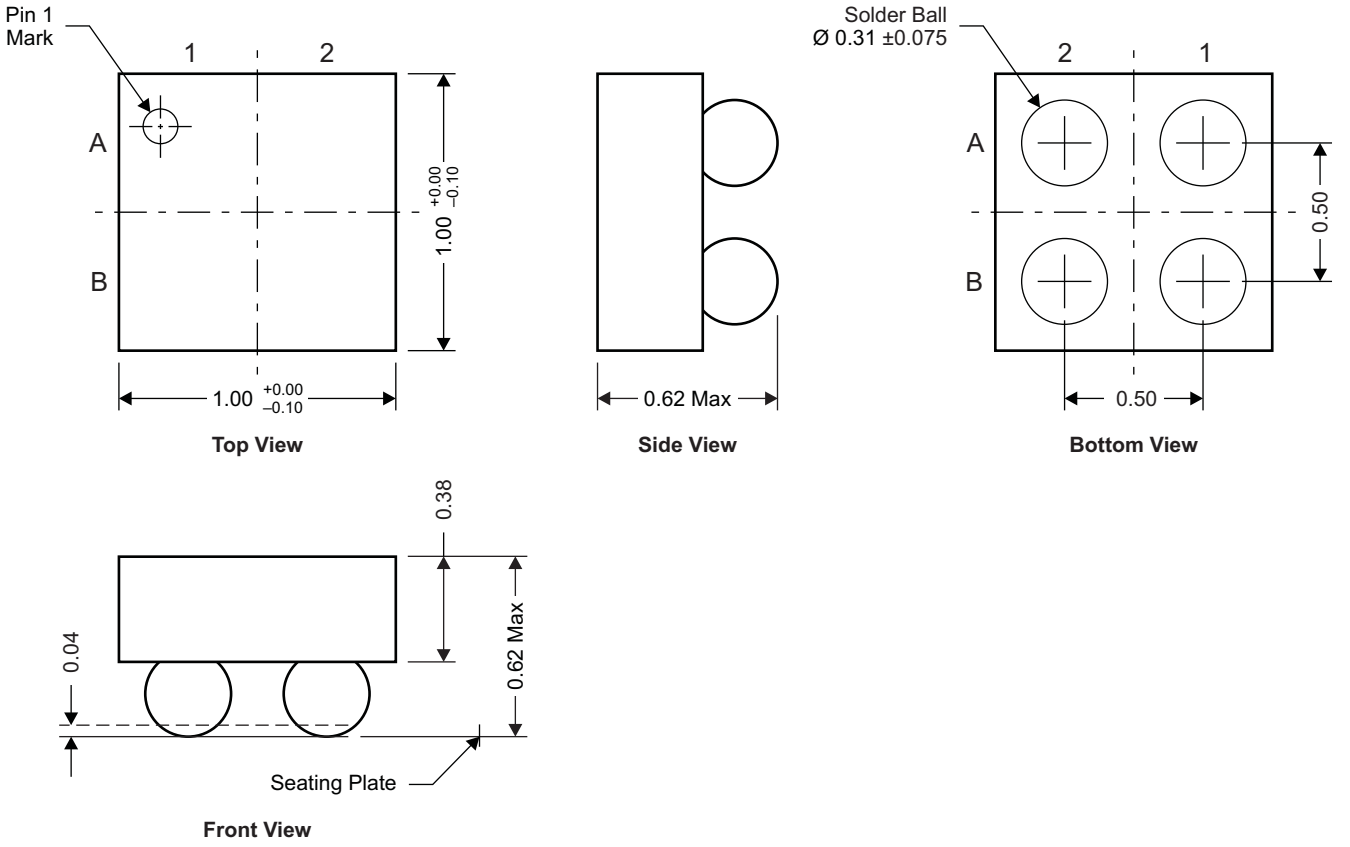
This glossary lists and explains terms, acronyms, and definitions.

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD13302W Package Dimensions



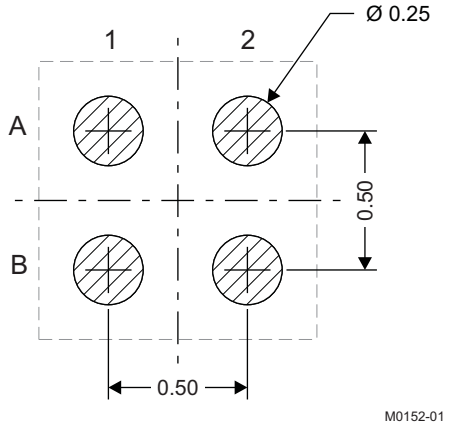
NOTE: All dimensions are in mm (unless otherwise specified)

Pin Configuration Table

POSITION	DESIGNATION
A2	Source
A1	Gate
B1, B2	Drain

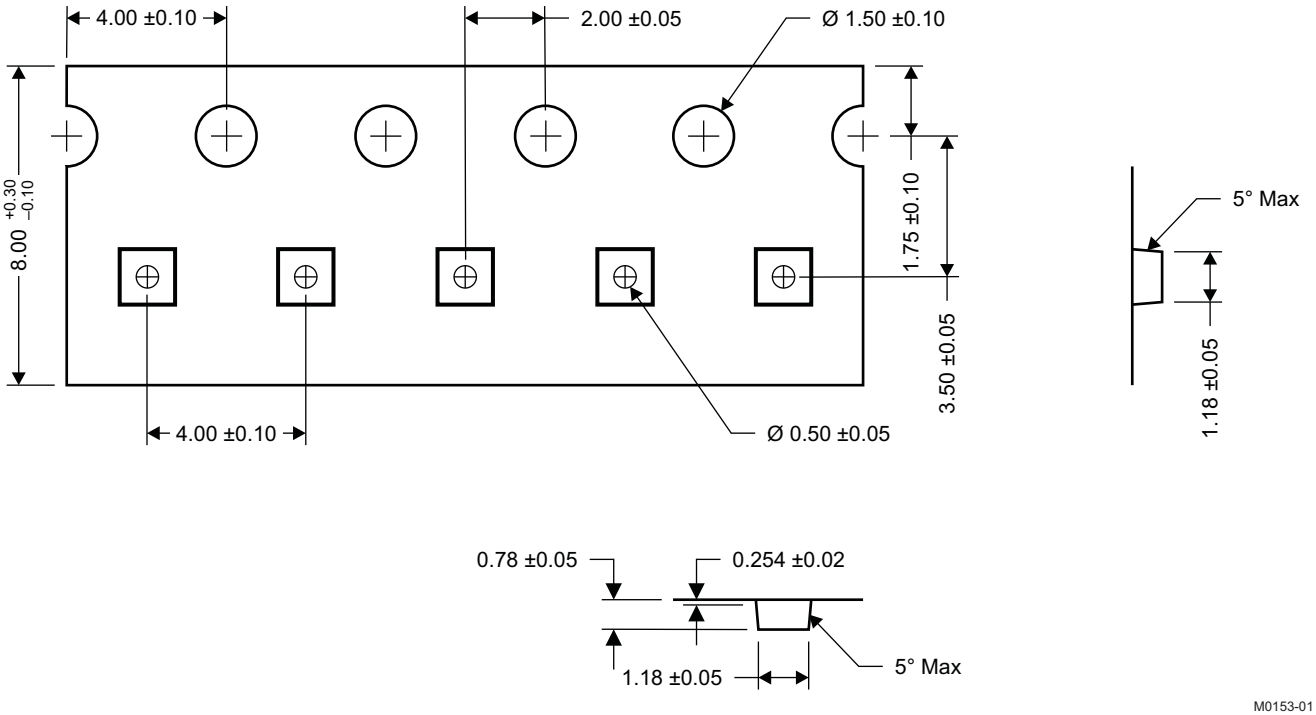
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Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

7.2 Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13302W	ACTIVE	DSBGA	YZB	4	3000	Green (RoHS & no Sb/Br)	Call TI | SNAGCU	Level-1-260C-UNLIM		302	Samples
CSD13302WT	ACTIVE	DSBGA	YZB	4	250	Green (RoHS & no Sb/Br)	Call TI | SNAGCU	Level-1-260C-UNLIM		302	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

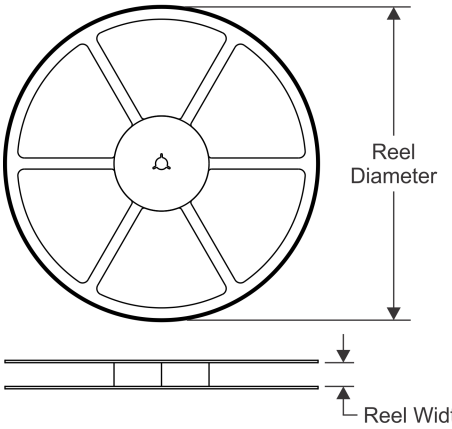
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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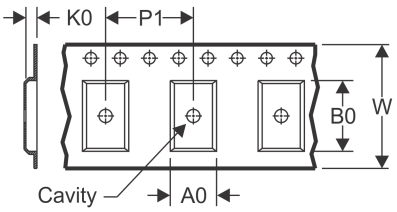
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

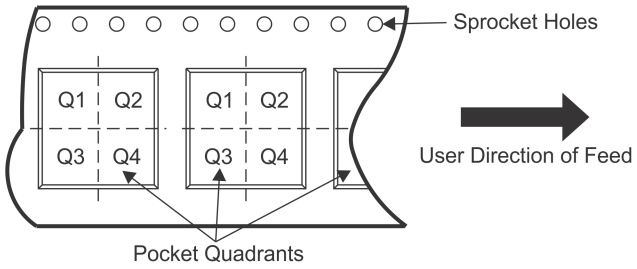


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

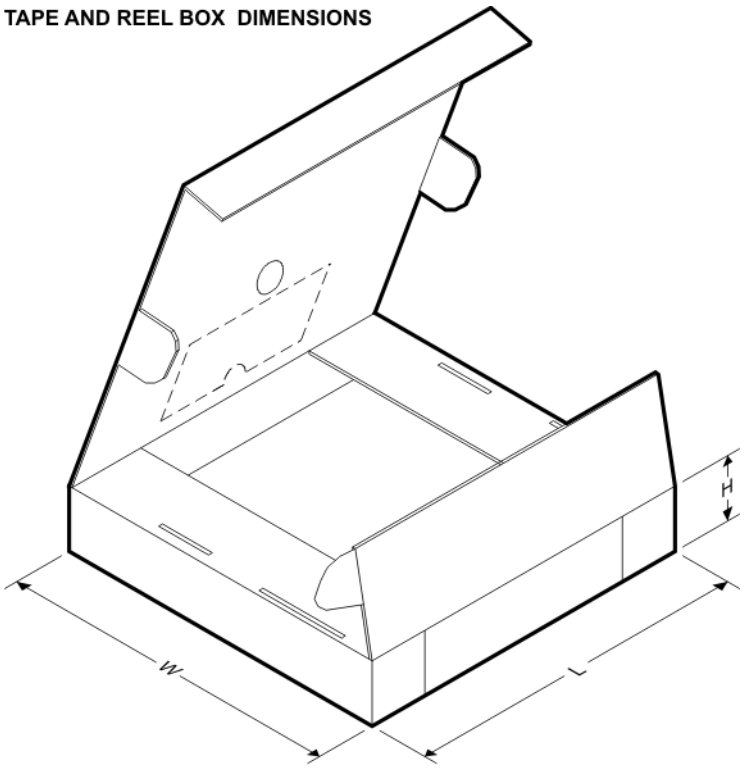
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13302W	DSBGA	YZB	4	3000	178.0	8.4	1.07	1.07	0.74	4.0	8.0	Q1
CSD13302W	DSBGA	YZB	4	3000	180.0	8.4	1.06	1.06	0.69	4.0	8.0	Q1
CSD13302WT	DSBGA	YZB	4	250	178.0	8.4	1.07	1.07	0.74	4.0	8.0	Q1
CSD13302WT	DSBGA	YZB	4	250	180.0	8.4	1.06	1.06	0.69	4.0	8.0	Q1

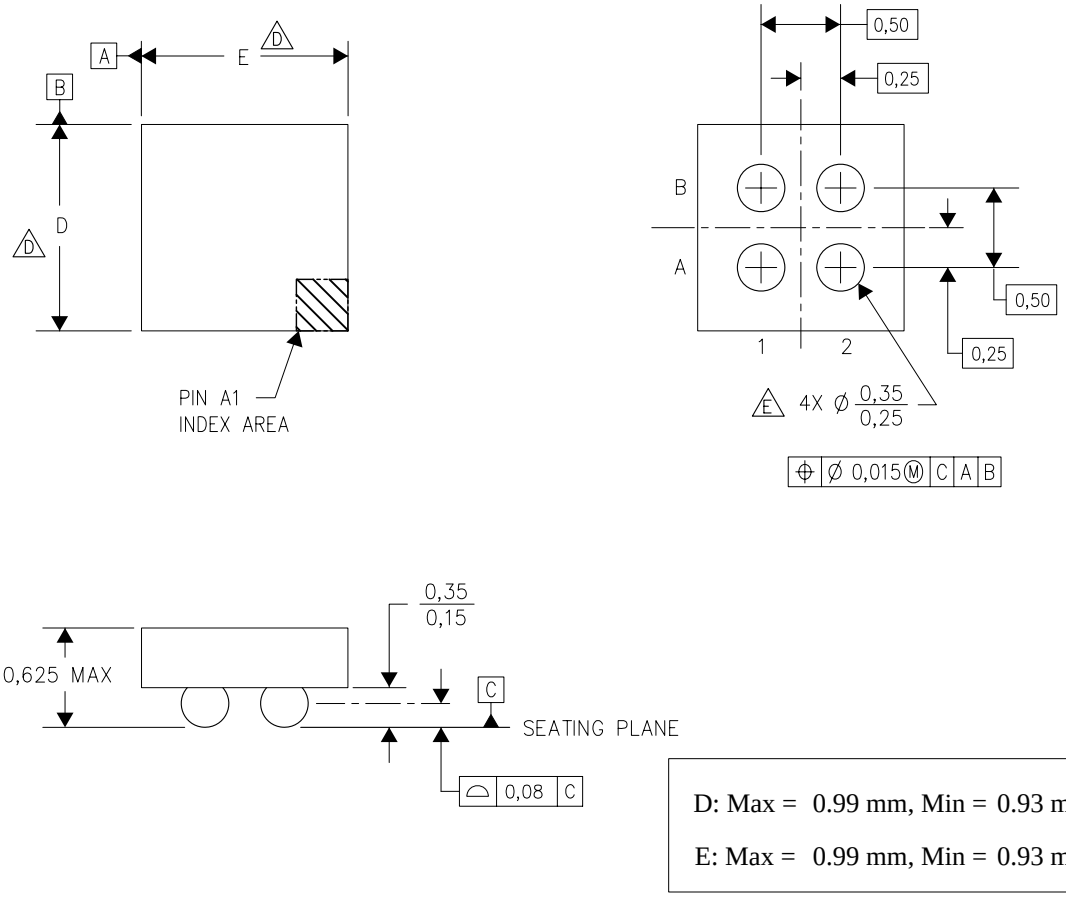
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13302W	DSBGA	YZB	4	3000	220.0	220.0	35.0
CSD13302W	DSBGA	YZB	4	3000	182.0	182.0	20.0
CSD13302WT	DSBGA	YZB	4	250	220.0	220.0	35.0
CSD13302WT	DSBGA	YZB	4	250	182.0	182.0	20.0

YZB (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEB (Drawing #4204178) for tin–lead (SnPb) balls.

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