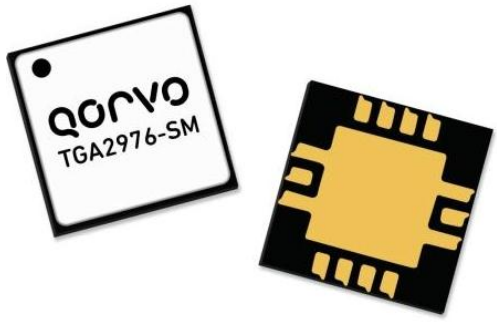
TGA2976-SM

0.1 – 3.0 GHz 10 W GaN Power Amplifier

Applications

- Commercial and military radar
- Communications
- Electronic Warfare

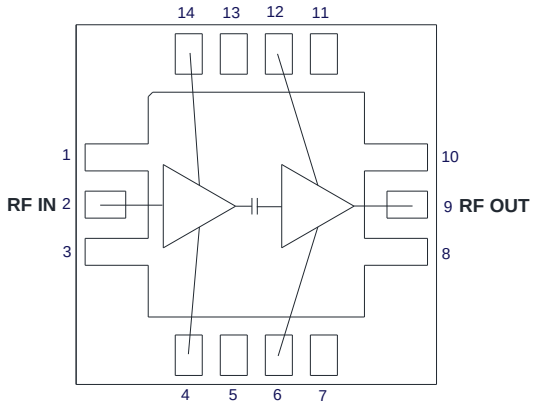


AC-QFN 4x4 mm 14L

Product Features

- Frequency Range: 0.1 – 3.0 GHz
- P_{SAT}: >40 dBm at P_{IN} = 27 dBm
- PAE: 48% @ midband
- Large Signal Gain: >13 dB
- Small Signal Gain: >20 dB
- Bias: V_D = 40 V, I_{DQ} = 360 mA, V_{G1} = -2.4 V Typical, V_{G2} = +17.7 V Typical
- Wideband Flat Gain and Power
- Package Dimensions: 4.0 x 4.0 x 1.64 mm

Functional Block Diagram



General Description

Qorvo's TGA2976-SM is a wideband cascode amplifier fabricated on Qorvo's production 0.25um GaN on SiC process. The cascode configuration offers exceptional wideband performance as well as supporting 40 V operation. The TGA2976-SM operates from 0.1 - 3.0 GHz and provides greater than 10 W of saturated output power with greater than 13 dB of large signal gain and greater than 38% power-added efficiency.

The TGA2976-SM is available in a low-cost, surface mount 14 lead 4x4 Air Cavity laminate package. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2976-SM is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Pad Configuration

Pad No.	Symbol
1, 3, 8, 10	GND
2	RF IN
4, 14	VG1
5, 7, 11, 13	N/C
6, 12	VG2
9	RF OUT / VD

Ordering Information

Part	ECCN	Description
TGA2976-SM	EAR99	0.1 – 3.0 GHz 10 W GaN Power Amplifier

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Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	80 V
Gate Voltage Range (V_{G1})	-8 to 0 V
Gate Voltage Range (V_{G2})	0 to 40 V
Drain Current (I_D)	760 mA
Gate Current (I_{G1})	See plot on pg. 3
Gate Current (I_{G2})	See plot on pg. 3
Power Dissipation (P_{DISS}), 85°C	28 W
Input Power (P_{IN}), CW, 50 Ω, 85°C,	33 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 40V, 85°C	33 dBm
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 Seconds)	260°C
Storage Temperature	-55 to 150°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	40 V
Drain Current (I_{DQ})	360 mA
Gate Voltage (V_{G1})	-2.4 V (Typ.)
Gate Voltage (V_{G2})	+17.7 V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25^{0}C, V_D = 40 V, I_{DQ} = 360 mA, V_{G1} = -2.4 V Typical, V_{G2} = +17.7 V Typical

Parameter	Min	Typical	Max	Units
Operational Frequency Range	0.1		3.0	GHz
Small Signal Gain		> 20		dB
Input Return Loss		> 5		dB
Output Return Loss		> 9		dB
Output Power (Pin = 27dBm)		> 40		dBm
Power Added Efficiency (Pin = 27dBm)		48 (mid band)		%
IM3 @ 120mA, POUT/tone = 28dBm		-30		dBc
IM5 @ 120mA, POUT/tone = 28dBm		-38		dBc
Small Signal Gain Temperature Coefficient		-0.03		dB/°C
Output Power Temperature Coefficient		-0.009		dBm/°C
Recommended Operating Voltage:		40	50	V

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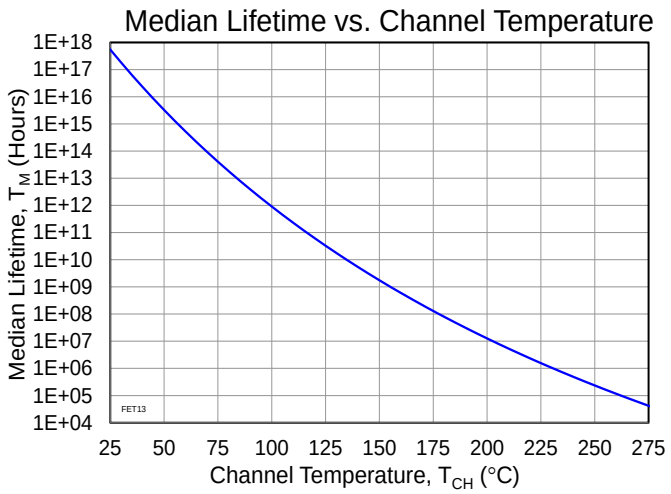
Thermal and Reliability Information

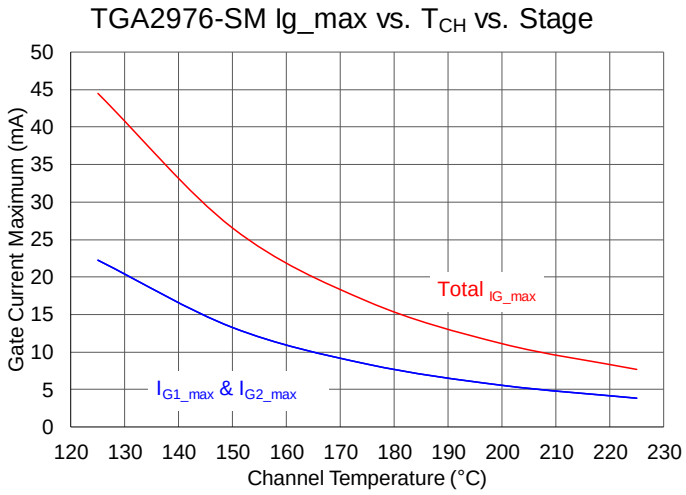
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, **V_D(2) = 40 V (CW)**	5.26	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)	I_{DQ} = 360 mA, $I_{D\ Drive}$ = 655 mA	177	°C
Median Lifetime (T_M)	P_{IN} = 27 dBm, P_{OUT} = 40 dBm, P_{DISS} = 17.4 W	1.07 x 10^8	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, **V_D(2) = 50 V (CW)**	5.72	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)	I_{DQ} = 360 mA, $I_{D\ Drive}$ = 665 mA	220	°C
Median Lifetime (T_M)	P_{IN} = 27 dBm, P_{OUT} = 40 dBm, P_{DISS} = 23.6 W	2.34x 10^6	Hrs

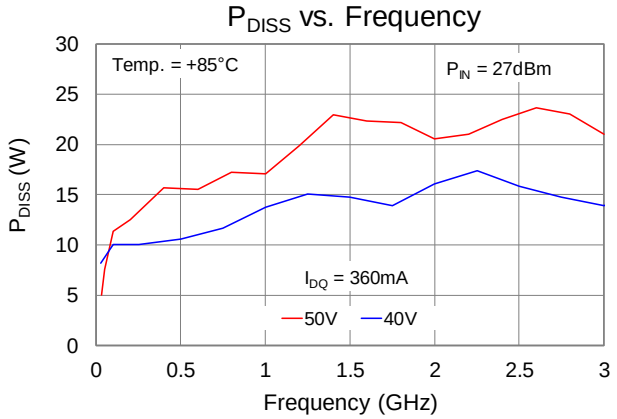
Notes:

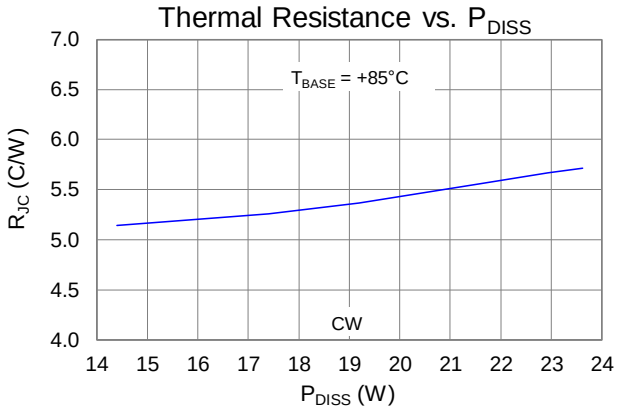
1. Thermal resistance measured to back of package.
2. The drain voltage for Cascode amplifier transistor is ½ of the V_D.

Test Conditions: V_D = 40 V; Failure Criteria = 10% reduction in I_{D_MAX}







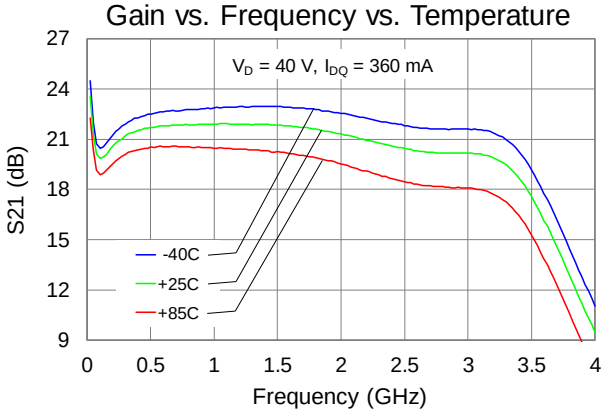


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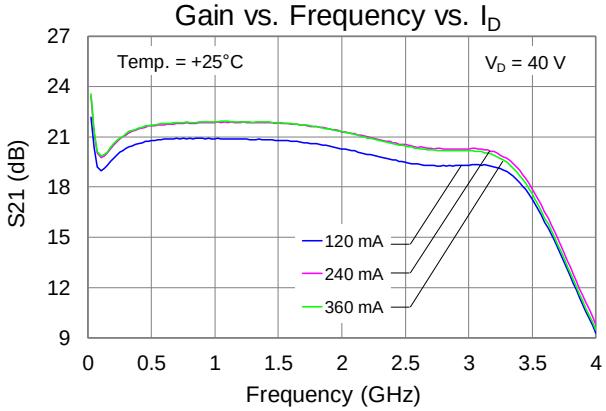
Typical Performance: Small Signal

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

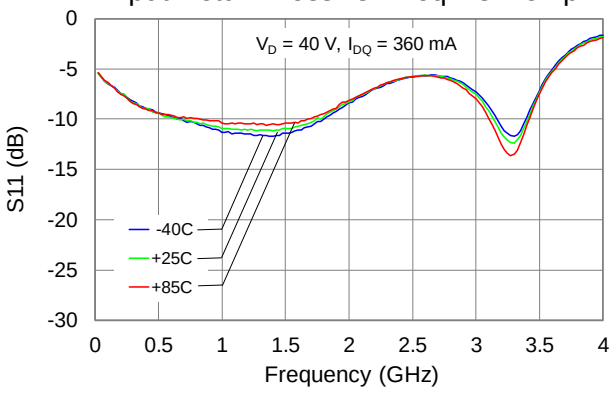
Gain vs. Frequency vs. Temperature



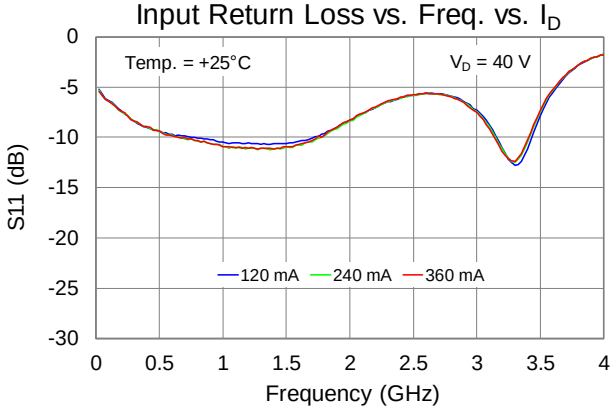
Gain vs. Frequency vs. I_D



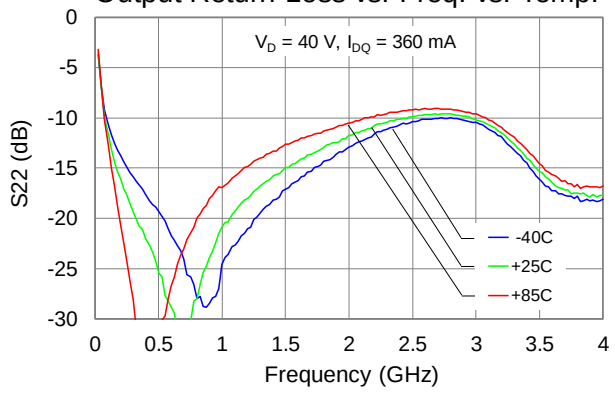
Input Return Loss vs. Freq. vs. Temp.



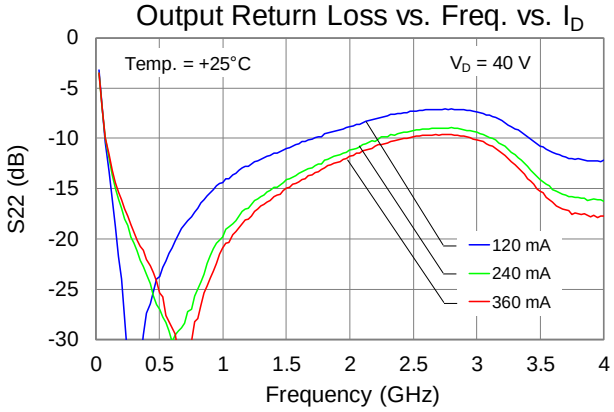
Input Return Loss vs. Freq. vs. I_D



Output Return Loss vs. Freq. vs. Temp.



Output Return Loss vs. Freq. vs. I_D

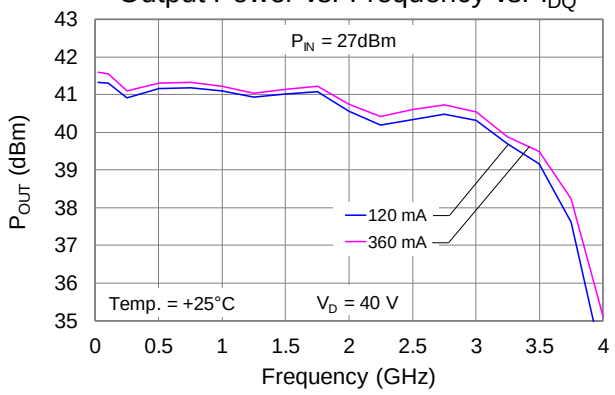


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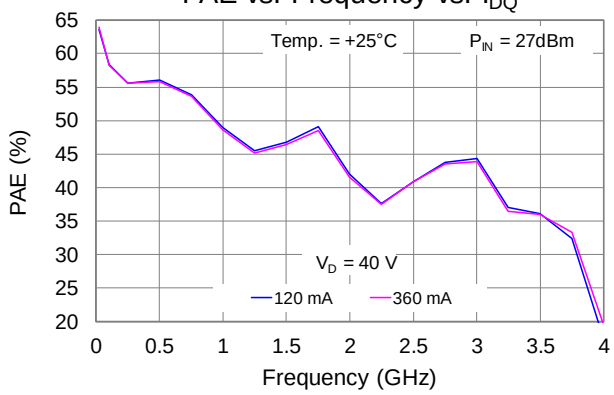
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

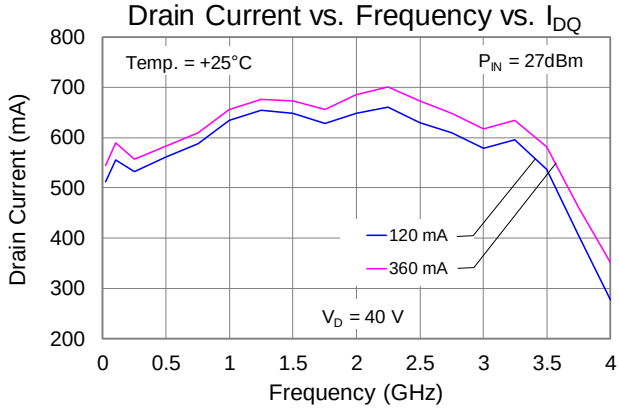
Output Power vs. Frequency vs. I_{DQ}



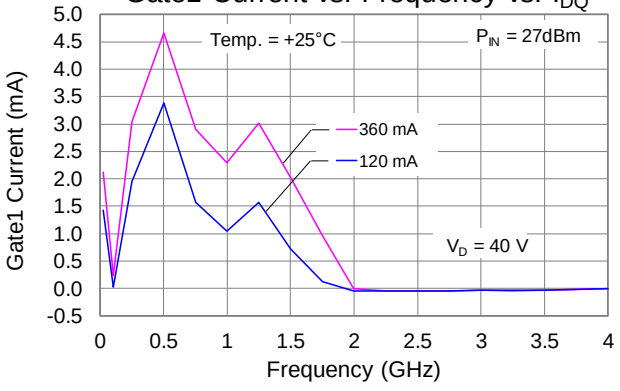
PAE vs. Frequency vs. I_{DQ}



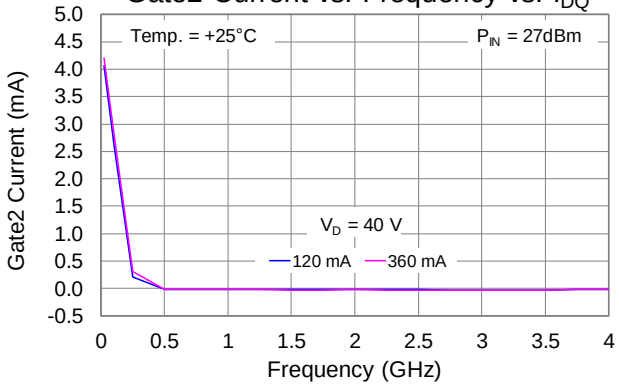
Drain Current vs. Frequency vs. I_{DQ}



Gate1 Current vs. Frequency vs. I_{DQ}



Gate2 Current vs. Frequency vs. I_{DQ}



Disclaimer: Subject to change without notice

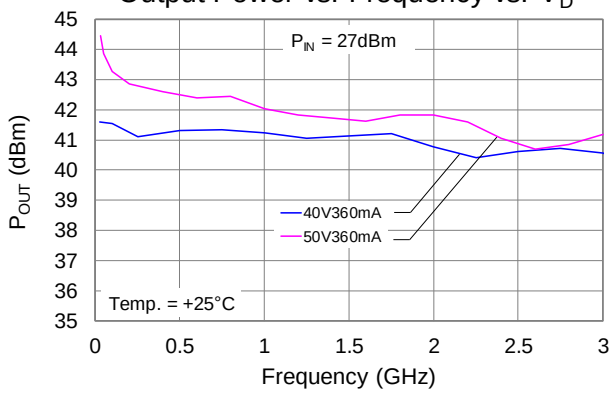
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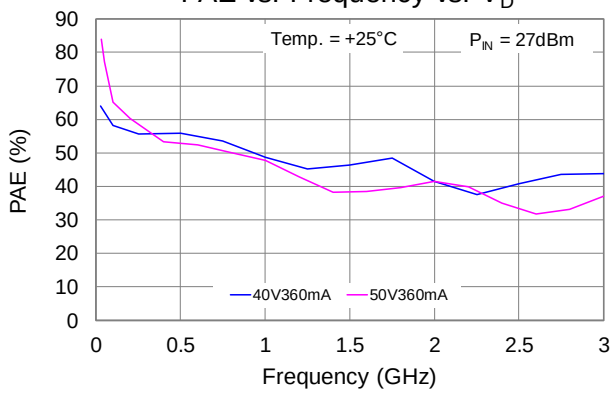
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

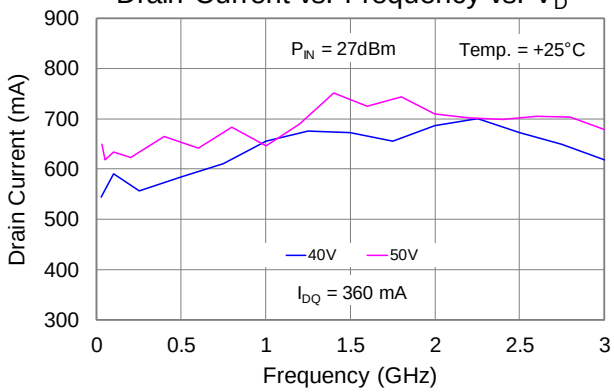
Output Power vs. Frequency vs. V_D



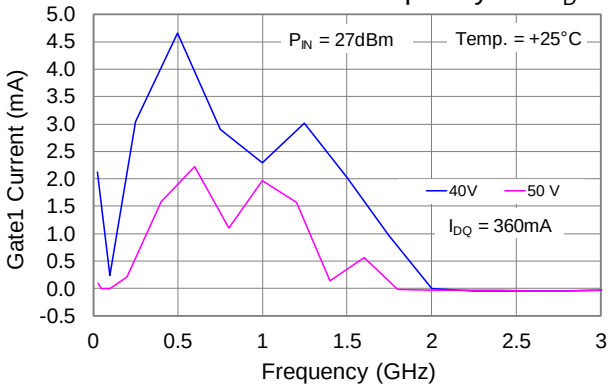
PAE vs. Frequency vs. V_D



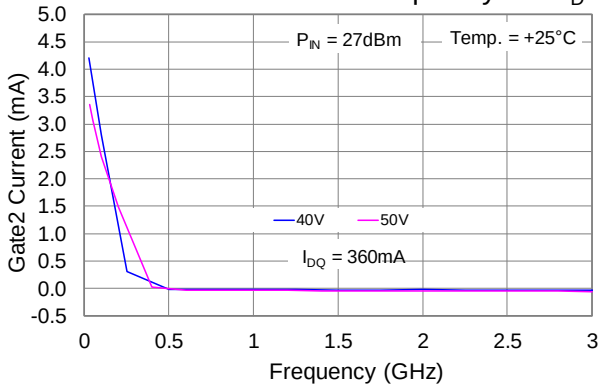
Drain Current vs. Frequency vs. V_D



Gate1 Current vs. Frequency vs. V_D



Gate2 Current vs. Frequency vs. V_D

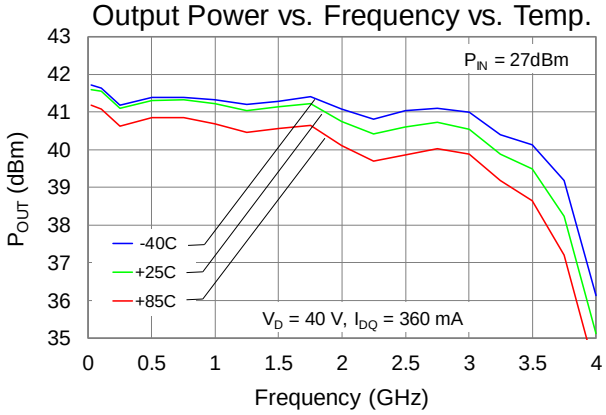


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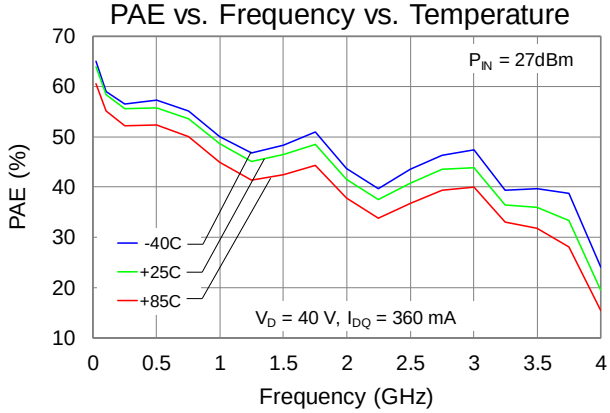
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

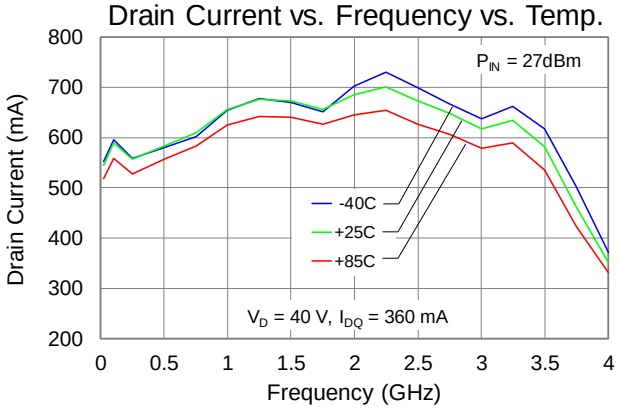
Output Power vs. Frequency vs. Temp.



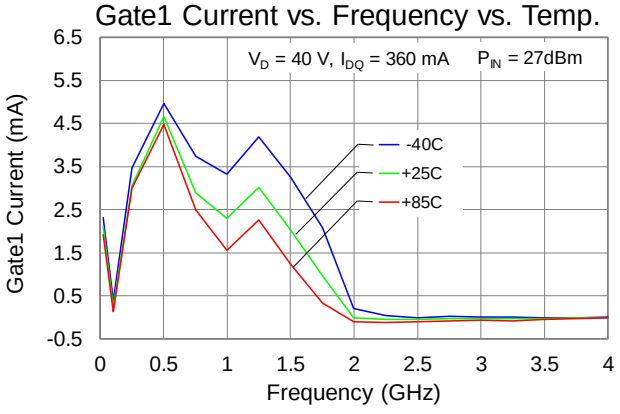
PAE vs. Frequency vs. Temperature



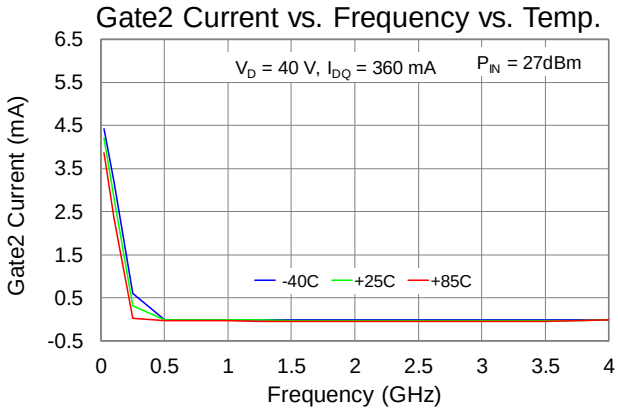
Drain Current vs. Frequency vs. Temp.



Gate1 Current vs. Frequency vs. Temp.



Gate2 Current vs. Frequency vs. Temp.



Disclaimer: Subject to change without notice

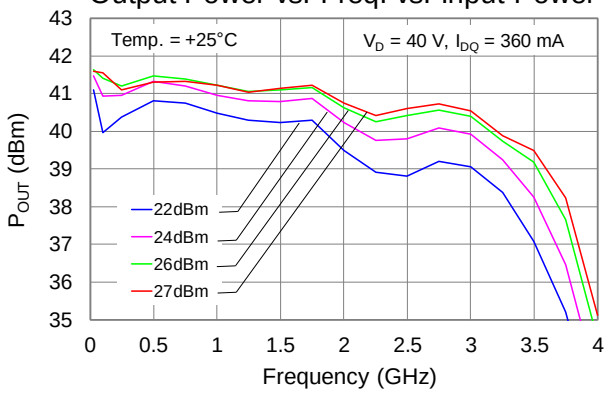
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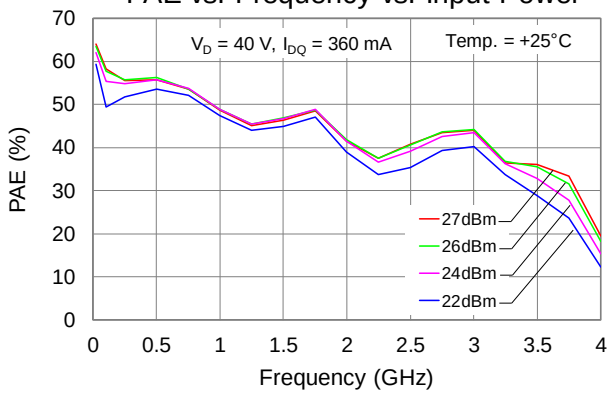
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

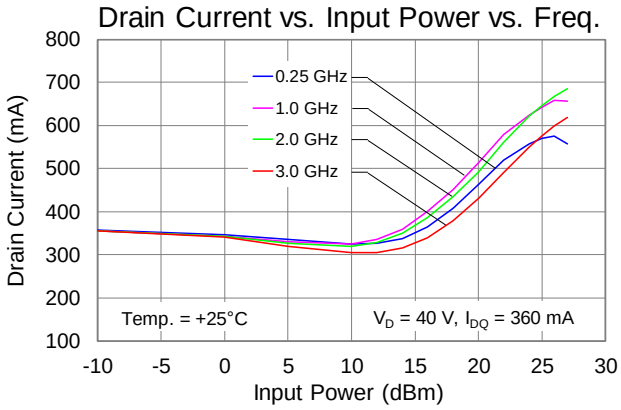
Output Power vs. Freq. vs. Input Power



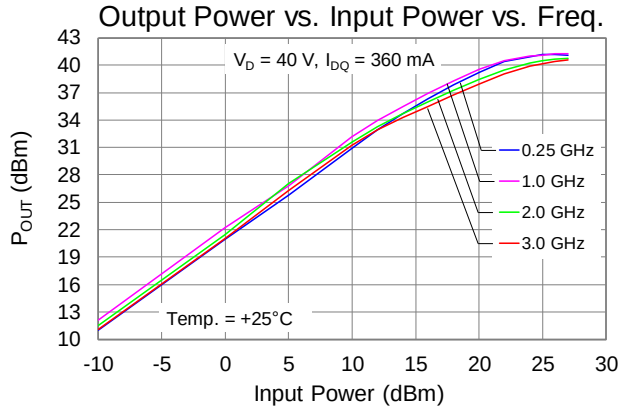
PAE vs. Frequency vs. Input Power



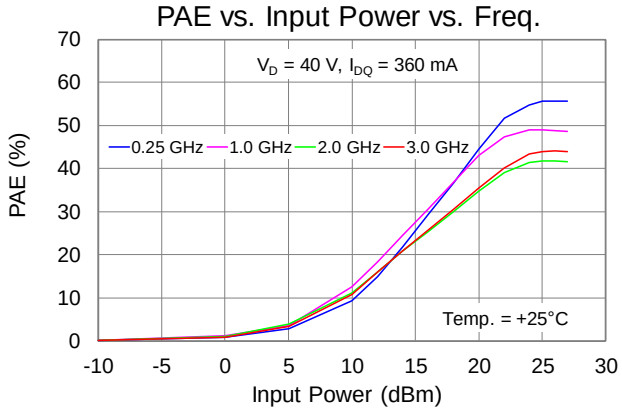
Drain Current vs. Input Power vs. Freq.



Output Power vs. Input Power vs. Freq.



PAE vs. Input Power vs. Freq.

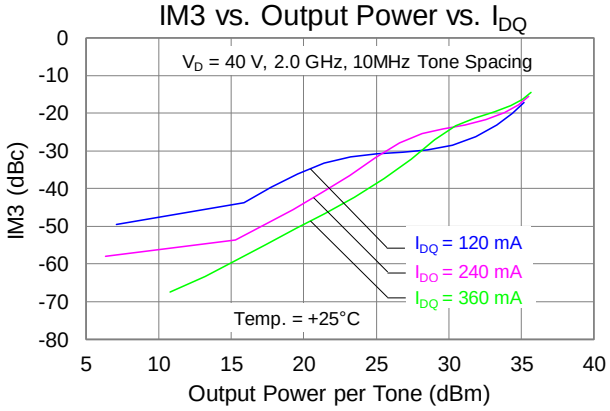


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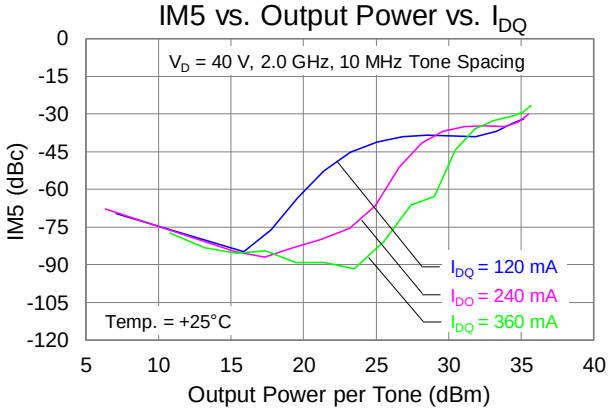
Typical Performance: Linearity

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

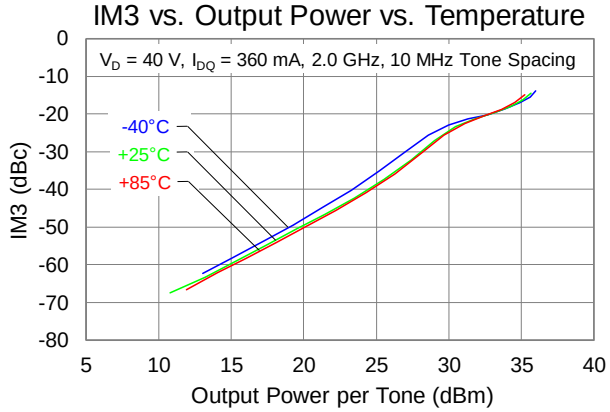
IM3 vs. Output Power vs. I_{DQ}



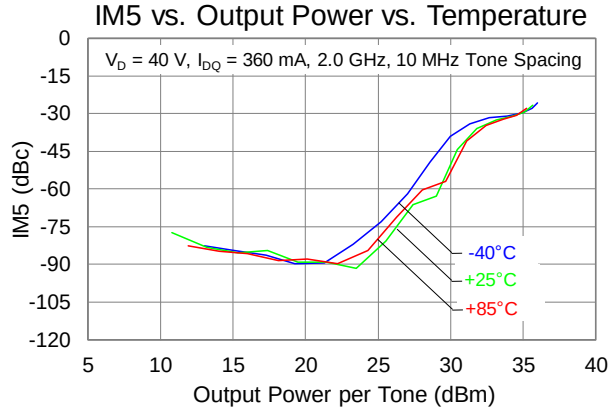
IM5 vs. Output Power vs. I_{DQ}



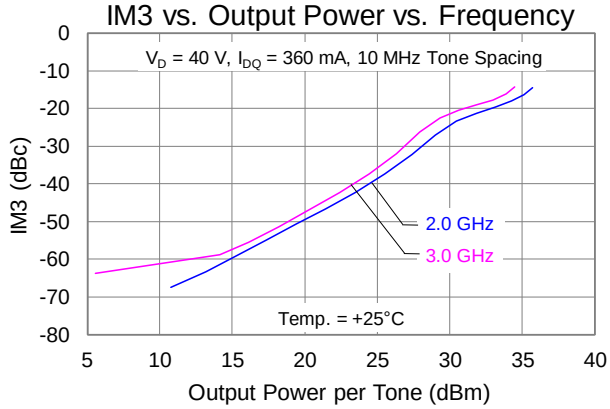
IM3 vs. Output Power vs. Temperature



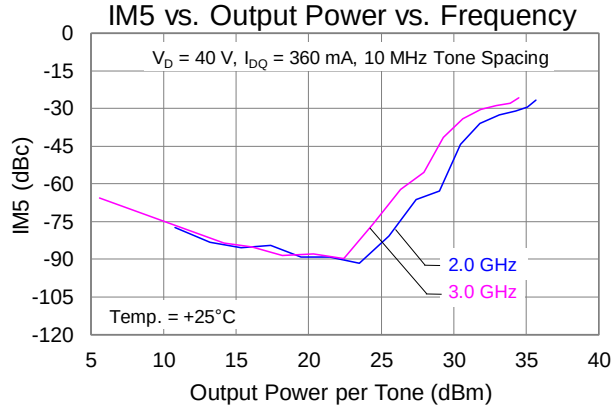
IM5 vs. Output Power vs. Temperature



IM3 vs. Output Power vs. Frequency



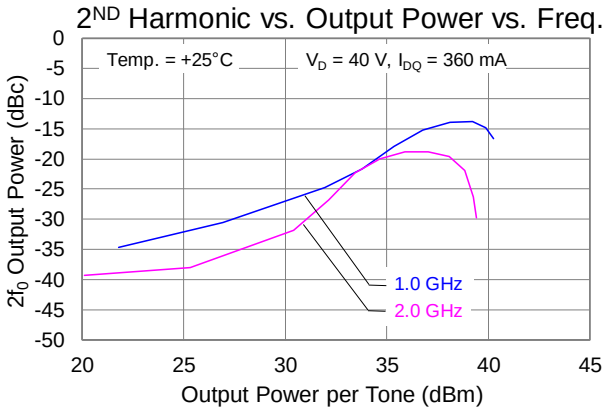
IM5 vs. Output Power vs. Frequency

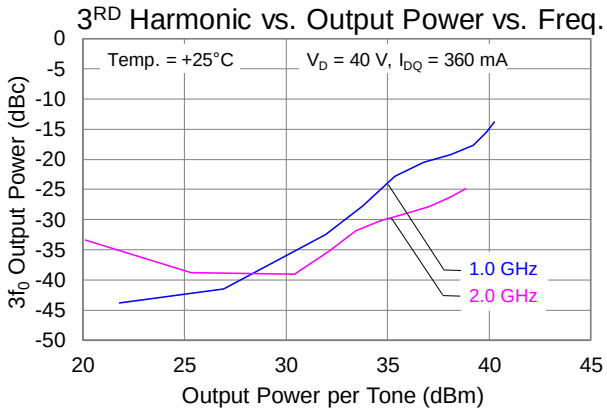


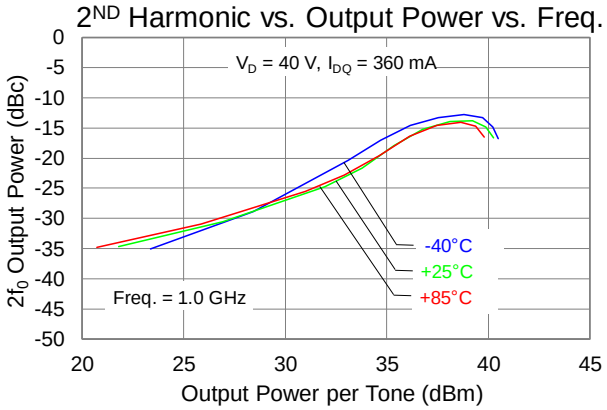
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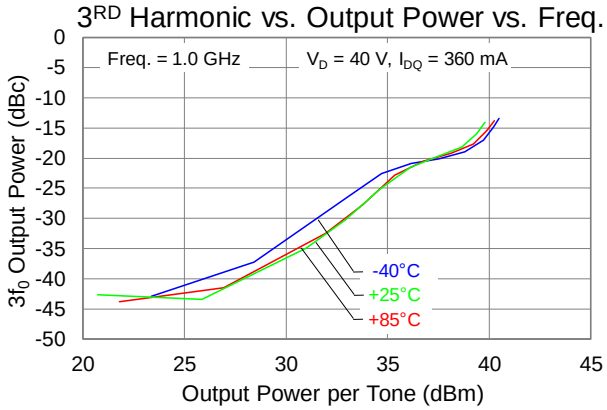
Typical Performance: Linearity

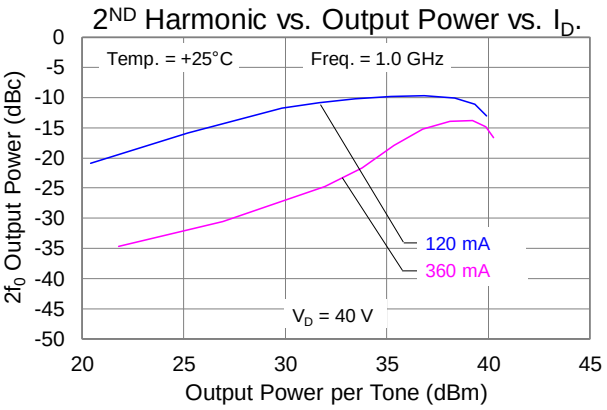
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 12)

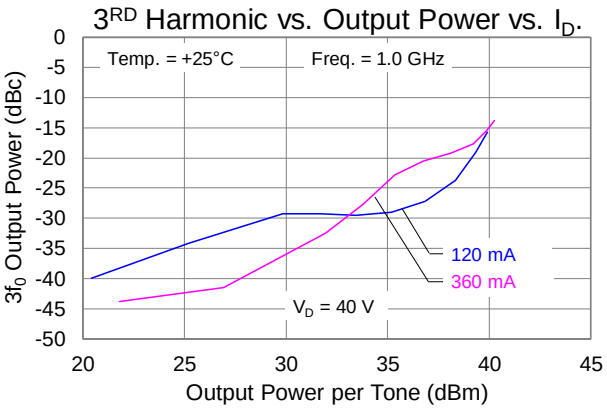










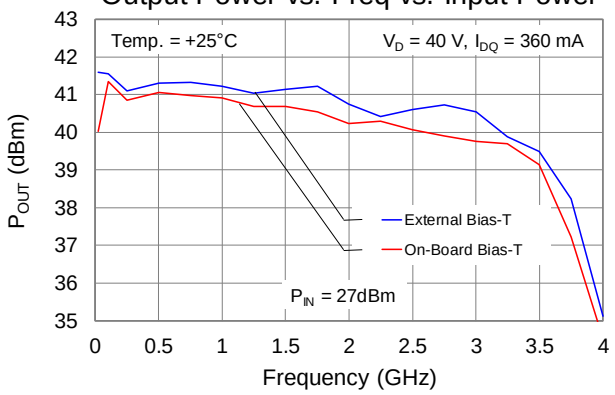


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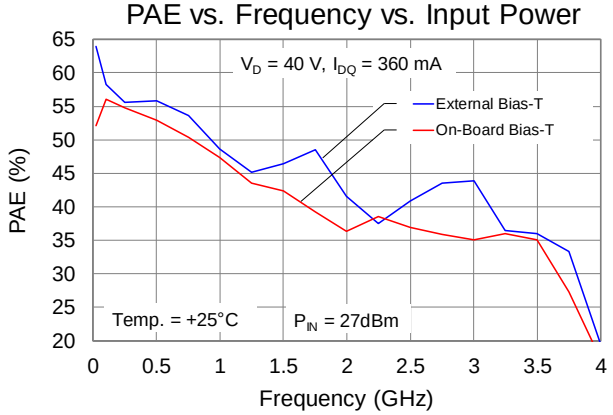
Typical Performance: Large Signal (CW), On-board vs. External Coaxial Bias-T

The plots below reflect performance measured between external bias tee and on-board bias tee
(See application circuit on pages 12 and 14)

Output Power vs. Freq vs. Input Power

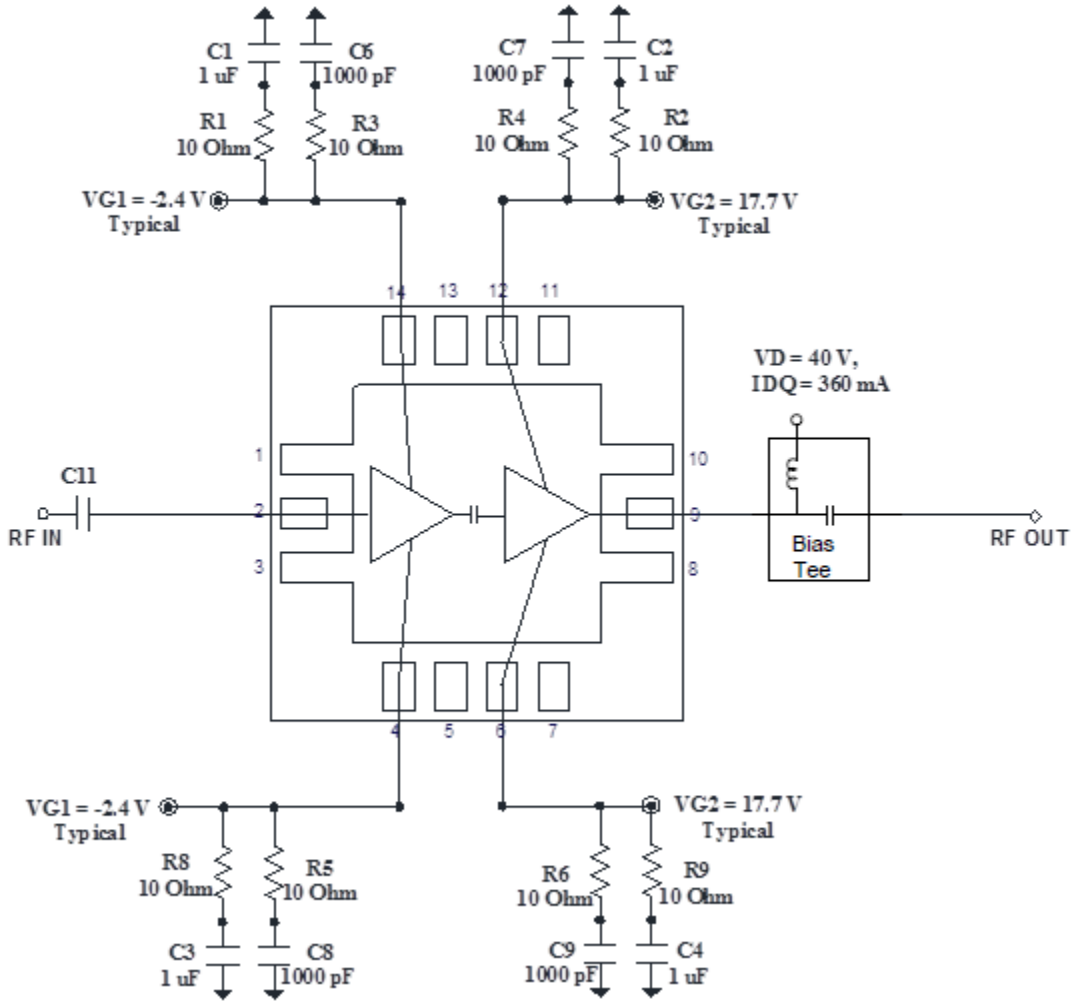


PAE vs. Frequency vs. Input Power



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Application Circuit (Coaxial input DC block and coaxial output bias tee)



Notes:

1. V_{G1} & V_{G2} can be biased from either side (Top or Bottom.)
2. Coaxial input DC block (C11) is used for input port (RF In.)
3. External wide bandwidth Bias-Tee is used for output port (RF Out). V_D is applied through the output Bias-Tee.

Bias-up Procedure

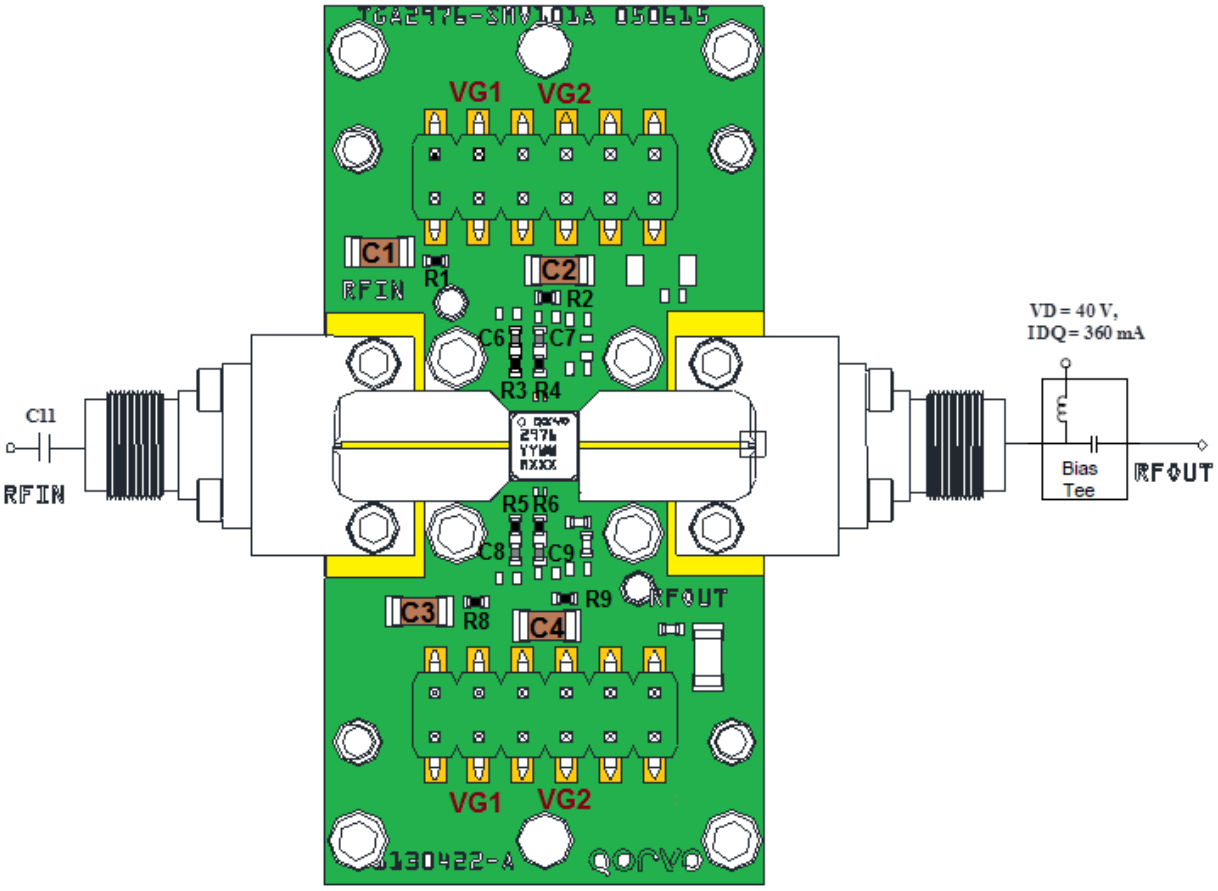
1. Set I_D limit to 755 mA, I_{G1} & I_{G2} limit to 5 mA
2. Set V_{G1} to -5.0 V
3. Set V_{G2} to (V_D/2) - 2.7 V or 40 V/2 - 2.7 V = 17.3 V
4. Set V_D +40 V
5. Adjust V_{G1} more positive until I_{DQ} = 360 mA (V_{G1} ~ -2.4 V Typical)
6. Adjust V_{G2} to (V_D/2) + V_{G1}; (V_{G2} ~ +17.7 V Typical)
7. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_{G1} to -5.0 V. Ensure I_{DQ} ~ 0mA
3. Reduce V_{G2} to 0 V.
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_{G2} supply
7. Turn off V_{G1} supply

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Assembly Drawing (Coaxial input DC block and coaxial output bias tee)



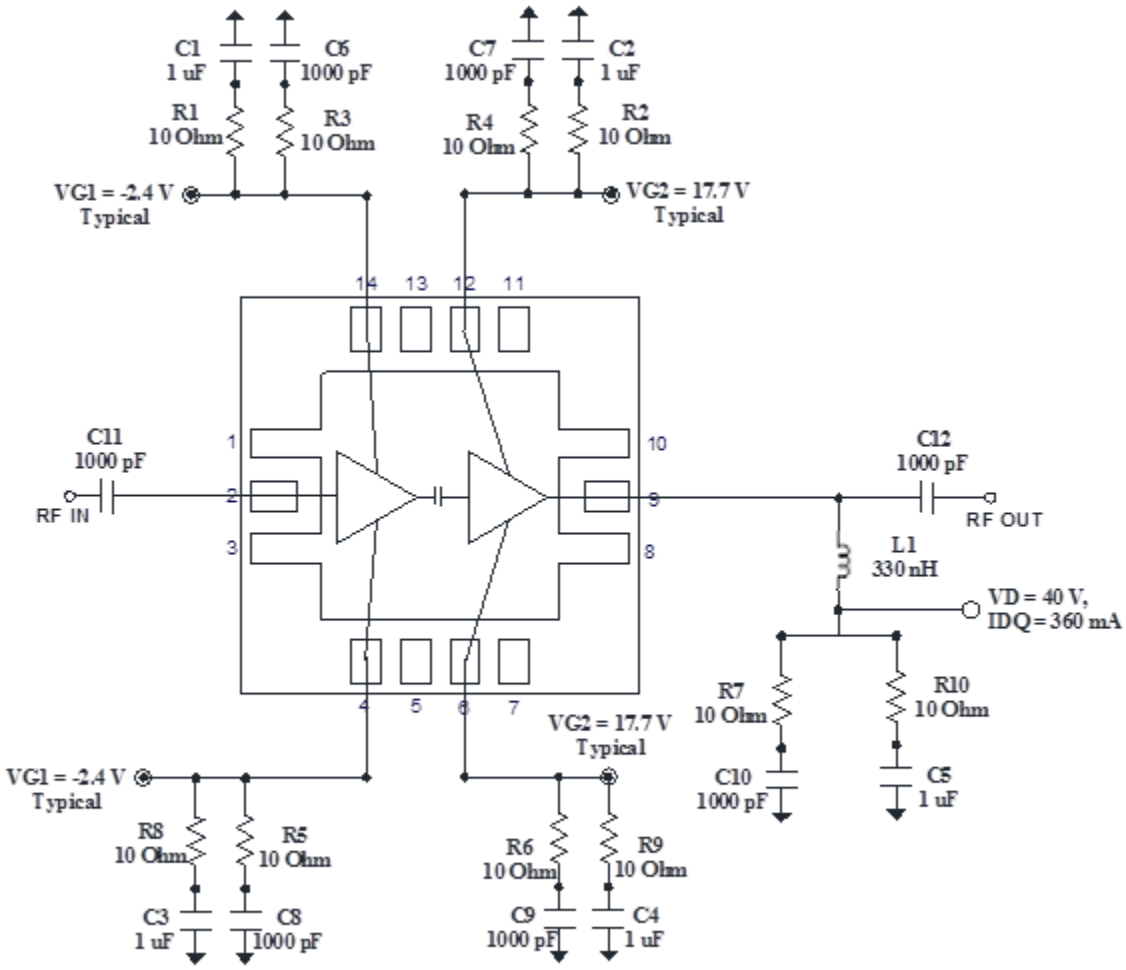
Bill of Materials

Reference Design	Value	Description	Manufacturer	Part Number
C1 – C4	1uF	Cap, 1206, 50V, 5%, X7R	Various	
C6 – C9	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
C11		DC Block	Various	
R1 – R6, R8 – R9	10Ω	Res, 0402, 5%	Various	

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Notes:

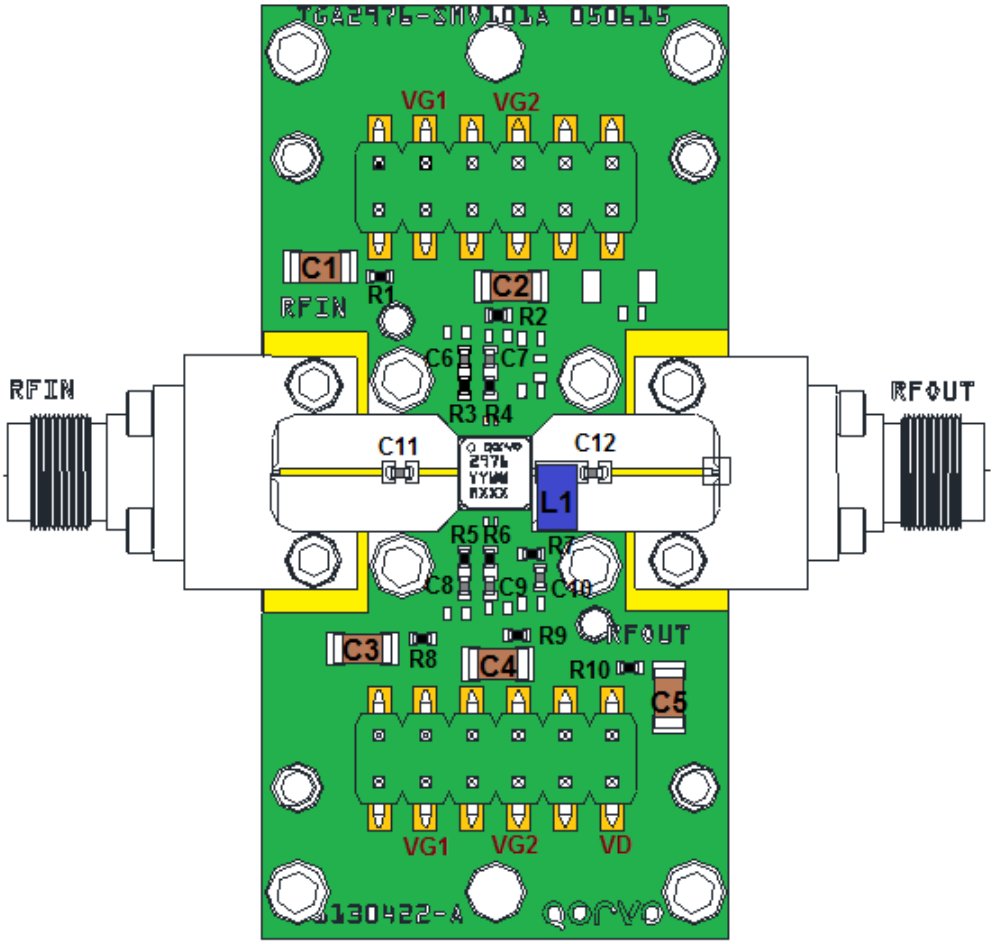
Application Circuit (Option with board-level DC blocks and output bias tee)



1. Performance of the DUT with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.
2. V_{G1} & V_{G2} can be biased from either side (Top or Bottom.)

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Evaluation Board Layout with On-Board DC Blocks and Output Bias-T Option

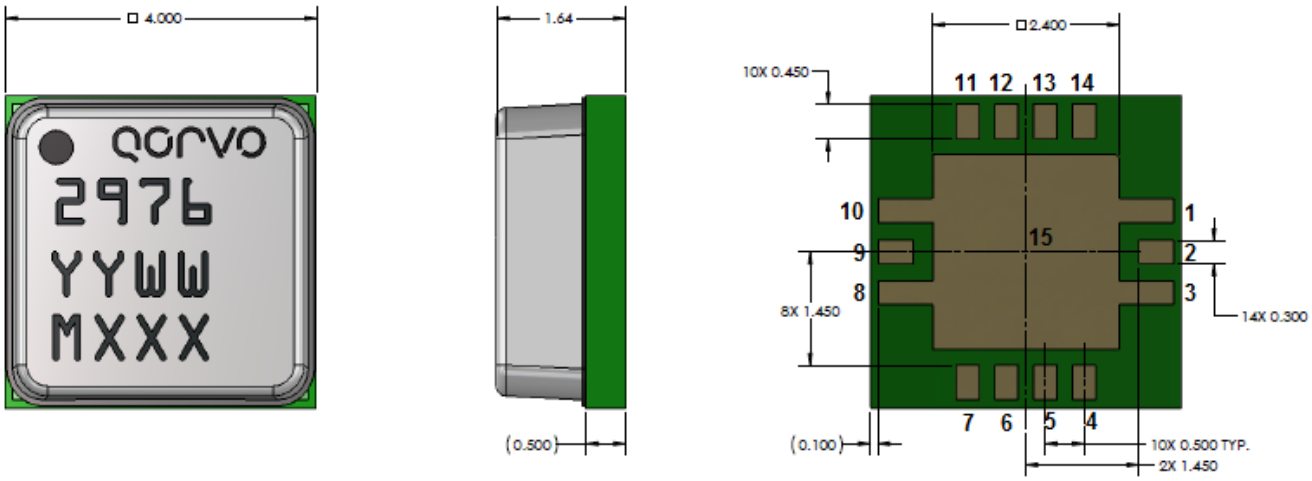


Bill of Materials For On-Board Bias-Tee

Reference Design	Value	Description	Manufacturer	Part Number
C1 – C5	1uF	Cap, 1206, 50V, 15%, X7R		
C6 – C12	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
L1	330nH	Ind, 1206, 850 mA	Various	
R1 – R10	10Ω	Res, 0402, 5%	Various	

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Mechanical drawing and Pin description



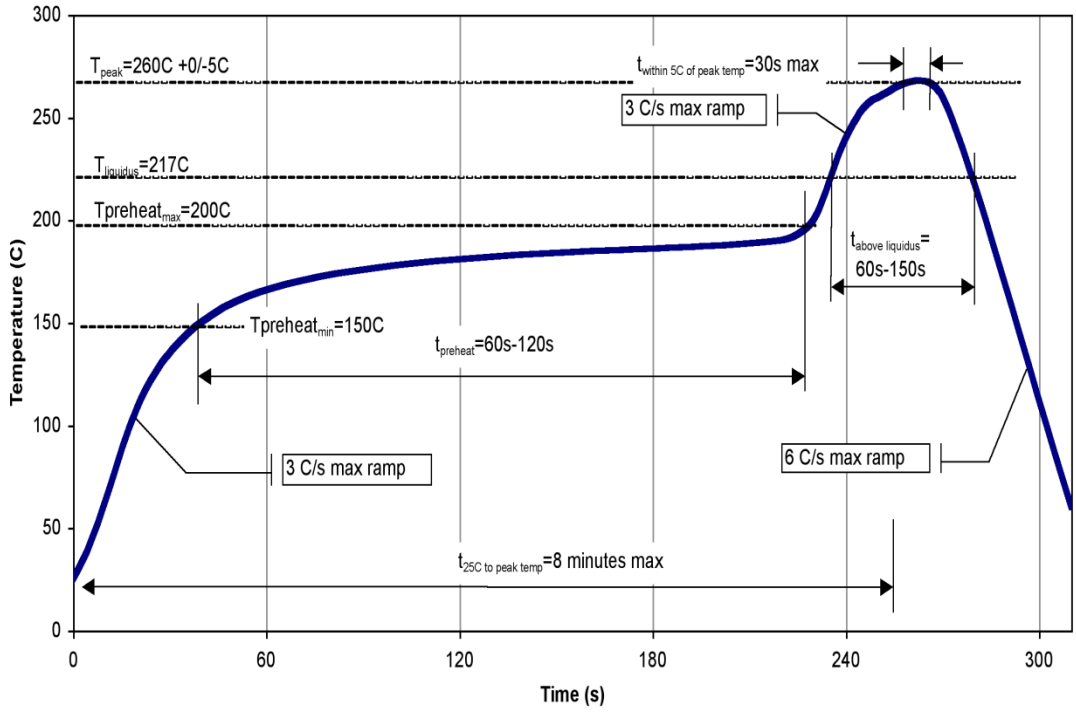
Units: Millimeter
Tolerances: unless specified
x.xx = ± 0.25
x.xxx = ± 0.100
Materials:
Base: Laminate
Lid: Plastic
All metalized features are gold plated
Part is epoxy sealed
Marking:
2976: Part number
YY: Part Assembly year
WW: Part Assembly weak
MXXX: Batch ID

Pin Description

Pin No.	Symbol	Description
1, 3, 8, 10	GND	Connected to ground paddle (pin 15); must be grounded on PCB.
2	RF IN	Input; matched to 50 Ω.
4, 14	GATE1	Gate voltage1; bias network is required; see recommended Application Information on page 12.
5, 7, 11, 13	N/C	
6, 12	GATE2	Gate voltage2; bias network is required; see recommended Application Information on page 12.
9	RF OUT/ DRAIN	Output; matched to 50 Ω.
15	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

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Recommended Soldering Temperature Profile



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Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ECCN

US Department of Commerce: EAR99

Solderability

Compatible with both lead-free (260 °C maximum reflow temperature) and tin/lead (245 °C maximum reflow temperature) soldering processes.

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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