Discontinued Product

DATA SHEET

OKI

MSM60804

PCMCIA Host Adapter

FIRST EDITION

ISSUE DATE : JAN. 1999

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OKI Semiconductor

This version: Jan. 1999

MSM60804

PCMCIA Host Adapter

GENERAL DESCRIPTION

The MSM60804 PCMCIA Host Adapter is a PCMCIA host interface chip capable of controlling two PCMCIA sockets. The MSM60804 is compatible with indutry standard 82365SL functions.

FEATURES

- Functionally compatible with 82365SL
- ISA bus interface
- Compliance with PCMCIA 2.1/JEIDA 4.2
- Mixed-voltage (3.3 V or 5.5 V) operation
- Dual PCMCIA socket interface:208-pin QFP
- 8-bit or 16-bit access supported
- Complies with both MEMORY CARD and I/O CARD
- Range of window setting:
  64KB I/O access space (0-FFFFH)
  64MB memory access space (0-3FFFFFFH) (common, attribute)
- One of IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10,
  IRQ11, IRQ12, IRQ14, IRQ15, and IOCHCK can be allocated to each slot
- Power supply control to each slot is available (5 V card and 3 V card are supported)
- Card power down control
- 4 slots are available by cascade connection
- Package:
  208-pin plastic QFP (QFP208-P-2828-0.50-K4) (Product name:MSM60804GS-K4)

BLOCK DIAGRAM

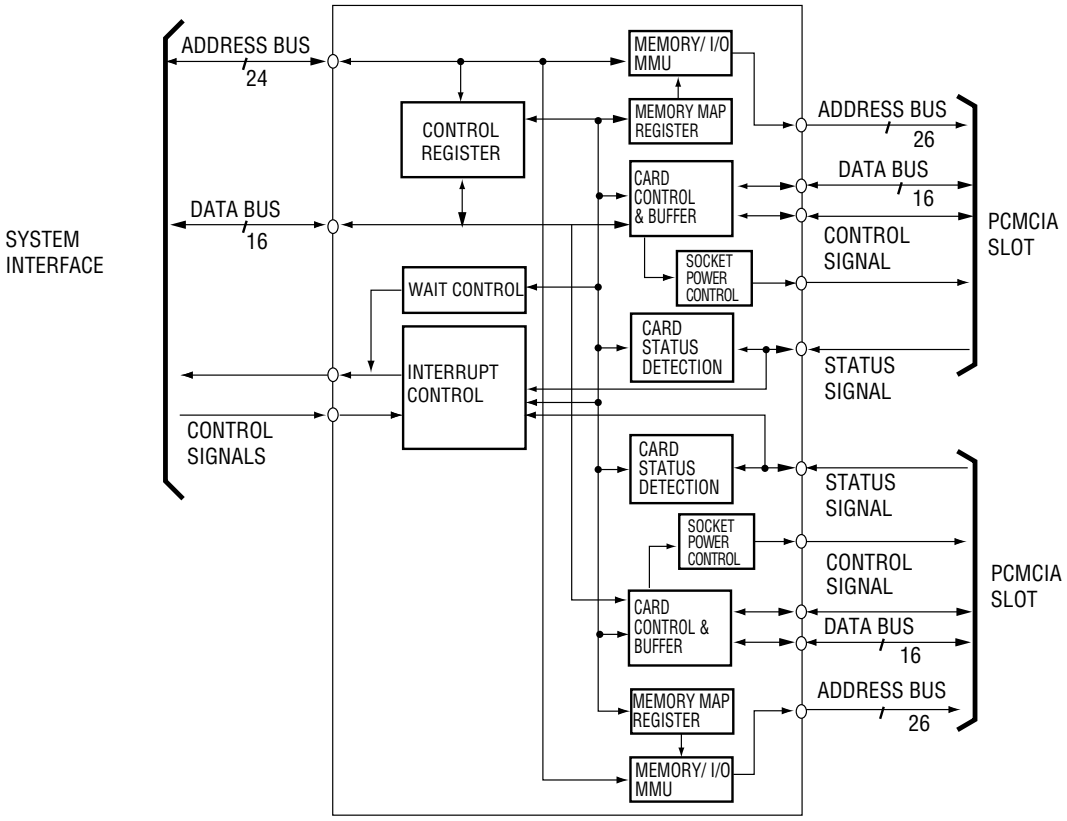
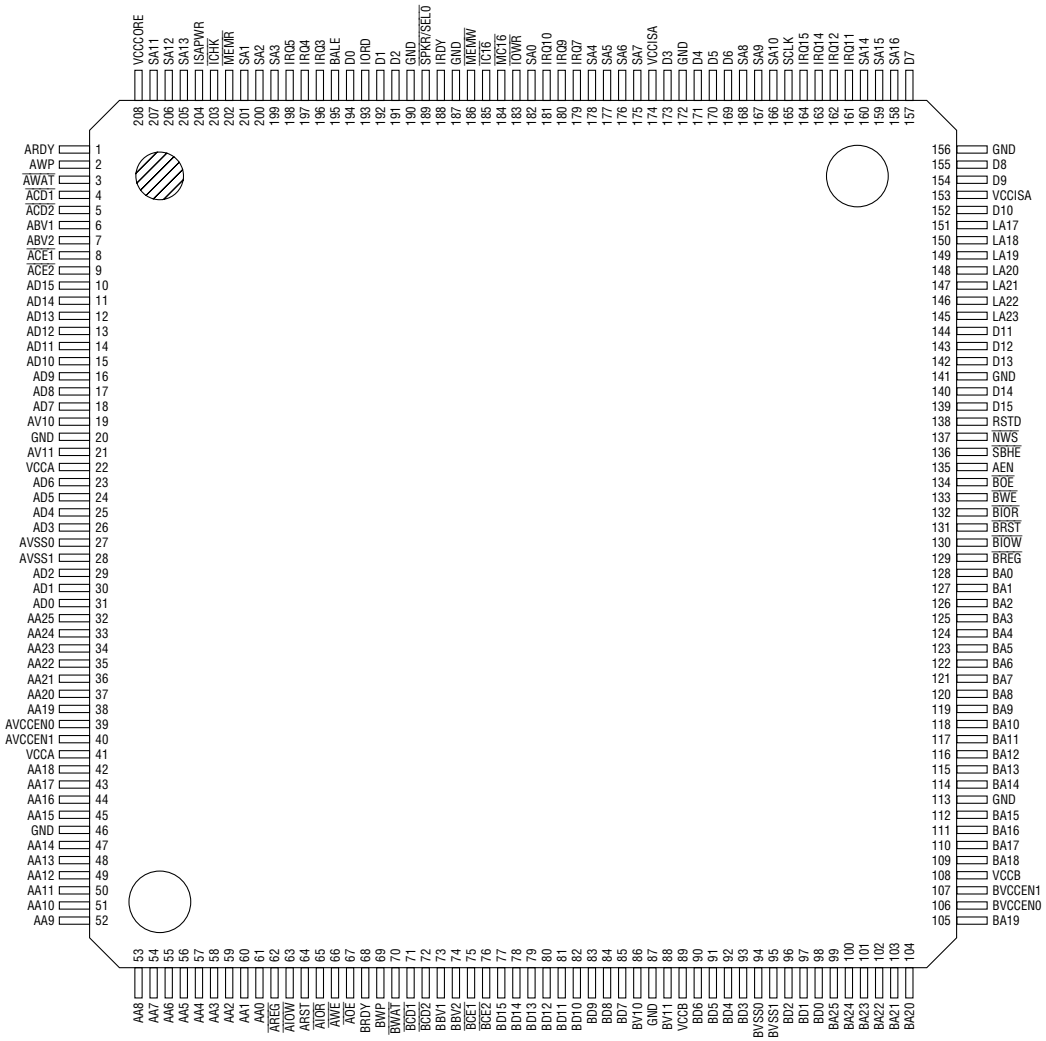


Figure 1 MSM60804 Block Diagram

PIN CONFIGURATION (TOP VIEW)



208-Pin Plastic QFP

Pin List

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1	$\overline{\text{ARDY}}$	31	AD0	61	AA0	91	BD5
2	AWP	32	AA25	62	$\overline{\text{AREG}}$	92	BD4
3	$\overline{\text{AWAT}}$	33	AA24	63	$\overline{\text{AIOW}}$	93	BD3
4	$\overline{\text{ACD1}}$	34	AA23	64	ARST	94	BVSS0
5	$\overline{\text{ACD2}}$	35	AA22	65	$\overline{\text{AIOR}}$	95	BVSS1
6	ABV1	36	AA21	66	$\overline{\text{AWE}}$	96	BD2
7	ABV2	37	AA20	67	$\overline{\text{AOE}}$	97	BD1
8	$\overline{\text{ACE1}}$	38	AA19	68	$\overline{\text{BRDY}}$	98	BD0
9	$\overline{\text{ACE2}}$	39	AVCCEN0	69	BWP	99	BA25
10	AD15	40	AVCCEN1	70	$\overline{\text{BWAT}}$	100	BA24
11	AD14	41	VCCA	71	$\overline{\text{BCD1}}$	101	BA23
12	AD13	42	AA18	72	$\overline{\text{BCD2}}$	102	BA22
13	AD12	43	AA17	73	BBV1	103	BA21
14	AD11	44	AA16	74	BBV2	104	BA20
15	AD10	45	AA15	75	$\overline{\text{BCE1}}$	105	BA19
16	AD9	46	GND	76	$\overline{\text{BCE2}}$	106	BVCCEN0
17	AD8	47	AA14	77	BD15	107	BVCCEN1
18	AD7	48	AA13	78	BD14	108	VCCB
19	AV10	49	AA12	79	BD13	109	BA18
20	GND	50	AA11	80	BD12	110	VA17
21	AV11	51	AA10	81	BD11	111	BA16
22	VCCA	52	AA9	82	BD10	112	BA15
23	AD6	53	AA8	83	BD9	113	GND
24	AD5	54	AA7	84	BD8	114	BA14
25	AD4	55	AA6	85	BD7	115	BA13
26	AD3	56	AA5	86	BV10	116	BA12
27	AVSS0	57	AA4	87	GND	117	BA11
28	AVSS1	58	AA3	88	BV11	118	BA10
29	AD2	59	AA2	89	VCCB	119	BA9
30	AD1	60	AA1	90	BD6	120	BA8

Pin List (continued)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
121	BA7	143	D12	165	SCLK	187	GND
122	BA6	144	D11	166	SA10	188	IRDY
123	BA5	145	LA23	167	SA9	189	$\overline{\text{SPKR}}$/SEL0
124	BA4	146	LA22	168	SA8	190	GND
125	BA3	147	LA21	169	D6	191	D2
126	BA2	148	LA20	170	D5	192	D1
127	BA1	149	LA19	171	D4	193	$\overline{\text{IORD}}$
128	BA0	150	LA18	172	GND	194	D0
129	$\overline{\text{BREG}}$	151	LA17	173	D3	195	BALE
130	$\overline{\text{BIOW}}$	152	D10	174	VCCISA	196	IRQ3
131	BRST	153	VCCISA	175	SA7	197	IRQ4
132	$\overline{\text{BIOR}}$	154	D9	176	SA6	198	IRQ5
133	$\overline{\text{BWE}}$	155	D8	177	SA5	199	SA3
134	$\overline{\text{BOE}}$	156	GND	178	SA4	200	SA2
135	AEN	157	D7	179	IRQ7	201	SA1
136	$\overline{\text{SBHE}}$	158	SA16	180	IRQ9	202	$\overline{\text{MEMR}}$
137	$\overline{\text{NWS}}$	159	SA15	181	IRQ10	203	$\overline{\text{ICHK}}$
138	RSTD	160	SA14	182	SA0	204	ISAPWR
139	D15	161	IRQ11	183	$\overline{\text{IOWR}}$	205	SA13
140	D14	162	IRQ12	184	$\overline{\text{MC16}}$	206	SA12
141	GND	163	IRQ14	185	$\overline{\text{IC16}}$	207	SA11
142	D13	164	IRQ15	186	$\overline{\text{MEMW}}$	208	VCCCORE

PIN DESCRIPTION

Symbol	I/O	Pin Count	Drive Current (mA)	Description
System Interface Pins				
LA [23 : 17] SA [16 : 0]	I	24	—	System Address Bus The address bus lines of host system interface. These lines enable direct addressing of the 16MB memory space on the card. In the Word Access mode, SA0 is not used. These lines are connected to LA[23:17] and SA[16:0] of the 16-bit ISA system.
D [15 : 0]	I/O	16	16	System Data bus The bidirectional 16-bit data bus lines of host system interface. The lower byte D[7:0] is also used to access a register in the PCIC. When the MSM60804 is connected to an 8-bit system, pins of the higher byte are pulled up.
RSTD	I	1	—	System Reset Drive An active-high System Reset signal This signal is used to reset the PCIC and also drive the Base Address Select signal of a register in the PCIC.
ISAPWR	I	1	—	ISA Power Supply This pin selects an interface type of pins connected to the system: high for 5 V TTL interface or low for the other interface type (3 V TTL interface or 5 V/3 V CMOS interface). This pin is internally pulled up.
BALE	I	1	—	Bus Address Latch Enable This pin is active high and used to latch LA[23:17] at the start of bus cycle timing.
SCLK	I	1	—	System Clock A system clock input of the ISA This pin determines $\overline{\text{ICHK}}$ timing and $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ delays in 16-bit accessing. The pulse width of $\overline{\text{ICHK}}$ is three times as wide as the clock cycle. When a bus cycle wait is set by a register, the pulse width of IRDY is equal to one SCLK (1 wait).
$\overline{\text{IOWR}}$	I	1	—	I/O Port Write An active-low I/O Write signal This pin drives data output to an I/O port pointed to by a system address.
$\overline{\text{IORD}}$	I	1	—	I/O Port Read An active-low I/O Read signal This pin drives data input from an I/O port pointed to by a system address.

Symbol	I/O	Pin Count	Drive Current (mA)	Description
System Interface Pins				
$\overline{IC16}$	OD	1	16	16bit I/O Select An active-low signal, indicating the host system that the PC card is in the 16-bit I/O Access mode.
IRDY	OD	1	16	I/O Channel Ready An active high signal, indicating the host system that the memory or I/O bus cycle has completed. While this signal is low, the host system is requested to wait.
$\overline{MEMW}$	I	1	—	System Memory Write An active-low memory write signal This pin drives data output to a PC card pointed to by a system address.
$\overline{MEMR}$	I	1	—	System Memory Read An active-low memory read signal This pin drives data input from a PC card pointed to by a system address.
$\overline{MC16}$	OD	1	16	16-bit Memory Select An active high signal, indicating to the host system that the PC card is in the 16-bit memory access mode.
AEN	I	1	—	System Address Enable
$\overline{SBHE}$	I	1	—	System Bus High Enable An active-low signal, indicating the high byte of the 16-bit system data bus
$\overline{SPKR}$/SEL0	I/O-pu	1	16	Register Base Address Select This pin selects the base address of a register. This pin is driven by a system reset signal (RSTD) and determines the address decode value of a register according to this input when PCICs are connected in a cascade fashion. While resetting is not executed, this pin works as a speaker-out output. (This pin is a bi-directional pin.) The digital audio signal from the card is output through this pin.
$\overline{NWS}$	OD	1	16	No-Wait State An active-low signal, indicates that the PC card executes no-wait accessing This pin is disabled during a 16-bit I/O cycle, and in the other cycle, is enabled by register setting.
IRQ (3-5, 7, 9-12, 14-15)	O	10	2	Interrupt Request An active-high signal, outputting an interrupt request to the host system. Each slot assigns one of the IRQ pins as an interrupt signal.
$\overline{ICHK}$	O	1	2	I/O Channel Interrupt An active-low signal, outputting a non-maskable interrupt request (NMI) to the CPU (maskable by system hardware configuration)

Symbol	I/O	Pin Count	Drive Current (mA)	Description
PCMCIA Card Socket Interface Pins				
$\overline{ACD1}$, $\overline{ACD2}$ $\overline{BCD1}$, $\overline{BCD2}$	I-pu	4	—	Card Detect An active-low signal detecting proper card insertion. The status of this pin is reflected on the contents of registers. The status transition of this pin can be used as an interrupt request by register setting.
ABV1, BBV1 ABV2, BBV2	I-pu	4	—	Battery Voltage Detect These signals are generated by the memory card as an indication of its battery condition. The status of these pins is reflected in the card status register. The status change of these pins is available for an interrupt request using the register. Status Change When I/O interface is selected, BV1 signal is replaced by an active-low card status change ($\overline{STSCHG}$). The status of this pin is reflected in the interface status register. The status change of this pin is available as an interrupt request by the register. Speaker In the I/O PC card, BV2 is replaced as an active-low audio digital wavefrom 1 ($\overline{SPKR}$). It is connected to the speaker out pin ($\overline{SPKR}$ or SEL0) to drive a host speaker.
$\overline{AWAT}$, $\overline{BWAT}$	I-pu	2	—	Bus Cycle Wait An active-low Wait Request signal, requesting a bus cycle wait signal from a PC card to the host system.
ARDY, BRDY	I-pu	2	—	Ready/Busy/Interrupt Request In memory Card mode, this signal is set active high to tell the host system that the memory PC card is ready to accept a next bus cycle. While low, this signal indicates that the memory PC card is busy processing previous bus cycle and not available to execute a next bus cycle. The status of this pin is reflected in the register. The status change of this pin can be used as an interrupt request by reading the interface status register.
AWP, BWP	I-pu	2	—	Write-protect/16-bit I/O-Access In memory Card mode, these pins detect the state of the Write Protect switch of a PC card. This signal, when active high, indicates the memory PC card is write-protected. To make a memory PC card without a Write Protect switch writable, these pins are grounded. To make a memory PC card read-only, these pins are connected to VCC. In I/O Card mode, these pins are active low to indicate 16-bit I/O accessing. ($\overline{IOIS16}$)

Symbol	I/O	Pin Count	Drive Current (mA)	Description
PCMCIA Card Socket Interface Pins				
AA [25 : 0] BA [25 : 0]	TO	52	2	Card Address Bus This bus enables the PCIC to directly access the 64M-byte memory address space on the card.
AD [15 : 0] BD [15 : 0]	I/O	32	2	Card Data Bus A bus for transferring 16-bit data to and from the PC card.
$\overline{ACE1}$, $\overline{ACE2}$ $\overline{BCE1}$, $\overline{BCE2}$	TO	4	2	Card Enable These signals enable setting of 8-bit or 16-bit accessing to the PC card and enable odd-numbered or even-numbered-address bytes. These signals are combined with A0 to determine a method to access the PC card. The $\overline{CE1}$ or $\overline{CE2}$ output is enabled according to the register setting or $\overline{IOIS16}$ setting.
$\overline{AREG}$, $\overline{BREG}$	TO	2	2	Attribute Memory Select When this signal is active low, access is limited to Attribute Memory. When this signal is high, Common Memory Access mode is set. In Common Memory Access mode, accessing to the I/O PC card is disabled.
$\overline{AIOW}$, $\overline{BIOW}$	TO	2	2	I/O Write An active-low signal to enable writing data to the PC card's I/O space. This signal is not available when the $\overline{REG}$ signal is inactive high.
$\overline{AIOR}$, $\overline{BIOR}$	TO	2	2	I/O Read An active-low signal to enable reading data from the PC card's I/O space. This signal is not available when the $\overline{REG}$ signal is inactive high.
$\overline{AWE}$, $\overline{BWE}$	TO	2	2	Write Enable An active-low signal to enable writing data in the PC card. This signal enables writing data in common memory of the memory PC card when the $\overline{REG}$ signal is high or in attribute memory of the I/O PC card or memory PC card when the $\overline{REG}$ signal is low.
$\overline{AOE}$, $\overline{BOE}$	TO	2	2	Output Enable An active-low signal is used to gate control memory read data from the PC card. When the $\overline{REG}$ signal is high, this signal enables reading data from memory of the memory PC card and when the $\overline{REG}$ signal is low from attribute memory of the I/O PC card memory PC card.
ARST, BRST	TO	2	2	Card Reset Active high signals reset the PC cards. These signals are set by PC IC's register.
AVSS1, AVSS0 BVSS1, BVSS0	I-pu	4	—	Voltage Sense Pins These signals indicate the voltages required for the PC card. The values of these signals are reflected to the PCIC register.

Symbol	I/O	Pin Count	Drive Current (mA)	Description
Card Power Supply Control and Power Supply Pins				
AVCCEN0 AVCCEN1 BVCCEN0 BVCCEN1 AV10, AV11 VB10, VB11	O	8	16	Power Supply Control These pins control power supplied to the PC cards and power to the buffer in the card interface of the PCIC. Their values are set by registers.
VCCISA VCCCORE	PW	3	—	System Interface Buffer / Core Power Supply These pins supply power to the buffer and the core on the system interface side. VCCISA and VCCCORE voltages must be equal.
VCCA, VCCB	PW	4	—	Card Interface Buffer Power Supply These pins supply power (of the same voltage as that of power supplied to the card slot) to the buffer on the card interface side.
GND	PW	9	—	Ground
System interface pins: 66 Card interface pins (per slot): 59 Card power supply pins (per slot): 4 Power supply pins: 16 Total number of pins: 208				

TO: Tristate
OD: Open Drain
PU: Pull Up
PW: Power Supply or GRD Pins.

Note: The above drive current values are for 5 V interface. The drive current values for 3 V interface are half of the above values.
The MSM60804 does not support the $\overline{\text{INPAK}}$ signal of the PCMCIA.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C V_{SS} = 0 V		–0.5 to +6.5	V
Input Voltage	V_I			–0.5 to V_{DD} + 0.5	
Output Voltage	V_O			–0.5 to V_{DD} + 0.5	
Input Current	I_I			–10 to +10	mA
Output Current	I_O		2 mA buffer	–25 to +25	
			16 mA buffer	–50 to +50	
Storage Temperature	T_{STG}	—		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	3 V	2.7	3.3	3.6	V
		5 V	4.5	5	5.5	
Operating Temperature	Top		–40	+25	+85	°C
Input Rise and Fall Times	tr, tf		—	2	20	ns

ELECTRICAL CHARACTERISTICS

DC Characteristics

3.3 V Interface

(V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V, Tj = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Level Input Voltage	V_{IH}	TTL Level Input (Note 2)	1.8	—	V_{DD} + 0.5	V
"L" Level Input Voltage	V_{IL}	TTL Level Input (Note 2)	–0.5	—	+0.8	V
"H" Level Output Voltage	V_{OH}	I_{OH} = –1, –8 mA	2.2	—	—	V
"L" Level Output Voltage	V_{OL}	I_{OL} = 1.8 mA	—	—	0.4	V
"H" Level Input Current	I_{IH}	$V_{IH} = V_{DD}$	—	0.01	1	µA
"L" Level Input Current	I_{IL}	$V_{IL} = V_{SS}$	–1	–0.01	—	µA
		$V_{IL} = V_{SS}$ (with 100 kΩ Pull-up)	–120	–35	–5	µA
Three-state Output Leakage Current	I_{OZH}	$V_{OH} = V_{DD}$	—	0.01	1	µA
	I_{OZL}	$V_{OL} = V_{SS}$	–1	–0.01	—	µA
		$V_{OL} = V_{SS}$ (with 100 kΩ Pull-up)	–120	–35	–5	µA
Supply Current (Stand by)	I_{DDS}	Output non-load ($V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$)	—	0.1	10	µA
Supply Current (Operating)	I_{DDO}	Output non-load ($V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$) f = 10 MHz	—	—	20	mA

Note 1 : Typical conditions are V_{DD} = 3.3 V, Tj = 25°C
Note 2 : 1 SA PWR pin should be held "low".
Voltage control register bit 2 should be set to "0".

5.0 V Interface

(V_{DD} = 4.5 V to 5.5 V, V_{SS} = 0 V, Tj = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Level Input Voltage	V_{IH}	TTL Level Input (Note 2)	2.2	—	V_{DD} + 0.5	V
"L" Level Input Voltage	V_{IL}	TTL Level Input (Note 2)	–0.5	—	+0.8	V
"H" Level Output Voltage	V_{OH}	I_{OH} = –2, –16 mA	3.7	—	—	V
"L" Level Output Voltage	V_{OL}	I_{OL} = 2, 16 mA	—	—	0.4	V
"H" Level Input Current	I_{IH}	$V_{IH} = V_{DD}$	—	0.01	10	µA
"L" Level Input Current	I_{IL}	$V_{IL} = V_{SS}$	–1	–0.01	—	µA
		$V_{IL} = V_{SS}$ (with 50 kΩ Pull-up)	–250	–100	–20	µA
Three-state Output Leakage Current	I_{OZH}	$V_{OH} = V_{DD}$	—	0.01	10	µA
	I_{OZL}	$V_{OL} = V_{SS}$	–10	–0.01	—	µA
		$V_{OL} = V_{SS}$ (with 50 kΩ Pull-up)	–250	–100	–20	µA
Supply Current (Stand by)	I_{DDS}	Output non-load ($V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$)	—	0.1	100	µA
Supply Current (Operating)	I_{DDO}	Output non-load ($V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$) f = 10 MHz	—	—	40	mA

Note 1 : Typical conditions are : V_{DD} = 3.3 V, Tj = 25°C
Note 2 : 1 SA PWR pin should be held "High".
Voltage Control register bit 2 should be set to "1".

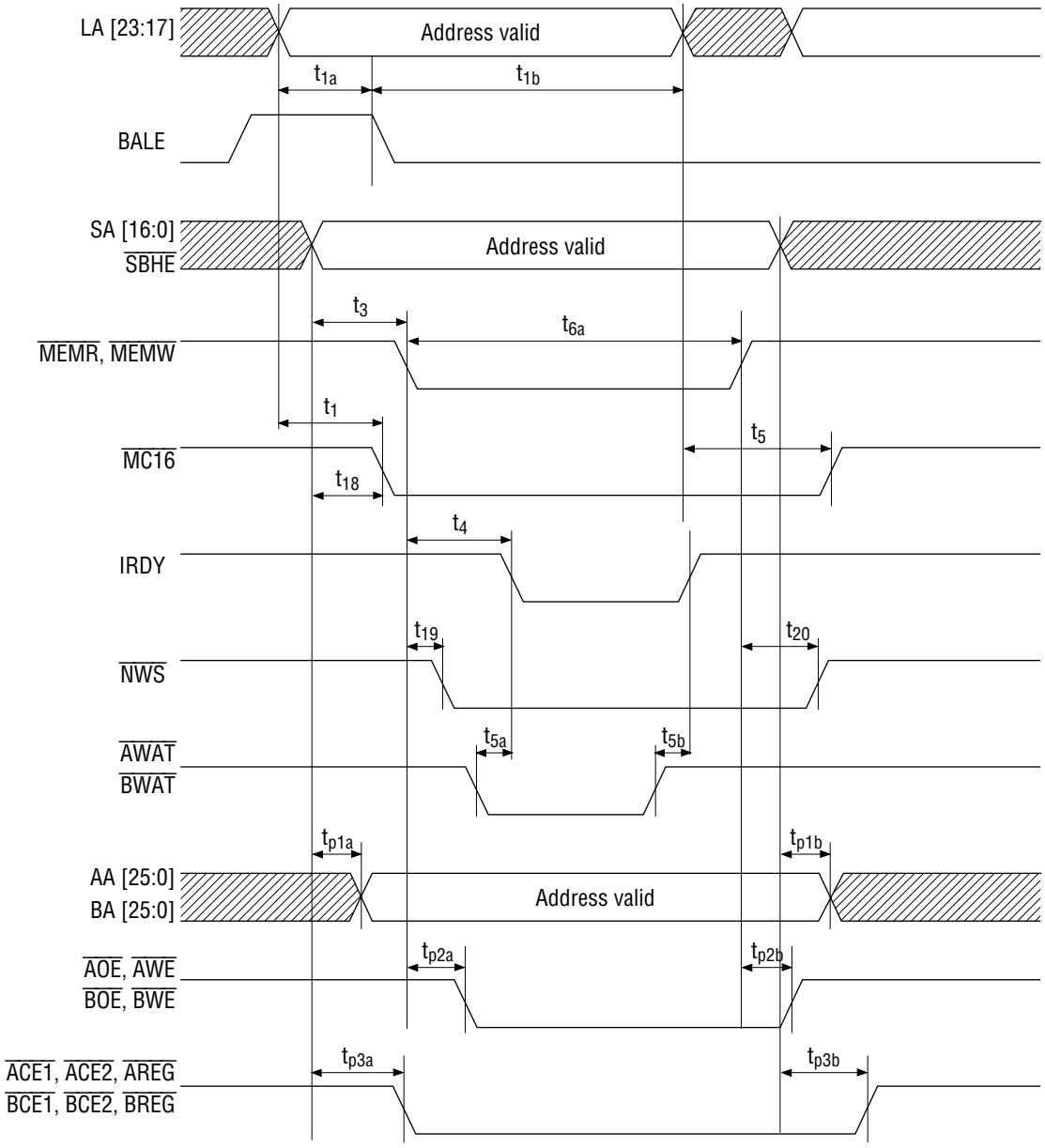
AC Characteristics

AC Timing Conditions

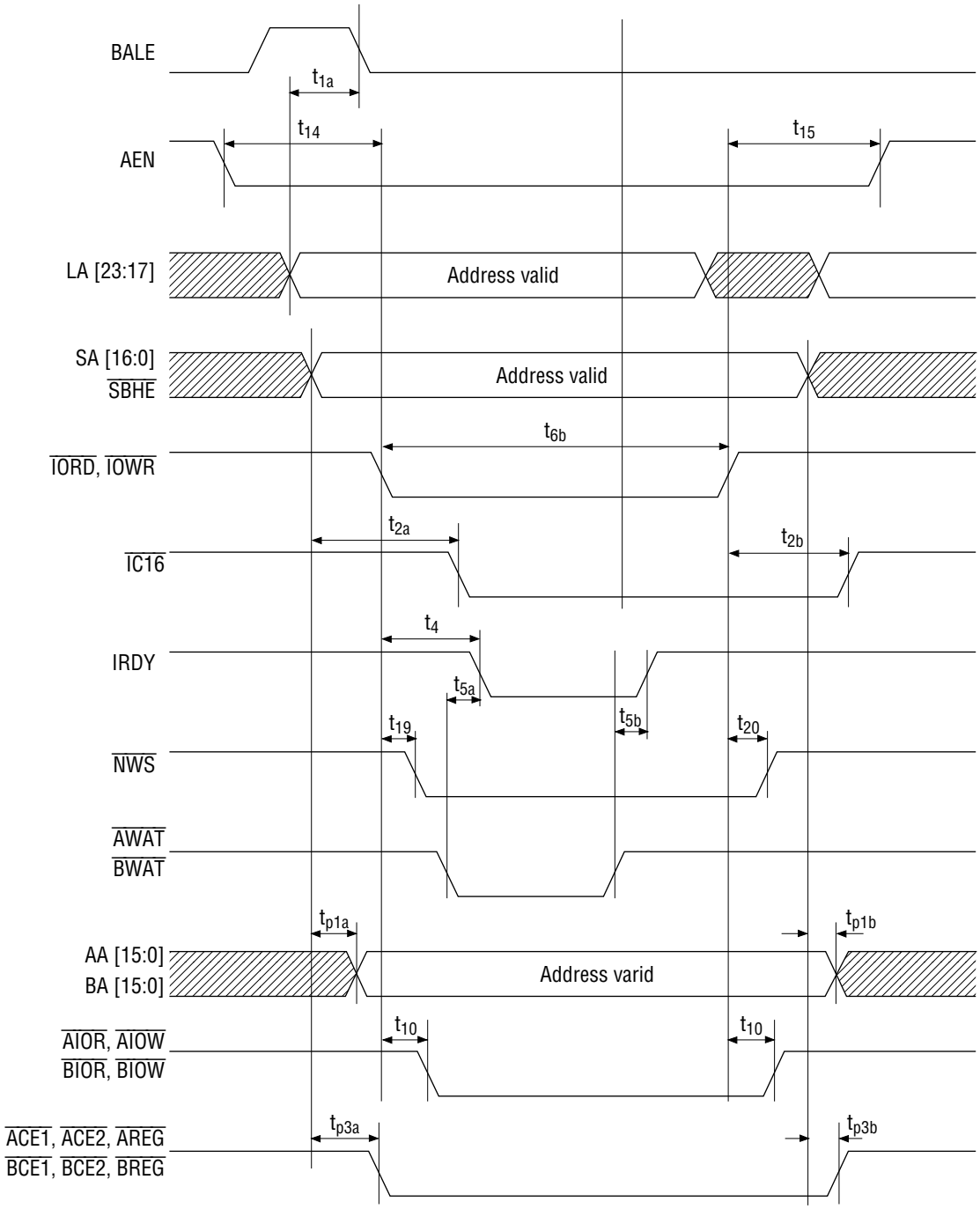
Symbol	Parameter	Min.	Max.	Unit
t_{1a}	LA <23:17> Setup Time to BALE Inactive	20	—	ns
t_{1b}	LA <23:17> Hold Time from BALE Inactive	0	—	
t_1	$\overline{MC16}$ Delay Time from LA <23:17> Valid	30	—	
t_5	$\overline{MC16}$ Delay Time from LA <23:17> Invalid	30	—	
t_3	SA [16:0] Setup Time to Command Active	20	—	
t_{6a}	$\overline{MEMR}$, $\overline{MEMW}$ Pulse Width	100	—	
t_{6b}	$\overline{IORD}$, $\overline{IOWR}$ Pulse Width	100	—	
t_{18}	$\overline{MC16}$ Delay Time from SA [16:0] Active	—	35	
t_{2a}	$\overline{IC16}$ Delay Time from SA [16:0] Active	—	40	
t_{2b}	IC16 Delay Time from Command Inactive	—	30	
t_{19}	$\overline{NWS}$ Delay Time from Command Active	—	25	
t_{20}	$\overline{NWS}$ Delay Time from Command Inactive	—	25	
t_4	Delay Time from Command Active to IRDY Inactive	—	20	
t_{5a}	Delay Time from $\overline{AWAY}$, $\overline{BWAT}$ Active to IRDY Inactive	—	12	
t_{5b}	Delay Time from $\overline{AWAY}$, $\overline{BWAT}$ Inactive to IRDY Active	—	20	
t_{p1a}	AA [25:0], BA [25:0] Delay Time from SA [16:0] Valid	—	55	
t_{p1b}	AA [25:0], BA [25:0] Delay Time from SA [16:0] Invalid	—	55	
t_{p2a}	Delay Time from Command Active to $\overline{OE}$, $\overline{WE}$ Valid	—	55	
t_{p2b}	Hold Time from Command Inactive to $\overline{OE}$, $\overline{WE}$ Valid	—	55	
t_{p3a}	Delay Time from SA [16:0] Valid to $\overline{CE}$, $\overline{REG}$ Valid	—	55	
t_{p3b}	Hold Time from SA [16:0] Invalid to $\overline{CE}$, $\overline{REG}$ Invalid	—	85	
t_{14}	AEN Inactive Setup Time to Command Active	15	—	
t_{15}	AEN Hold Time from Command Inactive	10	—	
t_9	Data Valid Setup Time to $\overline{IOWR}$ Inactive	10	—	
t_{10}	Data Valid Setup Hold Time from $\overline{IOWR}$ Inactive	5	—	
t_{11}	SD [7:0] Data Delay Time from $\overline{IORD}$ Active	—	55	
t_{13}	SD [7:0] Data Hold Time from $\overline{IORD}$ Inactive	—	50	
t_{piola}	IOR, IOW Delay Time from Command	—	45	

TIMING DIAGRAM

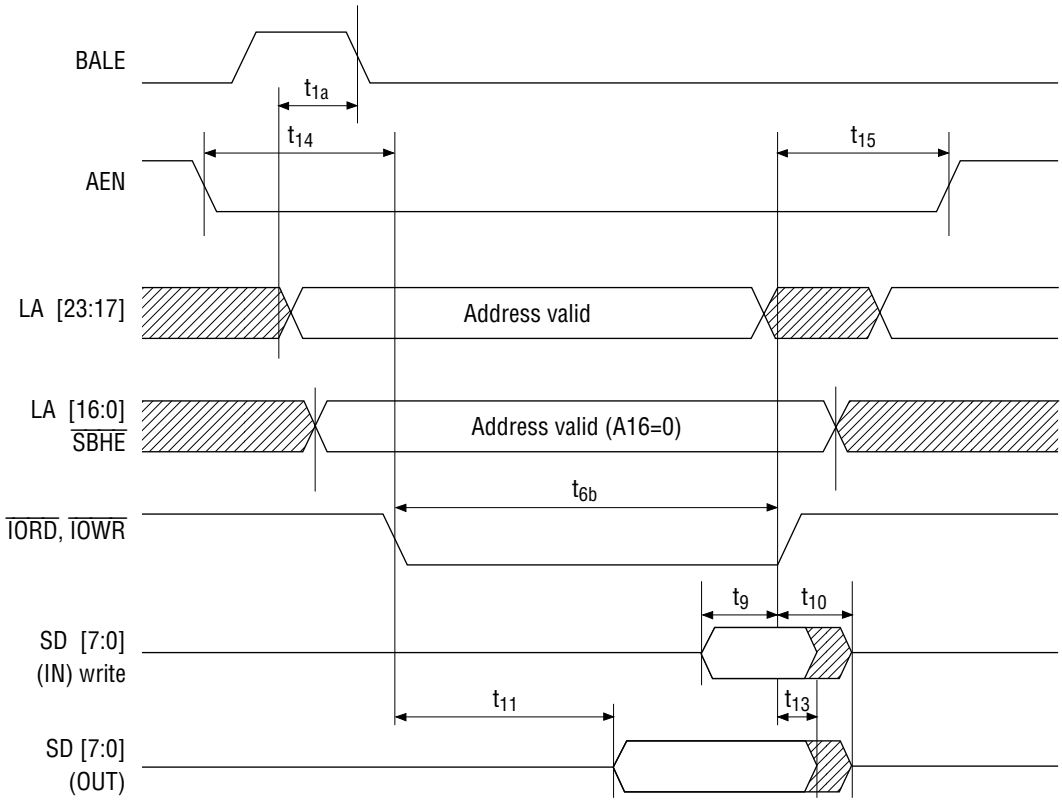
8/16-Bit Memory Cycle



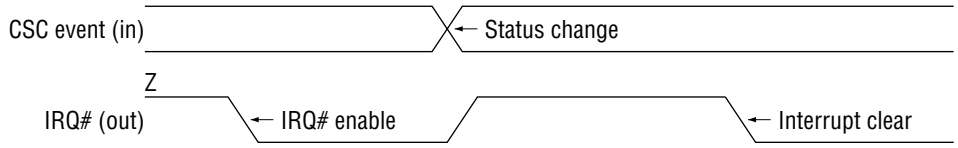
8/16-Bit I/O Cycle



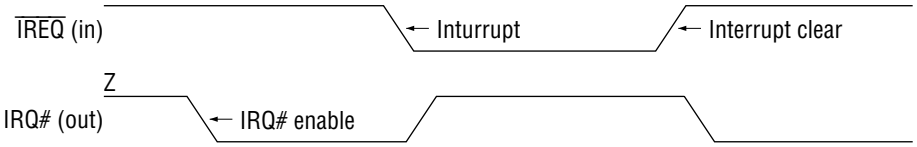
Register Access



Interrupt Request by a card status change

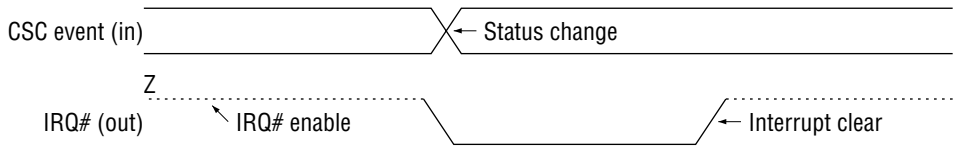


Interrupt Request from I/O card

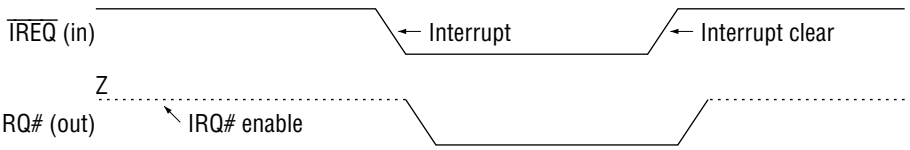


Edge Trigger Mode

Interrupt Request by a card status change



Interrupt request from I/O card



Level Mode

FUNCTIONAL DESCRIPTION

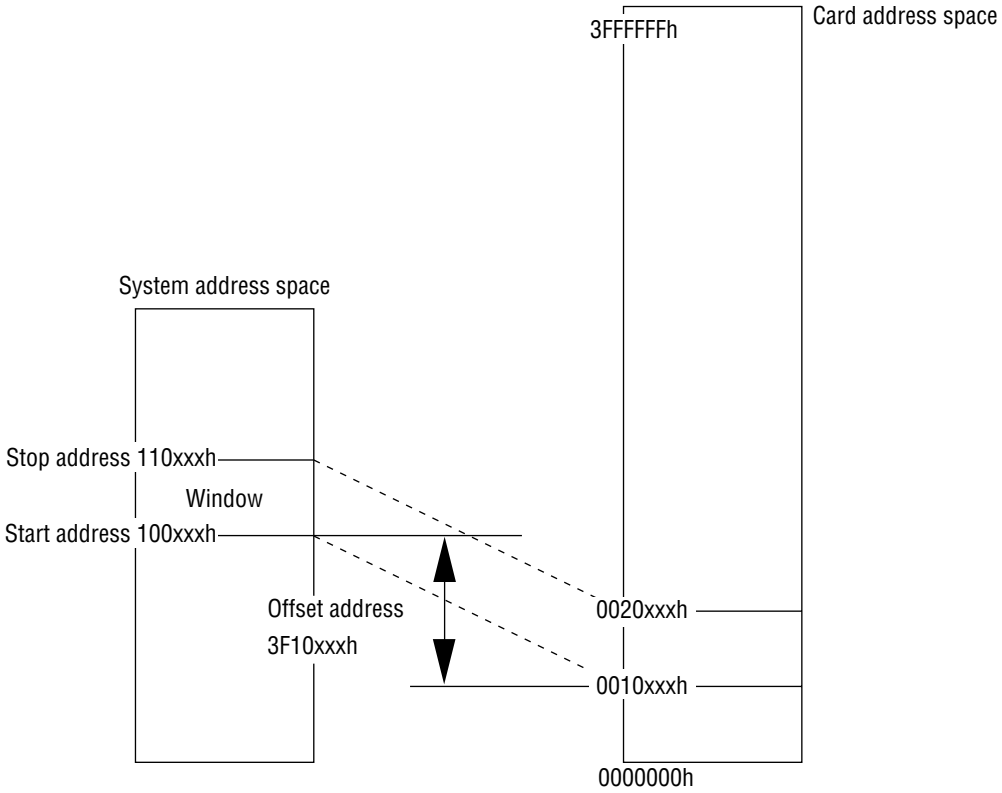
The MSM60804 offers PC card interface which is functionally compatible to the Intel SE82365SL. The MSM60804 supports the ISA on its system interface side and function to control 2 slots of the PCMCIA2.1 or JEIDA.2 on its card interface side. For details of pins and registers, see "Pin Description" and "Register Description".

Power Control

- The MSM60804 supplies 5 V or 3 V power to the PCIC core and to the interface buffer on the system side.
- This power is supplied through the VCCISA and VCCCORE pins.
- The VCCISA voltage must be equal to the VCCCORE voltage.
- The interface buffer on the system side supports 5 V or 3 V CMOS and 5 V or 3 V TTL interface levels.
- The levels are selected by the ISAPWR signal.
- Power supply voltage to the interface buffer on the card side is selected to each slot from either 5 V or 3 V according to the rated voltage of the PC card inserted into each slot.
- Power is supplied to the interface buffer on the card side through the VCCA and VCCB pins.
- Voltages supplied to VCCA and VCCB and voltages supplied to slots are determined by controlling the external power supply circuit by VCCEN0 and VCCEN1.
- The VCCEV0 and VCCEN1 outputs are determined by the voltage control registers (+17h and +57h).
- The voltage of VPP power supplied to card slots are determined by controlling the external supply by the V10 and V11 pins.
- The V10 and V11 outputs are determined by the power control registers (+02h and +42h).

Memory Access

- The memory address space of the PC card supports both attribute memory and common memory (maximum 64M bytes each).
- Attribute memory or common memory is selected by the $\overline{\text{REG}}$ signal.
- The $\overline{\text{REG}}$ signal output is determined by the following two registers:
  Interrupt and General-Purpose Register (+03h or +43h)
  Card Memory Offset Address # High Byte Register
- Accessing to the memory space of the PC card is made through the Memory Address Mapping window.
- The Memory Address Mapping window allocates the following three addresses as shown below:
  System memory mapping start address
  System memory mapping offset address
  Card memory offset address



Memory Window Mapping (Example)

- The above addresses (to each window) are set by the following registers:
  System Memory Address # Mapping Start Low Byte register
  System Memory Address # Mapping Start High Byte register
  System Memory Address # Mapping Stop Low Byte register
  System Memory Address # Mapping Stop High Byte register
  Card Memory Offset Address # Low Byte register
  Card Memory Offset Address # High Byte register
- Up to 16MB can be allocated to a signal Memory Address Mapping window.
- The window size is assigned by 4KB units.
- Five windows can be allocated to each slot.
- Each window is enabled by setting the following register:
  Address Window Enable register (+06h or +46h)
- The MSM60804 supports both 8-bit and 16-bit accessing modes on both systems interface and card interface sides.
- On the system interface side, the 8-bit and 16-bit accessing modes are switched by the $\overline{SBHE}$ signal.
- On the card interface side, the accessing method is determined by combinations of $\overline{CE1}$ and $\overline{CE2}$ signals.
- The values of $\overline{CE1}$ and $\overline{CE2}$ signals are set by A0 and the System Memory Address # Mapping Start High Byte register.

- A wait can be set for a memory access cycle of the PC card.
- A wait can be set for IRDY by a WAIT signal from the card.
- A wait can be set for each system clock cycle by the following register:
  System Memory Address # Mapping Start High Byte register
- The 0-wait state is reported to the $\overline{NWS}$ pin by the following register:
  System Memory Address # Mapping Start High Byte register

I/O Access

- The I/O address space of the PC card is 0 to FFFFh.
- Accessing to an I/O card is enabled by $\overline{REG}$, $\overline{OE}$, and $\overline{WE}$ signals.
- Accessing to the I/O address space of the PC card is made through the I/O Address Mapping window.
- The I/O Address Mapping window allocates the following two addresses:
  I/O address mapping start address
  I/O address mapping stop address
- The above address (for each window) is set by the following registers:
  I/O Address # Mapping Start Low Byte register
  I/O Address # Mapping Start High Byte register
  I/O Address # Mapping Stop Low Byte register
  I/O Address # Mapping Stop High Byte register
- An I/O address space of 0 to FFFh can be allocated to each single I/O address Mapping window.
- The window size is a multiple of 1 byte.
- Two windows can be allocated to each slot.
- Each window is enabled by setting the following register:
  Address Window Enable register (+06h and +46h)
- The MSM60804 supports both 8- bit and 16-bit accessing modes on both system interface and card interface sides.
- On the system interface side, the 8-bit and 16-bit accessing modes are switched by the SBHE signal.
- On the card interface side, the accessing method is determined by combinations of $\overline{CE1}$ and $\overline{CE2}$ signals.
- $\overline{CE1}$ and $\overline{CE2}$ signals are set by A0, IOIS16 and the I/O Control register (+07 and 47h).
- A wait can be set for an I/O access cycle of the PC card.
- A wait can be set for IRDY by a WAIT signal from the card.
- A wait can be set for each system clock cycle by the following register:
  I/O Control register (+07 and +47h)
- The 0-wait state is transferred to the $\overline{NWS}$ pin by the following register:
  I/O Control register (+07 and +47h)

PCIC Register Access

- The MSM60804 provides a 40h register space for each slot.
- The register address of slot A is 3Fh and the register address of slot B is 40h to 7Fh.
- When two MSM60804 chips are cascaded, register addresses are decoded according to the status of the SEL0 signal. Register addresses of slot C and slot D are respectively 80h to BFh and C0h to FFh.

SEL 0	Base Address	Index	Slot
0	0h	0h-3Fh	0 (A)
0	0h	40h-7Fh	1 (B)
1	80h	80h-BFh	2 (A)
1	80h	C0h-FFh	3 (B)

- Accessing to the register address space is indirect addressing through I/O addresses of 3E0h and 3E1h.
- The I/O address 3E0h specifies the register address to be accessed.
- The I/O address 3E1h accesses a register specified by 3E0h.

Selection of Memory Mode or I/O Mode

- The Memory PC Card Access Mode and the I/O PC Card Access mode are switched by register setting.
- A PC card access mode is selected by the following register:
  Interrupt & General Control Register (+03h and +43h)
- Functions of a specific pin of the PCMCIA are switched by mode switching.

Detection of Card Interface Status

- The MSM60804 detects the following seven PC card statuses and reflects them upon register values:
- The seven states are as follows:
  Card detection ($\overline{CD1}$ or $\overline{CD2}$)
  Card Power Supply Active (V10 or V11)
  Voltage Sense (VSS0 or VSS1)
  Ready/Busy (RDY) (for memory cards only)
  Write Protect (WP) (for memory cards only)
  Battery Voltage Detect (BV1 or BV2) (for memory cards only)
  Status Change (BV1) (for I/O mode only)
- The detected state is reflected upon the following two registers:
  Interface Status register (+02h and +42h)
  Voltage Control register (+17h and +57h)

Reset Control

- The MSM60804 is reset by the RSTD signal from the system.
- It is possible to read only the Configuration register when the PC card is removed by setting it on the register.
- Resetting of the Configuration register is enabled by the following register:
  Card Detection & General Control Register (+16h and +56h)
  For configuration registers, see the configuration register list.
- The PC card in each slot can be reset individually by register setting.
- Set the following register to reset the PC card:
  Interrupt & General Control Register (+03h and +43h)

Interrupt Control

- The MSM60804 supports interrupts by the $\overline{\text{IREQ}}$ signals from PC cards and interrupts due to card status changed.
- These interrupts can be assigned to each slot.
- The interrupt by the $\overline{\text{IREQ}}$ signal can be assigned to one of the IRQ pins.
- This assignment is set by the following register:
  Interrupt & General Control Register (+03 and +43h)
- The interrupt due to card status changed can be assigned to one of the IRQ numbers or to $\overline{\text{ICHK}}$.
- This assignment is set by the following registers:
  Interrupt & General Control Register (+03h and +43h)
  Card status Change Interrupt Configuration Register (+05h and +45h)
- Edge triggering or level triggering can be selected.
- This selection is set by the following register:
  General Control register (+1Eh ad +5Eh)

Power-Down Control

- The MSM60804 supports the Power-Down mode. This mode can be set for each slot.
- The Power-Down mode can be set by the following register:
  Voltage Control register (+17h and +57h)

Cascade Connection

- By internal decoding of register address, it is possible to connect two MSM60804 chips in a cascade manner and to support four slots simultaneously.
- When the base address is set by the $\overline{\text{SPKR}}$ or SEL0 input, the register address of the second MSM60804 is assigned to 80h to FFh.

REGISTERS

MSM60804 Register Table

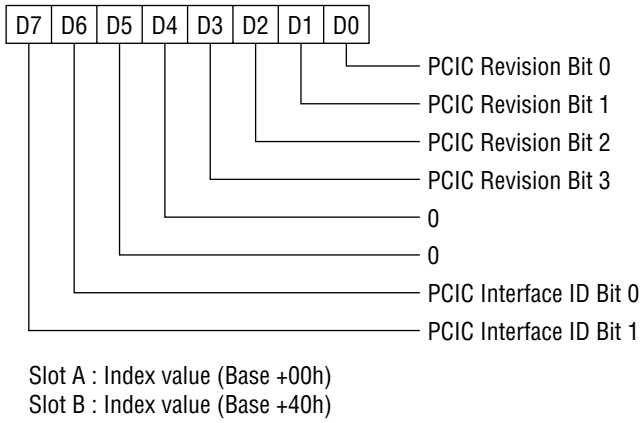
Slot A Offset	Slot B Offset	Register Name
+00h	+40h	Identification and Revision
+01h	+41h	Interface Status
+02h	+42h	Power Control
+03h	+43h	Interrupt and General Control
+04h	+44h	Card Status Change
+05h	+45h	Card Status Change Interrupt Configuration
+06h	+46h	Address Window Enable
+07h	+47h	I/O Control
+08h	+48h	I/O Address 0 Start Low Byte
+09h	+49h	I/O Address 0 Start High Byte
+0Ah	+4Ah	I/O Address 0 Stop Low Byte
+0Bh	+4Bh	I/O Address 0 Stop High Byte
+0Ch	+4Ch	I/O Address 1 Start Low Byte
+0Dh	+4Dh	I/O Address 1 Start High Byte
+0Eh	+4Eh	I/O Address 1 Stop Low Byte
+0Fh	+4Fh	I/O Address 1 Stop High Byte
+10h	+50h	System Memory Address 0 Mapping Start Low Byte
+11h	+51h	System Memory Address 0 Mapping Start High Byte
+12h	+52h	System Memory Address 0 Mapping Stop Low Byte
+13h	+53h	System Memory Address 0 Mapping Stop High Byte
+14h	+54h	Card Memory Offset Address 0 Low Byte
+15h	+55h	Card Memory Offset Address 0 High Byte
+16h	+56h	Card Detect and General Control
+17h	+57h	Voltage Control Register
+18h	+58h	System Memory Address 1 Mapping Start Low Byte
+19h	+59h	System Memory Address 1 Mapping Start High Byte
+1Ah	+5Ah	System Memory Address 1 Mapping Stop Low Byte
+1Bh	+5Bh	System Memory Address 1 Mapping Stop High Byte
+1Ch	+5Ch	Card Memory Offset Address 1 Low Byte
+1Dh	+5Dh	Card Memory Offset Address 1 High Byte
+1Eh	+5Eh	Global Control
+1Fh	+5Fh	Reserved
+20h	+60h	System Memory Address 2 Mapping Start Low Byte
+20h	+61h	System Memory Address 2 Mapping Start High Byte
+22h	+62h	System Memory Address 2 Mapping Stop Low Byte
+23h	+63h	System Memory Address 2 Mapping Stop Low Byte
+24h	+64h	Card Memory Offset Address 2 Low Byte
+25h	+65h	Card Memory Offset Address 2 High Byte

MSM60804 Register Table (continued)

Slot A Offset	Slot B Offset	Register Name
+26h	+66h	Reserved
+27h	+67h	Reserved
+28h	+68h	System Memory Address 3 Mapping Start Low Byte
+29h	+69h	System Memory Address 3 Mapping Start High Byte
+2Ah	+6Ah	System Memory Address 3 Mapping Stop Low Byte
+2Bh	+6Bh	System Memory Address 3 Mapping Stop High Byte
+2Ch	+6Ch	Card Memory Offset Address 3 Low Byte
+2Dh	+6Dh	Card Memory Offset Address 3 High Byte
+2Eh	+6Eh	Reserved
+2Fh	+6Fh	Reserved
+30h	+70h	System Memory Address 4 Mapping Start Low Byte
+31h	+71h	System Memory Address 4 Mapping Start High Byte
+32h	+72h	System Memory Address 4 Mapping Stop Low Byte
+33h	+73h	System Memory Address 4 Mapping Stop High Byte
+34h	+74h	Card Memory Offset Address 4 Low Byte
+35h	+75h	Card Memory Offset Address 4 High Byte
+36h	+76h	OKI Revision
+37h	+77h	Reserved
+38h	+78h	Reserved
+39h	+79h	Reserved
+3Ah	+7Ah	Reserved
+3Bh	+7Bh	Reserved
+3Ch	+7Ch	Reserved
+3Dh	+7Dh	Reserved
+3Eh	+7Eh	Reserved
+3Fh	+7Fh	Reserved

PCIC Revision Register

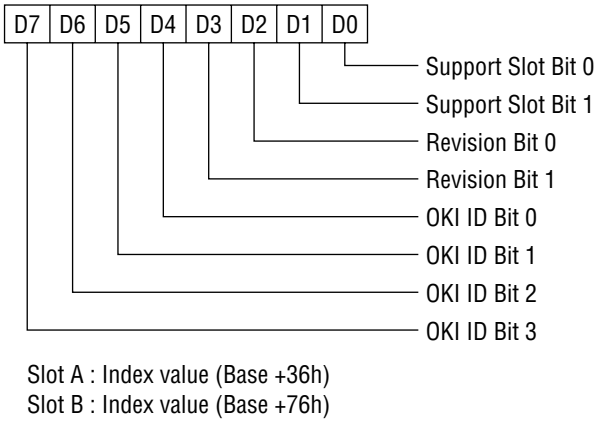
The Identification and Revision Register, as shown below is for read purposes only. 83h can be read from the Identification and Revision Register, similar to the 82365SL (Step B).



Identification and Revision Register (Read Only)

OKI Revision Register

The OKI revision register, as shown below, is for read purposes only.



OKI Revision Register (Read Only)

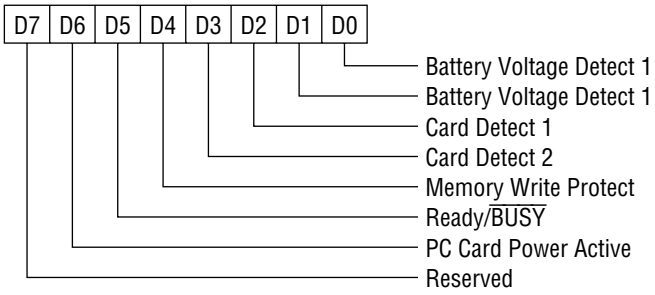
The OKI Revision Register shows the ID number of an OKI chip (B2h), as shown below.

OKI Revision Register

Bits	Values
ID	1011
Revision	00
Support Slot	10

Interface Status Register

The Interface Status Register is shown below. The bits are defined below.



Slot A : Index value (base + 01h)
Slot B : Index value (base + 41h)

Interface Status Register (Read Only)

Interface Status Register Description

D Bits	Description
Bit 6	PC Card Power Active. When set to "1", this bit indicates that V_{PP1} and V_{PP2} are active. When set to "0", this bit indicates that V_{PP1} and V_{PP2} are inactive.
Bit 5	Ready/$\overline{\text{BUSY}}$. When set to "1", this bit indicates that RDY/$\overline{\text{BSY}}$ is active (RDY/$\overline{\text{BSY}}$ = "1"). When set to "0", this bit indicates that RDY/$\overline{\text{BSY}}$ is inactive (RDY/$\overline{\text{BSY}}$ = "0").
Bit 4	Memory Write Protect. When set to "1", this bit indicates that WP is active (WP = "1"). When set to "0", this bit indicates that WP is inactive (WP = "0").
Bit 3	Card Detect 2. When set to "1", this bit indicates that $\overline{\text{CD2}}$ is active ($\overline{\text{CD2}}$ = "0"). When set to "0", this bit indicates that $\overline{\text{CD2}}$ is inactive ($\overline{\text{CD2}}$ = "1").
Bit 2	Card Detect 1. When set to "1", this bit indicates that $\overline{\text{CD1}}$ is active ($\overline{\text{CD1}}$ = "0"). When set to "0", this bit indicates that $\overline{\text{CD1}}$ is inactive ($\overline{\text{CD1}}$ = "1").
Bit 1	Battery Voltage Detect 2. When set to "1", this bit indicates that BVD2 is active (BVD2 = "1"). When set to "0", this bit indicates that BVD2 is inactive (BVD2 = "0"). In the case of ID Card Mode, this bit indicates the $\overline{\text{SKPR}}$ status.
Bit 0	Battery Voltage Detect 1. When set to "1", this bit indicates that BVD1 is active (BVD1 = "1"). When set to "0", this bit indicates that BVD1 is inactive (BVD1 = "0"). In the case of ID Card Mode, this bit indicates the $\overline{\text{STSCHG}}$ status.

The output statuses of CD1 and CD2 signals are shown below

Output Status of CD1 and CD2 Signals

$\overline{CD1}$	$\overline{CD2}$	Status
0	0	The card is inserted
0	1	The card has been taken out
1	0	The card has been taken out
1	1	The card has been completely removed (used for resetting)

BV1 and BV2 signals show the Memory Card Battery Status. Signals and the corresponding battery status are shown below.

Corresponding Status

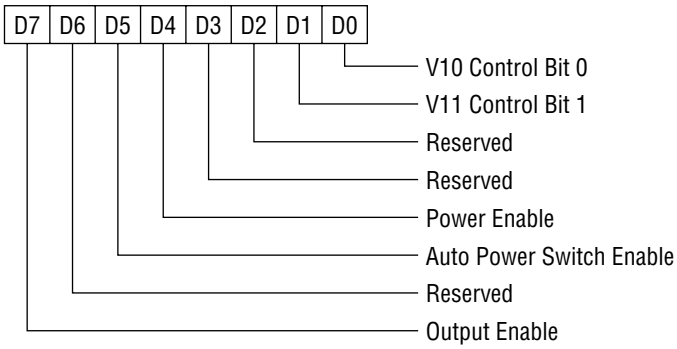
BV1	BV2	Status
0	0	Battery dead
0	1	Battery dead
1	0	Battery warning
1	1	Battery good

Card Power Control

The Card Power Control Function Block controls V10 and V11.

Power Control Register

The Power Control Register is shown below.



Slot A : Index value (base+02h)
Slot B : Index value (base+42h)

Power Control Register (Read/Write)

Output Enable and Power Active States

Power Control register			Card Detection		Tri-state	Bit 6 of Interface Status
bit 7	bit 5	bit 4	$\overline{CD1}$	$\overline{CD2}$	Output	Register (+01h)-bit 6
×	×	0	×	×	OFF	0
0	×	1	0	0	OFF	1
1	×	1	0	0	ON	1
×	0	1	×	1	OFF	1
×	0	1	1	×	OFF	1
×	1	1	×	1	OFF	0
×	1	1	1	×	OFF	0

*A [25:0], $\overline{CE1}$, $\overline{CE2}$, $\overline{IORD}$, $\overline{IOWR}$, $\overline{OE}$, $\overline{REG}$, RST, $\overline{WE}$

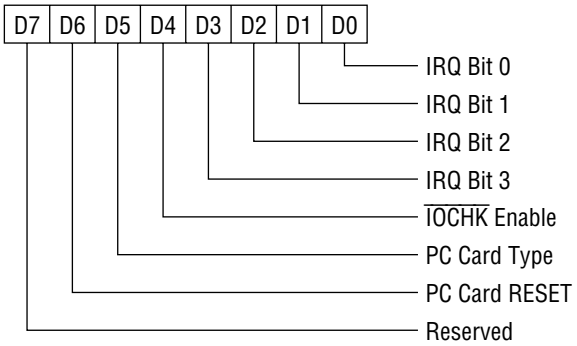
Below are explained the relationships between the states of V10 and V11 and power control bits (bit 0 and bit 1) and bit 6 of the Interface Status register (+01h).

V10, V11 Control

+01h (bit 6)	Bit 1	Bit 0	V_{11}	V_{10}
1	×	×	0	0
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	0

Interrupt and General Control Register

The Interrupt and General Control Registers is shown below.



Slot A : Index value (base+03h)
Slot B : Index value (base+43h)

Interrupt and General Control Register (Read/Write)

RESET Signal PC Card Register Description

Bits	Description
Bit 6	PC Card Reset When this bit is set to "0", a PC Card Reset signal is output.
Bit 5	PC Card Type When this bit is set to "1", the I/O Card mode is enabled. When this bit is set to "0", the Memory Card mode is enabled.
Bit 4	$\overline{\text{ICHK}}$ Enable When this bit is set to "1", the Status Change interrupt is output to the $\overline{\text{ICHK}}$ pin. See "Card Status Change Interrupt Configuration registers".

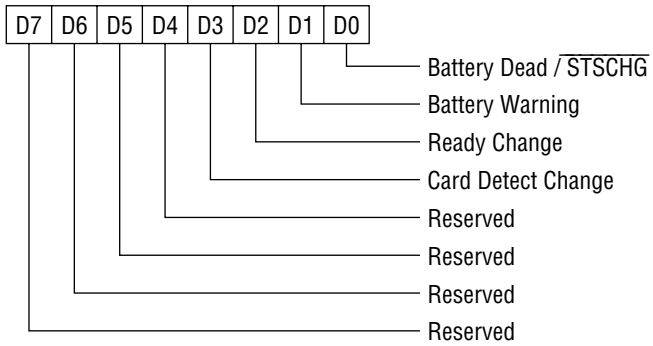
IRQ bits (bit 0 to bit 3) determine the output pin to which an interrupt due to IREQ (RDY/BSY pin is the I/O mode) will be output. See the table below.

$\overline{\text{IREQ}}$ Level Selected by Interrupt General Control Register

IRQ Bit 3	IRQ Bit 2	IRQ Bit 1	IRQ Bit 0	IREQ Level
0	0	0	0	Not selected
0	0	0	1	Not selected
0	0	1	0	Not selected
0	0	1	1	IRQ3
0	1	0	0	IRQ4
0	1	0	1	IRQ5
0	1	1	0	Not selected
0	1	1	1	IRQ7
1	0	0	0	Not selected
1	0	0	1	IRQ9
1	0	1	0	IRQ10
1	0	1	1	IRQ11
1	1	0	0	IRQ12
1	1	0	1	Not selected
1	1	1	0	IRQ14
1	1	1	1	IRQ15

Card Status Change Register

The Card Status Change Register indicates the cause of an interrupt, as shown below. The bits are defined below.



Slot A : Index value (base+04h)
Slot B : Index value (base+44h)

Card Status Change Register (Read/Write)

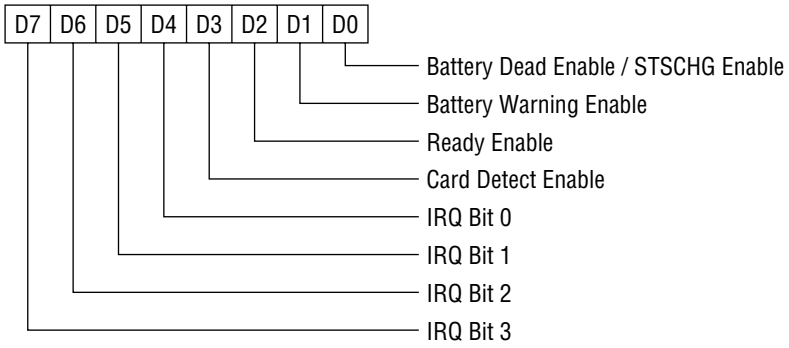
Card Status Change Register Description

Bits	Description
Bit 3	Card Detect Change. When set to "1", this bit indicates CD1 and CD2 Signal Status Change (L↔H).
Bit 2	Ready Change. When set to "1", this bit indicates a RDY/$\overline{BSY}$ Signal Change(L→H).
Bit 1	Battery Warning. When set to "1", this bit indicates a Battery Warning Status Change (Good→Warning, Dead→Warning).
Bit 0	Battery Dead. When set to "1", this bit indicates a Battery Dead Status Change (Good→Dead, Warning→Dead). Note that a $\overline{STSCHG}$ signal status change has taken place in I/O Card mode.

When the card status change explicit write back notification bit of the general control register (+1Eh, +5Eh) is "0", the contents of the register are cleared and the interrupt is canceled, by reading this register.

Card Status Change Interrupt Configuration Register

The Card Status Change Interrupt Configuration Register is shown below. The bits are defined below.



Slot A : Index value (base +05h)
Slot B : Index value (base +45h)

Card Status Interrupt Configuration Register (Read/Write)

Card Status Interrupt Configuration Register Description

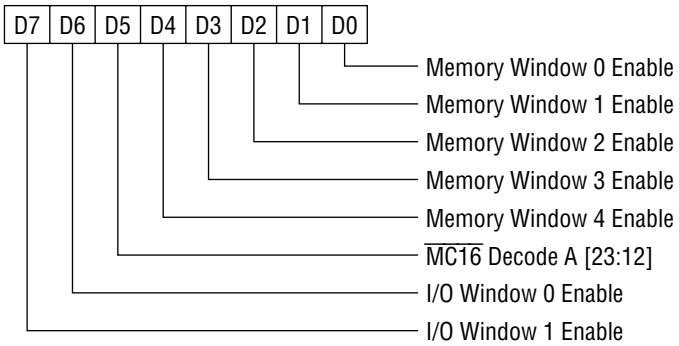
Bits	Description
Bit 3	Card Detect Enable. When set to "1", this bit enables an interrupt by CD1 and CD2 status change. When set to "0", this bit disables an interrupt by CD1 and CD2 status change common to both memory and I/O modes.
Bit 2	Ready Enable. In the memory mode, when set to "1", this bit enables an interrupt to RDY/$\overline{\text{BSY}}$ (L↔H). When set to "0", this bit disables an interrupt to RDY/$\overline{\text{BSY}}$ (L↔H).
Bit 1	Battery Warning Enable. In the memory mode, when set to "1", this bit enables an interrupt to Battery Warning State(Good→Warning, Dead→Warning). When set to "0", this bit disables an interrupt to Battery Warning State (Good→Warning, Dead→Warning).
Bit 0	Battery Dead Enable. In the memory mode, when set to "1", this bit enables an interrupt to Battery Dead State (Good→Dead, Warning→Dead) and also enables an interrupt to the $\overline{\text{STSCHG}}$ Signal Status Change in I/O card mode. When set to "0", this bit disables Battery State interrupt $\overline{\text{STSCHG}}$ change interrupt.

IRQ bits 0 to 3 set the IRQ Level selection as follows. When $\overline{\text{ICHK}}$ Enable Bit is "1", $\overline{\text{ICHK}}$ interrupt signal is selected independently of IRQ Bits setting.

$\overline{\text{ICHK}}$ Enable Bit	IRQ Bit 3	IRQ Bit 2	IRQ Bit 1	IRQ Bit 0	IRQ Level
0	0	0	0	0	Not selected
0	0	0	0	1	Not selected
0	0	0	1	0	Not selected
0	0	0	1	1	IRQ3
0	0	1	0	0	IRQ4
0	0	1	0	1	IRQ5
0	0	1	1	0	Not selected
0	0	1	1	1	IRQ7
0	1	0	0	0	Not selected
0	1	0	0	1	IRQ9
0	1	0	1	0	IRQ10
0	1	0	1	1	IRQ11
0	1	1	0	0	IRQ12
0	1	1	0	1	Not selected
0	1	1	1	0	IRQ14
0	1	1	1	1	IRQ15
1	×	×	×	×	$\overline{\text{ICHK}}$

Address Window Enable Register

The Address Window Enable Register is shown below. The bits are defined below.



Slot A : Index value (base+06h)
Slot B : Index value (base+46h)

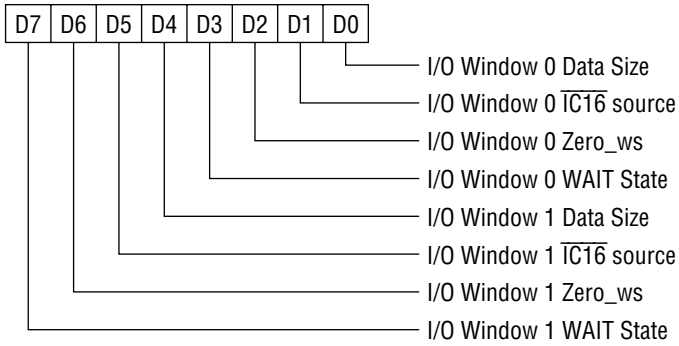
Address Window Enable Register (Read/Write)

Address Window Enable Register Description

Bits	Description
Bit 7	I/O Window 1 Enable. When set to "1", this bit enables the I/O Window 1.
Bit 6	I/O Window 0 Enable. When set to "1", this bit enables the I/O Window 0.
Bit 5	$\overline{MC16}$ Decode A [23:12] When this bit is set to "1", SA [23:12] is decoded into an $\overline{MC16}$ signal. When this bit is set to "0", LA [23:17] is decoded into an $\overline{MC16}$ signal.
Bit 4	Memory Window 4 Enable When this bit is set to "1", memory window 4 is enabled.
Bit 3	Memory Window 3 Enable When this bit is set to "1", memory window 3 is enabled.
Bit 2	Memory Window 2 Enable When this bit is set to "1", memory window 2 is enabled.
Bit 1	Memory Window 1 Enable When this bit is set to "1", memory window 1 is enabled.
Bit 0	Memory Window 0 Enable When this bit is set to "1", memory window 0 is enabled.

I/O Control Register

The I/O Control Register is shown below. The bits are defined below.



Slot A : Index value (base+07h)
Slot B : Index value (base+47h)

I/O Control Register (Read/Write)

I/O Control Register Description

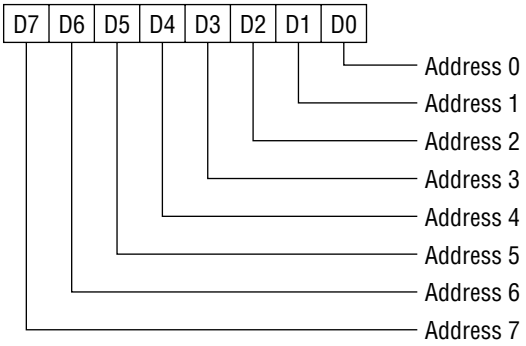
Bits	Description
Bit 7/Bit 3	I/O Window 1 WAIT State/ I/O Window 0 WAIT State. When these bits are set to "1" and a 16-bit I/O access is carried out, an IRDY signal is made low for 1 SCLK cycle as a 1 wait request. It is invalid in 8-bit I/O access.
Bit 6/Bit 2	I/O Window 1 Zero wait state I/O Window 0 Zero wait state. When these bits are set to "1" and an 8-bit I/O access is carried out, NWS signal is effective.
Bit 5/Bit 1	I/O Window $\overline{IC16}$ Source I/O Window 0 $\overline{IC16}$ Source. When these bits are set to "1", an IC16 signal is generated from an $\overline{IOIS16}$ signal:when these bits are set to "0", an $\overline{IC16}$ signal is generated from bit 4/bit 0.
Bit 4/Bit 0	I/O Window 1 Data Size I/O Window 0 Data Size. When these bits are set to "1", a 16-bit access is enabled: when these bits are set to "0", an 8-bit access is enabled.

CE1, CE2 and Output Control

bit 1, 5	bit 0, 4	$\overline{IOIS16}$	$\overline{SBHE}$	A0	$\overline{CE1}$	$\overline{CE2}$	$\overline{IS16}$
0	1	×	0	0	0	0	0
0	1	×	0	1	1	0	0
0	1	×	1	×	0	1	0
0	0	×	×	×	0	1	1
1	×	0	0	0	0	0	0
1	×	0	0	1	1	0	0
1	×	0	1	×	0	1	0
1	×	1	×	×	0	1	1

I/O Address # Start Low Byte Register

The I/O Address # Start Low Byte Register is shown below.

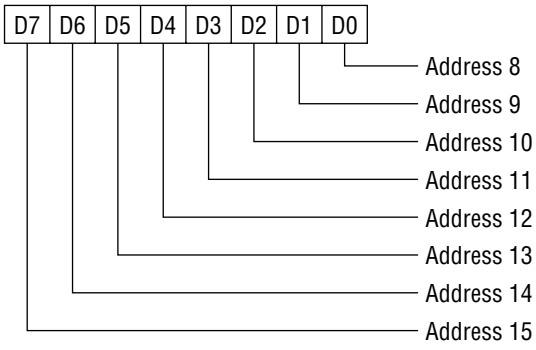


Slot A : Window 0 index value (base + 08h)
Slot A : Window 1 index value (base + 0Ch)
Slot B : Window 0 index value (base + 48h)
Slot B : Window 1 index value (base + 4Ch)

I/O Address # Start Low Byte Register (Read/Write)

I/O Address # Start High Byte Register

The I/O Address # Start High Byte Register is shown below.

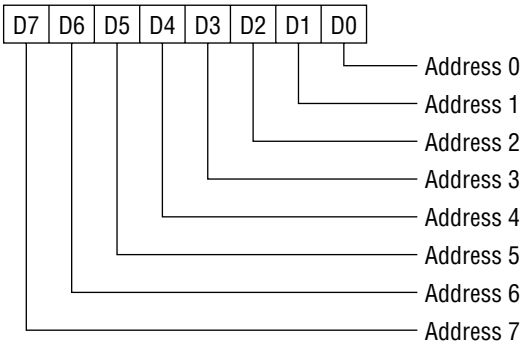


Slot A : Window 0 index value (base + 09h)
Slot A : Window 1 index value (base + 0Dh)
Slot B : Window 0 index value (base + 49h)
Slot B : Window 1 index value (base + 4Dh)

I/O Address # Start High Byte Register (Read/Write)

I/O Address # Stop Low Byte Register

The I/O Address # Stop Low Byte Register is shown below.

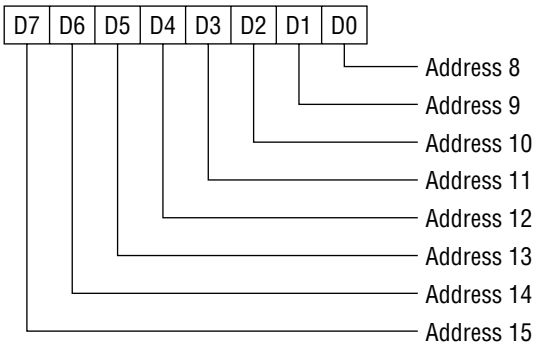


Slot A : Window 0 index value (base +0Ah)
Slot A : Window 1 index value (base +0Eh)
Slot B : Window 0 index value (base +4Ah)
Slot B : Window 1 index value (base +4Eh)

I/O Address # Stop Low Byte Register (Read/Write)

I/O Address # Start High Byte Register

The I/O Address # Start High Byte Register is shown below.

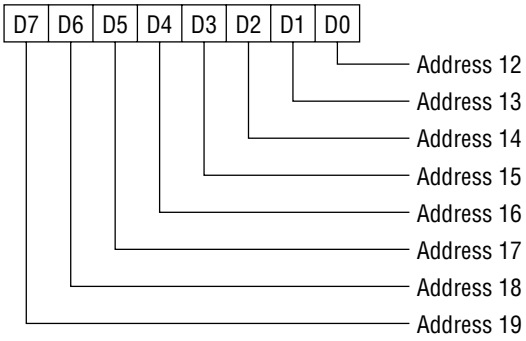


Slot A : Window 0 index value (base +0Bh)
Slot A : Window 1 index value (base +0Fh)
Slot B : Window 0 index value (base +4Bh)
Slot B : Window 1 index value (base +4Fh)

I/O Address # Stop High Byte Register (Read/Write)

System Memory Address # Mapping Start Low Byte Register

The system Memory Address # Mapping Start Low Byte Register is shown below.

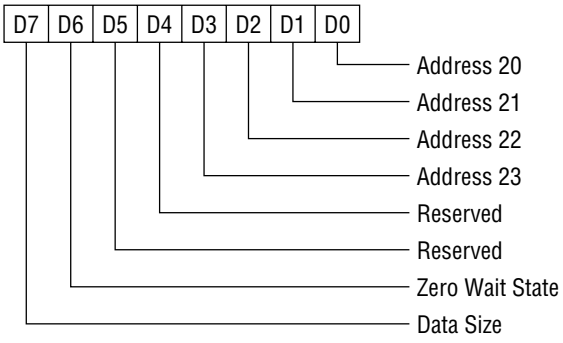


Slot A: Window 0 index value (base + 10h)
Slot A: Window 1 index value (base + 18h)
Slot A: Window 2 index value (base + 20h)
Slot A: Window 3 index value (base + 28h)
Slot A: Window 4 index value (base + 30h)
Slot B: Window 0 index value (base + 50h)
Slot B: Window 1 index value (base + 58h)
Slot B: Window 2 index value (base + 60h)
Slot B: Window 3 index value (base + 68h)
Slot B: Window 4 index value (base + 70h)

System Memory Address # Mapping Start Low Byte Register (Read/Write)

System Memory Address # Mapping Start High Byte Register

The System Memory Address # Mapping Start High Byte Register is shown below.



Slot A: Window 0 index value (base + 11h)
Slot A: Window 1 index value (base + 19h)
Slot A: Window 2 index value (base + 21h)
Slot A: Window 3 index value (base + 29h)
Slot A: Window 4 index value (base + 31h)
Slot B: Window 0 index value (base + 51h)
Slot B: Window 1 index value (base + 59h)
Slot B: Window 2 index value (base + 61h)
Slot B: Window 3 index value (base + 69h)
Slot B: Window 4 index value (base + 71h)

System Memory Address # Mapping Start High Byte Register (Read/Write)

System Memory Address # Mapping Start High Byte Register Description

Bits	Description
Bit 7	Data Size When this bit is set to "0", 8-bit memory accessing is enabled. When this bit is set to "1", 16-bit memory accessing by MC16 is enabled.
Bit 6	Zero Wait Enabled. When this bit is set to "0", $\overline{NWS}$ signal is not generated. When this bit is set to "1" and the IRDY pin is high, the $\overline{NWS}$ signal is generated. Note that the $\overline{NWS}$ signal does not become active, when 8-bit accessing, A0 = "0" and $\overline{SBHE}$ = "0".

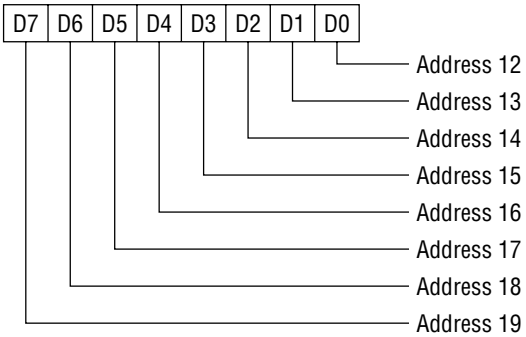
Control $\overline{CE1}$ and $\overline{CE2}$

Bit 7	$\overline{SBHE}$	A0	$\overline{CE1}$	$\overline{CE2}$	$\overline{MC16}$
1	0	0	0	0	0
1	0	1	1	0	0
1	1	×	0	1	0
0	×	×	0	1	1

The values set in the next two registers are the stop address of the Memory Windows.

System Memory Address # Mapping Stop Low Byte Register

The System Memory Address # Mapping Stop Low Byte Register is shown below.

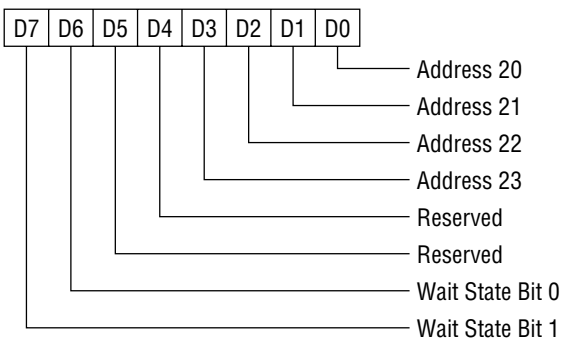


Slot A: Window 0 index value (base + 12h)
Slot A: Window 1 index value (base + 1Ah)
Slot A: Window 2 index value (base + 22h)
Slot A: Window 3 index value (base + 2Ah)
Slot A: Window 4 index value (base + 32h)
Slot B: Window 0 index value (base + 52h)
Slot B: Window 1 index value (base + 5Ah)
Slot B: Window 2 index value (base + 62h)
Slot B: Window 3 index value (base + 6Ah)
Slot B: Window 4 index value (base + 72h)

System Memory Address # Mapping Stop Low Byte Register (Read/Write)

System Memory Address # Mapping Stop High Byte Register

The System Memory Address # Mapping Stop High Byte Register is shown below.



Slot A: Window 0 index value (base + 13h)
Slot A: Window 1 index value (base + 1Bh)
Slot A: Window 2 index value (base + 23h)
Slot A: Window 3 index value (base + 2Bh)
Slot A: Window 4 index value (base + 33h)
Slot B: Window 0 index value (base + 53h)
Slot B: Window 1 index value (base + 5Bh)
Slot B: Window 2 index value (base + 63h)
Slot B: Window 3 index value (base + 6Bh)
Slot B: Window 4 index value (base + 73h)

System Memory Address # Mapping Stop High Byte Register (Read/Write)

System memory address # Mapping Stop High Byte Register Description

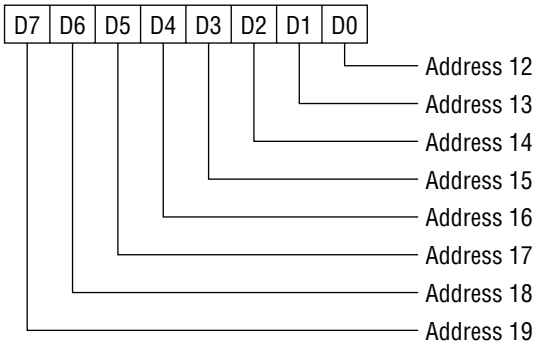
Bits	Description
Bit 7/Bit 6	Wait Status Bits 0 and 1 These bits specify the duration (in SCLK cycles) of a wait (low) given to IRDY. This function is valid only in the 16-bit access.

IRDY Output Function

Start High Byte Register Data Size Bit 7	Bit 7	Bit 6	IRDY
0	×	×	High
1	0	0	High
1	0	1	1SCLK Cycle Low
1	1	0	2SCLK Cycle Low
1	1	1	3SCLK Cycle Low

Card Memory Offset Address # Low Byte Register

The Card Memory Offset Address # Low Byte Register is shown below.

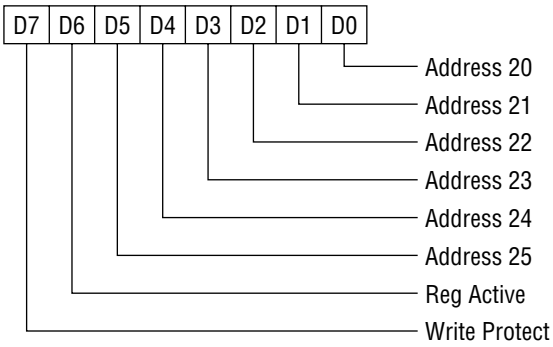


Slot A: Window 0 index value (base + 14h)
Slot A: Window 1 index value (base + 1Ch)
Slot A: Window 2 index value (base + 24h)
Slot A: Window 3 index value (base + 2Ch)
Slot A: Window 4 index value (base + 34h)
Slot B: Window 0 index value (base + 54h)
Slot B: Window 1 index value (base + 5Ch)
Slot B: Window 2 index value (base + 64h)
Slot B: Window 3 index value (base + 6Ch)
Slot B: Window 4 index value (base + 74h)

Card Memory Offset Address # Low Byte Register (Read/Write)

Card Memory Offset Address # High Byte Register

The Card Memory Offset Address # High Byte Register is shown below.



Slot A: Window 0 index value (base + 15h)
Slot A: Window 1 index value (base + 1Dh)
Slot A: Window 2 index value (base + 25h)
Slot A: Window 3 index value (base + 2Dh)
Slot A: Window 4 index value (base + 35h)
Slot B: Window 0 index value (base + 55h)
Slot B: Window 1 index value (base + 5Dh)
Slot B: Window 2 index value (base + 65h)
Slot B: Window 3 index value (base + 6Dh)
Slot B: Window 4 index value (base + 75h)

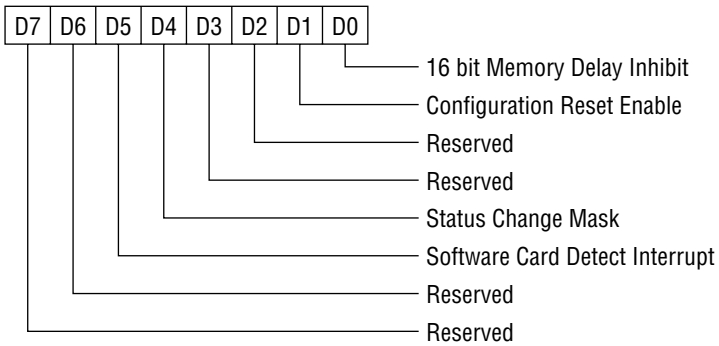
Card Memory Offset Address # High Byte Register (Read/Write)

Card Memory Offset Address # High Byte Register Description

Bits	Description
Bit 7	Write Protect : When this bit is set to "1", $\overline{WP}$ signal is made to "H" and write protect is enabled forcibly.
Bit 6	Reg Active : When this bit is set to "1", Attribute Memory Space Access is enabled by the active $\overline{REG}$ signal output.

Card Detect and General Control Register

The Card Detect and General Control Register is shown below.



Slot A : Index value (base + 16h)
Slot B : Index value (base + 56h)

Card Detect and General Control Register (Read/Write)

Card Detect and General Control Register Description

Bits	Description
Bit 5	Software Card Detect Interrupt : When this bit is set to 1 while the card detect change enable bit 4 of the card status change interrupt configuration register (+05h) is set to "1", a card detect change interrupt is generated the same as a hardware card detect interrupt.
Bit 4	Status Change Mask When this bit is set to "1", all interrupts due to status transitions are disabled. This masking is done regardless of the status of each Enable bit of the Card Status Change Interrupt Configuration registers (+05h and +45h).

Note : The software card detection interrupt bit is always reset to "0" when the card status change register is read.

Configuration Register Setting

CD1	CD2	Bit 1	Configuration Register Reset
×	×	0	No
0	0	1	Yes

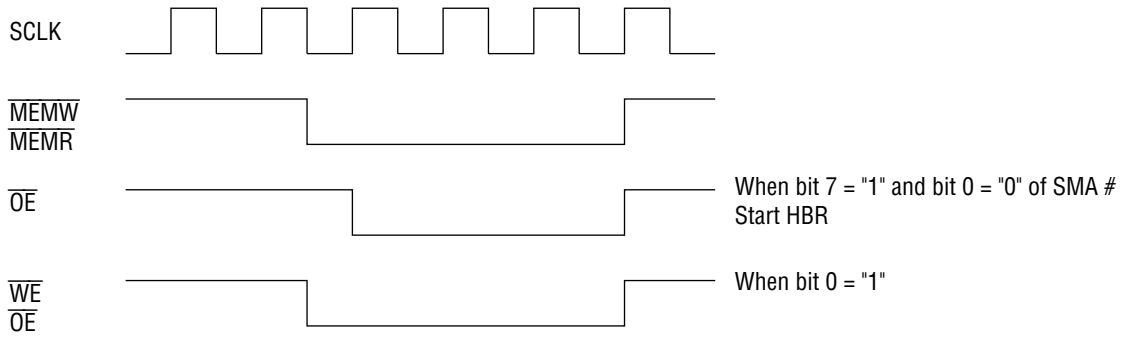
Configuration registers are shown on the next page.

The Configuration Registers are shown below.

Configuration Registers

Slot A Offset	Slot B Offset	Register Name
+03h	+43h	Interrupt and General Control (except $\overline{\text{ICHK}}$ enable bit)
+06h	+46h	Address Window Enable (except $\overline{\text{MC16}}$ decode A[23:12] bit)
+07h	+47h	I/O Control
+08h	+48h	I/O Address 0 Start Low Byte
+09h	+49h	I/O Address 0 Start High Byte
+0Ah	+4Ah	I/O Address 0 Stop Low Byte
+0Bh	+4Bh	I/O Address 0 Stop High Byte
+0Ch	+4Ch	I/O Address 1 Start Low Byte
+0Dh	+4Dh	I/O Address 1 Start High Byte
+0Eh	+4Eh	I/O Address 1 Stop Low Byte
+0Fh	+4Fh	I/O Address 1 Stop High Byte
+10h	+50h	System Memory Address 0 Mapping Start Low Byte
+11h	+51h	System Memory Address 0 Mapping Start High Byte
+12h	+52h	System Memory Address 0 Mapping Stop Low Byte
+13h	+53h	System Memory Address 0 Mapping Stop High Byte
+14h	+54h	Card Memory Offset Address 0 Low Byte
+15h	+55h	Card Memory Offset Address 0 High Byte
+18h	+58h	System Memory Address 1 Mapping Start Low Byte
+19h	+59h	System Memory Address 1 Mapping Start High Byte
+1Ah	+5Ah	System Memory Address 1 Mapping Stop Low Byte
+1Bh	+5Bh	System Memory Address 1 Mapping Stop High Byte
+1Ch	+5Ch	Card Memory Offset Address 1 Low Byte
+1Dh	+5Dh	Card Memory Offset Address 1 High Byte
+20h	+60h	System Memory Address 2 Mapping Start Low Byte
+21h	+61h	System Memory Address 2 Mapping Start High Byte
+22h	+62h	System Memory Address 2 Mapping Stop Low Byte
+23h	+63h	System Memory Address 2 Mapping Stop High Byte
+24h	+64h	Card Memory Offset Address 2 Low Byte
+25h	+65h	Card Memory Offset Address 2 High Byte
+28h	+68h	System Memory Address 3 Mapping Start Low Byte
+29h	+69h	System Memory Address 3 Mapping Start High Byte
+2Ah	+6Ah	System Memory Address 3 Mapping Stop Low Byte
+2Bh	+6Bh	System Memory Address 3 Mapping Stop High Byte
+2Ch	+6Ch	Card Memory Offset Address 3 Low Byte
+2Dh	+6Dh	Card Memory Offset Address 3 High Byte
+30h	+70h	System Memory Address 4 Mapping Start Low Byte
+31h	+71h	System Memory Address 4 Mapping Start High Byte
+32h	+72h	System Memory Address 4 Mapping Stop Low Byte
+33h	+73h	System Memory Address 4 Mapping Stop High Byte
+34h	+74h	Card Memory Offset Address 4 Low Byte
+35h	+75h	Card Memory Offset Address 4 High Byte

Bit	Description
Bit 0	16-Bit Memory Delay Inhibit. When this bit is set to "0" if 16-bit access (bit7 of System Memory Address # Mapping Start High Byte Register is "1"), $\overline{WE}$ and $\overline{OE}$ signals are output by one-stage synchronization of $\overline{IMEMW}$ and $\overline{IMEMR}$, at the falling edge of ISYSCLK. When this bit is set to "1", $\overline{WE}$ and $\overline{OE}$ signals are always output asynchronously with ISYSCLK. The timing diagram of SCLK synchronization of $\overline{WE}$, $\overline{OE}$ is shown below.



Timing Diagram of $\overline{IWE}$, $\overline{OWE}$ to SCLK

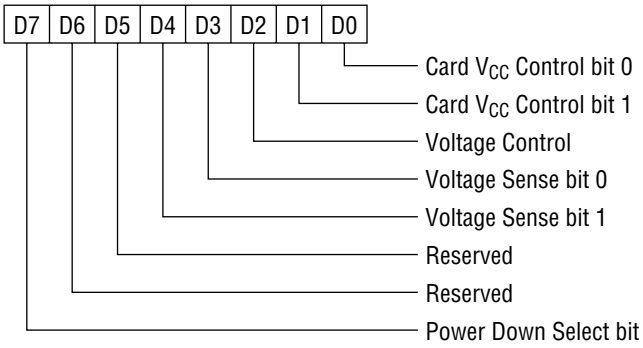
The SCLK synchronization of $\overline{WE}$, $\overline{OE}$ is shown below.

SCLK Synchronization of $\overline{WE}$, $\overline{OE}$

Bit 7 of SMA#M Start HBR	Bit 0	SCLK Sychronization of $\overline{WE}$, $\overline{OE}$
0	×	No
1	0	Yes
1	1	No

Voltage Control Register

The Voltage Control Register is shown below. The bits are defined below.



Slot A : Index value (base + 17h)
Slot B : Index value (base + 57h)

Voltage Control Register (Read/Write)

Voltage Control Register Description

D Bits	Description
Bit 7	Power Down Select : When set to "1", power down mode is set
Bit 4	Voltage sense bit 1 : This bit corresponds to state of V_{SS1} (voltage sense) pin
Bit 3	Voltage sense bit 0 : This bit corresponds to state of V_{SS0} (voltage sense) pin
Bit 2	Voltage_Control. When set to "1", PCMCIA input buffers will trigger to 5 V TTL levels: when set to "0", PCMCIA input buffers will trigger to 3 V TTL or 3 V/5 V CMOS input levels.
Bit 1	Card V_{CC} Control bit 1
Bit 0	Card V_{CC} Control bit 0

To enter power down mode the following should be done:
1. Bit 0 of Global General Control register (1E or 5E) is set to "1".
2. Bit 7 of Voltage control register 17 is set to "1".

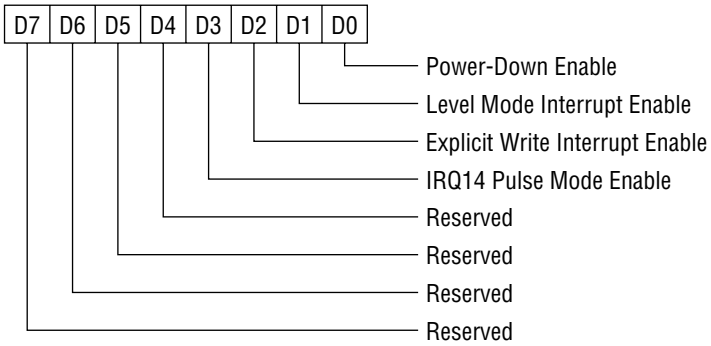
To leave the power down mode and enter a normal mode of operation the following should be done:
1. Bit 7 of Voltage control register (+17h, +57h) is set to "0".
2. Bit 0 of Global General Control register (+1Eh, +5Eh) is set to "0".

The power down mode affects only internal logic excluding registers +17h and +57h.
V_{CC} Control bits are encoded as follows:

Bit 1	Bit 0	VCCEN1	VCCEN0	Description
0	0	0	0	Not Connected
0	1	0	0	Reserved
1	0	1	0	5.0 V
1	1	0	1	3.3 V

Global Control Register

The Global Control Register is shown below. The bits are defined below.



Slot A : Index value (base + 1Eh)
Slot B : Index value (base + 5Eh)

Global Control Register (Read/Write)

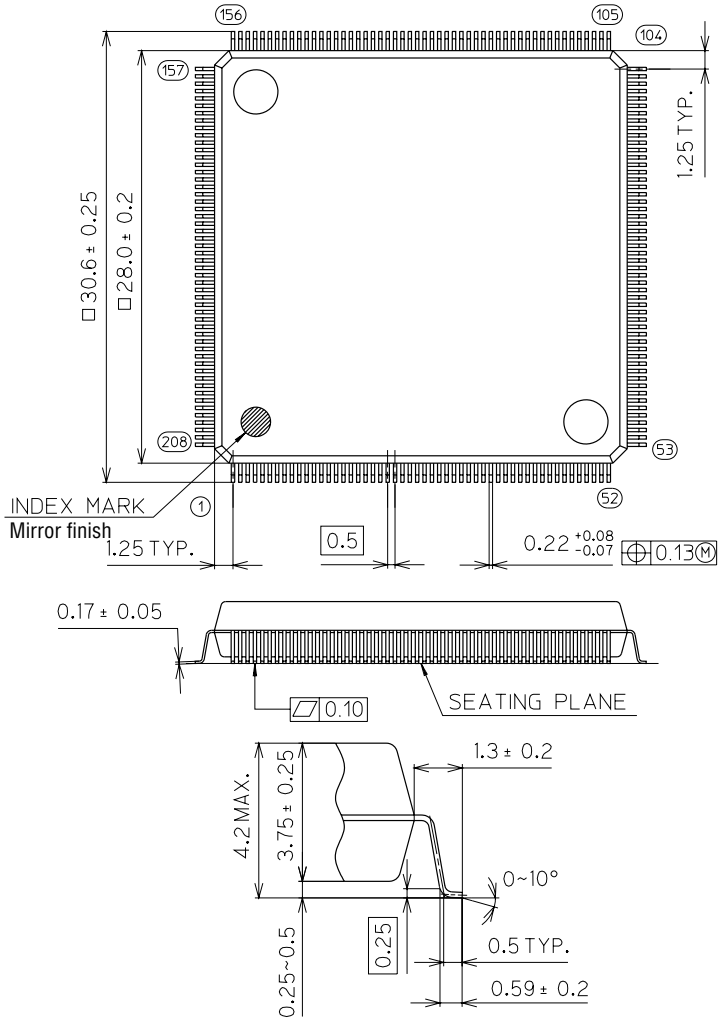
Global Control Register Description

Bits	Description
Bit 3	IRQ14 Pulse Mode Enable. When this bit is "1" and bit 1 is "0", an interrupt assigned to IRQ12 is set to level mode. Note that when bit 1 is set to "1" for level mode this bit is ineffective.
Bit 2	While this bit is set to "1", the content of the Card Status Change registers (+04h and +44h) will not be cleared after they are read. To clear the content of the register and reset the inturrupt, write "1" to the corresponding bit of the Card Status Change register. If a status change interrupt is disabled by the Card Status Change Interrupt Configuration registers (+05h and 45h) or the Card Detection Control registers (+16h and +56h), even when a status change interrupt occurs while this bit is set to "1", the Card Status Change register is cleared and the interrupt is reset.
Bit 1	Level Mode Interrupt Enable. This bit selects a mode for an interrupt signal, which is output to the IRQ#. When set to "1", level mode interrupt is selected. When set to "0", edge-triggered mode interrupt is selected.
Bit 0	Power-Down Enable When this bit is set to "1", the Power Down mode is enabled. When this bit is set to "0", the Power Down mode is disabled.

PACKAGE DIMENSIONS

(Unit : mm)

QFP208-P-2828-0.50-BK4



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	5.65 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).