

SBVS028A − DECEMBER 2000 − REVISED APRIL 2004

Miniature, 2W Isolated REGULATED DC/DC CONVERTERS

FEATURES

- UL1950 Recognized
- DIP-18 and SO-10 Packages
- 55W/in^3 (3.3W/cm^3) Power Density
- Device-to-Device Synchronization
- Thermal Protection
- 1000Vrms Isolation
- 400kHz Switching
- 125 FITS at 55°C
- Short-Circuit Protection
- 12V, 24V Inputs
- 5V Outputs

APPLICATIONS

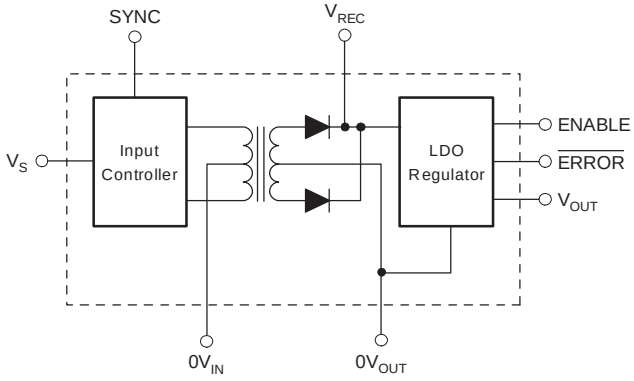
- Point-of-Use Power Conversion
- Digital Interface Power
- Ground Loop Elimination
- Power-Supply Noise Reduction

DESCRIPTION

The DCR02 family is a series of high-efficiency, input-isolated, output-regulated DC/DC converters. In addition to 2W nominal, galvanically-isolated output power capability, this range of converters offers very low output noise and high accuracy.

The DCR02 family is implemented in standard molded IC packaging, providing standard JEDEC outlines suitable for high-volume assembly.

The DCR is manufactured using the same technology as standard IC packages, thereby achieving very high reliability.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

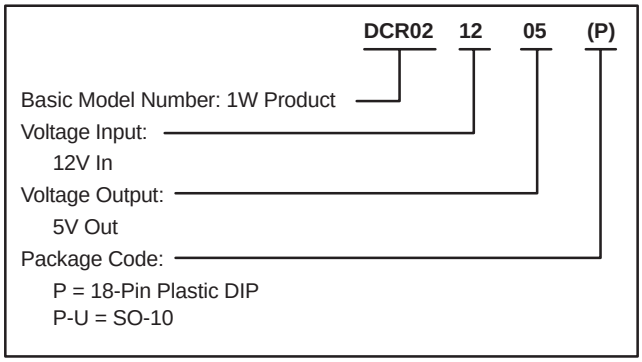
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DCR021205	DIP−18	NVE	−40°C to +70°C	DCR021205P	DCR021205P	Rail, 20
	SO−10(2)	DVS	−40°C to +70°C	DCR021205P−U	DCR021205P−U	Rail, 20
	SO−10(2)	DVS	−40°C to +70°C	DCR021205P−U	DCR021205P−U/700	Tape and Reel, 700
DCR022405	DIP−18	NVE	−40°C to +70°C	DCR022405P	DCR022405P	Rail, 20
	SO−10(2)	DVS	−40°C to +70°C	DCR022405P−U	DCR022405P−U	Rail, 20
	SO−10(2)	DVS	−40°C to +70°C	DCR022405P−U	DCR022405P−U/700	Tape and Reel, 700

(1) For the most current package and ordering information, refer to our web site at www.ti.com.
(2) SO−10 packages have 18 pins, but only 10 pins are active.

SUPPLEMENTAL ORDERING INFORMATION



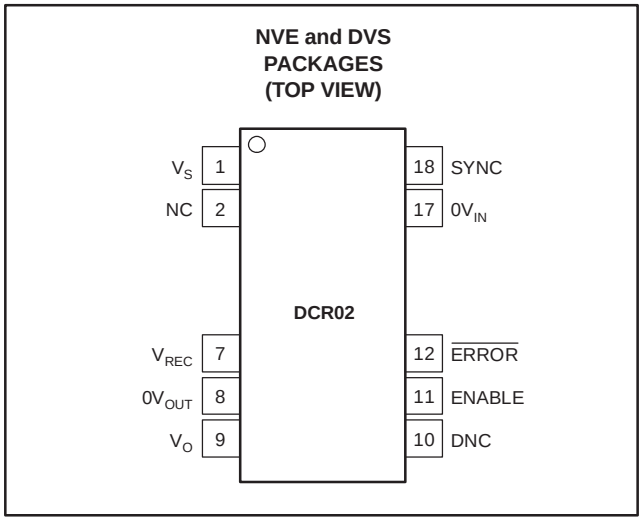
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		DCR02 SERIES	UNIT
Input Voltage	DCR0212	15	V
	DCR0224	29	V
Storage Temperature		−60 to +125	°C
Lead Temperature (soldering, 10s)		+270	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

PIN ASSIGNMENTS



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
V_S	1	I	Voltage input
NC	2		No connection
V_{REC}	7	O	Rectified output
$0V_{OUT}$	8	O	Output ground
V_O	9	O	Voltage output
DNC	10		Do not connect
ENABLE	11	O	Output voltage enable
$\overline{ERROR}$	12	O	Error flag active low
$0V_{IN}$	17	I	Input ground
SYNC	18	I	Synchronization input

NOTE: I = input and O = output.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = nominal, I_{OUT} = 10mA, C_{OUT} = 0.1µF ceramic, and C_{IN} = 2.2µF ceramic, unless otherwise noted(1).

PARAMETER		TEST CONDITIONS	DCR02 SERIES MIN	DCR02 SERIES TYP	DCR02 SERIES MAX	UNITS
Output						
Setpoint	DCR021205			5		V
	DCR022405			5		V
Setpoint accuracy				0.5	2.0	%
Maximum Output Current	DCR021205		400			mA
	DCR022405		400			mA
Output short-circuit protected		Duration		Infinite		
Line regulation	DCR021205			1		mV/V
	DCR022405			1		mV/V
Over line and load		10mA to 400mA load, over input voltage range		1.0	2.5	%
Versus temperature		−40°C to +70°C		1.0		%
Ripple and noise	DCR0212 ripple	20MHz bandwidth, 50% load(1)		18		mV_{PP}
	DCR0212 noise	100MHz bandwidth, 50% load(1)		20		mV_{PP}
	DCR0224 ripple	20MHz bandwidth, 50% load(1)		18		mV_{PP}
	DCR0224 noise	100MHz bandwidth, 50% load(1)		25		mV_{PP}
Input						
Nominal voltage, V_S	DCR021205			12		V
	DCR022405			24		V
Voltage range			−10		+10	%
Supply current	DCR021205	I_O = 0mA		15		mA
		I_O = 10mA		23		mA
		I_O = 400mA		250		mA
	DCR022405	I_O = 0mA		15		mA
		I_O = 10mA		17		mA
		I_O = 400mA		129		mA
Reflected ripple current		20MHz bandwidth, 100% load(1)		8		mA_{PP}
Isolation						
Voltage		1s flash test	1			kVrms
		60s test, UL1950(2)	1			kVrms
Input/output capacitance				25		pF
Output Enable Control						
Logic high input voltage			2.0		V_{REC}	V
Logic high input current		2.0 < V_{ENABLE} < V_{REC}		100		nA
Logic low input voltage			−0.2		0.5	V
Logic low input current		0 < V_{ENABLE} < 0.5		100		nA
Error Flag						
Logic high open collector leakage		V_{ERROR} = 5V			10	µA
Logic low output voltage		Sinking 2mA			0.4	V
Thermal Shutdown						
Junction temperature	Temp activated			+150		°C
	Temp deactivated			+130		°C

(1) Ceramic capacitors, C_{IN} = 2.2µF, C_{FILTER} = 1µF, and C_{OUT} = 0.1µF.
(2) During UL1950 recognition test only.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = nominal, I_{OUT} = 10mA, C_{OUT} = 0.1µF ceramic, and C_{IN} = 2.2µF ceramic, unless otherwise noted(1).

PARAMETER	TEST CONDITIONS	DCR02 SERIES			UNITS
		MIN	TYP	MAX	
Synchronization Pin					
Max external capacitance on SYNC pin				3	pF
Internal oscillator frequency		720	800	880	kHz
External synchronization frequency		720		880	kHz
External synchronization signal high		2.5	2.5	5.0	V
External synchronization signal low		0		0.4	V
Temperature Range					
Operating		−40		+70	°C

(1) Ceramic capacitors, C_{IN} = 2.2µF, C_{FILTER} = 1µF, and C_{OUT} = 0.1µF.
(2) During UL1950 recognition test only.

FUNCTIONAL DESCRIPTION

OVERVIEW

The DCR02 series offers isolation from an unregulated power supply operating from a choice of input voltages. This series provides a variety of regulated output voltages at a nominal output power of 2W.

POWER STAGE

The input supply is chopped at a frequency of 400kHz (internal oscillator divided by 2), which is used to drive the center-tapped toroidal transformer.

RECTIFICATION

The transformer output is full wave rectified and smoothed by the external capacitor connected to V_{REC}.

REGULATOR

The internal low-dropout regulator provides a well-regulated output voltage throughout the operating range of the device.

OSCILLATOR AND WATCHDOG

The DCR02 uses an internal saw-tooth generator to provide the 800kHz onboard oscillator that is used to drive the power switching circuit. The operation of the oscillator is monitored by the watchdog, which will tri-state the output driver circuit if the oscillator fails or if the SYNC pin is taken low (shutdown mode). When the SYNC pin is returned high, normal operation resumes.

SYNCHRONIZATION

If more than one DCR02 is being used, beat frequencies and other electrical interference can be generated. This interference is due to the small variations in switching frequencies between the converters. The DCR02 overcomes this by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the SYNC pins together, with care being taken to minimize the capacitance of tracking.

Significant stray capacitance on the SYNC pin reduces the frequency of the internal oscillator. If this reduction is large, the DCR02 may be taken out with its optimized operating parameters, and saturation of the magnetics may result, damaging the device.

If devices are synchronized, it should be noted that all devices will draw maximum current simultaneously at start up. This can cause the input voltage to dip. Should it fall below the minimum input voltage, the devices may not start up. A low equivalent series resistance (ESR) 2.2µF ceramic capacitor should be connected as close to the device input pins as possible.

If more than eight devices are required to be synchronized, it is recommended that external synchronization be used. Details of this procedure are contained in application report SBAA035, *External Synchronization of the DCP01/02 Series of DC/DC Converters,* available for download at www.ti.com.

CONSTRUCTION

The DCR02 is manufactured using the same technology as standard IC packages. There is no substrate within the package. The DCR02 is constructed using a driver IC, low-dropout voltage regulator, rectifier diodes, and a wound magnetic toroid, all mounted on a leadframe. The DCR02 requires no special printed circuit board (PCB) assembly processing, since there is no solder within the package. The result is an isolated DC/DC converter with inherently high reliability.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCR02 can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the SYNC pin is pulled low, the DCR02 will be disabled. The disable time depends upon the external loading. The internal disable function is implemented in 2µs. Removal of the pull down will enable the DCR02.

Capacitance loading on the SYNC pin should be minimized in order to prevent a reduction in the internal oscillator frequency. See application report SBAA035 for information on how to nullify the effects of additional capacitance on the SYNC pin. The oscillator frequency can be measured at V_{REC}, as this is the fundamental frequency of the ripple component.

OUTPUT ENABLE/DISABLE

The regulated output of the DCR02 can be disabled by pulling the ENABLE pin low (by connecting ENABLE to $0V_{OUT}$). Holding the ENABLE pin high (connect ENABLE to V_{REC}) enables the regulated output voltage, thus allowing the output to be controlled from the isolated side, as shown in Figure 1.

$\overline{\text{ERROR}}$ FLAG

The DCR02 has an $\overline{\text{ERROR}}$ pin which provides a *power good* flag, as long as the internal regulator is in regulation.

DECOUPLING

Ripple Reduction

Due to the very low forward resistance of the DMOS switching transistors, high-current demands are placed upon the input supply for a short time. By placing a good quality low ESR 2.2µF ceramic capacitor close to the IC supply input pins, the effects on the power supply can be minimized.

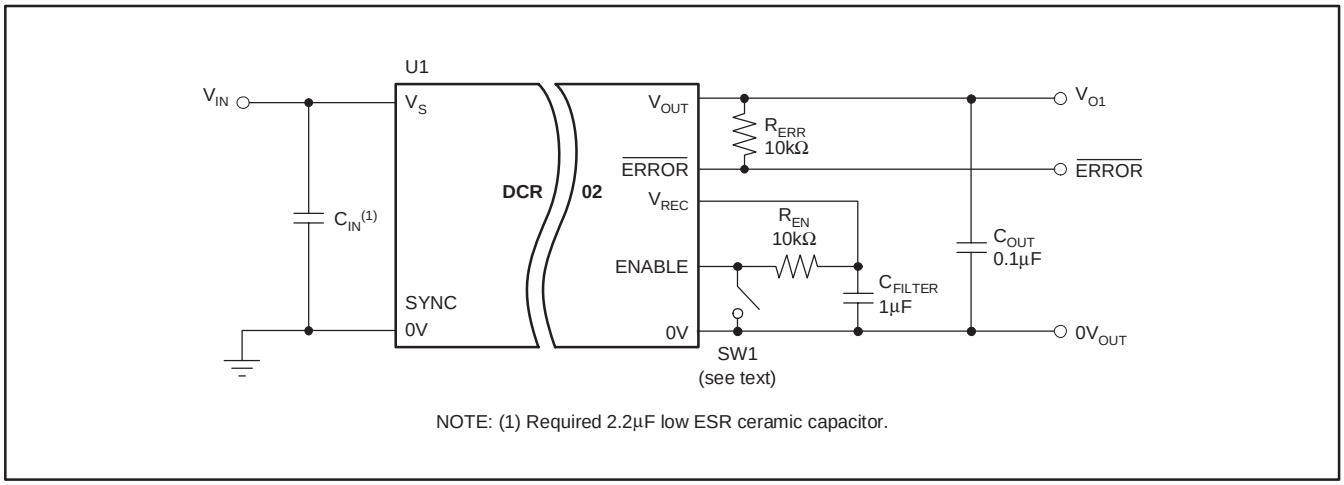
The high switching frequency of 400kHz allows relatively small values of capacitors to be used for filtering the rectified output voltage. A good quality, low ESR 1µF ceramic capacitor placed close to the V_{REC} pin and output ground will reduce the ripple.

It is not recommended that the DCR02 be fitted using an IC socket because this degrades performance.

The output at V_{REC} is full wave rectified and produces a ripple of 800kHz.

It is recommended that a 0.1µF low ESR ceramic capacitor be connected close to the output pin and ground to reduce noise on the output. The capacitor values listed are minimum values. If lower ripple is required, the ceramic filter capacitor should be increased in value to 2.2µF.

NOTE: As with all switching power supplies, the best performance is only obtained with low ESR ceramic capacitors connected close to the respective buses. If low ESR ceramic capacitors are not used, the ESR will generate a voltage drop when the capacitor is supplying the load power. Often a larger capacitor is chosen for this purpose when a low ESR smaller capacitance performs just as well.



NOTE: (1) Required 2.2µF low ESR ceramic capacitor.

Figure 1. DCR02 with a Single Output

APPLICATION NOTES

DCR02 SINGLE VOLTAGE OUTPUT

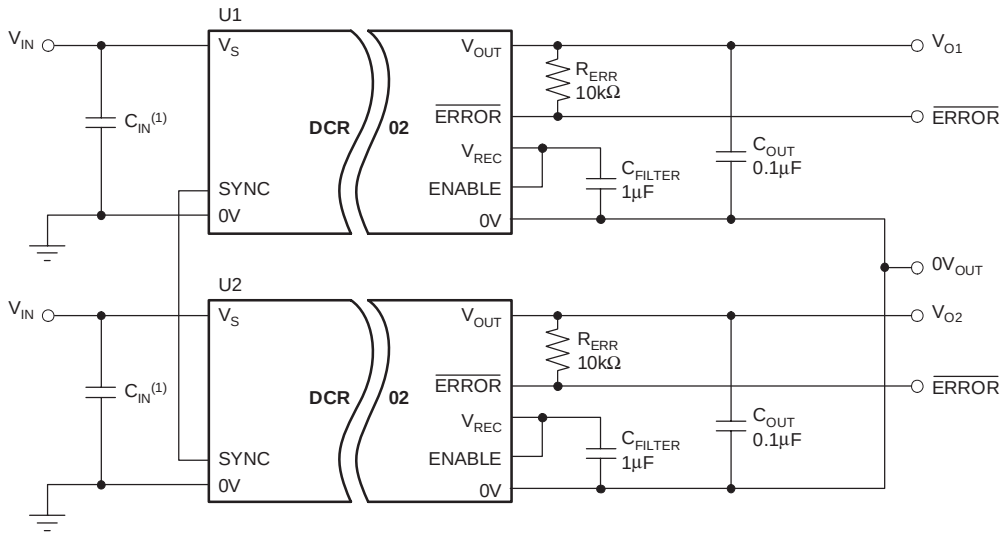
The DCR02 can be used to provide a single voltage output by connecting the circuit as shown in Figure 1. The $\overline{\text{ERROR}}$ output signal will be pulled up to the value of V_{OUT} for the particular DCR02 being used. The value of R_{ERR} will depend on the loading on the $\overline{\text{ERROR}}$ line; however, the total load on the $\overline{\text{ERROR}}$ line must not exceed the value given in the specification.

The output can be permanently enabled by connecting the ENABLE pin to the V_{REC} pin. The DCR02 can be enabled remotely by connecting the ENABLE pin to V_{REC} via a pull-up resistor (R_{EN}); the value of this resistor is not critical for the DCR02 since only a small current flows. Switch SW1 can be used to pull the ENABLE pin low, thus disabling the output. The switching devices can be a bipolar transistor, FET, or a mechanical device; the main load that it will see is R_{EN}.

GENERATING TWO POSITIVE OUTPUT VOLTAGES

Two DCR02s can be used to create two +5V output voltages, as shown in Figure 2. The two DCR02s are connected in self-synchronization, thus locking the oscillators of both devices to a single frequency.

The $\overline{\text{ERROR}}$ and ENABLE facilities can be used in a similar configuration for a single DCR02. The filter capacitors connected to the V_{REC} pins (C_{FILTER}) should be kept separate from each other and connected in close proximity to the respective DCR02. If similar output voltages are being used, it is not recommended that a single filter capacitor (with an increased capacitance) be used with both V_{REC} pins connected together, since this could result in the overloading of one of the devices.



NOTE: (1) Required 2.2µF low ESR ceramic capacitor.

Figure 2. Generating Two Positive Voltages from Self-Synchronized DCR02s

GENERATION OF DUAL POLARITY VOLTAGES FROM TWO SELF-SYNCHRONIZED DCR02s

Two DCR02s can be configured to produce a dual polarity supply (that is, ±5V); the circuit must be connected as shown in Figure 3.

It should be observed that both DCR02s are positive voltage regulators; therefore the $\overline{\text{ERROR}}$, ENABLE, and V_{REC} pins are relative to their respective devices, 0V, and must not be connected together.

PCB LAYOUT

RIPPLE AND NOISE

Careful consideration should be given to the layout of the PCB in order for the best results to be obtained.

The DCR02 is a switching power supply and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes should be used to track the power to the input of DCR02; this will also serve to reduce noise on the circuit. If this is not possible, the supplies must be connected in a star formation, with the tracks made as wide as possible.

If the SYNC pin is being used, the tracking between device SYNC pins should be short, to avoid stray capacitance. If the SYNC pin is not being used, it is advisable to place a guard ring (connected to input ground) around this pin to avoid any noise pickup.

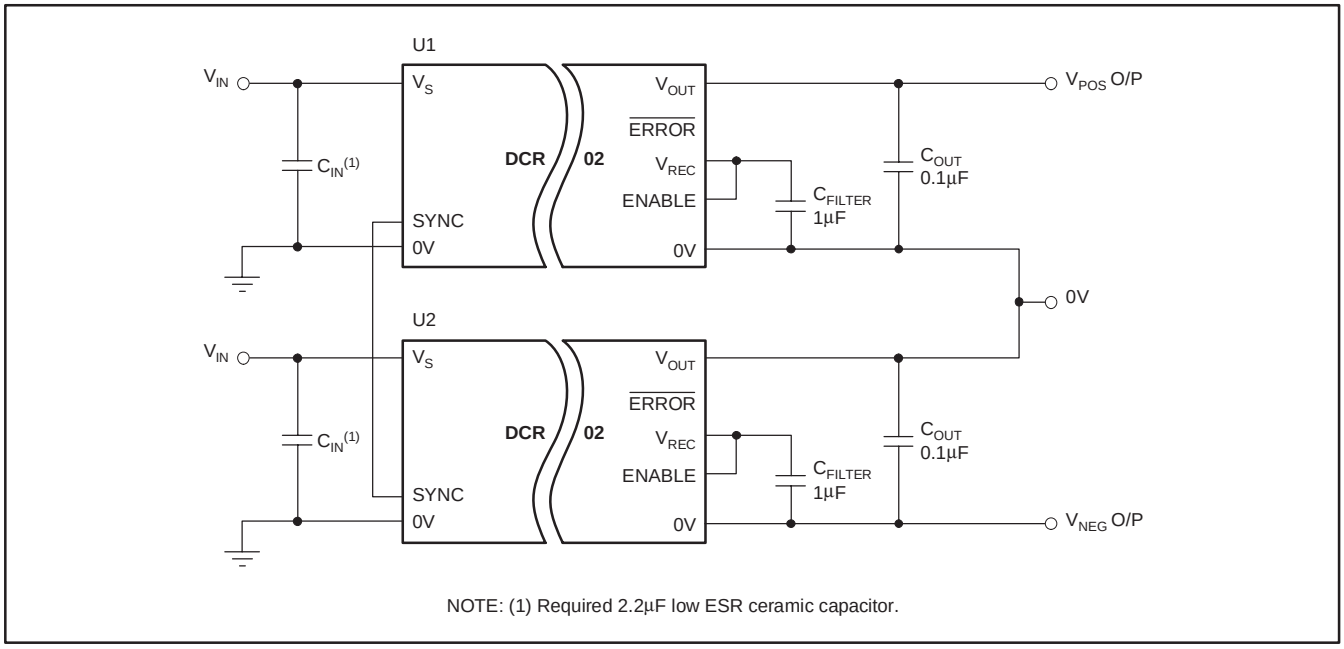
The output should be taken from the device using ground and power planes. This will ensure minimum losses.

A good quality, low ESR ceramic capacitor placed as close as practical across the input will reduce reflected ripple and ensure a smooth startup.

Additionally, a good quality, low ESR ceramic capacitor placed as close as practical across the rectifier output terminal and output ground will also give the best ripple and noise performance.

THERMAL MANAGEMENT

Due to the high power density of this device, it is advisable to provide a ground plane on the output. The output regulator is mounted on a copper leadframe, and a ground plane will serve as an efficient heatsink.



NOTE: (1) Required 2.2µF low ESR ceramic capacitor.

Figure 3. Dual Polarity Voltage Generation from Two Self-Synchronized DCR02s

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DCR021205P	ACTIVE	PDIP	NVE	10	20	TBD	CU SNPB	Level-NA-NA-NA
DCR021205P-U	ACTIVE	SOP	DVS	10	20	TBD	CU SNPB	Level-NA-NA-NA
DCR022405P	ACTIVE	PDIP	NVE	10	20	TBD	Call TI	Level-NA-NA-NA
DCR022405P-U	ACTIVE	SOP	DVS	10	20	TBD	Call TI	Level-NA-NA-NA
DCR022405P-U/700	ACTIVE	SOP	DVS	10	700	TBD	Call TI	Level-NA-NA-NA

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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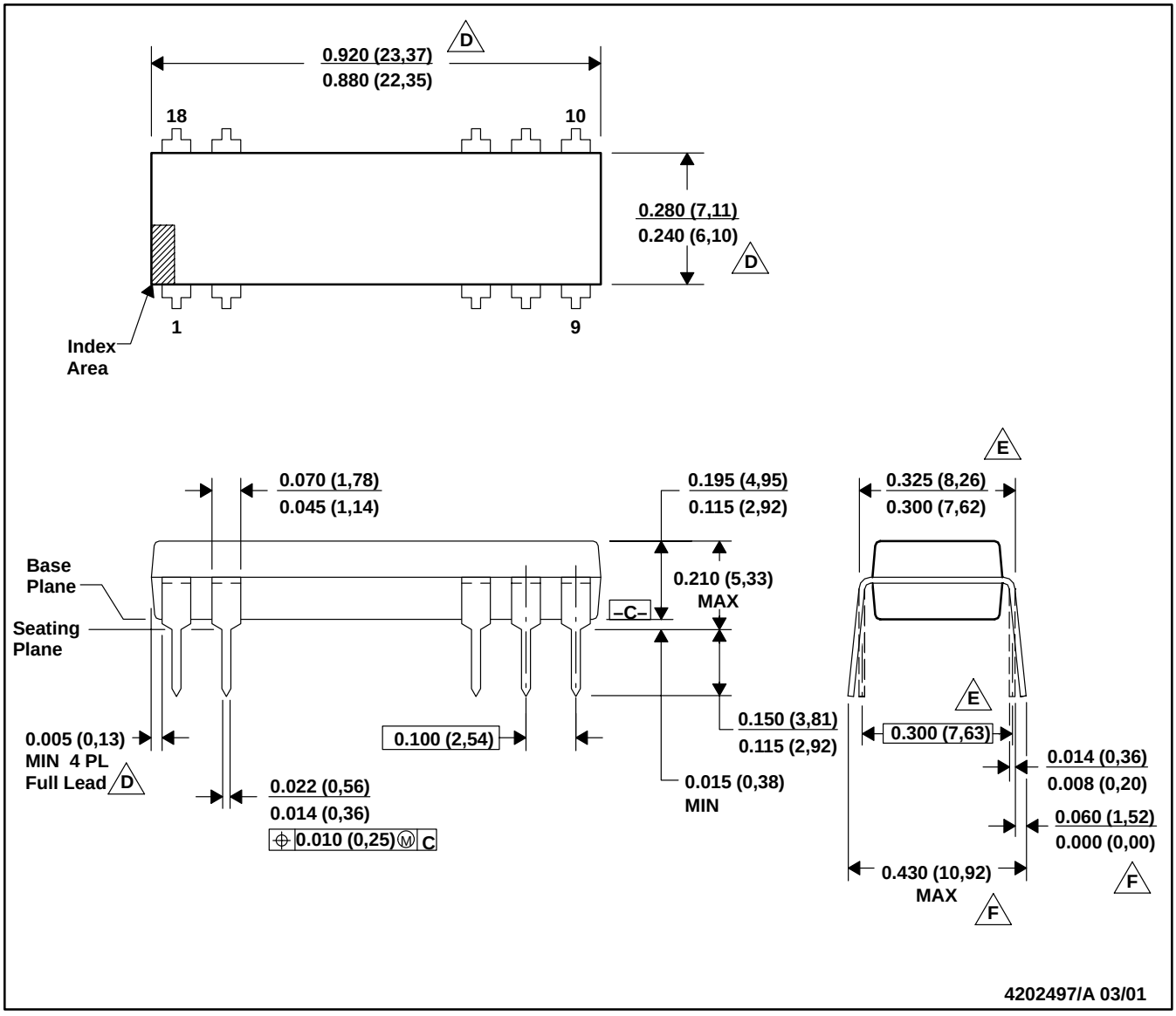
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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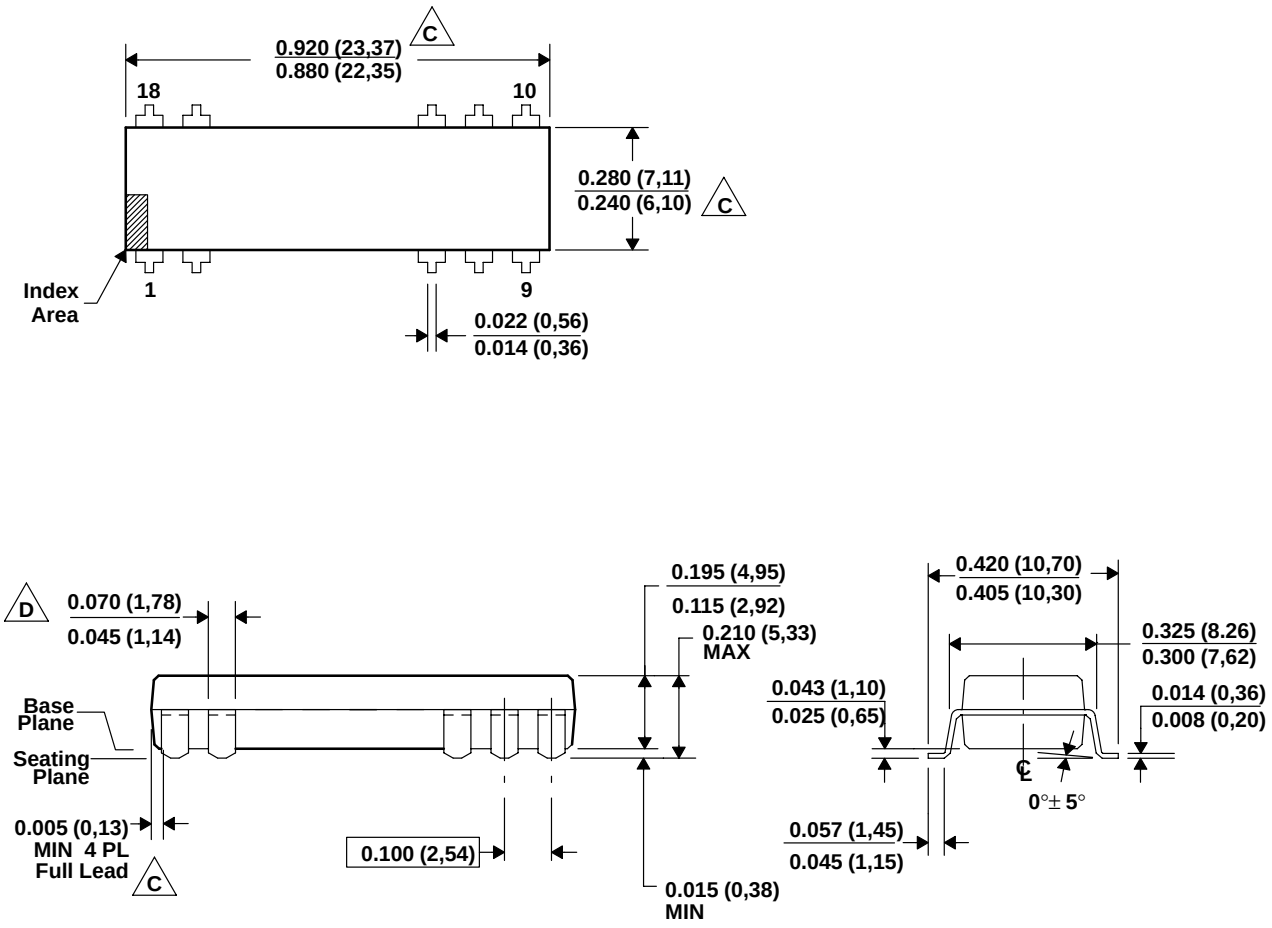
MPDI055 – APRIL 2001

NVE (R-PDIP-T10/18) **PLASTIC DUAL-IN-LINE**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001-AC with the exception of lead count.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. A visual index feature must be located within the cross-hatched area.

DVS (R-PDSO-G10/18) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
D. Maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25)
E. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
F. A visual index feature must be located within the cross–hatched area.
G. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

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