



# Pentium/Pro/II™ System Clock Chip

## General Description

The **ICS9248-55** is a Clock Synthesizer chip for Pentium and PentiumPro CPU based Desktop/Notebook systems that will provide all necessary clock timing.

Features include four CPU and eight PCI clocks. Three reference outputs are available equal to the crystal frequency. Additionally, the device meets the Pentium power-up stabilization requirement, assuring that CPU and PCI clocks are stable within 2ms after power-up.

PD# pin enables low power mode by stopping crystal OSC and PLL stages. Other power management features include CPU\_STOP#, which stops CPU (0:3) clocks, and PCI\_STOP#, which stops PCICLK (0:6) clocks.

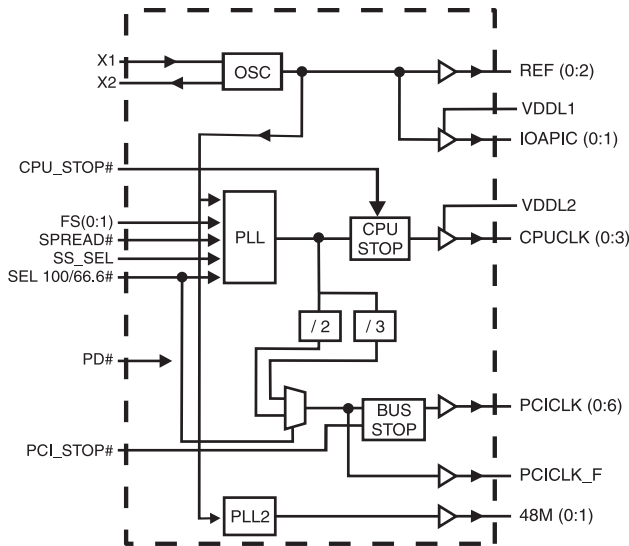
High drive CPUCLK outputs typically provide greater than 1 V/ns slew rate into 20pF loads. PCICLK outputs typically provide better than 1V/ns slew rate into 30pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

The **ICS9248-55** accepts a 14.318MHz reference crystal or clock as its input and runs on a 3.3V core supply.

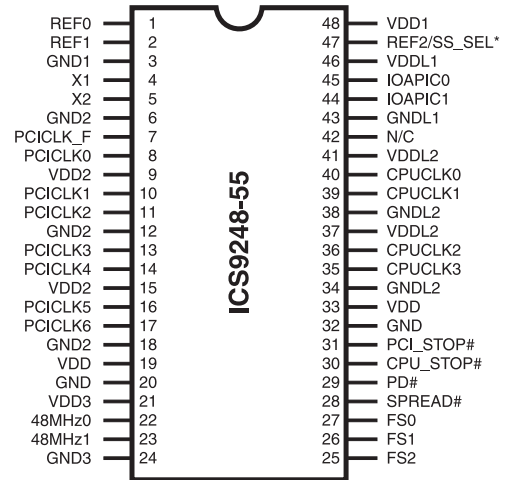
## Features

- Generates system clocks for CPU, IOAPIC, PCI, plus 14.314 MHz REF (0:2), USB, and Super I/O
- Supports single or dual processor systems
- Supports Spread Spectrum modulation for CPU & PCI clocks, down spread -0.5%
- Skew from CPU (earlier) to PCI clock (rising edges for 100/33.3MHz) 1.5 to 4ns
- Two fixed outputs at 48MHz.
- Separate 2.5V and 3.3V supply pins
- 2.5V or 3.3V output: CPU, IOAPIC
- 3.3V outputs: PCI, REF, 48MHz
- No power supply sequence requirements
- Uses external 14.318MHz crystal, no external load cap required for C<sub>L</sub>=18pF crystal
- 48 pin 300 mil SSOP

## Block Diagram



## Pin Configuration



**48-Pin SSOP**

\* Internal Pull-down Resistor of 240K to GND. on indicated inputs

## Power Groups

- VDD = Supply for PLL core
- VDD1 = REF (0:2), X1, X2
- VDD2 = PCICLK\_F, PCICLK (0:6)
- VDD3 = 48MHz0, 48MHz1
- VDDL1 = IOAPIC (0:1)
- VDDL2 = CPUCLK (0:3)

## Ground Groups

- GND = Ground for PLL core
- GND1 = REF (0:2), X1, X2
- GND2 = PCICLK\_F, PCICLK (0:6)
- GND3 = 48MHz0, 48MHz1
- GNDL1 = IOAPIC (0:1)
- GNDL2 = CPUCLK (0:3)

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## Pin Descriptions

| PIN NUMBER                | PIN NAME     | TYPE | DESCRIPTION   |
|---------------------------|--------------|------|---|
| 1, 2                      | REF0, REF1   | OUT  | 14.318MHz clock output  |
| 3                         | GND1         | PWR  | Ground for REF outputs  |
| 4                         | X1           | IN   | XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2        |
| 5                         | X2           | OUT  | XTAL_OUT Crystal output, has internal load cap 33pF   |
| 6, 12, 18                 | GND2         | PWR  | Ground for PCI outputs  |
| 7                         | PCICLK_F     | OUT  | Free Running PCI output   |
| 8, 10, 11, 13, 14, 16, 17 | PCICLK (0:6) | OUT  | PCI clock outputs. TTL compatible 3.3V  |
| 9, 15                     | VDD2         | PWR  | Power for PCICLK outputs, nominally 3.3V  |
| 19, 33                    | VDD          | PWR  | Isolated power for core, nominally 3.3V   |
| 20, 32                    | GND          | PWR  | Isolated ground for core  |
| 21                        | VDD3         | PWR  | Power for 48MHz outputs, nominally 3.3V   |
| 22, 23                    | 48MHz (0:1)  | OUT  | 48MHz outputs   |
| 24                        | GND3         | PWR  | Ground for 48MHz outputs  |
| 25, 26, 27                | FS (0:2)     | IN   | Frequency Select pins   |
| 28                        | SPREAD#      | IN   | Enables Spread Spectrum feature when LOW  |
| 29                        | PD#          | IN   | Powers down chip, active low  |
| 30                        | CPU_STOP#    | IN   | Halts CPU clocks at logic "0" level when low  |
| 31                        | PCI_STOP#    | IN   | Halts PCI Bus at logic "0" level when low   |
| 37, 41                    | VDDL2        | PWR  | Power for CPU outputs, nominally 2.5V   |
| 34, 38                    | GNDL2        | PWR  | Ground for CPU outputs.   |
| 35, 36, 39, 40            | CPUCLK (3:0) | OUT  | CPU and Host clock outputs @ 2.5V   |
| 42                        | N/C          | -    | Not internally connected  |
| 43                        | GNDL1        | PWR  | Ground for IOAPIC outputs   |
| 44, 45                    | IOAPIC (0:1) | OUT  | IOAPIC outputs (14.318MHz) @ 2.5V   |
| 46                        | VDDL1        | PWR  | Power for IOAPIC outputs, nominally 2.5V  |
| 47                        | SS_SEL       | IN   | ± 25% Spread Spectrum Selector at power up.<br>Logic 0 for Downspread<br>Logic 1 for Centerspread |
|                           | REF2         | OUT  | 14.318MHz clock output  |
| 48                        | VDD1         | PWR  | Supply for REF (0:2), X1, X2, nominal 3.3V  |

## Select Functions

| Functionality   | CPU                    | PCI,<br>PCI_F          | REF               | IOAPIC            | 48 MHz<br>Selection |
|-----------------|------------------------|------------------------|-------------------|-------------------|---------------------|
| Tristate        | HI - Z                 | HI - Z                 | HI - Z            | HI - Z            | HI - Z              |
| Testmode        | TCLK/2 <sup>1</sup>    | TCLK/6 <sup>1</sup>    | TCLK <sup>1</sup> | TCLK <sup>1</sup> | TCLK/2 <sup>1</sup> |
| Spread Spectrum | Modulated <sup>2</sup> | Modulated <sup>2</sup> | 14.318MHz         | 14.318MHz         | 48.0MHz             |

| FS2 | FS1 | FS0 | CPU MHz | PCI MHz |
|-----|-----|-----|---------|---------|
| 0   | 0   | 0   | 133     | 33.25   |
| 0   | 0   | 1   | 83.3    | 41.65   |
| 0   | 1   | 0   | 75      | 37.5    |
| 0   | 1   | 1   | 66.6    | 33.3    |
| 1   | 0   | 0   | 124     | 41.33   |
| 1   | 0   | 1   | 133     | 44.3    |
| 1   | 1   | 0   | 112     | 37.3    |
| 1   | 1   | 1   | 100     | 33.3    |



## Power Management

### Clock Enable Configuration

| CPU_STOP# | PCI_STOP# | PWR_DWN# | CPUCLK  | PCICLK  | Other Clocks,<br>REF,<br>IOAPICs,<br>48 MHz 0<br>48 MHz 1 | Crystal | VCOs    |
|-----------|-----------|----------|---------|---------|---|---------|---------|
| X         | X         | 0        | Low     | Low     | Stopped   | Off     | Off     |
| 0         | 0         | 1        | Low     | Low     | Running   | Running | Running |
| 0         | 1         | 1        | Low     | Running | Running   | Running | Running |
| 1         | 0         | 1        | Running | Low     | Running   | Running | Running |
| 1         | 1         | 1        | Running | Running | Running   | Running | Running |

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. During power up and power down operations using the PD# select pin will not cause clocks of a shorter or longer pulse than that of the running clock. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

### ICS9248-55 Power Management Requirements

| SIGNAL    | SIGNAL STATE                      | Latency<br>No. of rising edges of free<br>running PCICLK |
|-----------|-----------------------------------|--|
| CPU_STOP# | 0 (Disabled) <sup>2</sup>         | 1  |
|           | 1 (Enabled) <sup>1</sup>          | 1  |
| PCI_STOP# | 0 (Disabled) <sup>2</sup>         | 1  |
|           | 1 (Enabled) <sup>1</sup>          | 1  |
| PD#       | 1 (Normal Operation) <sup>3</sup> | 3ms  |
|           | 0 (Power Down) <sup>4</sup>       | 2max   |

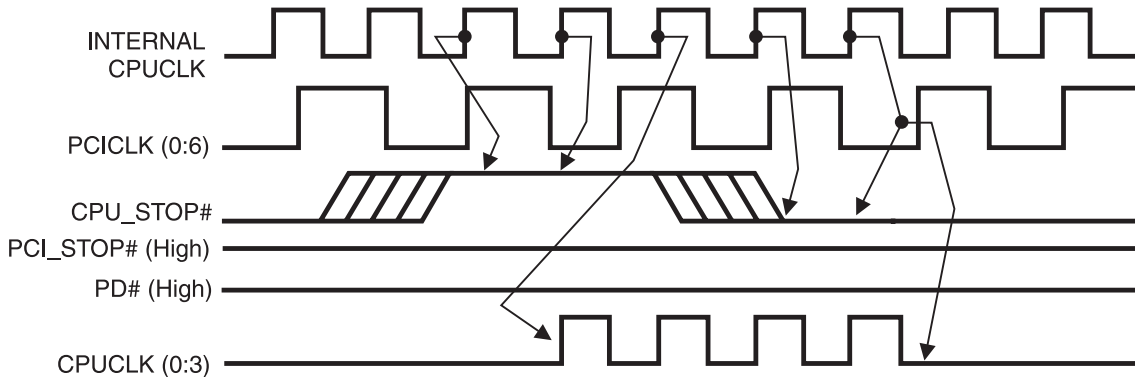
**Notes.**

1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, PCICLK only.  
The REF and IOAPIC will be stopped independent of these.



## CPU\_STOP# Timing Diagram

CPUSTOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU\_STOP# is synchronized by the ICS9248-55. The minimum that the CPUCLK is enabled (CPU\_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

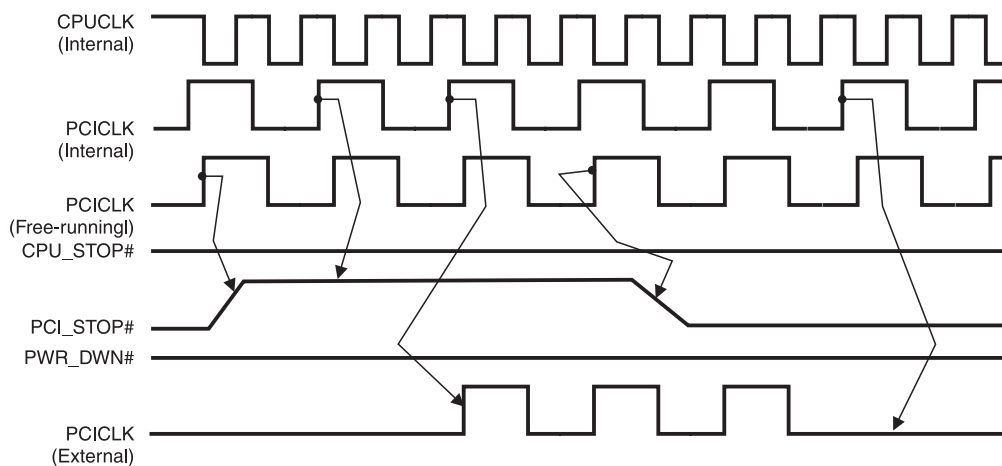


### Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU\_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the ICS9248-55.
3. All other clocks continue to run undisturbed.
4. PD# and PCI\_STOP# are shown in a high (true) state.

## PCI\_STOP# Timing Diagram

PCI\_STOP# is an asynchronous input to the ICS9248-55. It is used to turn off the PCICLK (0:6) clocks for low power operation. PCI\_STOP# is synchronized by the ICS9248-55 internally. The minimum that the PCICLK (0:6) clocks are enabled (PCI\_STOP# high pulse) is at least 10 PCICLK (0:6) clocks. PCICLK (0:6) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:6) clock on latency cycles are only one rising PCICLK. Clock off latency is one PCICLK clock.



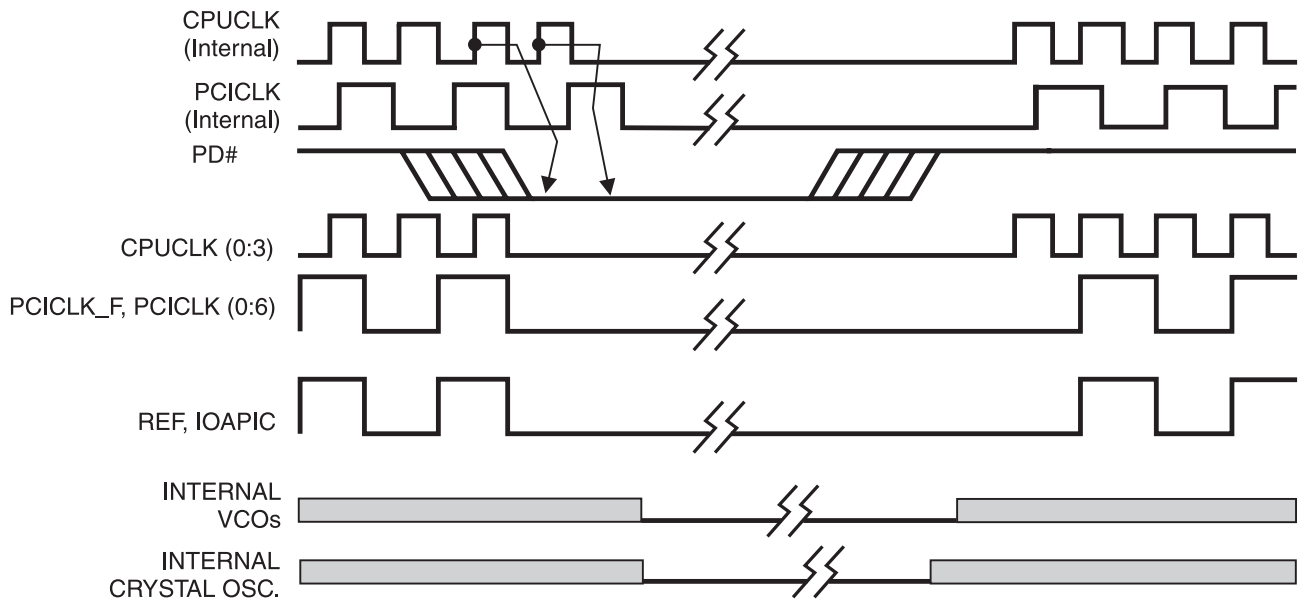
### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI\_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248-55.
3. All other clocks continue to run undisturbed.
4. PD# and CPU\_STOP# are shown in a high (true) state.



### PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internally by the ICS9248-55 prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3ms. The power down latency is less than three CPUCLK cycles. PCI\_STOP# and CPU\_STOP# are don't care signals during the power down operations.



**Notes:**

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9248.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.



## Absolute Maximum Ratings

|                               |                                      |
|-------------------------------|--------------------------------------|
| Supply Voltage                | 7.0 V                                |
| Logic Inputs                  | GND -0.5 V to V <sub>DD</sub> +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C                         |
| Storage Temperature           | -65°C to +150°C                      |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = V<sub>DDL</sub> = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER                      | SYMBOL                  | CONDITIONS  | MIN                  | TYP    | MAX                  | UNITS |
|--------------------------------|-------------------------|---|----------------------|--------|----------------------|-------|
| Input High Voltage             | V <sub>IH</sub>         |   | 2                    |        | V <sub>DD</sub> +0.3 | V     |
| Input Low Voltage              | V <sub>IL</sub>         |   | V <sub>SS</sub> -0.3 |        | 0.8                  | V     |
| Input High Current             | I <sub>IH</sub>         | V <sub>IN</sub> = V <sub>DD</sub>                                   |                      | 0.1    | 5                    | μA    |
| Input Low Current              | I <sub>IL1</sub>        | V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors             | -5                   | 2.0    |                      | μA    |
| Input Low Current              | I <sub>IL2</sub>        | V <sub>IN</sub> = 0 V; Inputs with pull-up resistors                | -200                 | -100   |                      | μA    |
| Operating Supply Current       | I <sub>DD3.3OP66</sub>  | C <sub>L</sub> = 0 pF; Select @ 66MHz                               |                      | 60     | 170                  | mA    |
|                                | I <sub>DD3.3OP100</sub> | C <sub>L</sub> = 0 pF; Select @ 100MHz                              |                      | 66     | 170                  | mA    |
| Power Down Supply Current      | I <sub>DD3.3PD</sub>    | C <sub>L</sub> = 0 pF; With input address to V <sub>DD</sub> or GND |                      | 70     | 600                  | μA    |
| Input frequency                | F <sub>i</sub>          | V <sub>DD</sub> = 3.3 V;  | 11                   | 14.318 | 16                   | MHz   |
| Input Capacitance <sup>1</sup> | C <sub>IN</sub>         | Logic Inputs  |                      |        | 5                    | pF    |
|                                | C <sub>INX</sub>        | X1 & X2 pins  | 27                   | 36     | 45                   | pF    |
| Transition Time <sup>1</sup>   | T <sub>trans</sub>      | To 1st crossing of target Freq.                                     |                      |        | 3                    | ms    |
| Settling Time <sup>1</sup>     | T <sub>s</sub>          | From 1st crossing to 1% target Freq.                                |                      | 5      |                      | ms    |
| Clk Stabilization <sup>1</sup> | T <sub>STAB</sub>       | From V <sub>DD</sub> = 3.3 V to 1% target Freq.                     |                      |        | 3                    | ms    |
| Skew <sup>1</sup>              | T <sub>CPU-PCI</sub>    | V <sub>T</sub> = 1.5 V;   | 1.5                  | 3      | 4                    | ns    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER                | SYMBOL                  | CONDITIONS                                       | MIN | TYP | MAX | UNITS |
|--------------------------|-------------------------|--|-----|-----|-----|-------|
| Operating Supply Current | I <sub>DD2.5OP66</sub>  | C <sub>L</sub> = 0 pF; Select @ 66.8 MHz         |     | 16  | 72  | mA    |
|                          | I <sub>DD2.5OP100</sub> | C <sub>L</sub> = 0 pF; Select @ 100 MHz          |     | 23  | 100 | mA    |
| Skew <sup>1</sup>        | t <sub>CPU-PCI2</sub>   | V <sub>T</sub> = 1.5 V; V <sub>TL</sub> = 1.25 V | 1.5 | 3   | 4   | ns    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



**Electrical Characteristics - CPUCLK**

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $V_{DDL} = 2.5 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

| PARAMETER              | SYMBOL                    | CONDITIONS                                       | MIN  | TYP  | MAX  | UNITS |
|------------------------|---------------------------|--|------|------|------|-------|
| Output High Voltage    | $V_{OH2B}$                | $I_{OH} = -12.0 \text{ mA}$                      | 2    | 2.3  |      | V     |
| Output Low Voltage     | $V_{OL2B}$                | $I_{OL} = 12 \text{ mA}$                         |      | 0.2  | 0.4  | V     |
| Output High Current    | $I_{OH2B}$                | $V_{OH} = 1.7 \text{ V}$                         |      | -41  | -19  | mA    |
| Output Low Current     | $I_{OL2B}$                | $V_{OL} = 0.7 \text{ V}$                         | 19   | 37   |      | mA    |
| Rise Time              | $t_{r2B}^1$               | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.0 \text{ V}$ |      | 1.25 | 1.6  | ns    |
| Fall Time              | $t_{f2B}^1$               | $V_{OH} = 2.0 \text{ V}, V_{OL} = 0.4 \text{ V}$ |      | 1    | 1.6  | ns    |
| Duty Cycle             | $d_{t2B}^1$               | $V_T = 1.25 \text{ V}$                           | 45   | 48   | 55   | %     |
| Skew                   | $t_{sk2B}^1$              | $V_T = 1.25 \text{ V}$                           |      | 30   | 175  | ps    |
| Jitter, Cycle-to-cycle | $t_{j\text{cyc-cyc}2B}^1$ | $V_T = 1.25 \text{ V}$                           |      | 150  | 200  | ps    |
| Jitter, One Sigma      | $t_{j1s2B}^1$             | $V_T = 1.25 \text{ V}$                           |      | 40   | 150  | ps    |
| Jitter, Absolute       | $t_{j\text{abs}2B}^1$     | $V_T = 1.25 \text{ V}$                           | -250 | 140  | +250 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - IOAPIC**

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $V_{DDL} = 2.5 \text{ V} \pm 5\%$ ;  $C_L = 20 \text{ pF}$

| PARAMETER                      | SYMBOL              | CONDITIONS                                       | MIN | TYP  | MAX | UNITS |
|--------------------------------|---------------------|--|-----|------|-----|-------|
| Output High Voltage            | $V_{OH4B}$          | $I_{OH} = -18 \text{ mA}$                        | 2   | 2.2  |     | V     |
| Output Low Voltage             | $V_{OL4B}$          | $I_{OL} = 18 \text{ mA}$                         |     | 0.33 | 0.4 | V     |
| Output High Current            | $I_{OH4B}$          | $V_{OH} = 1.7 \text{ V}$                         |     | -41  | -28 | mA    |
| Output Low Current             | $I_{OL4B}$          | $V_{OL} = 0.7 \text{ V}$                         | 29  | 37   |     | mA    |
| Rise Time <sup>1</sup>         | $T_{r4B}$           | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.0 \text{ V}$ |     | 1.5  | 2   | ns    |
| Fall Time <sup>1</sup>         | $T_{f4B}$           | $V_{OH} = 2.0 \text{ V}, V_{OL} = 0.4 \text{ V}$ |     | 1.3  | 2   | ns    |
| Duty Cycle <sup>1</sup>        | $D_{t4B}$           | $V_T = 1.25 \text{ V}$                           | 45  | 54   | 55  | %     |
| Skew <sup>1</sup>              | $t_{sk4B}^1$        | $V_T = 1.25 \text{ V}$                           |     | 60   | 250 | ps    |
| Jitter, One Sigma <sup>1</sup> | $T_{j1s4B}$         | $V_T = 1.25 \text{ V}$                           |     | 1    | 3   | %     |
| Jitter, Absolute <sup>1</sup>  | $T_{j\text{abs}4B}$ | $V_T = 1.25 \text{ V}$                           | -5  |      | 5   | %     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - PCICLK

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 30 \text{ pF}$

| PARAMETER                      | SYMBOL      | CONDITIONS                                       | MIN  | TYP | MAX | UNITS |
|--------------------------------|-------------|--|------|-----|-----|-------|
| Output High Voltage            | $V_{OH1}$   | $I_{OH} = -11 \text{ mA}$                        | 2.4  | 3.1 |     | V     |
| Output Low Voltage             | $V_{OL1}$   | $I_{OL} = 9.4 \text{ mA}$                        |      | 0.1 | 0.4 | V     |
| Output High Current            | $I_{OH1}$   | $V_{OH} = 2.0 \text{ V}$                         |      | -62 | -22 | mA    |
| Output Low Current             | $I_{OL1}$   | $V_{OL} = 0.8 \text{ V}$                         | 16   | 57  |     | mA    |
| Rise Time <sup>1</sup>         | $t_{r1}$    | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ |      | 1.5 | 2   | ns    |
| Fall Time <sup>1</sup>         | $t_{f1}$    | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ |      | 1.1 | 2   | ns    |
| Duty Cycle <sup>1</sup>        | $d_{t1}$    | $V_T = 1.5 \text{ V}$                            | 45   | 50  | 55  | %     |
| Skew <sup>1</sup>              | $t_{sk1}$   | $V_T = 1.5 \text{ V}$                            |      | 140 | 500 | ps    |
| Jitter, One Sigma <sup>1</sup> | $t_{j1s1}$  | $V_T = 1.5 \text{ V}$                            |      | 17  | 150 | ps    |
| Jitter, Absolute <sup>1</sup>  | $t_{jabs1}$ | $V_T = 1.5 \text{ V}$                            | -500 | 70  | 500 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - REF

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

| PARAMETER                      | SYMBOL      | CONDITIONS                                       | MIN | TYP  | MAX | UNITS |
|--------------------------------|-------------|--|-----|------|-----|-------|
| Output High Voltage            | $V_{OH5}$   | $I_{OH} = -12 \text{ mA}$                        | 2.6 | 3.1  |     | V     |
| Output Low Voltage             | $V_{OL5}$   | $I_{OL} = 9 \text{ mA}$                          |     | 0.17 | 0.4 | V     |
| Output High Current            | $I_{OH5}$   | $V_{OH} = 2.0 \text{ V}$                         |     | -44  | -22 | mA    |
| Output Low Current             | $I_{OL5}$   | $V_{OL} = 0.8 \text{ V}$                         | 29  | 42   |     | mA    |
| Rise Time <sup>1</sup>         | $t_{r5}$    | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ |     | 1.4  | 2   | ns    |
| Fall Time <sup>1</sup>         | $t_{f5}$    | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ |     | 1.1  | 2   | ns    |
| Duty Cycle <sup>1</sup>        | $d_{t5}$    | $V_T = 1.5 \text{ V}$                            | 45  | 53   | 55  | %     |
| Jitter, One Sigma <sup>1</sup> | $t_{j1s5}$  | $V_T = 1.5 \text{ V}$                            |     | 1    | 3   | %     |
| Jitter, Absolute <sup>1</sup>  | $t_{jabs5}$ | $V_T = 1.5 \text{ V}$                            |     | 3    | 5   | %     |

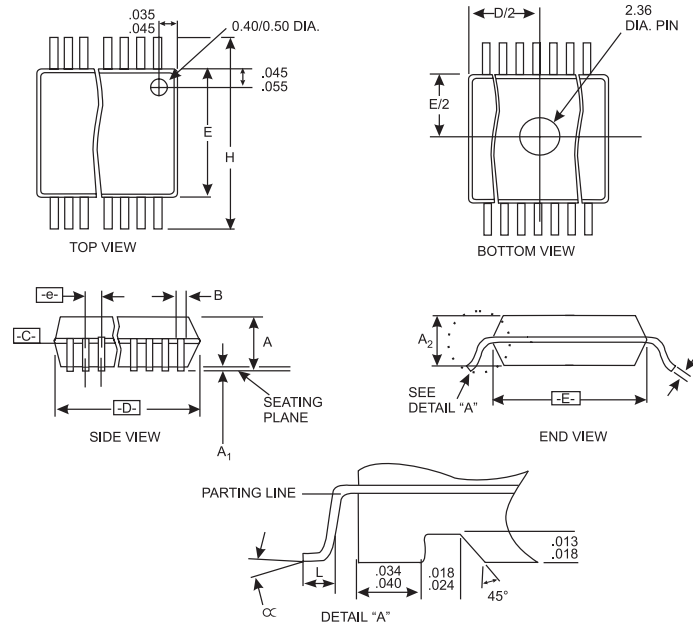
<sup>1</sup>Guaranteed by design, not 100% tested in production.



**Electrical Characteristics - 48 MHz** $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

| PARAMETER                       | SYMBOL       | CONDITIONS                                       | MIN | TYP  | MAX | UNITS |
|---------------------------------|--------------|--|-----|------|-----|-------|
| Frequency Accuracy <sup>1</sup> | $F_{ACC48m}$ |  |     |      | 167 | ppm   |
| Output High Voltage             | $V_{OH5}$    | $I_{OH} = -12 \text{ mA}$                        | 2.6 | 3    |     | V     |
| Output Low Voltage              | $V_{OL5}$    | $I_{OL} = 9 \text{ mA}$                          |     | 0.14 | 0.4 | V     |
| Output High Current             | $I_{OH5}$    | $V_{OH} = 2.0 \text{ V}$                         |     | -44  | -22 | mA    |
| Output Low Current              | $I_{OL5}$    | $V_{OL} = 0.8 \text{ V}$                         | 16  | 42   |     | mA    |
| Rise Time <sup>1</sup>          | $t_{r5}$     | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ |     | 1.2  | 4   | ns    |
| Fall Time <sup>1</sup>          | $t_{f5}$     | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ |     | 1.2  | 4   | ns    |
| Duty Cycle <sup>1</sup>         | $d_{t5}$     | $V_T = 1.5 \text{ V}$                            | 45  | 52   | 55  | %     |
| Jitter, One Sigma <sup>1</sup>  | $t_{j1s5}$   | $V_T = 1.5 \text{ V}$                            |     | 1    | 3   | %     |
| Jitter, Absolute <sup>1</sup>   | $t_{jabs5}$  | $V_T = 1.5 \text{ V}$                            |     | 3    | 5   | %     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



**SSOP Package**

| SYMBOL | COMMON DIMENSIONS |      |       | VARIATIONS | D    |      |      | N  |
|--------|-------------------|------|-------|------------|------|------|------|----|
|        | MIN.              | NOM. | MAX.  |            | MIN. | NOM. | MAX. |    |
| A      | .095              | .101 | .110  | AC         | .620 | .625 | .630 | 48 |
| A1     | .008              | .012 | .016  | AD         | .720 | .725 | .730 | 56 |
| A2     | .088              | .090 | .092  |            |      |      |      |    |
| B      | .008              | .010 | .0135 |            |      |      |      |    |
| C      | .005              | .006 | .0085 |            |      |      |      |    |
| D      | See Variations    |      |       |            |      |      |      |    |
| E      | .292              | .296 | .299  |            |      |      |      |    |
| e      | 0.025 BSC         |      |       |            |      |      |      |    |
| H      | .400              | .406 | .410  |            |      |      |      |    |
| h      | .010              | .013 | .016  |            |      |      |      |    |
| L      | .024              | .032 | .040  |            |      |      |      |    |
| N      | See Variations    |      |       |            |      |      |      |    |
| ∞      | 0°                | 5°   | 8°    |            |      |      |      |    |
| X      | .085              | .093 | .100  |            |      |      |      |    |

This table in inches

**Ordering Information**

**ICS9248BF-55**

Example:

**ICS XXXX F - PPP**

