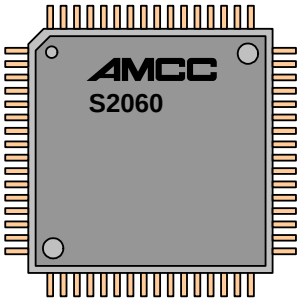


Description

The S2060 transmitter and receiver chip facilitates high speed serial transmission of data over fiber optic, coax, or twinax interfaces. The device is functionally compliant with the requirements of the IEEE 802.3z Gigabit Ethernet (GE) and ANSI X3T11 Fibre Channel (FC) specifications and operates at the full rates of 1250.0 and 1062.5 Mbps data rates, respectively, with an associated 10-bit data word. The device also provides half rate operation at 625 and 531 Mbps.

The chip provides parallel-to-serial and serial-to-parallel conversion, clock generation/recovery, and optional framing for 8B/10B encoded data. The on-chip transmit PLL synthesizes the high-speed clock from an external low-speed reference. The on-chip receive PLL performs clock recovery and data re-timing on the serial bit stream. The transmitter and receiver each support differential LVPECL compatible I/O for copper or fiber optic component interfaces with excellent signal integrity.

Local loopback mode allows for system diagnostics. The chip requires a +3.3 V power supply and dissipates typically 620 mW.

The S2060 can be used for a variety of applications including GE, FC, serial backplanes, and proprietary point-to-point links. Figure 1 shows a typical configuration incorporating the chip.

Overview

The S2060 transmitter and receiver provide serialization and deserialization (SERDES) functions for 8B/10B encoded data to implement a GE or FC interface. The sequence of transmitter and receiver functions are as follows:

Transmitter Operations:

1. 10-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

4. Clock and data recovery from serial input
5. Serial-to-parallel conversion
6. Frame detection
7. 10-bit parallel output

The 10-bit parallel data input to the S2060 should be from a DC-balanced encoding scheme, such as that of the 8B/10B transmission code1, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters.

– At a Glance –

Features

- 1250 MHz (Gigabit Ethernet) line rate
- 1062 MHz (Fibre Channel) line rate
- 531 MHz and 625 MHz half rate operation
- Functionally compliant to IEEE 802.3z Gigabit Ethernet and ANSI X3T11 Fibre Channel Specifications
- Receiver and Transmitter incorporates PLLs for clock/data recovery and synthesis
- Continuous downstream clocking from receiver
- 10-bit parallel LVTTL compatible I/O interface
- Low-jitter serial LVPECL compatible interface
- Local loopback
- Drives 30 m of Twinax cable directly
- Single +3.3 V supply, 620 mW power dissipation
- 64 PQFP or TQFP package with Green/RoHS compliant lead free options
- Commercial and industrial temperature range

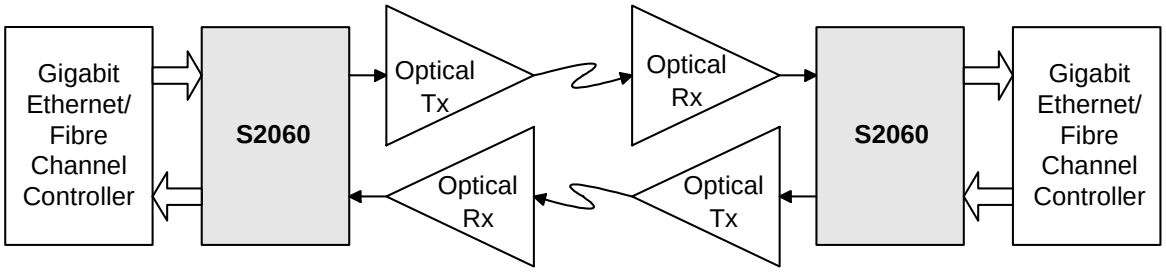


Figure 1. System Block Diagram

Prefix	Device	Package
S	2060	A: (64 PQFP 10mm) Standard Package, Commercial Temp QSC: (64 PQFP 10mm) Green/RoHS Compliant Package, Commercial Temp B: (64 PQFP 14mm) Standard Package, Commercial Temp D: (64 PQFP 14mm) Standard Package, Industrial Temp QSIAB: (64 PQFP 14mm) Green/RoHS Compliant Package, Industrial Temp C: (64 TQFP 10mm) Standard Package, Commercial Temp

X	XXXX	XXXXX
Prefix	Device	Package

Figure 2. S2060 Ordering Information

Applications

- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended back-planes

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