PANAVISION
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Image Sensor Products

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High Performance Linear Image Sensors
ELIS-1024 IMAGER

The Panavision SVI ELIS is a high performance linear image sensor designed to replace CCD's in a wide variety of applications, including:

- **Edge Detection**
- **Contact Imaging**
- **Bar Code Reading**
- **Finger Printing**
- **Encoding and Positioning**
- **Text Scanning**

P/N: ELIS-1024-LG
16-pin LCC package

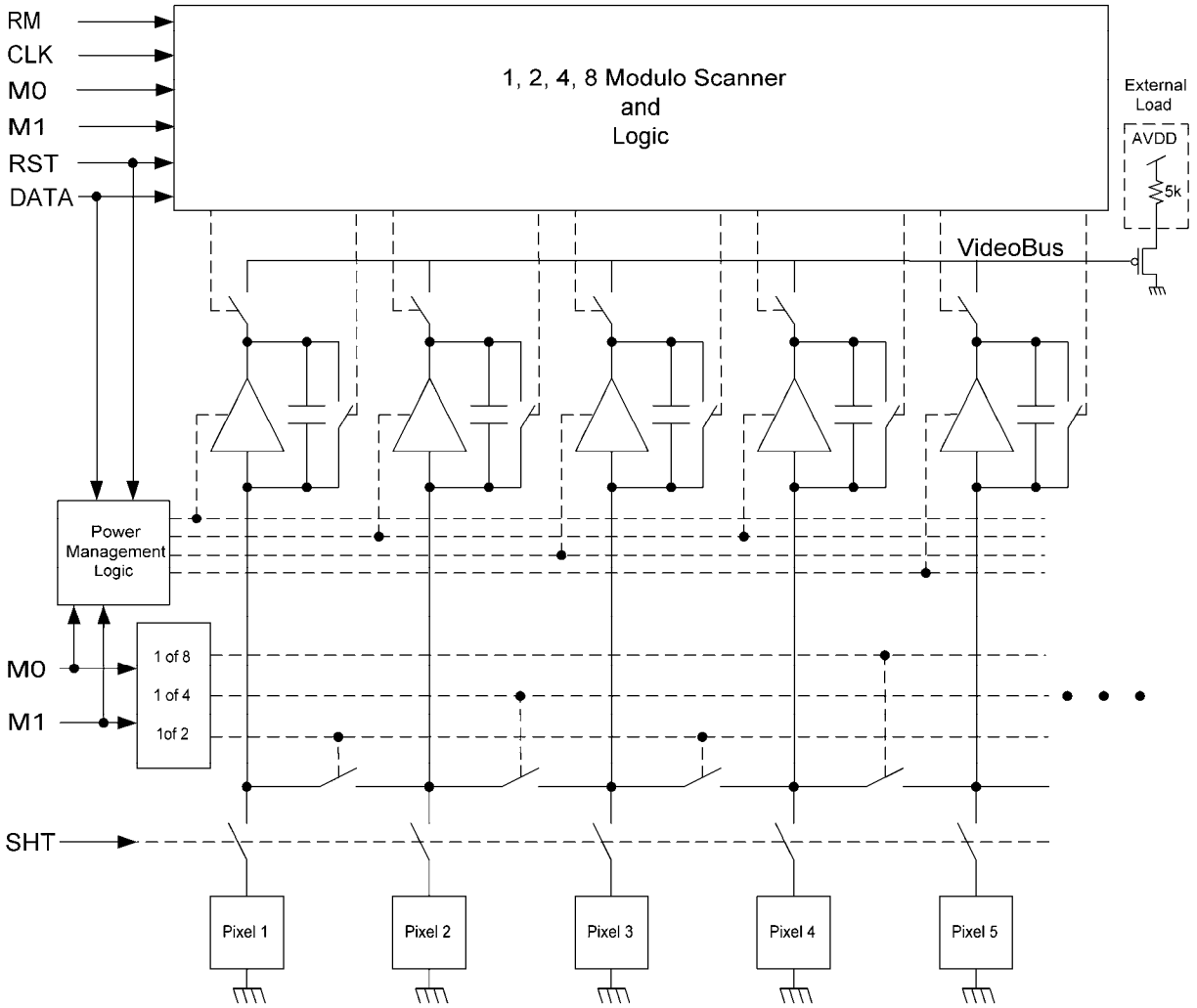
Description

The ELIS-1024 Linear Image Sensor consists of an array of high performance, low dark current photo-diode pixels. The sensor features sample and hold capability, selectable resolution and advanced power management. The device can operate at voltages as low as 2.8V making it ideal for portable applications. A key feature over traditional CCD technology is that the device can be read and reread Non-Destructively, allowing the user to maximize signal to noise and dynamic range. Internal logic automatically reduces power consumption when lower resolution settings are selected. A low power standby mode is also available to reduce system power consumption when the imager is not in use.

Key Features

- Low Cost
- Single Voltage Operation, Wide Operating Range
- Selectable Resolutions of 1024, 512, 256 and 128 pixels
- Intelligent Power Management and Low-Power Standby Mode
- Sample and Hold
- Full Frame Shutter and Dynamic Pixel Reset (DPR) Modes
- High Sensitivity
- High Signal to Noise
- Non-Destructive Read Capable, extremely low noise capable via signal averaging
- 1.0 kHz to 30.0 MHz Operation
- Very Low Dark Current
- Completely Integrated Timing and Control
- Replaces Entire CCD Systems, Not Just the Sensor

FUNCTIONAL BLOCK DIAGAM



PIN DESCRIPTION – 16-Pin LCC Package

1, 12	AGND		Analog Ground
2, 11	AVDD		Analog Power
3	DATA	Input	Start Readout
4	RST	Input	Reset
5	M0	Input	Bin Select Bit 0
6	M1	Input	Bin Select Bit 1
7	SHT	Input	Shutter
8, 9	N/C		No Connection
10	VOUT	Output	Analog Video Output (requires external pull-up resistor)
13	RM	Input	Reset Mode: RM = 0 for frame mode, RM = 1 for DPR mode
14	DVDD		Digital Power
15	DGND		Digital Ground
16	CLK	Input	Master Clock (@ pixel rate)

Electro-Optical Characteristics

Specs given at 24°C, 5.0V, 1MHz clock with 50% duty cycle and a 3200K light source unless otherwise noted.

Parameter	Min	Typical	Max	Units
Supply Voltage	2.80	5.0	5.5	V
Supply Current (see Note 1): Res = 1024 Res = 512 Res = 256 Res = 128		20.0 10.0 6.0 3.0		mA
Standby Current		16		µA
Input High Logic Level	V_{DD}-0.6V			V
Input Low Logic Level			0.6	V
Clock Frequency/Pixel Read Rate (see Note 3)	1.0	1000	30,000	kHz
External Pull-up Load		5000		Ω
Output Voltage at Saturation (see Note 4) Vsat	4.5	4.8		V
Output Voltage at Dark Vdark	1.9	2.1	2.5	V
Output Voltage Swing (Vsat – Vdark)	2.0	2.7		
Conversion Gain	0.40	0.51		$\mu V/e^-$
Full Well: Res = 1024 Res = 512 Res = 256 Res = 128		800 1600 3200 6400		ke^-
Dynamic Range	66	71		dB
Pixel Non-Uniformity Dark		±0.2	±0.5	%Sat
Photo Response Non-Uniformity		3%	8%	%Sat
Linearity (see Note 2)		0.3	0.5	%
Output due to Dark Current (note 6)		6		mV/s
Fill Factor		100		%Area
Absolute QE at peak (675nm)		60		%
Read Noise (see Note 5)		0.8	1.9	mVrms

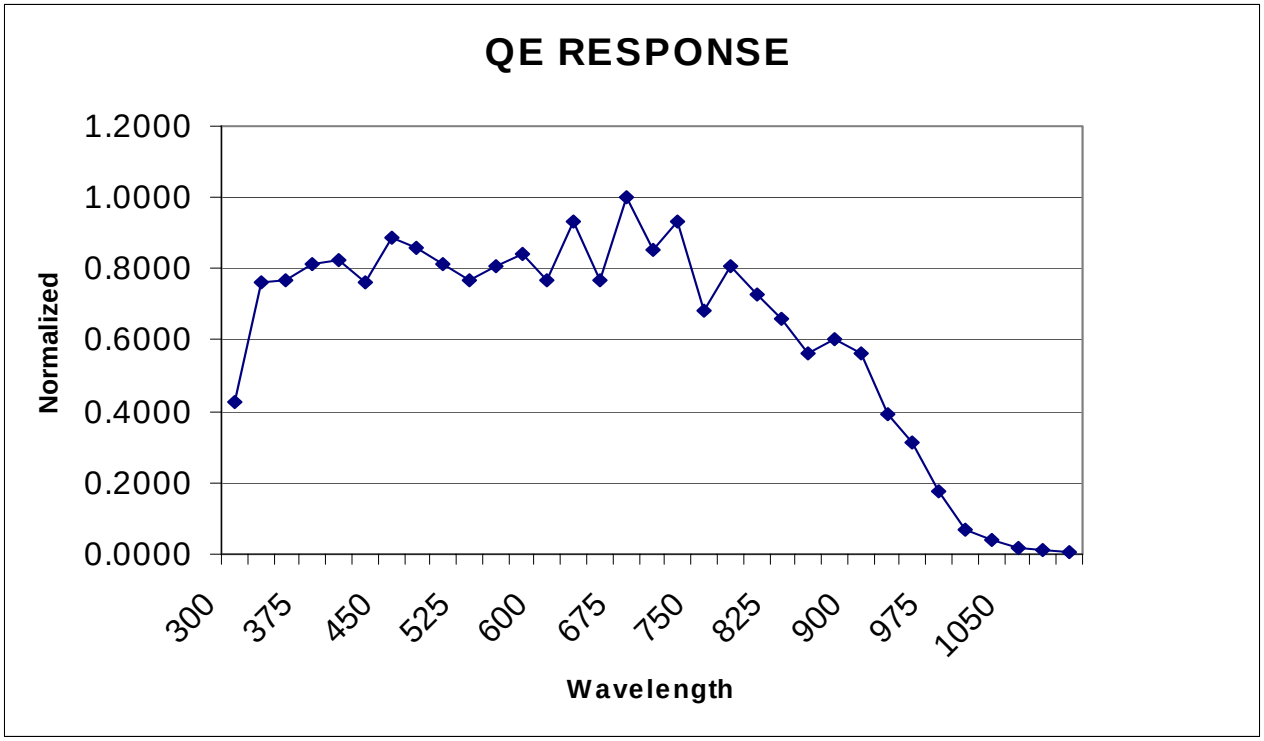
Notes
1. Includes 5k load resistor and measured at dark. Increased speed increases power consumption.
2. Pixel average from 5% - 75% saturation ass defined as the difference between the best fit straight line from the actual response from 5% to 75% of Vsat.
3. Specs given at pixel read rates of 1 MHz at 24°C. At greater read rates MTF and Dynamic Range begin to degrade. Higher speeds may not be possible at lower supply voltages.
4. At supply voltages less than saturation voltage, Vout is clipped by supply, no load applied.
5. Temporal rms noise @ 1 MHz pixel rate and 500kHz video bandwidth filter applied, values are typical and may vary. Higher Dynamic Range is possible with lower pixel rates and bandwidths.
6. Output due to dark current changes approximately 1.4mV/°C.
7. For characterization information and definitions, see section 'Characterization Criteria' at the end of this specification.

Absolute maximum ratings, T_A = 25°C unless otherwise noted, see Note 1, below. †

Supply voltage range, V_{DD} . . . . . 0 V to 6.0 V
Digital input current range, I_I . . . . . –16 mA to 16 mA
Operating case temperature range, T_C (see Note 2) . . . . . 0°C to 70°C
Operating free-air temperature range, T_A . . . . . 0°C to 50°C
Storage temperature range . . . . . –20°C to 85°C
Humidity range, RH . . . . . 0-100%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 10 seconds . . . . . 235°C

† Exceeding the ranges specified under "absolute maximum ratings" can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated under "recommended operating conditions" is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.

NOTES: 1. Voltage values are with respect to the device GND terminal.
2. Case temperature is defined as the surface temperature of the package measured directly over the integrated circuit.



Note: Data below 350nm not measured, but device is sensitive to 200 nm. The QE peaks at 675nm. Shown for un-encapsulated device.

Resolution Selection

By setting the M0 and M1 inputs as indicated in Table 1, several effective resolutions can be realized. The effective imager length is 7.987mm regardless of the selected resolution. Internally, the device has 1024 pixels. As the resolution decreases the effective pixel area increases as in Table 1. When the resolution is set to 512, the photodiodes of pixels 1 and 2 are averaged and output as a single value, pixels 3 and 4 are averaged and output as a single value, and so on. If set to 256 resolution, then pixels 1 through 4 are averaged and output as a single value, 5 through 8 are averaged and output as a single value, and so on. The internal control logic determines the resolution and always outputs a valid pixel per clock cycle. For example, if the imager is selected for 256-pixel resolution, then only 256 clock cycles are needed to read out the imager once DATA is set. Thus, for lower resolutions higher frame rates are possible as indicated in Table 1.

Table 1: Resolution Select.

M1	M0	Resolution	Effective Pixel Size	Maximum Frame Rate @ 1MHz (frames/s)
0	0	1024	7.8 x 125µm	976
0	1	512	15.6 x 125µm	1953
1	0	256	31.2 x 125µm	3906
1	1	128	64.4 x 125µm	7812

Power Management and Standby Mode

This device incorporates internally controlled power management features and an externally controlled low-power Standby Mode. When resolutions lower than 1024-pixels are selected, internal logic disables the unused amplifiers reducing the power consumption. Utilizing the existing external signals RST and DATA a low-power Standby Mode is possible. When RST and DATA are simultaneously held high the entire imager is put into Standby Mode. In this mode all internal amplifiers are disabled, the internal clocks are stopped and the output amplifier is also disabled. The clock can be held low or high or remain running while the imager is held in standby.

Frame Mode Timing (RM = 0)

In Frame Mode three signals are required for operation not including resolution selection and CLK. These being reset (RST), shutter (SHT) and start data readout (DATA). Both RST and SHT are asynchronous to the system clock, which allows unlimited reset and integration timing resolution.

Standard Timing

The timing relations for Standard Timing are shown in Figure 1 and detailed descriptions are given below. In the VIDEO waveform the 'X Clock Cycles' is determined by the resolution selected. The clock should be 50% duty cycle.

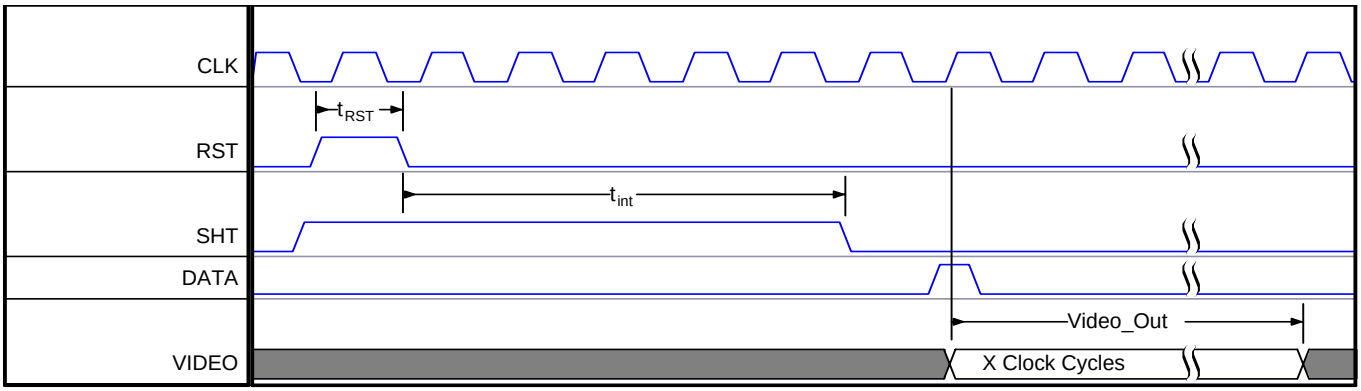


Figure 1: Start of Frame Timing Diagram.

Device Reset:
The pixels are simultaneously reset while the RST and SHT inputs are both held high for at least 200ns, as indicated by t_{RST}. The imager can be held in reset indefinitely by keeping both inputs high. When RST is high the internal clocks to the shift register are disabled and the shift register is held in reset. Once RST goes low the shift register comes out of reset and the clocks begin running.

Integration:
Once RST goes low (while SHT is high), the pixels begin to integrate. Integration continues until SHT goes low as indicated by t_{int}.

Readout:
Readout will begin on the first rising edge of CLK after the DATA input is set high. DATA must be brought low prior to the next rising edge of CLK, otherwise pixel 1 is again output along with pixel 2. See Figure 2 for details. The RST pulse always resets the internal shift register, thus the next pixel to be readout after the first rising edge of CLK when DATA is asserted is the first pixel. The timing details of the DATA pulse are shown below, t_D = 10ns.

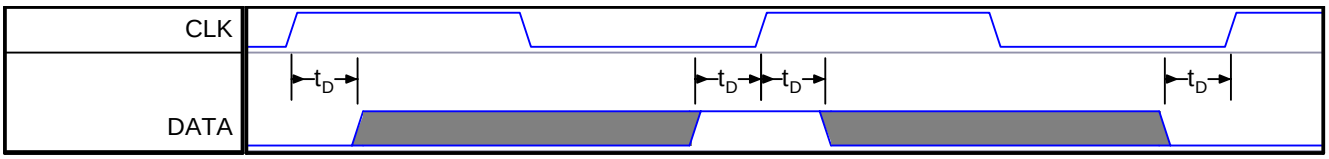


Figure 2: Detailed DATA Pulse Timing Diagram.

Non-Destructive Readout (NDRO)

NDRO mode is similar to the standard mode of operation except that the pixels are readout multiple times for a single integration time. The required signal timings are shown in Figure 3.

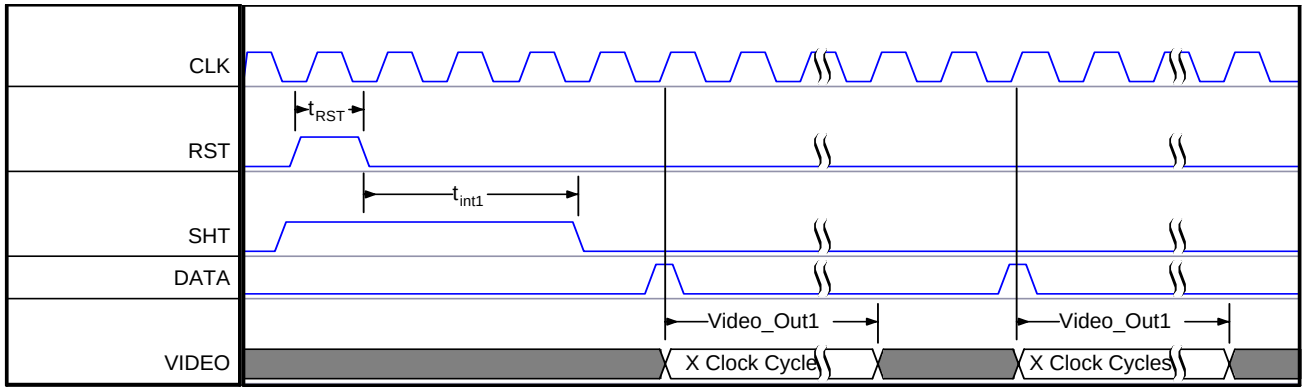


Figure 3: Non-Destructive Readout Timing Diagram.

Dynamic Pixel Reset (DPR) Mode Timing (RM = 1)

In DPR mode the pixels are reset by internal signals, which eliminates the need for using the external reset pin. When operating in DPR mode RST must be held low otherwise the internal logic will be held in reset. However, RST does NOT reset the pixels in DPR mode. Since the pixels are continuously integrating (except the one clock cycle they are being reset) the SHT pin should always be held high. The first frame readout will be invalid because the pixels will have been integrating for an unknown period of time. Valid video will be generated during the second frame. The required signal timings are illustrated in Figure 4.

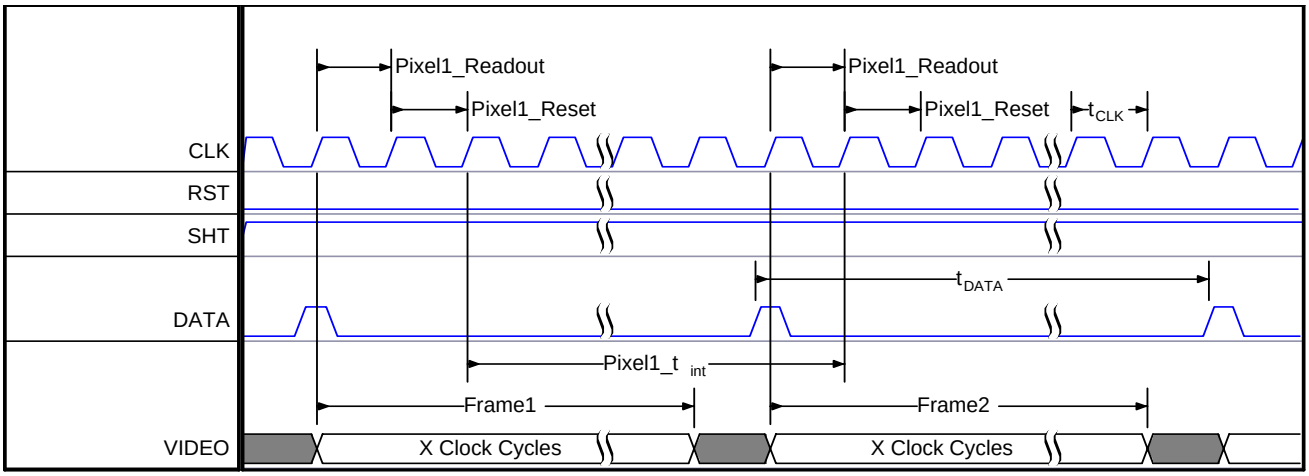


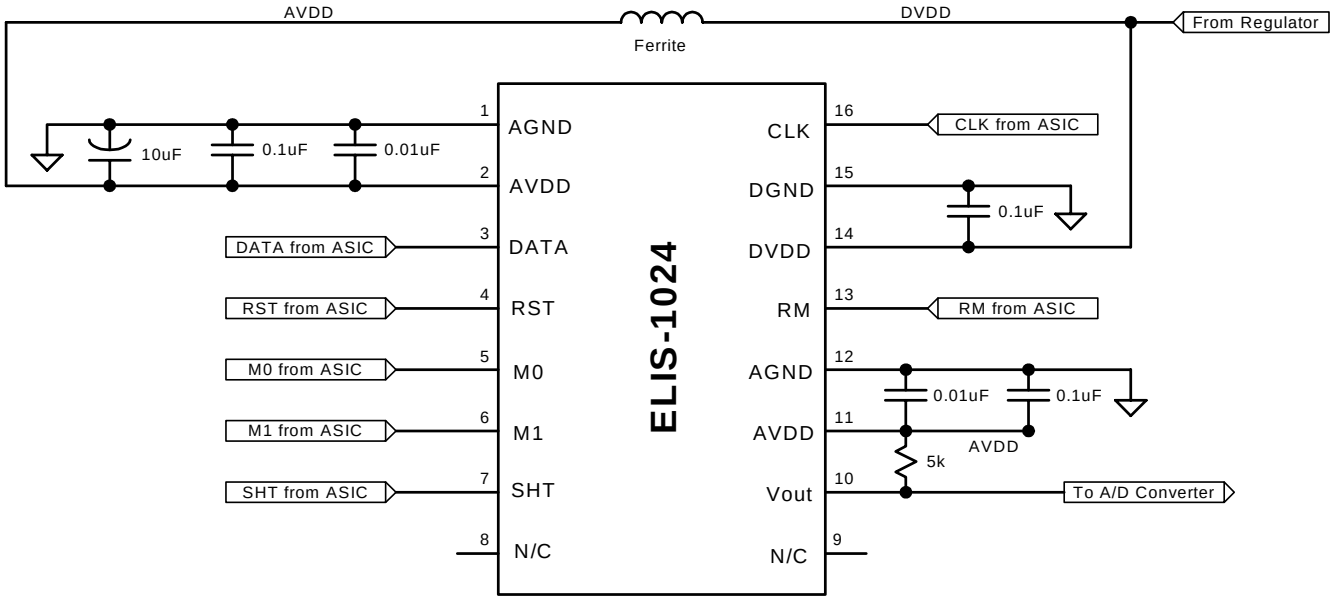
Figure 4: DPR Mode Timing Diagram.

Pixel 1 was used as an example to show the key timing situations. During the first clock cycle after DATA is high pixel 1 is readout. Then while pixel 2 is being readout during the second clock cycle pixel one is being reset. The integration time for pixel 1 then becomes the time between the rising

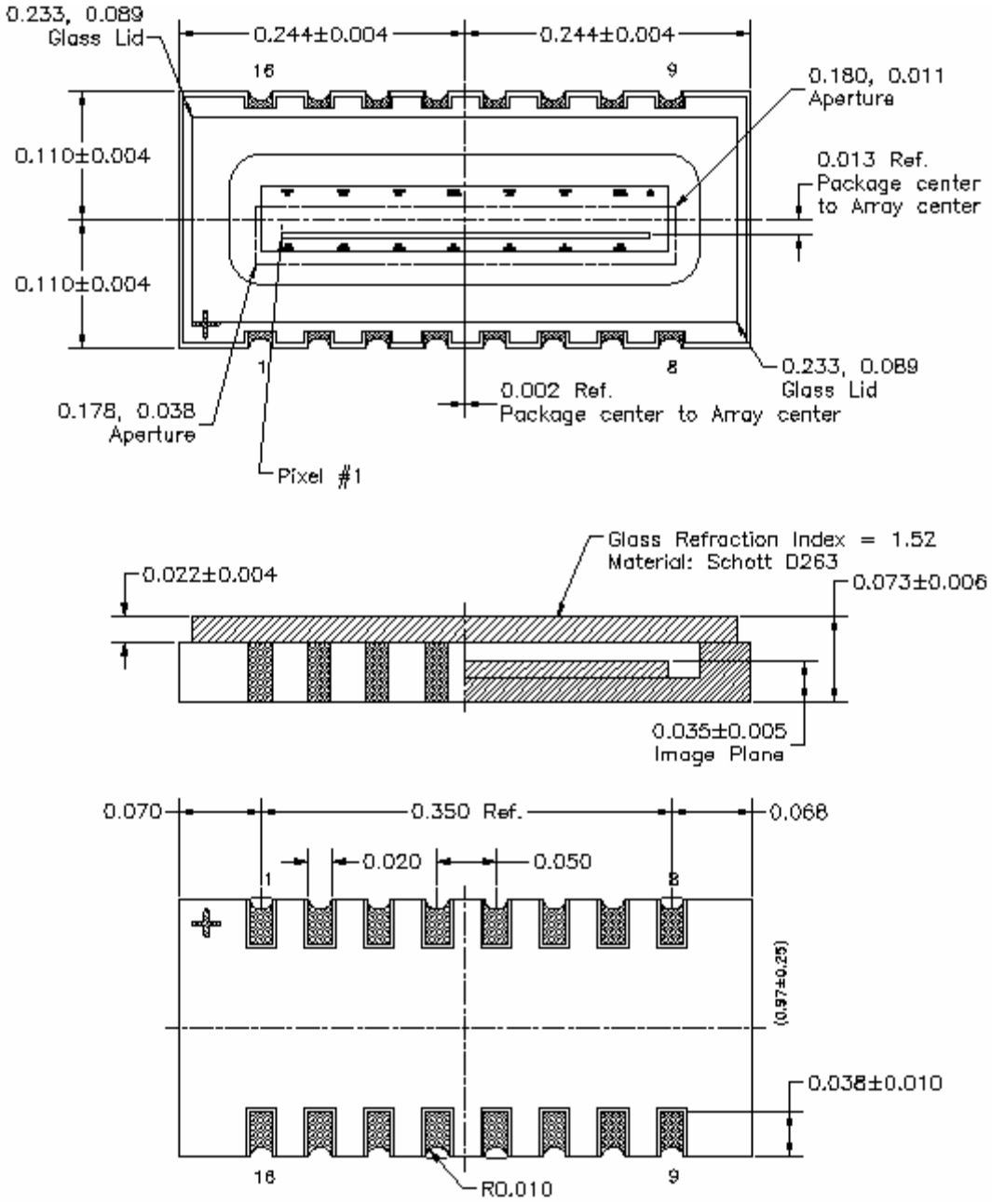
edge of the third clock pulse of Frame 1 to the rising edge of the second clock of Frame 2. In general the integration time is the period of DATA less one clock cycle ($t_{int} = t_{DATA} - t_{CLK}$). In reality the integration time ends when the signal is sampled by the external circuitry.

A one-clock cycle delay between the end of Frame 1 and start of Frame 2 is shown in Figure 4. This delay can be as low as zero clock cycles and as high as desired. There is no restriction to the delay between frames but at very long integration times dark current may become an issue.

Typical Application Circuit



LCC Package Mechanical Information



ORDERING INFORMATION

These devices are offered in a Leadless Chip Carrier package.

ELIS-1024-LG Leadless Chip Carrier (LCC)

Contact Panavision SVI, LLC or your local authorized representative for availability.

Characterization Criteria

Characterization measurements are guaranteed by design and are not tested for production parts. Unless otherwise specified, the measurements described herein are characterization measurements.

Pixel Clock Frequency

The pixel clock frequency is the frequency at which adjacent pixels can be reliably read.

Full Well

Full well (or Saturation Exposure) is the maximum number of photon-generated and/or dark current-generated electrons a pixel can hold. Full well is based on the capacitance of the pixel at a given bias. Full well is determined by measuring the capacitance of all pixels for the operational bias. In reality, the pixel analog circuitry will limit the signal swing on the pixel, so full well is defined as the number of electrons that will bring the output to the specified saturation voltage.

Quantum Efficiency

Quantum Efficiency is a measurement of the pixel ability to capture photon-generated charge as a function of wavelength. This is measured at 10nm increments over the wavelength range of the sensor typically over the range 300 to 1100 nm. Measurements are taken using a stable light source that is filtered using a monochromator. The exiting light from the monochromator is collimated to provide a uniform flux that overfills a portion of the sensor area. The flux at a given wavelength is measured using a calibrated radiometer and then the device under test is substituted and its response measured.

Linearity

Linearity is an equal corresponding output signal of the sensor for a given amount of photons incident on the pixel active area. Linearity is measured by plotting the imager transfer function from dark to saturation and fitting a 'best fit' straight line from 5% to 75% of saturation. The maximum peak-peak deviation of the output voltage from the 'best fit' straight line is computed (E_{pp}) over the fitting range. Linearity (L) is then computed as shown below where V_{FS} is the full-scale voltage swing from dark to saturation measured with sensor gain at 0.0 dB.

$$L = \left(1 - {E_{pp}}/{V_{FS}}\right) \times 100\%$$

Average Dark Offset

The 'dark offset' is the voltage proportional to the accumulated electrons for a given integration period, that were not photon generated i.e. dark current. There are a few sources in CMOS circuits for the dark current and the dark current levels will vary even for a given process. Dark offset is measured as the delta in output voltage from integration time 0 sec. to 1.0 sec with no light at $T_A = 24°C$.

Read Noise

Read noise is the temporal or time variant noise in the analog signal due to thermal noise in the analog path. Read noise does not include spatial noise such as fixed pattern noise (FPN). Read noise is measured at the output of the imager with proper loading and bandwidth filtering at 50% saturation and is calculated using the following;

$$TemporalRMSnoise = \sqrt{\frac{1}{1024}\sum_{i=1}^{1024}\sigma_i^2}$$

Image Lag

Image lag is the amount of residual signal in terms of percent of full well on the current frame of video after injecting the previous frame of video. Image lag is measured by illuminating an ROI to 50% of saturation for one frame and then rereading those pixels for the next and subsequent frames without light exposure. Any remaining residual signal will be measured and recorded in terms of percent of full well.

Dynamic Range

Dynamic range is determined by dividing the full-scale output voltage swing by the root mean squared (rms) temporal read noise voltage and expressed as a ratio or in decibels.

$$DR = 20\log\left[{V_{FS}}/{e_n}\right]$$

Modulation Transfer Function (MTF)

MTF is a measure of the imager's ability to sense and reproduce contrast as a function of spatial frequency. MTF is measured by illuminating a sensor with a Davidson Optronics PR-10 squarewave burst pattern having 11 discrete spatial frequencies. Therefore, strictly speaking, we are measuring Contrast Transfer Function (CTF) since squarewave targets are easier to obtain and work with. Images are captured with the input pattern oriented both horizontally and vertically and saved as 8-bit images. The sensor's response is derived from the captured images as shown below where M is the measured modulation and S_{MAX}, S_{MIN} are the digital numbers (DN) associated with the spatial frequency under evaluation.

$$M \equiv \frac{S_{MAX} - S_{MIN}}{S_{MAX} + S_{MIN}}$$

$$MTF \approx CTF \equiv M_{output} / M_{input}$$

Dark Signal Non-Uniformity (DSNU))

Dark signal non-uniformity (DSNU), also known as Fixed Pattern Noise (FPN), is a measure of pixel-to-pixel variation when the array is in the dark. It is primarily due to dark current differences, reset noise and synchronous timing effects. It is a signal-independent noise and is additive to the other noise powers. The FPN associated with the sensor consists of variations in pixel offset. Offset variations within any pixel are inherently low due to the ACS technology. Similarly, gain related FPN is almost non-existent due the ACS technology. FPN is measured as a peak-to-peak variation along a line of video averaged to remove temporal noise.

Photo-Response Non-Uniformity (PRNU)

Photo Response Nonuniformity is pixel-to-pixel variation in the response of an array to a fixed-intensity light.

$$PRNU \equiv \Delta X / Xm$$

Where Xm is the average of the total signal outputs and ΔX is the maximum deviation from Xm under uniform lighting and measured at about 50% of Vsat.

NOTICE

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