DATA SHEET



SAA7370A
Digital servo processor and Compact Disc decoder (CD7)

Product specification
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PHILIPS

Digital servo processor and Compact Disc decoder (CD7) SAA7370A

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Digital servo processor and Compact Disc decoder (CD7)

SAA7370A

1 FEATURES

- CD-ROM mode
- Up to 8 times-speed mode
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed-loop gain control available for focus and radial loops
- Pulsed sledge support
- Up to 80 kHz (8.4672 MHz crystal) or 16 MHz (16.9344 MHz crystal) jump performance
- Electronic damping of fast radial actuator during long jump
- Microcontroller loading LOW
- High level servo control option
- High level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I^2C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal for up to 4 times speed mode or 16.9344 MHz crystal for up to 8 times-speed mode.

2 GENERAL DESCRIPTION

The SAA7370A (CD7) is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.75	5.0	5.25	V
I_{DD}	supply current	n = 1 mode	–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		0	–	+70	°C
T_{stg}	storage temperature		–55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7370A	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

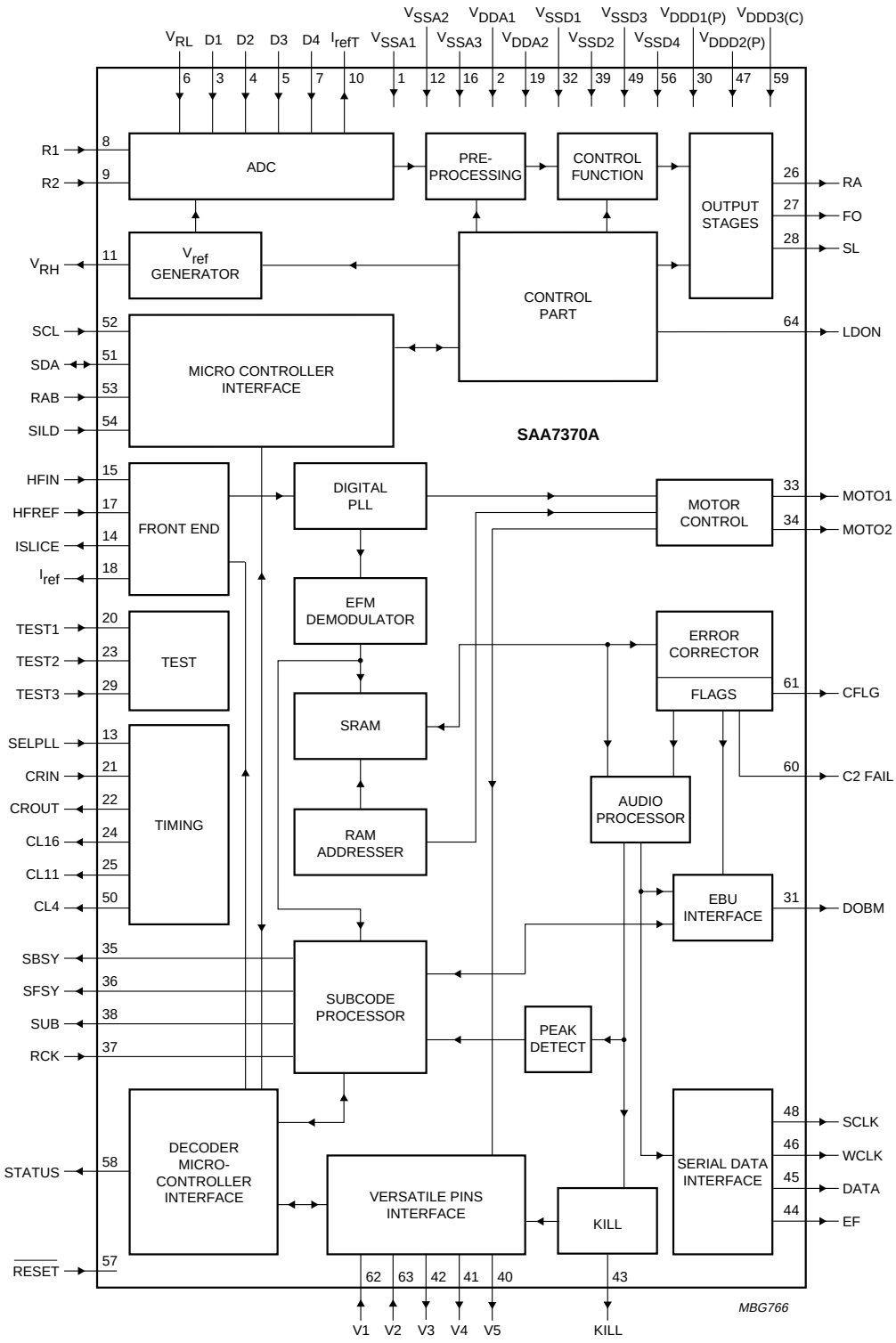


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz (or 33.8688 MHz) system clock output
CL11	25	11.2896 or 5.6448 MHz (or 22.5792 MHz) clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode bits output (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
EF	44	C2 error flag; output only defined in CD ROM modes (3-state)
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47(1)	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49(1)	digital ground 3
CL4	50	4.2336 MHz (or 8.4672 MHz) microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56(1)	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59(1)	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

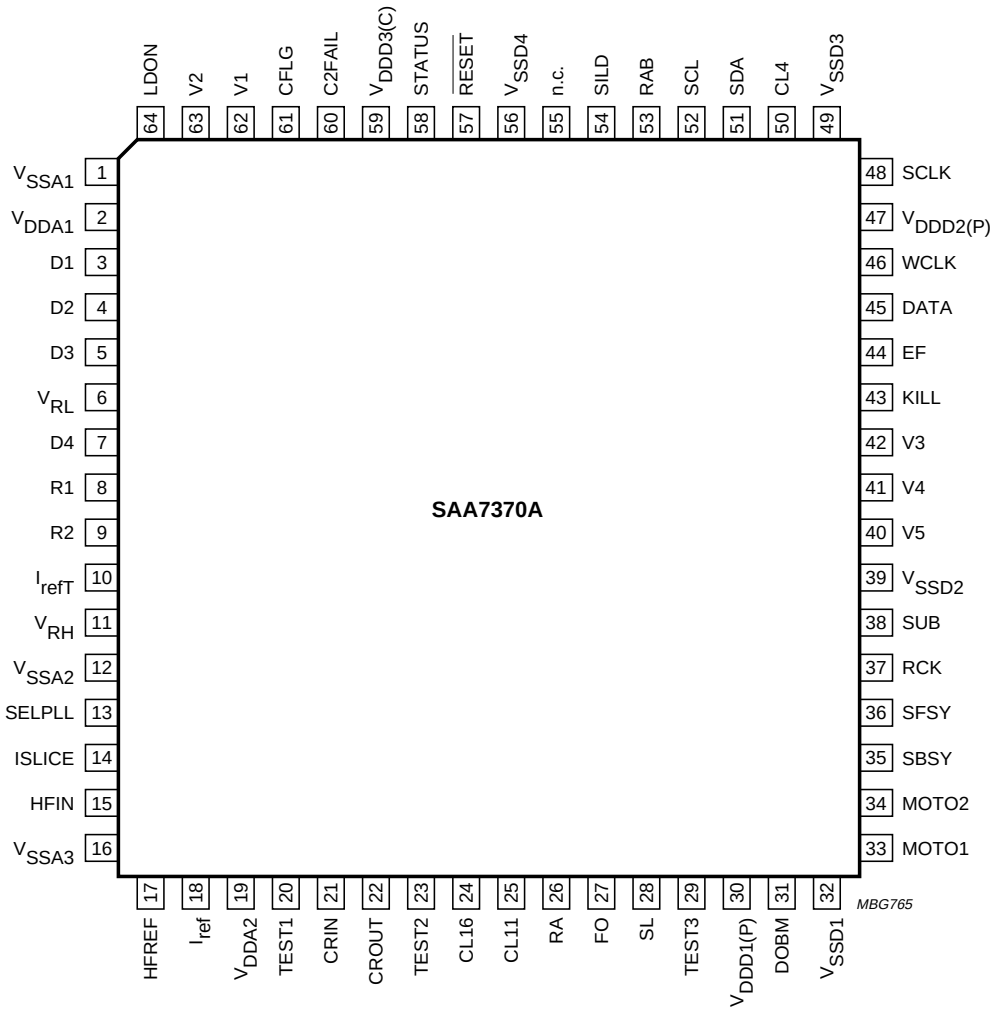


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Decoder part

7.1.1 PRINCIPLE OPERATIONAL MODES OF THE DECODER

The decoding part can operate at different disc speeds, from single-speed (n = 1) up to 8 times speed (n = 8). The factor 'n' is called the overspeed factor. A simplified data flow through the decoder part is illustrated in Fig.6.

7.1.2 DECODING SPEED AND CRYSTAL FREQUENCY

The SAA7370A is a multi-speed decoding device, with an internal phase-locked loop (PLL) clock multiplier. Depending on the crystal frequency used and the internal clock settings (selectable via registers B and E), the playback speeds shown in Table 1 are possible, where 'n' is the overspeed factor.

An internal clock multiplier is present, controlled by SELPLL, and should only be used if an 8.4672 MHz or 16.9344 MHz crystal, ceramic resonator or external clock is present.

7.1.3 LOCK-TO-DISC MODE

For high speed CD-ROM applications, the SAA7370A has a special mode, the lock-to-disc mode. This allows Constant Angular Velocity (CAV) disc playback with varying input data rates from the inside-to-outside of the disc. In the lock-to-disc mode, the FIFO is blocked and the decoder will adjust its output data rate to the disc speed. Hence, the frequency of the I^2S-bus (WCLK and SCLK) clocks are dependent on the disc speed.

In the lock-to-disc mode there is a limit on the maximum variation in disc speed that the SAA7370A will follow. Disc speeds must always be within 25% to 100% range of their nominal value. The lock-to-disc mode is enabled/disabled by register E.

7.1.4 STANDBY MODES

The SAA7370A may be placed in two standby modes selected by register B (it should be noted that the device core is still active):

Standby 1: 'CD-STOP' mode. Most I/O functions are switched off.

Standby 2: 'CD-PAUSE' mode. Audio output features are switched off, but the motor loop, the motor output and the subcode interfaces remain active. This is also called a 'Hot Pause'.

In the standby modes the various pins will have the following values:

MOTO1 and MOTO2: put in high-impedance, PWM mode (standby 1 and reset: operating in standby 2). Put in high-impedance, PDM mode (standby 1 and reset: operating in standby 2).

SCL, SDA, SILD and RAB: no interaction. Normal operation continues.

SCLK, WCLK, DATA, EF, CL11 and DOBM: 3-state in both standby modes. Normal operation continues after reset.

CRIN, CROUT, CL16 and CL4: no interaction. Normal operation continues.

V1, V2, V3, V4, V5, CFLG and C2FAIL: no interaction. Normal operation continues.

Table 1 Playback speeds

REGISTER B	REGISTER E	SELPLL	CRYSTAL FREQUENCY (MHz)			CL11 FREQUENCY (MHz)[2]
			33.8688	16.9344	8.4672	
00xx	0xxx	0	n = 1	–	–	11.2896
00xx	0xxx	1	–	n = 2[1]	n = 1	11.2896
01xx	0xxx	0	–	n = 1	–	5.6448
10xx	0xxx	0	n = 2	–	–	11.2896
10xx	0xxx	1	–	n = 4[1]	n = 2	11.2896
11xx	0xxx	0	–	n = 2[3]	–	5.6448
00xx	1xxx	0	n = 4[3]	–	–	11.2896
00xx	1xxx	1	–	n = 8[1]	n = 4	11.2896
01xx	1xxx	0	–	n = 4[3]	–	5.6448
10xx	1xxx	1	–	–	n = 8[3]	11.2896

Notes

1. Only if SELPLL = 1, then the CL11 output will be 22.5792 MHz, CL16 will be 33.8688 MHz and CL4 will be 8.4672 MHz.
2. The CL11 output is always a 5.6448 MHz clock if a 16.9344 MHz external clock is used and SELPLL = 0.
3. Data capture performance is not optimized for these options.

7.2 Crystal oscillator

The crystal oscillator is a conventional 2 pin design operating between 8 MHz and 35 MHz. This oscillator is capable of operating with ceramic resonators and with both fundamental and third overtone crystals. External components should be used to suppress the fundamental output of the third overtone crystals as shown in Figs 3 and 4. Typical oscillation frequencies required are 8.4672, 16.9344 or 33.8688 MHz depending on the internal clock settings used and whether or not the clock multiplier is enabled.

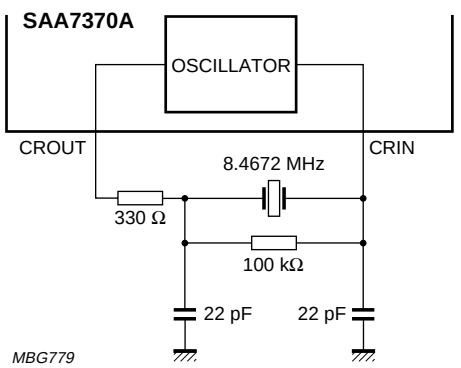


Fig.3 8.4672 MHz fundamental configuration.

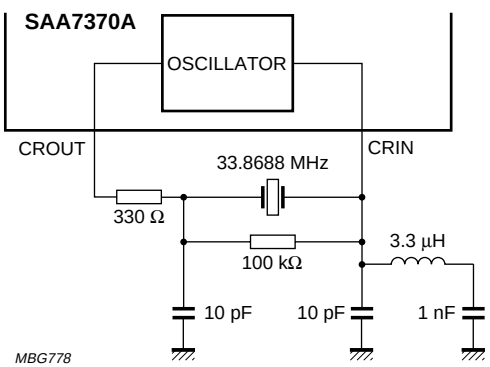


Fig.4 33.8688 MHz overtone configuration.

7.3 Data slicer and clock regenerator

The SAA7370A has an integrated slice level comparator which can be clocked by the crystal frequency clock, or 8 times the crystal frequency clock (if SELPLL is set HIGH while using an 8.4672 MHz crystal, and register 4 is set to 0xxx). The slice level is controlled by an internal current source applied to an external capacitor under the control of the Digital Phase-Locked Loop (DPLL).

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required and the bit clock is not output. The PLL has two registers (8 and 9) for selecting bandwidth and equalization.

For certain applications an offtrack input is necessary. This is internally connected from the servo part (its polarity can be changed by the foc_parm1 parameter), but may be input via the V1 pin if selected by register C. If this flag is HIGH, the SAA7370A will assume that its servo part is following on the wrong track, and will flag all incoming HF data as incorrect.

7.4 Demodulator

7.4.1 Frame sync protection

A double timing system is used to protect the demodulator from erroneous sync patterns in the serial data.
The master counter is only reset if:

- A sync coincidence detected; sync pattern occurs 588 ±1 EFM clocks after the previous sync pattern
- A new sync pattern is detected within ±6 EFM clocks of its expected position.

The sync coincidence signal is also used to generate the PLL lock signal, which is active HIGH after 1 sync coincidence found, and reset LOW if during 61 consecutive frames no sync coincidence is found.
The PLL lock signal can be accessed via the SDA or STATUS pins selected by register 2 and 7.

Also incorporated in the demodulator is a Run Length 2 (RL2) correction circuit. Every symbol detected as RL2 will be pushed back to RL3. To do this, the phase error of both edges of the RL2 symbol are compared and the correction is executed at the side with the highest error probability.

7.4.2 EFM demodulation

The 14-bit EFM data and subcode words are decoded into 8-bit symbols.

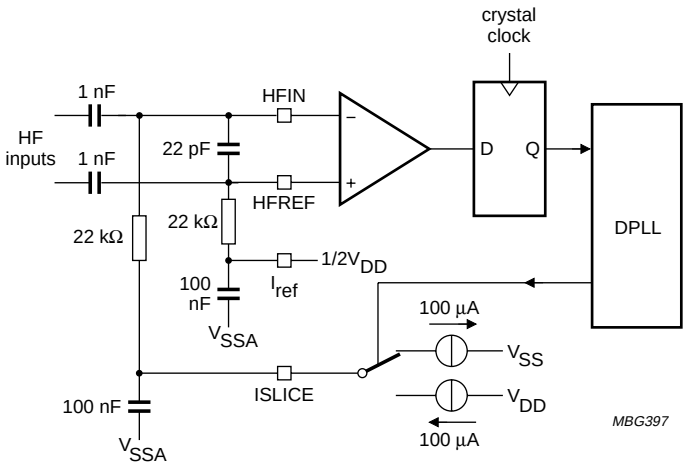


Fig.5 Data slicer showing typical application components (for n = 4).

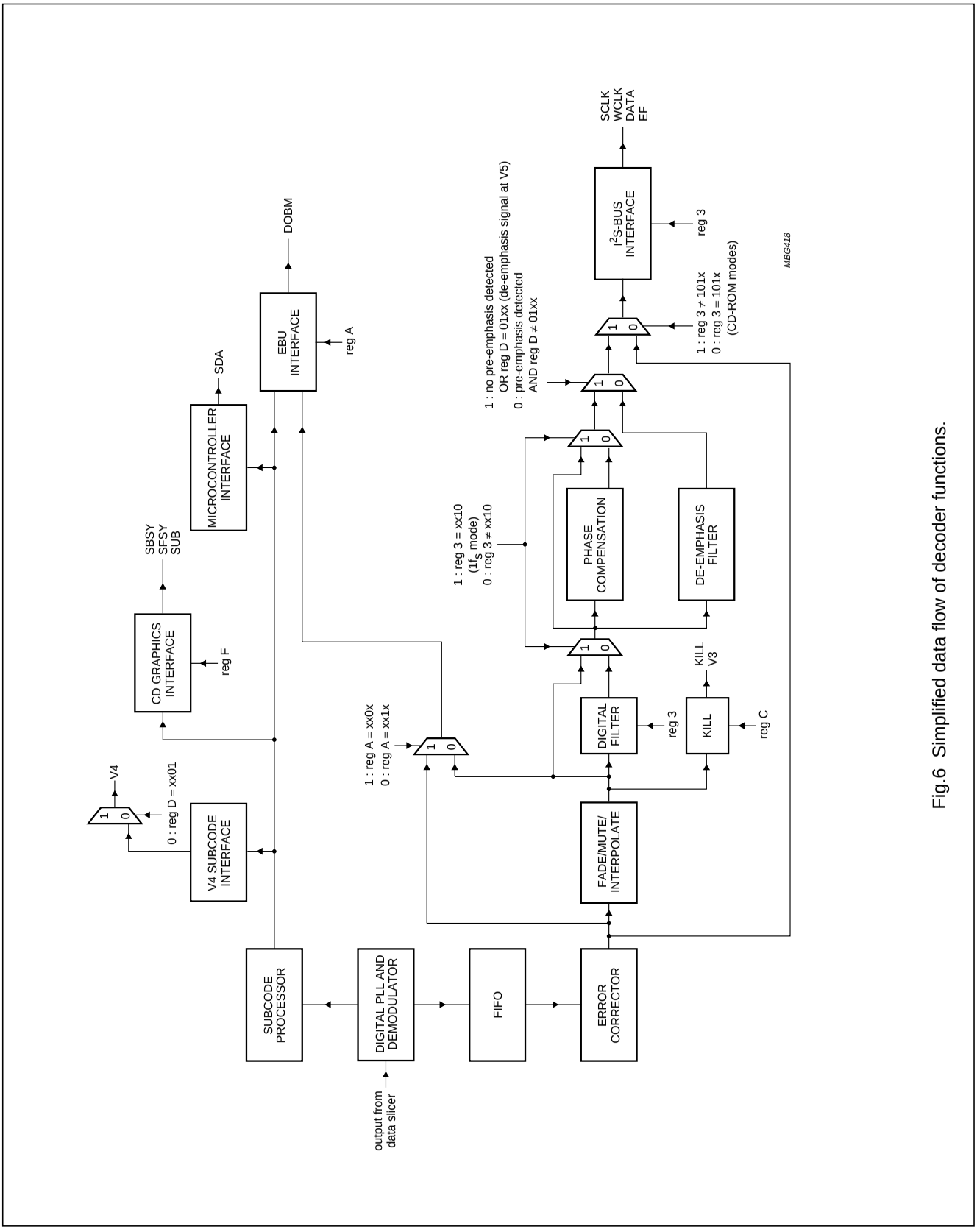


Fig.6 Simplified data flow of decoder functions.

7.5 Subcode data processing

7.5.1 Q-CHANNEL PROCESSING

The 96-bit Q-channel word is accumulated in an internal buffer. The last 16 bits are used internally to perform a Cyclic Redundancy Check (CRC). If the data is good, the SUBQREADY-I signal will go LOW. SUBQREADY-I can be read via the SDA or STATUS pins, selected via register 2. Good Q-channel data may be read from SDA.

7.5.2 EIAJ 3 AND 4-WIRE SUBCODE (CD GRAPHICS) INTERFACES

Data from all the subcode channels (P-to- W) may be read via the subcode interface, which conforms to EIAJ CP-2401. The interface is enabled and configured as either a 3-wire or 4-wire interface via register F.
The subcode interface output formats are illustrated in Fig.7, where the RCK signal is supplied by another device such as a CD graphics decoder.

7.5.3 V4 SUBCODE INTERFACE

Data of subcode channels, Q-to-W, may be read via pin V4 if selected via register D. The format is similar to RS232 and is illustrated in Fig.8. The subcode sync word is formed by a pause of (200/n) µs minimum. Each subcode byte starts with a logic 1 followed by 7 bits (Q-to-W). The gap between bytes is variable between (11.3/n) µs and (90/n) µs.

The subcode data is also available in the EBU output (DOBM) in a similar format.

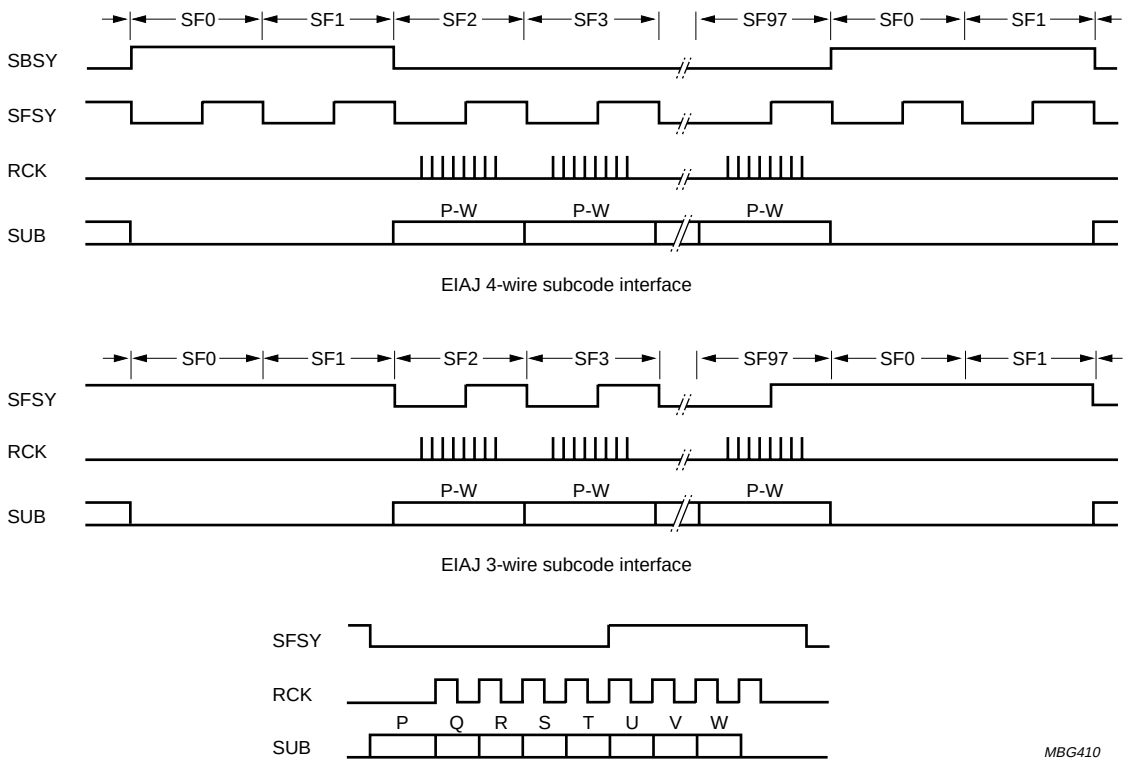
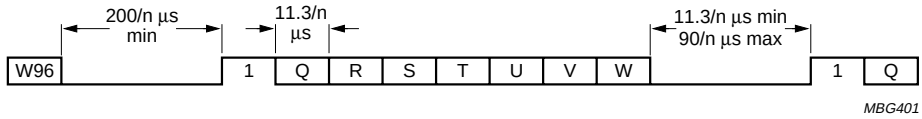


Fig.7 EIAJ subcode (CD graphics) interface format.



n = disc speed.

Fig.8 Subcode format and timing on pin V4.

7.6 FIFO and error corrector

The SAA7370A has a ±8 frame FIFO. The error corrector is a t = 2, e = 4 type, with error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. This error corrector can correct up to two errors on the C1 level and up to four errors on the C2 level.

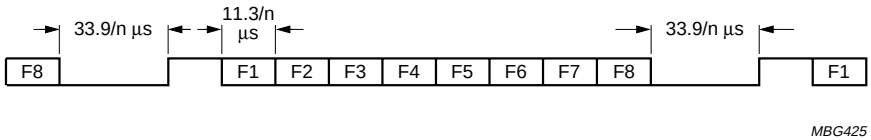
The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read after (de-interleaving) by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of uncorrectable errors. They are also output via the EBU signal (DOBM) and the EF output with I^2S-bus for CD-ROM applications.

7.6.1 FLAGS OUTPUT (CFLG)

The flags output pin CFLG (open-drain) shows the status of the error corrector and interpolator and is updated every frame (7.35 × n kHz). In the SAA7370A chip a 1-bit flag is present on the CFLG pin as illustrated in Fig.9. This signal shows the status of the error corrector and interpolator.

The first flag bit, F1, is the absolute time sync signal, the FIFO-passed subcode sync and relates the position of the subcode sync to the audio data (DAC output). This flag may also be used in a super FIFO or in the synchronization of different players. The output flags can be made available at bit 4 of the EBU data format (LSB of the 24-bit data word), if selected by register A.



n = disc speed.

Fig.9 Flag output timing diagram.

Table 2 Output flags

F1	F2	F3	F4	F5	F6	F7	F8	DESCRIPTION
0	x	x	x	x	x	x	x	no absolute time sync
1	x	x	x	x	x	x	x	absolute time sync
x	0	0	x	x	x	x	x	C1 frame contained no errors
x	0	1	x	x	x	x	x	C1 frame contained 1 error
x	1	0	x	x	x	x	x	C1 frame contained 2 errors
x	1	1	x	x	x	x	x	C1 frame uncorrectable
x	x	x	0	0	x	x	0	C2 frame contained no errors
x	x	x	0	0	x	x	1	C2 frame contained 1 error
x	x	x	0	1	x	x	0	C2 frame contained 2 errors
x	x	x	0	1	x	x	1	C2 frame contained 3 errors
x	x	x	1	0	x	x	0	C2 frame contained 4 errors
x	x	x	1	1	x	x	1	C2 frame uncorrectable
x	x	x	x	x	0	0	x	no interpolations
x	x	x	x	x	0	1	x	at least one 1-sample interpolation
x	x	x	x	x	1	0	x	at least one hold and no interpolations
x	x	x	x	x	1	1	x	at least one hold and one 1-sample interpolation

7.6.2 C2FAIL

The C2FAIL pin indicates that invalid data has occurred on the I²S-bus interface. However, due to the structure of the corrector it is impossible to determine which byte has failed. C2FAIL will go LOW for (140/n) µs when invalid data is detected, this data may then occur (15/n) µs before or after the pin is activated.

7.7 Audio functions

7.7.1 De-emphasis and phase linearity

When pre-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section controls the phase of the digital oversampling filter to $\leq \pm 1°$ within the band 0 to 16 kHz. With de-emphasis the filter is not phase linear.

If the de-emphasis signal is set to be available at V5, selected via register D, then the de-emphasis filter is bypassed.

7.7.2 Digital oversampling filter

The SAA7370A contains a 2 to 4 times oversampling IIR filter. The filter specification of the 4 times oversampling filter is given in Table 3.

These attenuations do not include the sample-and-hold at the external DAC output or the DAC post filter. When using the oversampling filter, the output level is scaled –0.5 dB down, to avoid overflow on full scale sine wave inputs (0 to 20 kHz).

Table 3 Filter specification

PASS BAND	STOP BAND	ATTENUATION
0 to 9 kHz	–	≤0.001 dB
19 to 20 kHz	–	≤0.03 dB
–	24 kHz	≥25 dB
–	24 to 27 kHz	≥38 dB
–	27 to 35 kHz	≥40 dB
–	35 to 64 kHz	≥50 dB
–	64 to 68 kHz	≥31 dB
–	68 kHz	≥35 dB
–	69 to 88 kHz	≥40 dB

7.7.3 CONCEALMENT

A 1 sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators. If more than one consecutive non-correctable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample (see Fig.10).

In CD ROM modes (i.e. the DAC interface is selected to be in a CD ROM format) concealment is not executed.

7.7.4 MUTE, FULL-SPEED, ATTENUATION AND FADE

A digital level controller is present on the SAA7370A which performs the functions of soft mute, full scale, attenuation and fade; these are selected via register 0:

Mute: signal reduced to 0 in a maximum of 128 steps; (3/n) μs.

Attenuate: signal scaled by –12 dB.

Full scale: ramp signal back to 0 dB level. From mute takes (3/n) μs.

Fade: activates a 128 stage counter which allows the signal to be scaled up/down by 0.07 dB steps

128 = full scale.

120 = –0.5 dB (i.e. full scale if oversampling filter used).

32 = –12 dB.

0 = mute.

7.7.5 PEAK DETECTOR

The peak detector measures the highest audio level (absolute value) on positive peaks for left and right channels. The 8 most significant bits are output in the Q-channel data in place of the CRC bits. Bits 81 to 88 contain the left peak value (bit 88 = MSB) and bits 89 to 96 contain the right peak value (bit 96 = MSB). The values are reset after reading Q-channel data via SDA.

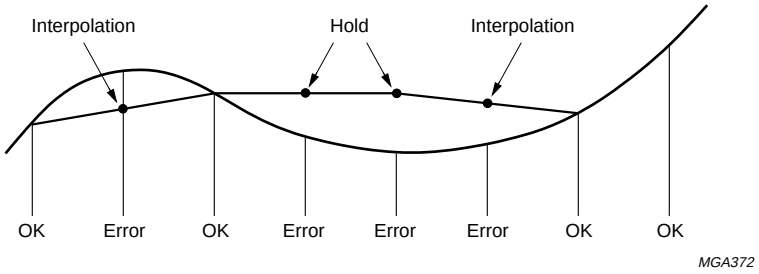


Fig.10 Concealment mechanism.

7.8 DAC interface

The SAA7370A is compatible with a wide range of digital-to-analog converters (DACs). Eleven formats are supported and are given in Table 4. Figures 11 and 12 show the Philips I^{2}S-bus and the EIAJ data formats respectively. When the decoder is operated in lock-to-disc mode, the SCLK frequency is dependent on the disc speed factor 'd'. All formats are MSB first and f_s is (44.1 × n) kHz. The polarity of the WCLK and the data can be inverted; selectable by register 7.
It should be noted that EF is only a defined output in CD ROM modes.

Table 4 DAC interface formats

REGISTER 3	SAMPLE FREQUENCY	NUMBER OF BITS	SCLK (MHz)	FORMAT	INTERPOLATION
1010	f_s	16	2.1168 × n	CD ROM (I^{2}S-bus)	no
1011	f_s	16	2.1168 × n	CD ROM (EIAJ)	no
1110	f_s	16/18[1]	2.1168 × n	Philips I^{2}S-bus 16/18 bits[1]	yes
0010	f_s	16	2.1168 × n	EIAJ 16 bits	yes
0110	f_s	18	2.1168 × n	EIAJ 18 bits	yes
0000	$4f_s$[2]	16	8.4672 × n	EIAJ 16 bits	yes
0100	$4f_s$[2]	18	8.4672 × n	EIAJ 18 bits	yes
1100	$4f_s$[2]	18	8.4672 × n	Philips I^{2}S-bus 18 bits	yes
0011	$2f_s$	16	4.2336 × n	EIAJ 16 bits	yes
0111	$2f_s$	18	4.2336 × n	EIAJ 18 bits	yes
1111	$2f_s$	18	4.2336 × n	Philips I^{2}S-bus 18 bits	yes

Notes

1. in this mode the first 16 bits contain data, but if any of the fade, attenuate or de-emphasis filter functions are activated then the first 18 bits contain data.
2. Cannot be used in the n = 8 mode.

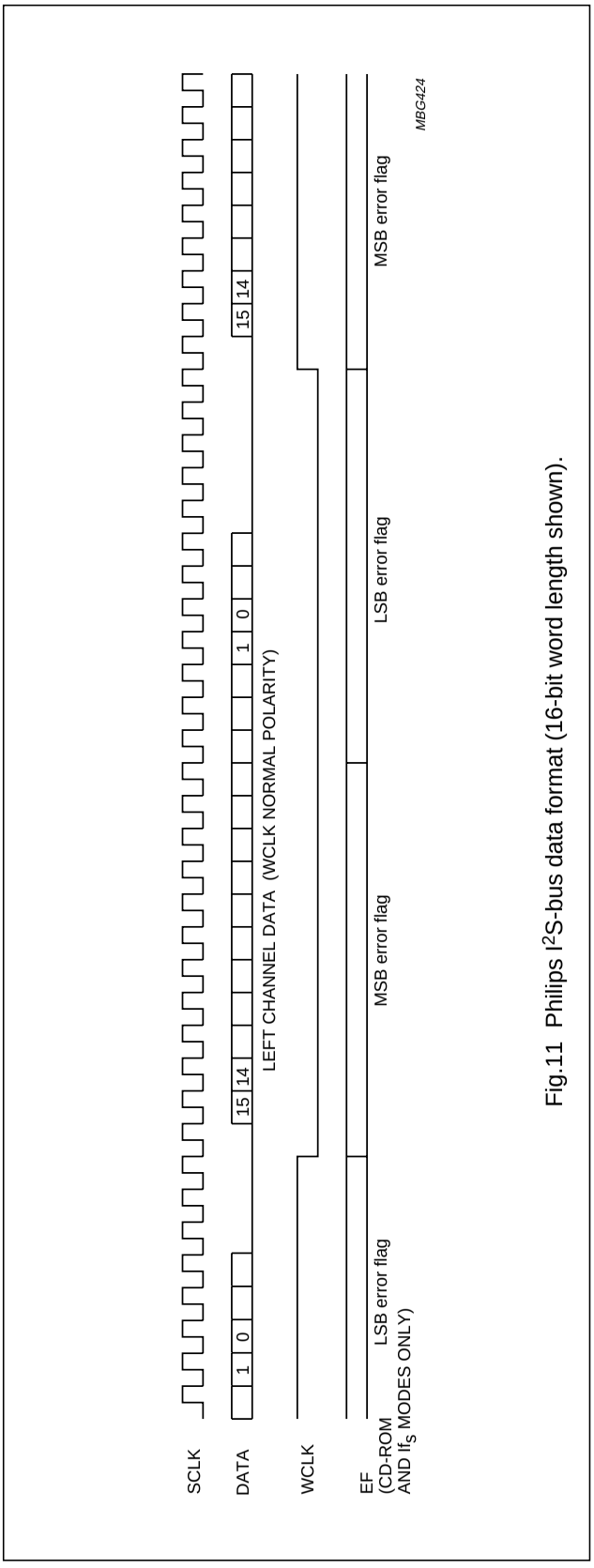


Fig.11 Philips I²S-bus data format (16-bit word length shown).

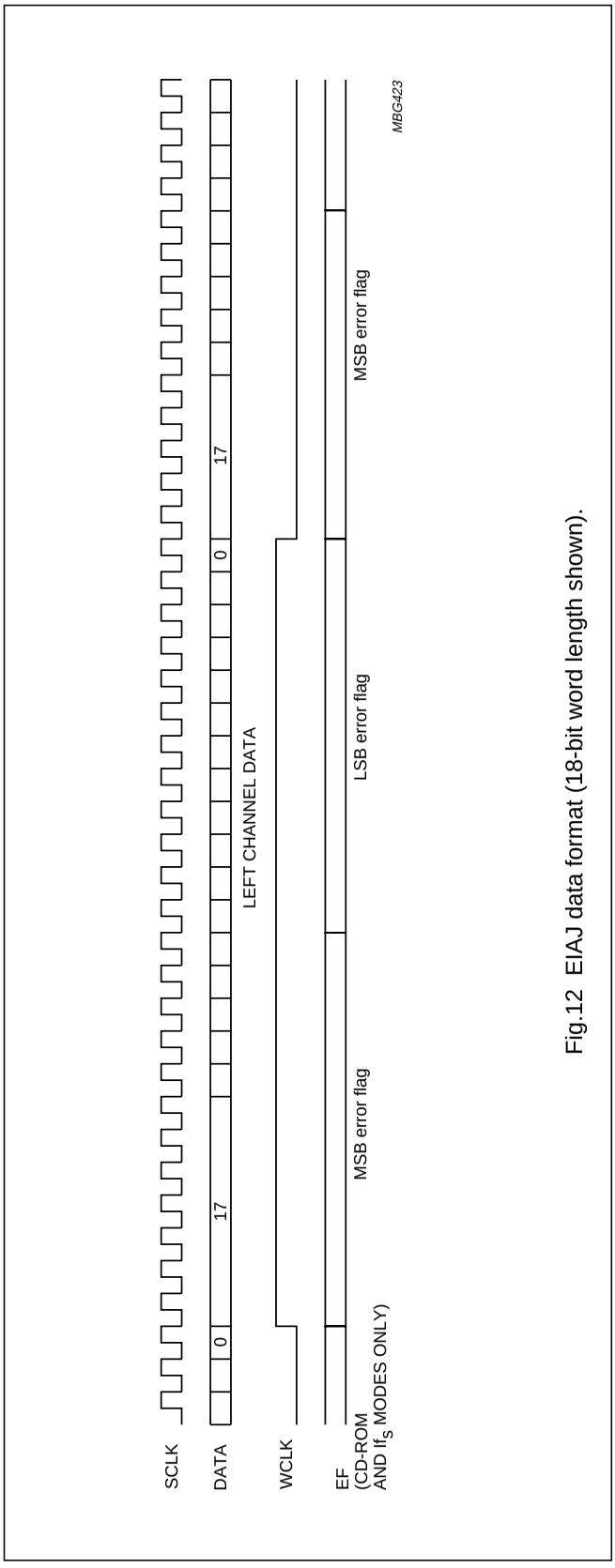


Fig.12 EIAJ data format (18-bit word length shown).

7.9 EBU interface

The bi-phase mark digital output signal at pin DOBM is in accordance with the format defined by the IEC958 specification. Three different modes can be selected via register A;

- DOBM pin held LOW.
- Data taken before concealment, mute and fade (must always be used for CD ROM modes).
- Data taken after concealment, mute and fade.

7.9.1 FORMAT

The digital audio output consists of 32-bit words ('subframes') transmitted in bi-phase mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384. Table 5 gives the formats.

Table 5 Format

FUNCTION	BITS	DESCRIPTION
Sync	0 to 3	–
Auxiliary	4 to 7	not used; normally zero
Error flags	4	CFLG error and interpolation flags when selected by register A
Audio sample	8 to 27	first 4 bits not used (always zero). 2's compliment. LSB = bit 12, MSB = bit 27
Validity flag	28	valid = logic 0
User data	29	used for subcode data (Q-to-W)
Channel status	30	control bits and category code
Parity bit	31	even parity for bits 4 to 30

Table 6 Description of Table 5

FUNCTION	DESCRIPTION
Sync	The sync word is formed by violation of the bi-phase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The 3 different sync patterns indicate the following situations: sync B: start of a block (384 words), word contains left sample; sync M: word contains left sample (no block start) and sync W: word contains right sample.
Audio sample	Left and right samples are transmitted alternately.
Validity flag	Audio samples are flagged (bit 28 = 1) if an error has been detected but was uncorrectable. This flag remains the same even if data is taken after concealment.
User data	Subcode bits Q-to-W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.
Channel status	The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is given in Table 7.

Table 7 Bit assignment

FUNCTION	BITS	DESCRIPTION
Control	0 to 3	copy of CRC checked Q-channel control bits 0 to 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has pre-emphasis
Reserved mode	4 to 7	always zero
Category code	8 to 15	CD: bit 8 = logic, all other bits = logic 0
Clock accuracy	28 to 29	set by register A; 10 = level I; 00 = level II; 01 = level III
Remaining	6 to 27 and 30 to 191	always zero

7.10 KILL circuit

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left or right channel before the digital filter. The output is switched active LOW when silence has been detected for at least 250 ms, or if mute is active, or in CD-ROM modes. Two modes are available which can be selected by register C;

1 pin kill: KILL active LOW indicates silence detected on both left and right channels.

2 pin kill: KILL active LOW indicates silence detected on left channel. V3 active LOW indicates silence detected on right channel.

It should be noted that when mute is active or in CD-ROM modes the output(s) are switched LOW.

7.11 Audio features off

The audio features can be turned off (selected by register E) which affects the following functions;

- Digital filter, fade, peak detector, KILL circuit (but outputs KILL, V3 still active) are disabled.
- V5 (if selected to be the de-emphasis flag output) and the EBU outputs become undefined.

It should be noted that the EBU output should be set LOW prior to switching the audio features off and after switching audio features back on a full-scale command should be given.

7.12 The VIA interface

The SAA7370A has five pins that can be reconfigured for different applications (see Table 8).

Table 8 Pin applications

PIN NAME	PIN NUMBER	TYPE	CONTROL REGISTER ADDRESS	CONTROL REGISTER DATA	FUNCTION
V1	62	input	1100	xxx1	external offtrack signal input
			–	xxx0	internal offtrack signal used Input may be read via decoder status bit; selected via register 2
V2	63	input	–	–	input may be read via decoder status bit; selected via register 2
V3	42	output	1100	xx0x	KILL output for right channel
			–	x01x	output = 0
			–	x11x	output = 1
V4	41	output	1101	0000	4-line motor drive (using V4 and V5)
			–	xx01	Q-to-W subcode output
			–	xx10	output = 0
			–	xx11	output = 1
V5	40	output	1101	01xx	de-emphasis output (active HIGH)
			–	10xx	output = 0
			–	11xx	output = 1

7.13 Spindle motor control

7.13.1 MOTOR OUTPUT MODES

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal ±8 frame FIFO and disc speed information are used to calculate the motor control output signals. Several output modes, selected by register 6, are supported:

- Pulse density, 2-line (true complement output), $(1 \times n)$ MHz sample frequency
- PWM output, 2-line, $(22.05 \times n)$ kHz modulation frequency
- PWM output, 4-line, $(22.05 \times n)$ kHz modulation frequency
- CDV motor mode.

7.13.1.1 Pulse density output mode

In the pulse density mode the motor output pin (MOTO1) is the pulse density modulated motor output signal. A 50% duty factor corresponds with the motor not actuated, higher duty factors mean acceleration, lower mean braking. In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a $(1 \times n)$ MHz internal clock signal. Possible application diagrams are illustrated in Fig.13.

7.13.1.2 PWM output mode (2-line)

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output. The motor braking signal is pulse-width modulated on the MOTO2 output. The timing is illustrated in Fig.14. A typical application diagram is illustrated in Fig.15.

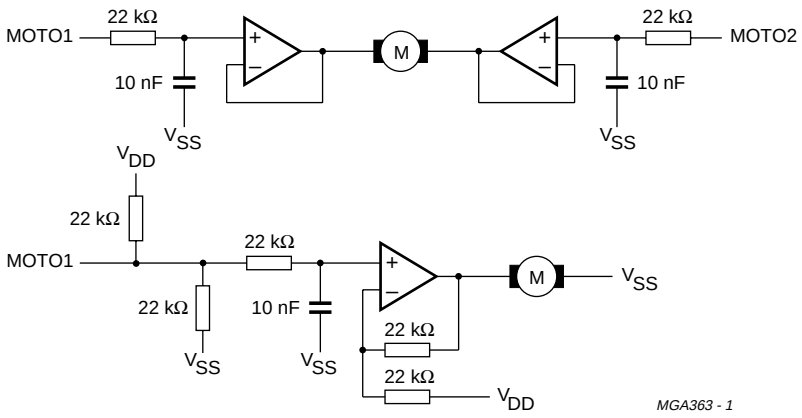


Fig.13 Motor pulse density application diagrams.

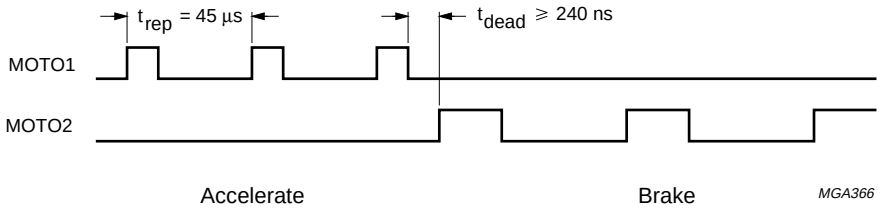


Fig.14 2-line PWM mode timing.

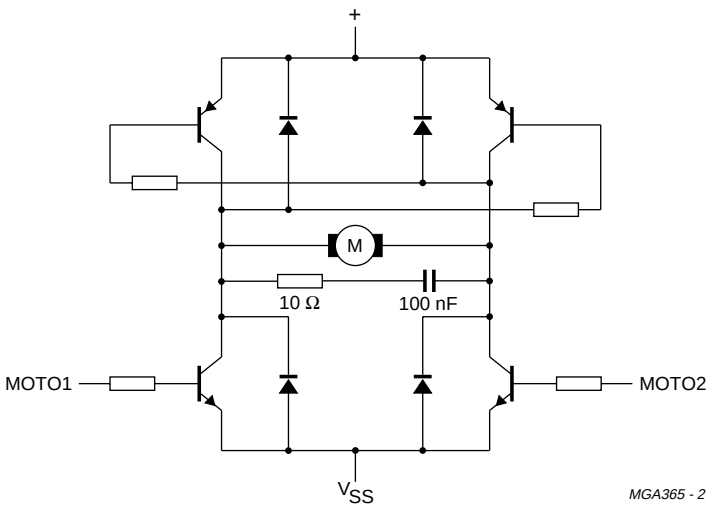


Fig.15 Motor 2-line PWM mode application diagram.

7.13.1.3 PWM output mode (4-line)

Using two extra outputs from the versatile pins Interface, it is possible to use the SAA7370A with a 4-input motor bridge. The timing is illustrated in Fig.16. A typical application diagram is illustrated in Fig.17.

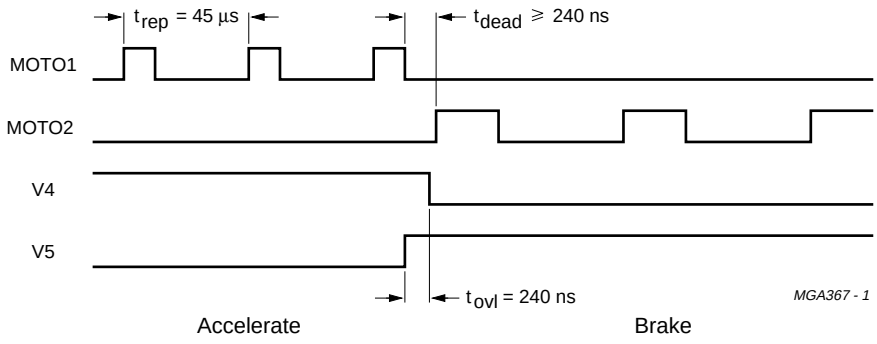


Fig.16 4-line PWM mode timing.

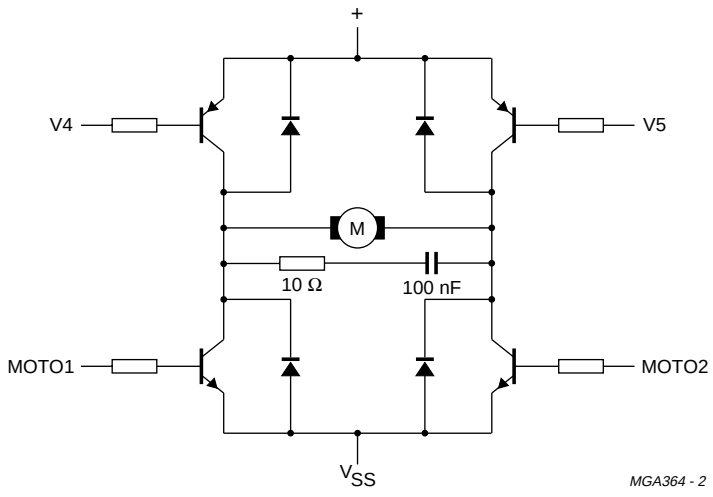


Fig.17 Motor 4-line PWM mode application diagram.

7.13.1.4 CDV/CAV output mode

In the CDV motor mode, the FIFO position will be put in pulse-width modulated form on the MOTO1 pin [carrier frequency (300 × d) Hz], where 'd' is the disc speed factor. The PLL frequency signal will be put in pulse-density modulated form (carrier frequency 4.23 × n MHz) on the MOTO2 pin. The integrated motor servo is disabled in this mode.

The PWM signal on MOTO1 corresponds to a total memory space of 20 frames, therefore the nominal FIFO position (half full) will result in a PWM output of 60%.

In the lock to-disc (CAV) mode the CDV motor mode is the only mode that can be used to control the motor.

7.13.2 SPINDLE MOTOR OPERATING MODES

The operation modes of the motor servo is controlled by register 1 (see Table 9).

In the SAA7370A decoder there is an anti-windup mode for the motor servo, selected via register 1. When the anti-wind-up mode is activated the motor servo integrator will hold if the motor output saturates.

7.13.2.1 Power limit

In start mode 1, start mode 2, stop mode 1 and stop mode 2, a fixed positive or negative voltage is applied to the motor.

This voltage can be programmed as a percentage of the maximum possible voltage, via register 6, to limit current drain during start and stop.
The following power limits are possible;

100% (no power limit), 75%, 50%, or 37% of maximum.

7.13.3 LOOP CHARACTERISTICS

The gain and crossover frequencies of the motor control loop can be programmed via registers 4 and 5.
The following parameter values are possible;

Gains: 3.2, 4.0, 6.4, 8.0, 12.8, 16, 25.6 and 32

Crossover frequency f_4: 0.5 × n Hz, 0.7 × n Hz, 1.4 × n Hz, 2.8 × n Hz

Crossover frequency f_3: 0.85 × n Hz, 1.71 × n Hz, 3.42 × n Hz

It should be noted that the crossover frequencies f_3 and f_4 are scaled with the overspeed factor 'n' whereas the gains are not.

7.13.4 FIFO OVERFLOW

If FIFO overflow occurs during Play mode (e.g.: as a result of motor rotational shock), the FIFO will be automatically reset to 50% and the audio interpolator tries to conceal as much as possible to minimise the effect of data loss.

Table 9 Operating modes

MODE	DESCRIPTION
Start mode 1	The disc is accelerated by applying a positive voltage to the spindle motor. No decisions are involved and the PLL is reset. No disc speed information is available for the microcontroller.
Start mode 2	The disc is accelerated as in start mode 1, however the PLL will monitor the disc speed. When the disc reaches 75% of its nominal speed, the controller will switch to jump mode. The motor status signals selectable via register 2 are valid.
Jump mode	Motor servo enabled but FIFO kept reset at 50%, integrator is held. The audio is muted but it is possible to read the subcode. It should be noted that in the CD-ROM modes the data, on EBU and the I^2S-bus is not muted.
Jump mode 1	Similar to jump mode but motor integrator is kept at zero. Used for long jumps where there is a large change in disc speed.
Play mode	FIFO released after resetting to 50%. Audio mute released.
Stop mode 1	Disc is braked by applying a negative voltage to the motor. No decisions are involved.
Stop mode 2	The disc is braked as in stop mode 1 but the PLL will monitor the disc speed. As soon as the disc reaches 12% (or 6%, depending on the programmed brake percentage, via register E) of its nominal speed, the MOTSTOP status signal will go HIGH and switch the motor servo to Off mode.
Off mode	Motor not steered.

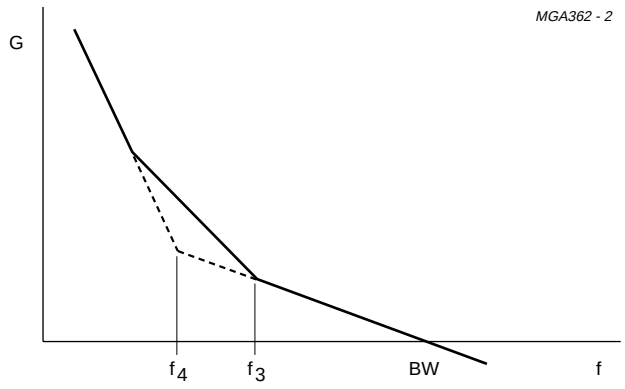


Fig.18 Motor servo mode diagram.

7.14 Servo part

7.14.1 DIODE SIGNAL PROCESSING

The photo detector in conventional two-stage three-beam compact disc systems normally contains six discrete diodes. Four of these diodes (three for single foucault systems) carry the central aperture signal (CA) while the other two diodes (satellite diodes) carry the radial tracking information. The CA signal is processed into an HF signal (for the decoder function) and LF signal (information for the focus servo loop) before it is supplied to the SAA7370A.

The analog signals from the central and satellite diodes are converted into a digital representation using analog-to-digital converters (ADCs). The ADCs are designed to convert unipolar currents into a digital code. The dynamic range of the input currents is adjustable within a given range, which is dependent on the value of external resistor connected to pin I_{refT}. The maximum current for the central diodes and satellite diodes is given in the following formulae;

$$I_{in\,(max,\,central)} = \left(\frac{2.4 \times 10^{-6}}{R_{IrefT}}\right)\ \mu A$$

$$I_{in\,(max,\,satellite)} = \left(\frac{1.2 \times 10^{-6}}{R_{IrefT}}\right)\ \mu A$$

The V_{RH} voltage is internally generated by control circuitry which ensures that the V_{RH} voltage is adjusted depending on the spread of internal capacitors, using the reference current generated by the external resistor on I_{refT}. In the application V_{RL} is connected to V_{SSA1}. The maximum input currents for a range of resistors is given Table 10.

Table 10 Maximum current input

R_{IrefT} (kΩ)	DIODE INPUT CURRENT RANGE	
	D1 to D4 (μA)	R1 and R2 (μA)
220	10.909	5.455
240	10.000	5.000
270	8.889	4.444
300	8.000	4.000
330	7.273	3.636
360	6.667	3.333
390	6.154	3.077
430	5.581	2.791
470	5.106	2.553
510	4.706	2.353
560	4.286	2.143
620	3.871	1.935

This mode of V_{RH} automatic adjustment can be selected by the preset latch command.

Alternatively, the dynamic range of the input currents can be made dependent on the ADC reference voltages VRL and VRH. The maximum current for the central diodes and satellite diodes is given in the following formulae;

$$I_{in\,(max,\,central)} = f_{sys} \times (V_{RH} - V_{RL}) \times 1.0 \times 10^{-6}\ \mu A$$

$$I_{in\,(max,\,satellite)} = f_{sys} \times (V_{RH} - V_{RL}) \times 1.0 \times 10^{-6}\ \mu A$$

where f_{sys} = 4.2336 MHz.

V_{RH} is generated internally, and there are 32 levels which can be selected under software control via the preset latch command. With this command the V_{RH} voltage can be set to 2.5 V then modified, decremented one level or incremented, by resending the command the required number of times. In the application V_{RL} is connected to V_{SSA1}.

7.14.2 Signal conditioning

The digital codes retrieved from the ADCs are applied to logic circuitry to obtain the various control signals. The signals from the central aperture diodes are processed to obtain a normalised focus error signal.

$$FE_n = \frac{D1 - D2}{D1 + D2} - \frac{D3 - D4}{D3 + D4}$$

where the detector set-up is assumed as shown in Fig.19.

In the event of single Foucault focusing method, the signal conditioning can be switched under software control such that the signal processing is as follows:

$$FE_n = 2 \times \frac{D1 - D2}{D1 + D2}$$

The error signal, FE_n, is further processed by a proportional integral and differential (PID) filter section.

A Focus OK (FOK) flag is generated by means of the central aperture signal and an adjustable reference level. This signal is used to provide extra protection for the track-loss (TL) generation, the focus start-up procedure and the drop out detection.

The radial or tracking error signal is generated by the satellite detector signals R1 and R2. The radial error signal can be formulated as follows:

$$RE_s = (R1 - R2) \times re_gain + (R1 - R2) \times re_gain$$

where the index ‘s’ indicates the automatic scaling operation which is performed on the radial error signal. This scaling is necessary to avoid non-optimum dynamic range usage in the digital representation and reduces the radial bandwidth spread. Furthermore, the radial error signal will be made free from offset during start up of the disc.

The four signals from the central aperture detectors, together with the satellite detector signals generate a track position signal (TPI) which can be formulated as follows:

$$TPI = sign\,[(D1 + D2 + D3 + D4) - (R1 + R2) \times sum_gain$$

where the weighting factor sum_gain is generated internally by the SAA7370A during initialization.

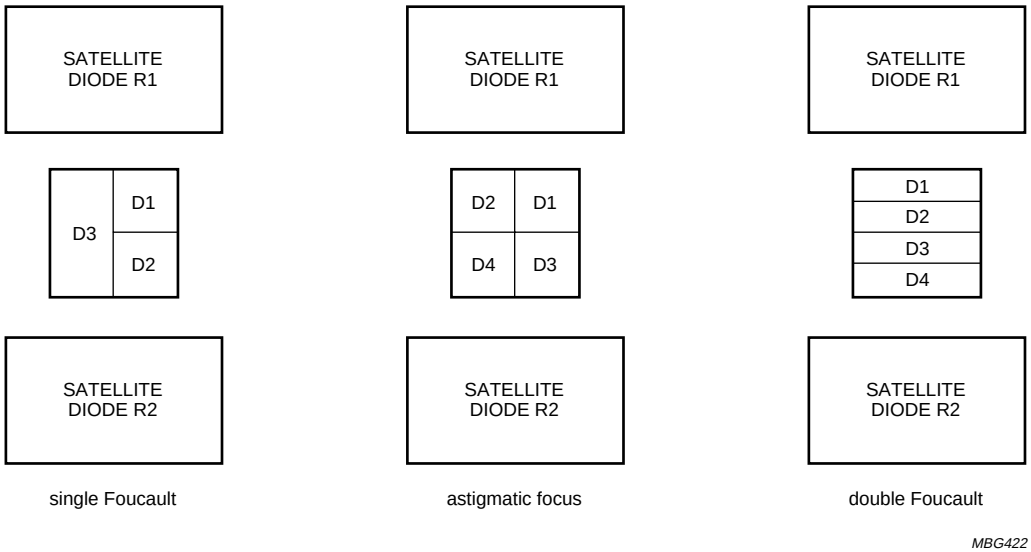


Fig.19 Detector arrangement.

7.14.3 FOCUS SERVO SYSTEM

7.14.3.1 Focus start-up

Five initially loaded coefficients influence the start-up behaviour of the focus controller. The automatically generated triangle voltage can be influenced by 3 parameters; for height (ramp_height) and DC offset (ramp_offset) of the triangle and its steepness (ramp_incr).

For protection against false focus point detections two parameters are available which are an absolute level on the CA-signal (CA_start) and a level on the FE_n signal (FE_start). When this CA level is reached the FOK signal becomes true.

If the FOK signal is true and the level on the FE_n signal is reached, the focus PID is enabled to switch on when the next zero crossing is detected in the FE_n signal.

7.14.3.2 Focus position control loop

The focus control loop contains a digital PID controller which has 5 parameters which are available to the user. These coefficients influence the integrating (foc_int), proportional (foc_lead_length, part of foc_parm3) and differentiating (foc_pole_lead, part of foc_parm1) action of the PID and a digital low-pass filter (foc_pole_noise, part of foc_parm2) following the PID. The fifth coefficient foc_gain influences the loop gain.

7.14.3.3 Drop-out detection

This detector can be influenced by one parameter (CA_drop). The FOK signal will become false and the integrator of the PID will hold if the CA signal drops below this programmable absolute CA level. When the FOK signal becomes false it is assumed, initially, to be caused by a black dot.

7.14.3.4 Focus loss detection and fast restart

Whenever FOK is false for longer than approximately 3 ms, it is assumed that the focus point is lost. A fast restart procedure is initiated which is capable of restarting the focus loop within 200 to 300 ms depending on the programmed coefficients of the microcontroller.

7.14.3.5 Focus loop gain switching

The gain of the focus control loop (foc_gain) can be multiplied by a factor of 2 or divided by a factor of 2 during normal operation. The integrator value of the PID is corrected accordingly. The differentiating (foc_pole_lead) action of the PID can be switched at the same time as the gain switching is performed.

7.14.3.6 Focus automatic gain control loop

The loop gain of the focus control loop can be corrected automatically to eliminate tolerances in the focus loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated for a short time (for example, when starting a new disc).

7.14.4 RADIAL SERVO SYSTEM

7.14.4.1 Level initialization

During start-up an automatic adjustment procedure is activated to set the values of the radial error gain (re_gain), offset (re_offset) and satellite sum gain (sum_gain) for TPI level generation. The initialization procedure runs in a radial open loop situation and is ≤300 ms. This start-up time period may coincide with the last part of the motor start-up time period.

Automatic gain adjustment: as a result of this initialization the amplitude of the RE signal is adjusted to within ±10% around the nominal RE amplitude.

Offset adjustment: the additional offset in RE due to the limited accuracy of the start-up procedure is less than ±50 nm.

TPI level generation: the accuracy of the initialization procedure is such that the duty factor range of TPI becomes 0.4 < duty factor < 0.6 (default duty factor = TPI HIGH/TPI period).

7.14.4.2 Sledge control

The microcontroller can move the sledge in both directions via the steer sledge command.

7.14.4.3 Tracking control

The actuator is controlled using a PID loop filter with user defined coefficients and gain. For stable operation between the tracks, the S-curve is extended over 0.75 of the track. On request from the microcontroller, S-curve extension over 2.25 tracks is used, automatically changing to access control when exceeding those 2.25 tracks.

Both modes of S-curve extension make use of a track-count mechanism. In this mode, track counting results in an ‘automatic return-to-zero track’, to avoid major music rhythm disturbances in the audio output for improved shock resistance.
The sledge is continuously controlled, or provided with

step pulses to reduce power consumption using the filtered value of the radial PID output. Alternatively, the microcontroller can read the average voltage on the radial actuator and provide the sledge with step pulses to reduce power consumption. Filter coefficients of the continuous sledge control can be preset by the user.

7.14.4.4 Access

The access procedure is divided into two different modes (see Table 11), depending on the requested jump size.

Table 11 Access modes

ACCESS TYPE	JUMP SIZE(1)	ACCESS SPEED
Actuator jump	1 - brake_distance	decreasing velocity
Sledge jump	brake_distance - 32768	maximum power to sledge(1)

Note

1. Microcontroller presettable.

The access procedure makes use of a track counting mechanism, a velocity signal based on a fixed number of tracks passed within a fixed time interval, a velocity set point calculated from the number of tracks to go and a user programmable parameter indicating the maximum sledge performance.

If the number of tracks remaining is greater than the brake_distance then the sledge jump mode should be activated or, the actuator jump should be performed. The requested jump size together with the required sledge breaking distance at maximum access speed defines the brake_distance value.

During the actuator jump mode, velocity control with a PI controller is used for the actuator. The sledge is then continuously controlled using the filtered value of the radial PID output. All filter parameters (for actuator and sledge) are user programmable.

In the sledge jump mode maximum power (user programmable) is applied to the sledge in the correct direction while the actuator becomes idle (the contents of the actuator integrator leaks to zero just after the sledge jump mode is initiated). The actuator can be electronically damped during sledge jump. The gain of the damping loop is controlled via the hold_mult parameter.

Fast track jumping circuitry can be enabled/disabled via the xtra_preset parameter.

7.14.4.5 Radial automatic gain control loop

The loop gain of the radial control loop can be corrected automatically to eliminate tolerances in the radial loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated for a short time (for example, when starting a new disc).

This gain control differs from the level initialization. The level initialization should be performed first. The disadvantage of using the level initialization without the gain control is that only tolerances from the front-end are reduced.

7.14.5 Off-track counting

The track position signal (TPI) is a flag which is used to indicate whether the radial spot is positioned on the track, with a margin of $\pm\frac{1}{4}$ of the track-pitch. In combination with the radial polarity flag (RP) the relative spot position over the tracks can be determined. These signals are, however, afflicted with some uncertainties caused by;

- Disc defects such as scratches and fingerprints
- The HF information on the disc, which is considered as noise by the detector signals.

In order to determine the spot position with sufficient accuracy, extra conditions are necessary to generate a track loss signal (TL) and an off-track counter value. These extra conditions influence the maximum speed and this implies that, internally, one of the following three counting states is selected;

1. Protected state: used in normal play situations. A good protection against false detection caused by disc defects is important in this state.
2. Slow counting state: used in low velocity track jump situations. In this state a fast response is important rather than the protection against disc defects (if the phase relationship between TL and RP of $\frac{1}{2\pi}$ radians is affected too much, the direction cannot then be determined accurately).
3. Fast counting state: used in high velocity track jump situations. Highest obtainable velocity is the most important feature in this state.

7.14.6 DEFECT DETECTION

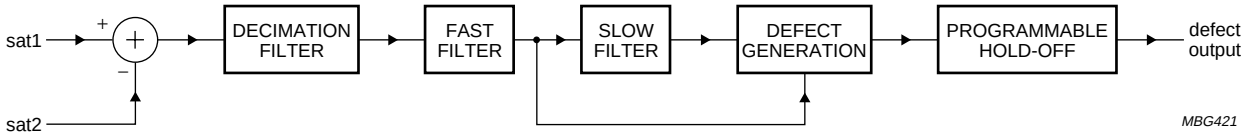


Fig.20 Block diagram of defect detector.

A defect detection circuit is incorporated into the SAA7370A. If a defect is detected, the radial and focus error signals may be zeroed, resulting in better playability. The defect detector can be switched off, applied only to focus control or applied to both focus and radial controls under software control (part of foc_parm1).

The defect detector (see Fig.20) has programmable set points selectable by the parameter defect_parm.

7.14.7 OFF-TRACK DETECTION

During active radial tracking, off-track detection has been realised by continuously monitoring the off-track counter value. The off-track flag becomes valid whenever the off-track counter value is not equal to zero. Depending on the type of extended S-curve, the off-track counter is reset after 0.75 extend or at the original track in the 2.25 track extend mode.

7.14.8 HIGH-LEVEL FEATURES

7.14.8.1 Interrupt mechanism and STATUS pin

The STATUS pin is an output which is active LOW, its output is selected by register 7 to be either the status bit (active LOW) selected by register 2 (only available in 4-wire bus mode) or the interrupt signal generated by the servo part.

8 signals from the interrupt status register are selectable from the servo part via the interrupt_mask parameter. The interrupt is reset by sending the read high-level status command. The 8 signals are as follows;

1. Focus lost: drop out of longer than 3 ms.
2. Subcode ready.
3. Subcode absolute seconds changed.
4. Subcode discontinuity detected: new subcode time before previous subcode time, or more than 10 frames later than previous subcode time.
5. Radial error: during radial on-track, no new subcode frame occurs within time defined by playwatchtime parameter. During radial jump, less than 4 tracks have been crossed during time defined by jumpwatchtime parameter.
6. Autosequencer state change.
7. Autosequencer error.
8. Subcode interface blocked: the internal decoder interface is being used.

It should be noted that if the STATUS pin output is selected via register 2 and either the microcontroller writes a different value to register 2 or the decoder interface is enabled then the STATUS output will change.

7.14.8.2 Decoder interface

The decoder interface allows registers 0 to F to be programmed and subcode Q-channel data to be read via servo commands. The interface is enabled/disabled by the preset latch command (and the xtra_preset parameter).

7.14.8.3 Automatic error handling

Three watchdogs are present:

1. Focus: detects focus drop out of longer than 3 ms, sets focus lost interrupt, switches off radial and sledge servos, disables drive to disc motor.
2. Radial play: started when radial servo is on-track mode and a first subcode frame is found. Detects when maximum time between two subcode frames exceeds time set by playwatchtime parameter; then sets radial error interrupt, switches radial and sledge servos off, puts disc motor in jump mode.
3. Radial jump: active when radial servo in long jump or short jump modes. Detects when the off-track counter value decreases by less than 4 tracks between two readings (time interval set by jumpwatchtime parameter); then sets radial jump error, switches radial and sledge servos off to cancel jump.

The focus watchdog is always active, the radial watchdogs are selectable via the radcontrol parameter.

7.14.8.4 Automatic sequencers and timer interrupts

Two automatic sequencers are implemented (and must be initialized after power-on);

1. Autostart sequencer: controls the start-up of focus, radial and motor.
2. Autostop sequencer: brakes the disc and shuts down servos.

When the automatic sequencers are not used it is possible to generate timer interrupts, defined by the time_parameter coefficient.

7.14.8.5 High-level status

The read high-level status command can be used to obtain the interrupt, decoder, autosequencer status registers and the motor start time. Use of the read high-level status command clears the interrupt status register, and re-enables the subcode read via a servo command.

7.14.9 DRIVER INTERFACE

The control signals (pins RA, FO and SL) for the mechanism actuators are pulse density modulated. The modulating frequency can be set to either 1.0584 MHz (DSD mode) or 2.1168 MHz; controlled via the xtra_preset parameter (it should be noted that these frequencies are doubled if a 16.9344 MHz crystal is used with SELPLL = 1). An analog representation of the output signals can be achieved by connecting a first-order low-pass filter to the outputs.

During reset (i.e. RESET pin is held LOW) the RA, FO and SL pins are high-impedance.

7.14.10 LASER INTERFACE

The LDON pin (open-drain output) is used to switch the laser off and on. When the laser is on the output is high-impedance. The action of the LDON pin is controlled by the xtra_preset parameter; the pin is automatically driven if the focus control loop is active.

7.14.11 RADIAL SHOCK DETECTOR

The shock detector (see Fig.21) can be switched on during normal track following, and detects within an adjustable frequency whether disturbances in the radial spot position relative to the track exceed an adjustable level (controlled by shock_level). Every time the radial tracking error (RE) exceeds this level the radial control bandwidth is switched to twice its original bandwidth and the loop gain is increased by a factor of 4.

The shock detection level is adjustable in 16 steps from 0 to 100% of the traverse radial amplitude which is sent to an amplitude detection unit via an adjustable band-pass filter (controlled by sledge_parm1); lower corner frequency can be set at either 0 or 20 Hz, and upper corner frequency at 750 or 1850 Hz. The shock detector is switched off automatically during jump mode.



Fig.21 Block diagram of radial shock detector.

7.15 Microcontroller interface

Communication on the microcontroller interface can be set-up in two different modes;

1. 4-wire bus mode: protocol compatible with SAA7345 (CD6) and TDA1301 (DSIC2) where;
   a) SCL = serial bit clock.
   b) SDA = serial data.
   c) RAB = R/$\overline{W}$ control and data strobe (active HIGH) for writing to registers 0 to F, reading status bit selected via register 2 and reading Q-channel subcode.
   d) SILD = $\overline{R}$/W control and data strobe (active LOW) for servo commands.
2. I^2C-bus mode: I^2C-bus protocol where SAA7370A behaves as slave device, activated by setting RAB = HIGH and SILD = LOW where;
   a) I^2C-bus slave address (write mode) = 30H.
   b) I^2C-bus slave address (read mode) = 31H.
   c) Maximum data transfer rate = 400 kbits/s.

It should be noted that only servo commands can be used therefore, writing to registers 0 to F, reading decoder status and reading Q-channel subcode data must be performed by servo commands.

7.15.1 Microcontroller interface (4-wire bus mode)

7.15.1.1 Writing data to registers 0 to F

The sixteen 4-bit programmable configuration registers, 0 to F (see Table 12), can be written to via the microcontroller interface using the protocol shown in Fig.22.

It should be noted that SILD must be held HIGH; A3 to A0 identifies the register number and D3 to D0 is the data; the data is latched into the register on the LOW-to-HIGH transition of RAB.

7.15.1.2 Writing repeated data to registers 0 to F

The same data can be repeated several times (e.g. for a fade function) by applying extra RAB pulses as shown in Fig.23. It should be noted that SCL must stay HIGH between RAB pulses.

7.15.1.3 Reading decoder status information on SDA

There are several internal status signals, selected via register 2, which can be made available on the SDA line;

SUBQREADY-I: LOW if new subcode word is ready in Q-channel register.

MOTSTART1: HIGH if motor is turning at 75% or more of nominal speed.

MOTSTART2: HIGH if motor is turning at 50% or more of nominal speed.

MOTSTOP: HIGH if motor is turning at 12% or less of nominal speed. Can be set to indicate 6% or less (instead of 12% or less) via register E.

PLL Lock: HIGH if sync coincidence signals are found.

V1: follows input on V1 pin.

V2: follows input on V2 pin.

MOTOR-OV: HIGH if the motor servo output stage saturates.

FIFO-OV: HIGH if FIFO overflows.

SHOCK: $\overline{\text{MOTSTART2}}$ + $\overline{\text{PLL Lock}}$ + MOTOR-OV + FIFO-OV + servo interrupt signal + OTD (HIGH if shock detected).

LA-SHOCK: latched SHOCK signal.

The status read protocol is shown in Fig.24. It should be noted that SILD must be held HIGH.

7.15.1.4 Reading Q-channel subcode

To read the Q-channel subcode direct in the 4-wire bus mode, the SUBQREADY-I signal should be selected as status signal. The subcode read protocol is illustrated in Fig.25.

It should be noted that SILD must be held HIGH; after subcode read starts, the microcontroller may take as long as it wants to terminate the read operation; when enough subcode has been read (1 to 96 bits), terminate reading by pulling RAB LOW.

Alternatively, the Q-channel subcode can be read using a servo command as follows:

- Use the read high-level status command to monitor the subcode ready signal.
- Send the read subcode command, and read the required number of bytes (up to 12).
- Send the read high-level status command; to re-enable the decoder interface.

7.15.1.5 Behaviour of the SUBQREADY-I signal

When the CRC of the Q-channel word is good, and no subcode is being read, the SUBQREADY-I status signal will react as shown in Fig.26. When the CRC is good and the subcode is being read, the timing in Fig.27 applies.

If t_1 (SUBQREADY-I status LOW to end of subcode read) is below 2.6/n ms, then t_2 = 13.1/n ms (i.e.: the microcontroller can read all subcode frames if it completes the read operation within 2.6/n ms after the subcode is ready). If this criterion is not met, it is only possible to guarantee that t_3 will be below 26.2/n ms (approximately).

If subcode frames with failed CRCs are present, the t_2 and t_3 times will be increased by 13.1/n ms for each defective subcode frame.

It should be noted that in the lock-to-disc mode 'n' is replaced by 'd', which is the disc speed factor.

7.15.1.6 Write servo commands

A write data command is used to transfer data (a number of bytes) from the microcontroller, using the protocol shown in Fig.28. The first of these bytes is the command byte and the following are data bytes; the number (between 1 and 7) depends on the command byte.

It should be noted that RAB must be held LOW; the command or data is interpreted by the SAA7370A after the HIGH-to-LOW transition of SILD; there must be a minimum time of 70 µs between SILD pulses.

7.15.1.7 Writing repeated data in servo commands

The same data byte can be repeated by applying extra SILD pulses as illustrated in Fig.29. SCL must be HIGH between the SILD pulses.

7.15.1.8 Read servo commands

A read data command is used to transfer data (status information) to the microcontroller, using the protocol shown in Fig.30. The first byte written determines the type of command. After this byte a variable number of bytes can be read. It should be noted that RAB must be held LOW; after the end of the command byte (LOW-to-HIGH transition on SILD) there must be a delay of 70 µs before reading data is started (i.e. the next HIGH-to-LOW transition on SILD); there must be a minimum time of 70 µs between SILD pulses.

7.15.2 MICROCONTROLLER INTERFACE (I^2C-BUS MODE)

Bytes are transferred over the interface in groups (i.e. servo commands) of which there are two types: write data commands and read data commands.

The sequence for a write data command (that requires 3 data bytes) is as follows;

- Send START condition
- Send address 30H (write)
- Write command byte
- Write data byte 1
- Write data byte 2.
- Write data byte 3
- Send STOP condition.

It should be noted that more than one command can be sent in one write sequence.

The sequence for a read data command (that reads 2 data bytes) is as follows;

- Send START condition
- Send address 30H (write)
- Write command byte
- Send STOP condition.
- Send START condition
- Send address 31H (read)
- Read data byte 1
- Read data byte 2
- Send STOP condition.

It should be noted that the timing constraints specified for the read and write servo commands must still be adhered to.

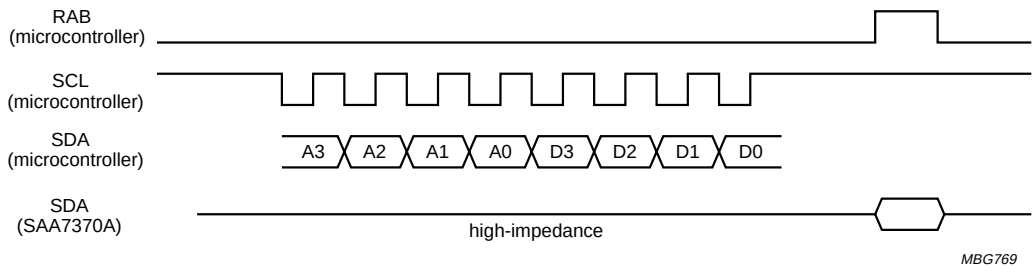


Fig.22 Microcontroller write protocol for registers 0 to F.

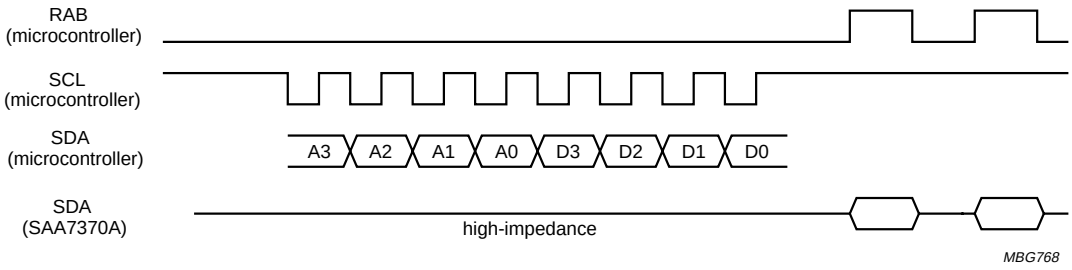


Fig.23 Microcontroller write protocol for registers 0 to F (repeat mode).

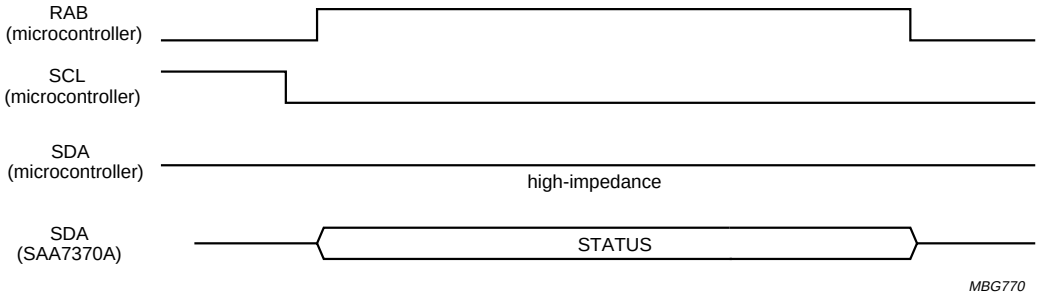


Fig.24 Microcontroller read protocol for decoder status on SDA.

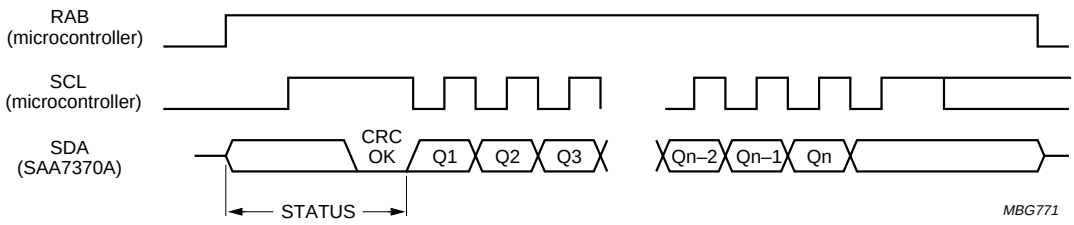


Fig.25 Microcontroller protocol for reading Q-channel subcode.

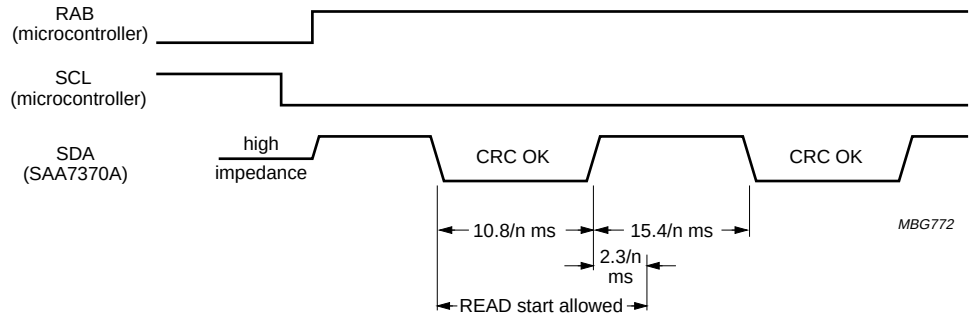


Fig.26 SUBQREADY-I status timing when no subcode is read.

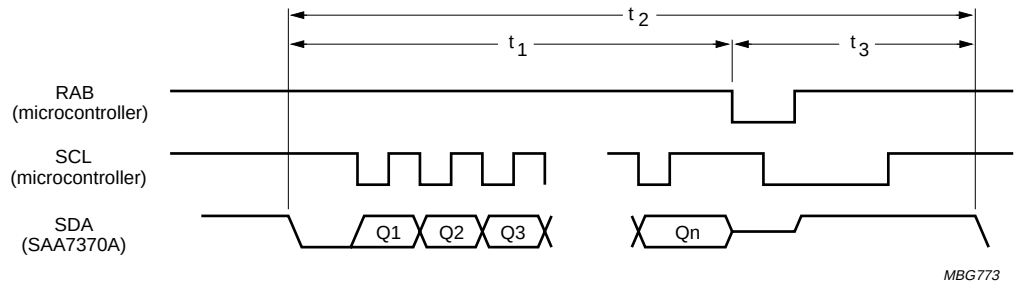


Fig.27 SUBQREADY-I status timing when subcode is read.

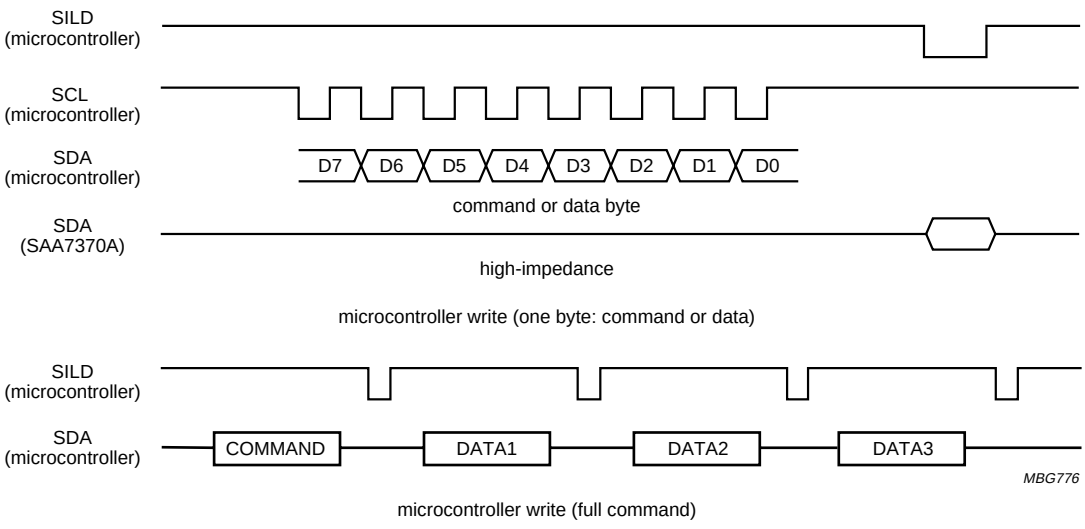
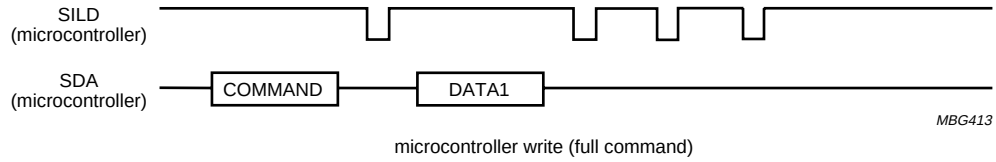


Fig.28 Microcontroller protocol for write servo commands.



microcontroller write (full command)

Fig.29 Microcontroller protocol for repeated data in write servo commands.

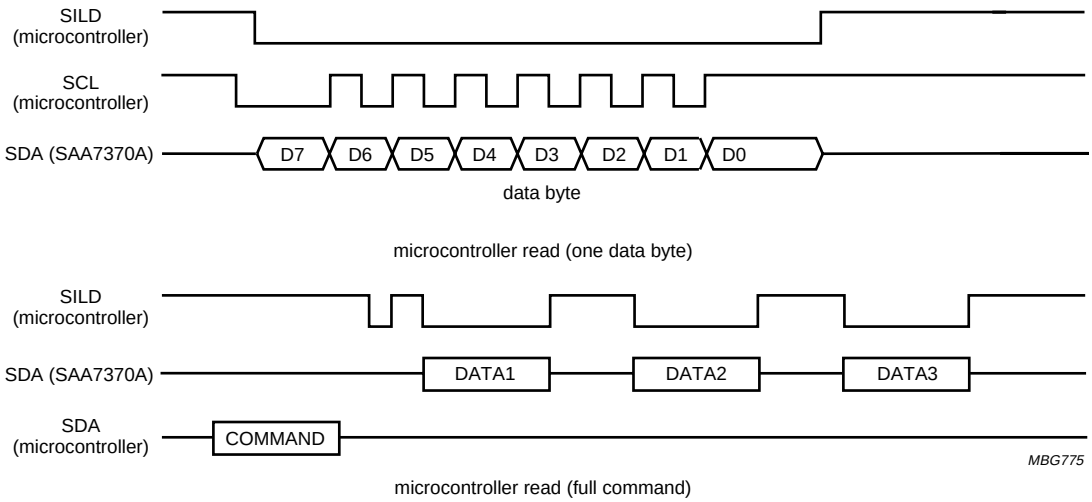


Fig.30 Microcontroller protocol for read servo commands.

7.15.3 Summary of functions controlled by registers 0 to F

Table 12 Registers 0 to F

REGISTER	ADDRESS	DATE	FUNCTION	INITIAL(1)
0 (fade and attenuation)	0000	0000	mute	reset
		0010	attenuate	–
		0001	full scale	–
		0100	step down	–
		0101	step up	–
1 (motor mode)	0001	x000	motor off mode	reset
		x 001	motor stop mode 1	–
		x010	motor stop mode 2	–
		x011	motor start mode 1	–
		x100	motor start mode 2	–
		x101	motor jump mode	–
		x111	motor play mode	–
		x110	motor jump mode 1	–
		1xxx	anti-windup active	–
		0xxx	anti-windup off	reset
2 (status control)	0010	0000	status = SUBQREADY-I	reset
		0001	status = MOTSTART1	–
		0010	status = MOTSTART2	–
		0011	status = MOTSTOP	–
		0100	status = PLL Lock	–
		0101	status = V1	–
		0110	status = V2	–
		0111	status = MOTOR-OV	–
		1000	status = FIFO overflow	–
		1001	status = shock detect	–
		1010	status = latched shock detect	–
		1011	status = latched shock detect reset	–
3 (DAC output)	0011	1010	I^2S-bus; CD-ROM mode	–
		1011	EIAJ; CD-ROM mode	–
		1100	I^2S-bus; 18-bit; $4f_s$ mode	reset
		1111	I^2S-bus; 18-bit; $2f_s$ mode	–
		1110	I^2S-bus; 16-bit; f_s mode	–
		0000	EIAJ; 16-bit; $4f_s$	–
		0011	EAIJ; 16-bit; $2f_s$	–
		0010	EIAJ; 16-bit; f_s	–
		0100	EIAJ; 18-bit; $4f_s$	–
		0111	EIAJ; 18-bit; $2f_s$	–
		0110	EIAJ; 18-bit; f_s	–

REGISTER	ADDRESS	DATE	FUNCTION	INITIAL(1)
4 (motor gain)	0100	x000	motor gain G = 3.2	reset
		x001	motor gain G = 4.0	–
		x010	motor gain G = 6.4	–
		x011	motor gain G = 8.0	–
		x100	motor gain G = 12.8	–
		x101	motor gain G = 16.0	–
		x110	motor gain G = 25.6	–
		x111	motor gain G = 32.0	–
		0xxx	disable comparator clock divider	reset
		1xxx	enable comparator clock divider; only if SELLPLL set HIGH	–
5 (motor bandwidth)	0101	xx00	motor f4 = 0.5 × n Hz	reset
		xx01	motor f4 = 0.7 × n Hz	–
		xx10	motor f4 = 1.4 × n Hz	–
		xx11	motor f4 = 2.8 × n Hz	–
		00xx	motor f3 = 0.85 × n Hz	reset
		01xx	motor f3 = 1.71 × n Hz	–
		10xx	motor f3 = 3.42 × n Hz	–
6 (motor output configuration)	0110	xx00	motor power maximum 37%	reset
		xx01	motor power maximum 50%	–
		xx10	motor power maximum 75%	–
		xx11	motor power maximum 100%	–
		00xx	MOTO1, MOTO2 pins 3-state	reset
		01xx	motor PWM mode	–
		10xx	motor PDM mode	–
		11xx	motor CDV mode	–
7 (DAC output and status control)	0111	xx00	interrupt signal from servo at STATUS pin	reset
		xx10	status bit from decoder status register at STATUS pin	–
		x0xx	DAC data normal value	reset
		x1xx	DAC data inverted value	–
		0xxx	left channel first at DAC (WCLK normal)	reset
		1xxx	right channel first at DAC (WCLK inverted)	–
8 (PLL loop filter bandwidth)			see Table 13	–
9 (PLL equalization)	1001	0011	PLL loop filter equalization	reset
		0001	PLL 30 ns over-equalization	–
		0010	PLL 15 ns over-equalization	–
		0100	PLL 15 ns under-equalization	–
		0101	PLL 30 ns under-equalization	–

REGISTER	ADDRESS	DATE	FUNCTION	INITIAL(1)
A (EBU output)	1010	xx0x	EBU data before concealment	–
		xx1x	EBU data after concealment and fade	reset
		x0x0	level II clock accuracy (<1000 ppm)	reset
		x0x1	level I clock accuracy (<50 ppm)	–
		x1x0	level III clock accuracy (>1000 ppm)	–
		x1x1	EBU off - output low	–
		0xxx	flags in EBU off	reset
		1xxx	flags in EBU on	–
B (speed control)	1011	x0xx	33.8688 MHz crystal present, or 8.4672 MHz (or 16.9344 MHz) crystal with SELPLL set HIGH	reset
		x1xx	16.9344 MHz crystal present (single-speed mode only)	–
		0xxx	single-speed mode (if register E = 0xxx) four times speed mode (if register E = 1xxx); note 2	reset
		1xxx	double-speed mode (if register E = 0xxx) eight times speed mode (if register E = 1xxx); note 2	–
		xx00	standby 1: ‘CD-STOP’ mode	reset
		xx10	standby 2: ‘CD-PAUSE’ mode	–
		xx11	operating mode	–
C (versatile pins interface)	1100	xxx1	external off-track signal input at V1	–
		xxx0	internal off-track signal used (V1 may be read via status)	reset
		xx0x	kill-L at KILL output, kill-R at V3 output	–
		001x	V3 = 0; single KILL output	reset
		011x	V3 = 1; single KILL output	–
D (versatile pins interface)	1101	0000	4-line motor (using V4 and V5)	–
		xx01	Q-to-W subcode at V4	–
		xx10	V4 = 0	–
		xx11	V4 = 1	reset
		01xx	de-emphasis signal at V5, no internal de-emphasis filter	–
		10xx	V5 = 0	–
		11xx	V5 = 1	reset
E	1110	0xxx	bit controls operating speed mode, see register B	reset
		x0xx	audio features disabled	–
		x1xx	audio features enabled	reset
		xx0x	lock-to-disc mode disabled	reset
		xx1x	lock-to-disc mode enabled	–
		xxx0	motor brakes to 12%	reset
		xxx1	motor brakes to 6%	–

REGISTER	ADDRESS	DATE	FUNCTION	INITIAL(1)
F (subcode interface)	1111	x000	subcode interface off	reset
		x100	subcode interface on	–
		0xxx	4-wire subcode	reset
		1xxx	3-wire subcode	–

Note

1. The initial column shows the power-on reset state.
2. The speed is doubled if using a 16.9344 MHz crystal with SELPLL set HIGH.

Table 13 Loop filter bandwidth

REGISTER	ADDRESS	DATA	FUNCTION			INITIAL(1)
			LOOP BANDWIDTH (Hz)	INTERNAL BANDWIDTH (Hz)	LOW-PASS BANDWIDTH (Hz)	
8 (PLL loop filter bandwidth)	1000	0000	1640 × n	525 × n	8400 × n	–
		0001	3279 × n	263 × n	16800 × n	–
		0010	6560 × n	131 × n	33600 × n	–
		0100	1640 × n	1050 × n	8400 × n	–
		0101	3279 × n	525 × n	16800 × n	–
		0110	6560 × n	263 × n	33600 × n	–
		1000	1640 × n	2101 × n	8400 × n	–
		1001	3279 × n	1050 × n	16800 × n	reset
		1010	6560 × n	525 × n	33600 × n	–
		1100	1640 × n	4200 × n	8400 × n	–
		1101	3279 × n	2101 × n	16800 × n	–
		1110	6560 × n	1050 × n	33600 × n	–

Note

1. The initial column shows the power-on reset state.

7.15.4 SUMMARY OF SERVO COMMANDS

A list of the servo commands are given in Table 14. It should be noted that these are not fully backwards compatible with DSIC2.

Table 14 CD7 servo commands

COMMANDS	CODE	BYTES	PARAMETERS
Write commands			
Write_focus_coefs1	17H	7	<foc_parm3> <foc_int> <ramp_incr> <ramp_height> <ramp_offset> <FE_start> <foc_gain>
Write_focus_coefs2	27H	7	<defect_parm> <rad_parm_jump> <vel_parm2> <vel_parm1> <foc_parm1> <foc_parm2> <CA_drop>
Write_focus_command	33H	3	<foc_mask> <foc_stat> <shock_level>
Focus_gain_up	42H	2	<foc_gain> <foc_parm1>
Focus_gain_down	62H	2	<foc_gain> <foc_parm1>
Write_radial coefs	57H	7	<rad_length_lead> <rad_int> <rad_parm_play> <rad_pole_noise> <rad_gain> <sledge_parm2> <sledge_parm_1>
Preset_Latch	81H	1	<chip_init>
Radial_off	C1H	1	‘1CH’
Radial_init	C1H	1	‘3CH’
Short_jump	C3H	3	<tracks_hi> <tracks_lo> <rad_stat>
Long_jump	C5H	5	<brake_dist> <sledge_U_max> <tracks_hi> <tracks_lo> <rad_stat>
Steer_sledge	B1H	1	<sledge_level>
Preset_init	93H	3	<re_offset> <re_gain> <sum_gain>
Write_decoder_reg(1)	D1H	1	<decoder_reg_data>
Write_parameter	A2H	2	<param_ram_addr> <param_data>
Read commands			
Read_Q_subcode(1)(2)	0H	up to 12	<Q_sub1..10> <peak_l> <peak_r>
Read_status	70H	up to 5	<foc_stat> <rad_stat> <rad_int_lpf> <tracks_hi> <tracks_lo>
Read_hilevel_status(3)	E0H	up to 4	<intreq> <dec_stat> <seq_stat> <motor_start_time>
Read_aux_status	F0H	up to 3	<re_offset> <re_gain> <sum_gain>

Notes

1. These commands only available when internal decoder interface is enabled.
2. <peak_l> and <peak_r> bytes are clocked out LSB first.
3. Decoder status flag information in <dec_stat> is only valid when the internal decoder interface is enabled.

7.15.5 SUMMARY OF SERVO COMMAND PARAMETERS

Table 15 Servo command parameters

PARAMETER	RAM ADDRESS	AFFECTS	POR VALUE	DETERMINES
foc_parm_1	–	focus PID	–	end of focus lead
				defect detector enabling
foc_parm_2	–	focus PID	–	focus low-pass
				focus error normalising
foc_parm_3	–	focus PID	–	focus lead length
				minimum light level
foc_int	14H	focus PID	–	focus integrator crossover frequency
foc_gain	15H	focus PID	70H	focus PID loop gain
CA_drop	12H	focus PID	–	sensitivity of drop-out detector
ramp_offset	16H	focus ramp	–	asymmetry of focus ramp
ramp_height	18H	focus ramp	–	peak-to-peak value of ramp voltage
ramp_incr	–	focus ramp	–	slope of ramp voltage
FE_start	19H	focus ramp	–	minimum value of focus error
rad_parm_play	28H	radial PID	–	end of radial lead
rad_pole_noise	29H	radial PID	–	radial low-pass
rad_length_lead	1CH	radial PID	–	length of radial lead
rad_int	1EH	radial PID	–	radial integrator crossover frequency
rad_gain	2AH	radial PID	70H	radial loop gain
rad_parm_jump	27H	radial jump	–	filter during jump
vel_parm1	1FH	radial jump	–	PI controller crossover frequencies
vel_parm2	32H	radial jump	–	jump pre-defined profile
speed_threshold	48H	radial jump	–	maximum speed in fastrad mode
hold_mult	49H	radial jump	00H	electronic damping
				sledge bandwidth during jump
brake_dist_max	21H	radial jump	–	maximum sledge distance allowed in fast actuator steered mode
sledge_long_brake	58H	radial jump	7FH	brake distance of sledge
sledge_Umax	–	sledge	–	voltage on sledge during long jump
sledge_level	–	sledge	–	voltage on sledge when steered
sledge_parm_1	36H	sledge	–	sledge integrator crossover frequency
sledge_parm_2	17H	sledge	–	sledge low-pass frequencies
				sledge gain
				sledge operation mode
sledge_pulse1	46H	pulsed sledge	–	pulse width
sledge_pulse2	64H	pulsed sledge	–	pulse height
defect_parm	–	defect detector	–	defect detector setting
shock_level	–	shock detector	–	shock detector operation
playwatchtime	54H	watchdog	–	radial on-track watchdog time

PARAMETER	RAM ADDRESS	AFFECTS	POR VALUE	DETERMINES
jumpwatchtime	57H	watchdog	–	radial jump watchdog time-out
radcontrol	59H	watchdog	–	enable/disable automatic radial off feature
chip_init	–	set-up	–	V_{RH} level setting
				enable/disable decoder interface
xtra_preset	4AH	set-up	38H	laser on/off
				RA, FO and SL PDM modulating frequency
				microcontroller communication to decoder part
				fast jumping circuit on/off
cd6cmd	4DH	decoder interface	–	decoder part commands
interrupt_mask	53H	STATUS pin	–	enabled interrupts
seq_control	42H	autosequencer	–	autosequencer control
focus_start_time	5EH	autosequencer	–	focus start time
motor_start_time1	5FH	autosequencer	–	motor start 1 time
motor_start_time2	60H	autosequencer	–	motor start 2 time
radial_init_time	61H	autosequencer	–	radial initialization time
brake_time	62H	autosequencer	–	brake time
RadCmdByte	63H	autosequencer	–	radial command byte
osc_inc	68H	focus/radial AGC	–	AGC control
				frequency of injected signal
phase_shift	67H	focus/radial AGC	–	phase shift of injected signal
level1	69H	focus/radial AGC	–	amplitude of signal injected
level2	6AH	focus/radial AGC	–	amplitude of signal injected
agc_gain	6CH	focus/radial AGC	–	focus/radial gain

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–0.5	+6.5	V
$V_{I(max)}$	maximum Input voltage (any input)		–0.5	V_{DD} + 0.5	V
V_O	output voltage (any output)		–0.5	+6.5	V
V_{DDdiff}	difference between V_{DDA} and V_{DDD}		–	± 0.25	V
I_O	output current (continuous)		–	± 20	mA
I_{IK}	DC input diode current (continuous)		–	± 20	mA
V_{es}	electrostatic handling	note 2	–2000	+2000	V
		note 3	–200	+200	V
T_{amb}	operating ambient temperature		0	+70	°C
T_{stg}	storage temperature		–55	+125	°C

Notes

1. All V_{DD} and V_{SS} connections must be made externally to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

9 CHARACTERISTICS

V_{DD} = 4.75 to 5.25 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.75	5.0	5.25	V
I_{DD}	supply current	V_{DD} = 5 V; n = 1 mode	–	49	–	mA
Decoder analog front-end (V_{DDA} = 5 V; V_{SSA} = 0 V; T_{amb} = 25 °C)						
COMPARATOR INPUTS: HFIN AND HFREF						
f_{clk}	clock frequency	note 1	8	–	140	MHz
$V_{th(sw)}$	switching voltage threshold		1.2	–	V_{DD} – 0.8	V
V_{15}	input voltage level (pin 15)		–	1.0	–	V
REFERENCE GENERATOR: I_{REF}						
V_{Iref}	reference voltage level (pin 18)		–	0.5V_{DD}	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Servo analog part (V_{DDA} = 5 V; V_{SSA} = 0 V; T_{amb} = 25 °C)						
PINS D1 TO D4, R1, R2, V_{RH}, V_{RL} AND I_{refT}						
I_{refT}	input reference current (pin 10)		1.935	–	5.45	µA
R_{IrefT}	external resistor on pin 10		220	–	620	kΩ
V_{IrefT}	voltage on reference current input (pin 10)		–	1.2	–	V
$I_{D(max)}$	maximum input current for central diode input signal	note 2	3.871	–	10.9	µA
$I_{R(max)}$	maximum input current for satellite diode input signal	note 2	1.935	–	5.45	µA
V_{RL}	LOW level reference voltage		0	0	0	V
V_{RH}	HIGH level reference voltage	output state 0; note 3	–	0.5	–	V
		output state v; note 3	–30%	$0.5 \times 10^{v/44.4}$	+30%	V
		output state 31; note 3	–	2.5	–	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB; note 4	–	–50	–45	dB
S/N	signal-to-noise ratio		–	55	–	dB
PSRR	power supply rejection at V_{DDA2}	note 5	–	45	–	dB
G_{tol}	gain tolerance	note 6	–12	0	+12	%
G_v	variation of gain between channels		–	–	2	%
α_{cs}	channel separation		–	60	–	dB
Digital inputs						
INPUTS: RESET, V1, V2, SELPLL (CMOS INPUT WITH PULL-UP RESISTOR AND HYSTERESIS)						
$V_{thr(sw)}$	switching voltage threshold rising		–	–	$0.8V_{DDD}$	V
$V_{thf(sw)}$	switching voltage threshold falling		$0.2V_{DDD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DDD}$	–	V
$R_{I(pu)}$	input pull-up resistance	V_i = 0 V	–	50	–	kΩ
C_{in}	input capacitance		–	–	10	pF
t_{resL}	reset pulse width (active LOW)	$\overline{\text{RESET}}$ only	1	–	–	µs
INPUTS: SCL, RAB, SILD AND RCK (CMOS INPUT)						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.3	V
I_{LI}	input leakage current	V_i = 0 – V_{DDD}	–10	–	+10	µA
C_{in}	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs						
OUTPUT: CL4						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{DDD} – 0.4	–	V_{DDD}	V
C_L	load capacitance		–	–	25	pF
t_r	output rise time	C_L = 20 pF; 0.8 to (V_{DDD} – 0.8)	–	–	20	ns
t_f	output fall time	C_L = 20 pF; (V_{DDD} – 0.8) to 0.8	–	–	20	ns
OUTPUT: CL16						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{DDD} – 0.4	–	V_{DDD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; 0.8 – (V_{DDD} – 0.8)	–	–	15	ns
t_f	output fall time	C_L = 20 pF; (V_{DDD} – 0.8) – 0.8	–	–	15	ns
OUTPUTS: V4 AND V5						
V_{OL}	LOW level output voltage	I_{OL} = 10 mA	0	–	1.0	V
V_{OH}	HIGH level output voltage	I_{OH} = –10 mA	V_{DDD} – 1	–	V_{DDD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; 0.8 – (V_{DDD} – 0.8)	–	–	10	ns
t_f	output fall time	C_L = 20 pF; (V_{DDD} – 0.8) – 0.8	–	–	10	ns
Open-drain outputs						
OUTPUTS: CFLG, C2FAIL, STATUS, KILL, V3 AND LDON (OPEN-DRAIN OUTPUT WITH PROTECTION DIODE TO V_{DD})						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
I_{OL}	LOW level output current		–	–	2	mA
C_L	load capacitance		–	–	25	pF
t_f	output fall time	C_L = 20 pF; (V_{DDD} – 0.8) – 0.8	–	–	30	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
3-state outputs						
OUTPUTS: EF, CLK, WCLK, DATA AND CL11						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; 0.8 – (V_{DD} – 0.8)	–	–	15	ns
t_f	output fall time	C_L = 20 pF; (V_{DD} – 0.8) – 0.8	–	–	15	ns
I_{ZO}	output 3-state leakage current	V_i = 0 – V_{DD}	–10	–	+10	µA
OUTPUT: CL11						
t_H	output HIGH time (relative to clock period)	V_o = 1.5 V	45	50	55	%
OUTPUTS: RA, FO, SL, SBSY, SFSY AND SUB						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = –1 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	25	pF
t_r	output rise time	C_L = 20 pF; 0.8 – (V_{DD} – 0.8)	–	–	20	ns
t_f	output fall time	C_L = 20 pF; (V_{DD} – 0.8) – 0.8	–	–	20	ns
I_{ZO}	3-state leakage current	V_i = 0 – V_{DD}	–10	–	+10	µA
OUTPUTS: MOTO1, MOTO2 AND DOBM						
V_{OL}	LOW level output voltage	I_{OL} = 10 mA	0	–	1.0	V
V_{OH}	HIGH level output voltage	I_{OH} = –10 mA	V_{DD} – 1	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	C_L = 20 pF; 0.8 – (V_{DD} – 0.8)	–	–	10	ns
t_f	output fall time	C_L = 20 pF; (V_{DD} – 0.8) – 0.8	–	–	10	ns
I_{ZO}	3-state leakage current	V_i = 0 – V_{DD}	–10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input/output						
INPUT/OUTPUT: SDA [CMOS INPUT/OPEN-DRAIN I^2C-BUS OUTPUT (WITH PROTECTION DIODE TO V_{DDD})]						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.3	V
I_{ZO}	3-state leakage current	$V_i = 0 – V_{DDD}$	–10	–	+10	µA
C_{in}	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.4	V
I_{OL}	LOW level output current		–	–	4	mA
C_L	load capacitance		–	–	50	pF
t_f	output fall time	C_L = 20 pF; $(V_{DDD} – 0.8) – 0.8$	–	–	15	ns
Crystal oscillator						
INPUT: CRIN (EXTERNAL CLOCK)						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current		–10	–	+10	µA
C_{in}	input capacitance		–	–	10	pF
OUTPUT: CROUT; see Figs 3 and 4						
f_{xtal}	crystal frequency	note 7	8	8.4672	35	MHz
g_m	mutual conductance at 100 kHz		–	10	–	mA/V
G_v	small signal voltage gain	$G_v = g_m \times R_O$	–	18	–	V/V
C_{fb}	feedback capacitance		–	–	5	pF
C_{out}	output capacitance		–	–	10	pF

Notes

1. Highest clock frequency at which data slicer produces 1010 output in analog self-test mode.
2. V_{RL} = 0 V, f_{sys} = 4.2336 MHz. The maximum input current depends on the value of the external resistor connected to I_{refT}:
   a) For D1 to D4: $I_{max} = 2.4/R_{IrefT} \Rightarrow 2.4/220\ k\Omega = 10.9\ \mu A$.
   b) For R1 and R2:$I_{max} = 1.2/R_{IrefT} \Rightarrow 1.2/220\ k\Omega = 5.45\ \mu A$.
3. Internal reference source with 32 different output voltages. Selection is achieved during a calibration period or via the serial interface. The values given are for an unloaded V_{RH}.
4. V_{RH} = 2.5 V and V_{RL} = 0 V, measuring bandwidth: 200 Hz to 20 kHz, $f_{i(ADC)}$ = 1 kHz.
5. f_{ripple} = 1 kHz, V_{ripple} = 0.5 V (p-p).
6. Gain of the ADC is defined as $G_{ADC} = f_{sys}/I_{max}$ (counts/µA); thus digital output = $I_i \times G_{ADC}$ where:
   a) Digital output = the number of pulses at the digital output in counts/s and I_i = the DC input current in µA.
   b) The maximum input current depends on the system frequency (f_{sys} = 4.2336 MHz) and on $V_{RH} – V_{RL}$.
   c) The gain tolerance is the deviation from the calculated gain regarding note 2.
7. It is recommended that the series resistance of the crystal or ceramic resonator is ≤60 Ω.

10 OPERATING CHARACTERISTICS (SUBCODE INTERFACE TIMING)

V_{DD} = 4.75 to 5.25 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Subcode interface timing (single speed × n); see Fig.31**;** note 1						
INPUT: RCK						
t_H	input clock HIGH time		2/n	4/n	6/n	µs
t_L	input clock LOW time		2/n	4/n	6/n	µs
t_r	input clock rise time		–	–	80/n	ns
t_f	input clock fall time		–	–	80/n	ns
t_{dC}	delay time SFSY to RCK		10/n	–	20/n	µs
OUTPUTS: SBSY, SFSY AND SUB (C_L = 20 pF)						
t_{Bcy}	block cycle		12.0/n	13.3/n	14.7/n	ms
t_{BW}	SBSY pulse width		–	–	300/n	µs
t_{Fcy}	frame cycle		122/n	136/n	150/n	µs
t_{FW}	SFSY pulse width (3-wire mode only)		–	–	366/n	µs
t_{FH}	SFSY HIGH time		–	–	66/n	µs
t_{FL}	SFSY LOW time		–	–	84/n	µs
t_{dPAC}	delay time SFSY to SUB (P data) valid		–	–	1/n	µs
t_{dAC}	delay time RCK falling to SUB		–	–	0	µs
t_{hD}	hold time RCK to SUB		–	–	0.7/n	µs

Note

1. The subcode timing is directly related to the overspeed factor ‘n’ in normal operating mode. ‘n’ is replaced by the disc speed factor ‘d’, in the lock-to-disc mode.

11 OPERATING CHARACTERISTICS (I^2S-BUS TIMING)

V_{DD} = 4.75 to 5.25 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2S-bus timing (single speed × n); see Fig.32**;** note 1						
CLOCK OUTPUT: SCLK (C_L = 20 pF)						
T_{cy}	output clock period	sample rate = f_s	–	472.4/n	–	ns
		sample rate = $2f_s$	–	236.2/n	–	ns
		sample rate = $4f_s$	–	118.1/n	–	ns
t_{CH}	clock HIGH time	sample rate = f_s	166/n	–	–	ns
		sample rate = $2f_s$	83/n	–	–	ns
		sample rate = $4f_s$	42/n	–	–	ns
t_{CL}	clock LOW time	sample rate = f_s	166/n	–	–	ns
		sample rate = $2f_s$	83/n	–	–	ns
		sample rate = $4f_s$	42/n	–	–	ns
OUTPUTS: WCLK, DATA AND EF (C_L = 20 pF)						
t_{su}	set-up time	sample rate = f_s	95/n	–	–	ns
		sample rate = $2f_s$	48/n	–	–	ns
		sample rate = $4f_s$	24/n	–	–	ns
t_h	hold time	sample rate = f_s	95/n	–	–	ns
		sample rate = $2f_s$	48/n	–	–	ns
		sample rate = $4f_s$	24/n	–	–	ns

Note

1. The I^2S-bus timing is directly related to the overspeed factor ‘n’ in the normal operating mode. In the lock-to-disc mode ‘n’ is replaced by the disc speed factor ‘d’.

12 OPERATING CHARACTERISTICS (MICROCONTROLLER INTERFACE TIMING)

V_{DD} = 4.75 to 5.25 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	NORMAL MODE		LOCK-TO-DISC MODE		UNIT
			MIN.	MAX.	MIN.	MAX.	
Microcontroller interface timing (4-wire bus mode; writing to registers 0 to F; reading Q-channel subcode and decoder status); see Figs 33 and 34; note 1							
INPUTS SCL AND RAB							
t_{CL}	input LOW time		480/n + 20	–	2400/n + 20	–	ns
t_{CH}	input HIGH time		480/n + 20	–	2400/n + 20	–	ns
t_r	rise time		–	480/n	–	480/n	ns
t_f	fall time		–	480/n	–	480/n	ns
READ MODE (C_L = 20 pF)							
t_{dRD}	delay time RAB to SDA valid		–	50	–	50	ns
t_{PD}	propagation delay SCL to SDA		720/n – 20	960/n + 20	720/n + 20	4800/n + 20	ns
t_{dRZ}	delay time RAB to SDA high-impedance		–	50	–	50	ns
WRITE MODE ((C_L = 20 pF)							
t_{suD}	set-up time SDA to SCL	note 2	20 – 720/n	–	20 – 720/n	–	ns
t_{hD}	hold time SCL to SDA		–	960/n + 20	–	4800/n + 20	ns
t_{suCR}	set-up time SCL to RAB		240/n + 20	–	1200/n + 20	–	ns
t_{dWZ}	delay time SDA high-impedance to RAB		0	–	0	–	ns
Microcontroller interface timing (4-wire bus mode; servo commands); see Figs 35 and 36**;** notes 3 and 4							
INPUTS SCL AND SILD							
t_L	Input LOW time		710	–	710	–	ns
t_H	Input HIGH time		710	–	710	–	ns
t_r	rise time		–	240	–	240	ns
t_f	fall time		–	240	–	240	ns
READ MODE (C_L = 20 pF)							
t_{dLD}	delay time SILD to SDA valid		–	25	–	25	ns
t_{PD}	propagation delay SCL to SDA		–	950	–	950	ns
t_{dLZ}	delay time SILD to SDA high-impedance		–	50	–	50	ns
t_{sCLR}	set-up time SCL to SILD		480	–	480	–	ns
t_{hCLR}	hold time SILD to SCL		830	–	830	–	ns

SYMBOL	PARAMETER	CONDITIONS	NORMAL MODE		LOCK-TO-DISC MODE		UNIT
			MIN.	MAX.	MIN.	MAX.	
WRITE MODE (C_L = 20 pF)							
t_{sD}	set-up time SDA to SCL		0	–	0	–	ns
t_{hD}	hold time SCL to SDA		950	–	950	–	ns
t_{sCL}	set-up time SCL to SILD		480	–	480	–	ns
t_{hCL}	hold time SILD to SCL		120	–	120	–	ns
t_{dPLP}	delay between two SILD pulses		70	–	70	–	µs
t_{dWZ}	delay time SDA high-impedance to SILD		0	–	0	–	ns

Notes

1. The 4-wire bus mode microprocessor interface timing for writing to registers 0 to F, and reading Q-channel subcode and decoder status, is a function of the overspeed factor ‘n’. In the lock-to-disc mode the maximum data rate is lower.
2. Negative set-up time means that the data may change after clock transition.
3. If a 16.9344 MHz crystal is used and SELPLL = 1 then the timings are divided-by-2.
4. If a 16.9344 MHz crystal is used and SELPLL = 0 then the timings are divided-by-2 until the microcontroller has written x1xx to register B.

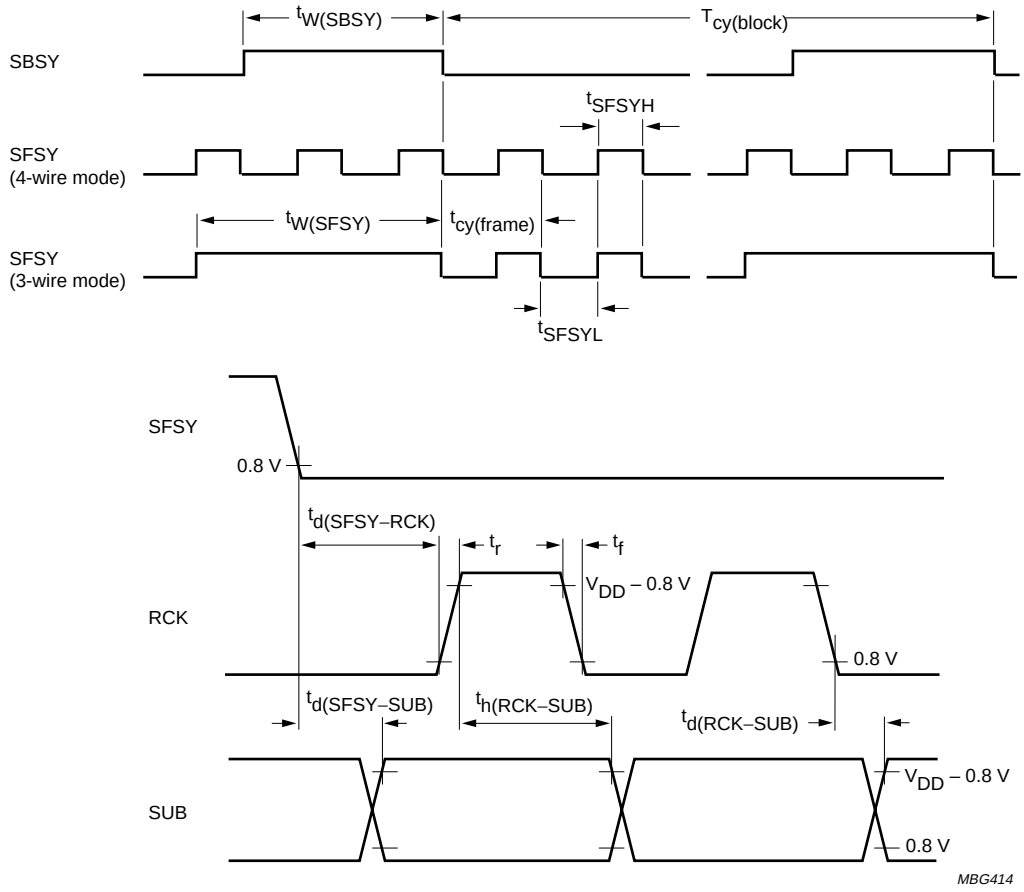


Fig.31 Subcode interface timing diagram.

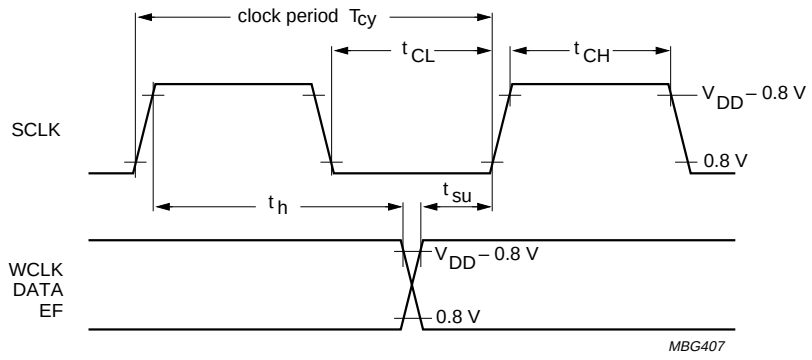


Fig.32 I²S-bus timing diagram.

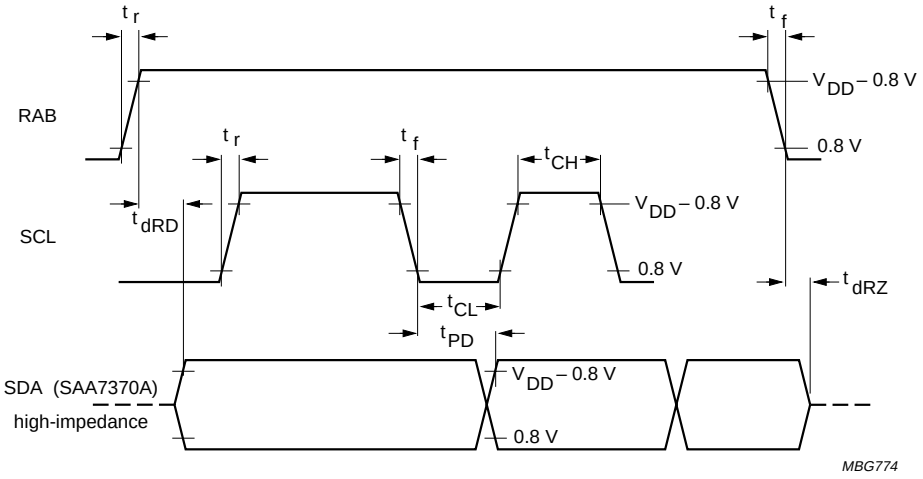


Fig.33 4-wire bus microcontroller timing; read mode (Q-channel subcode and decoder status information).

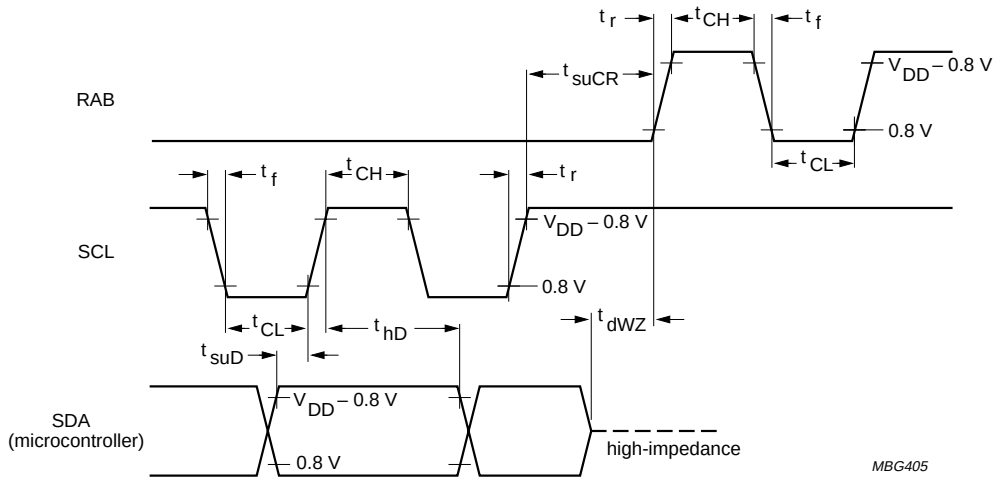


Fig.34 4-wire bus microcontroller timing; write mode (registers 0 to F).

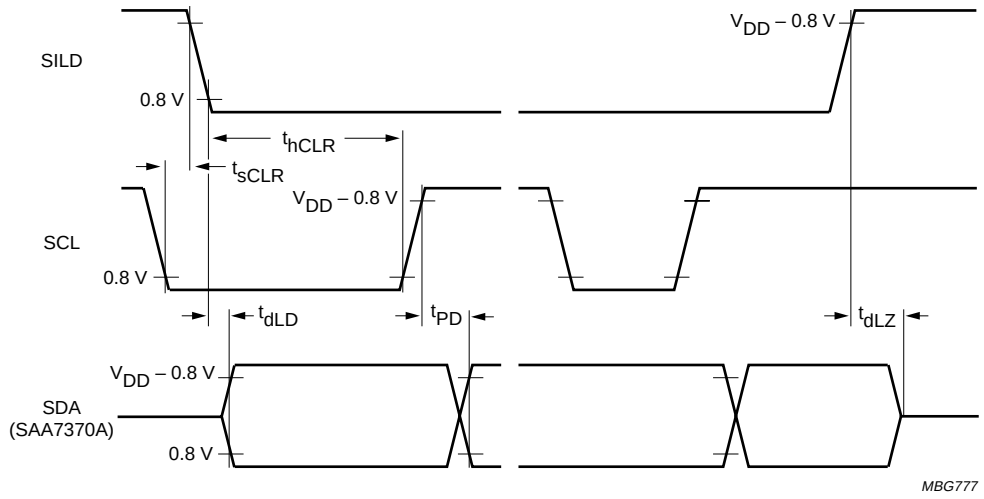


Fig.35 4-wire bus microcontroller timing; read mode (servo commands).

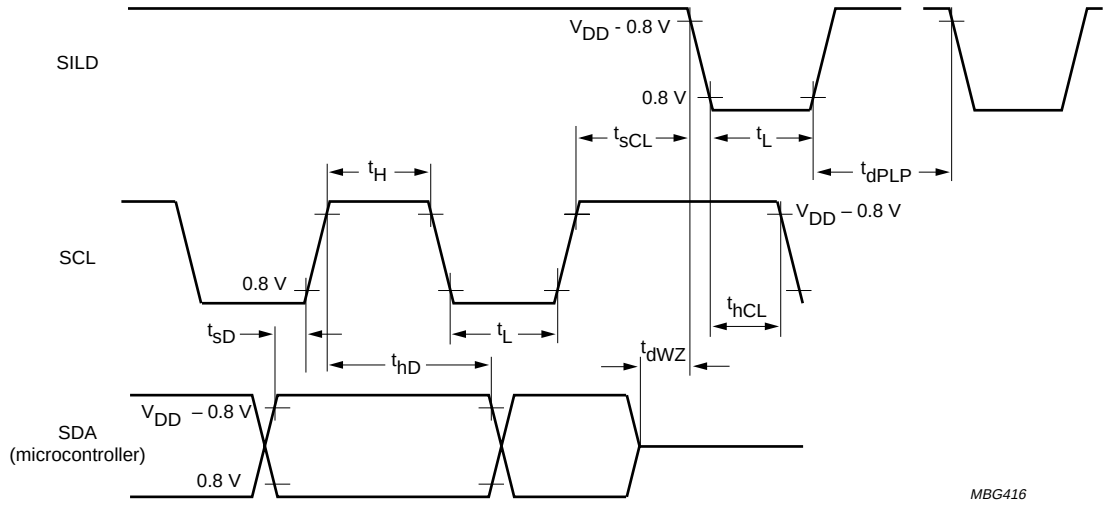


Fig.36 4-wire bus microcontroller timing; write mode (servo commands).

13 APPLICATION INFORMATION

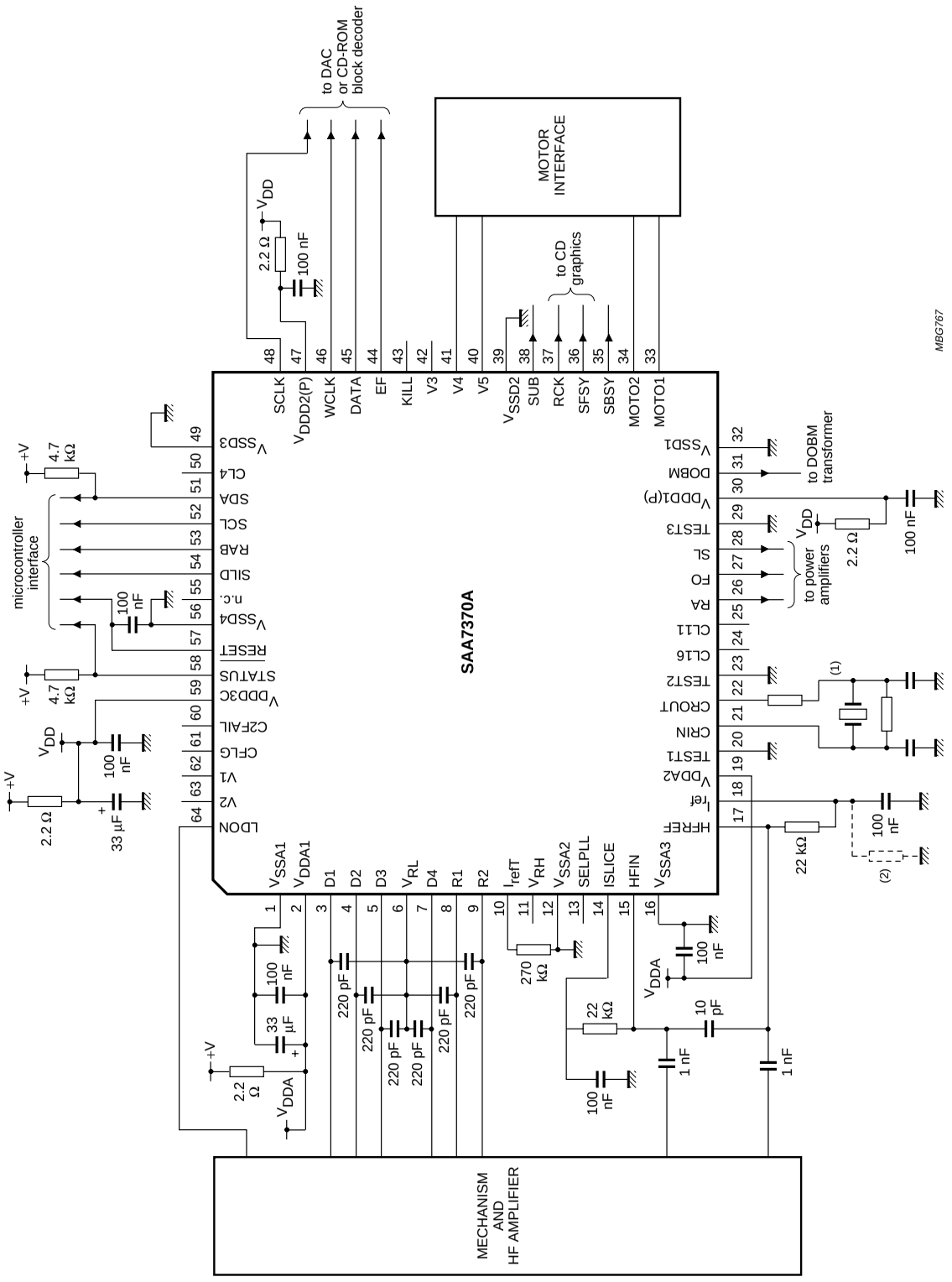
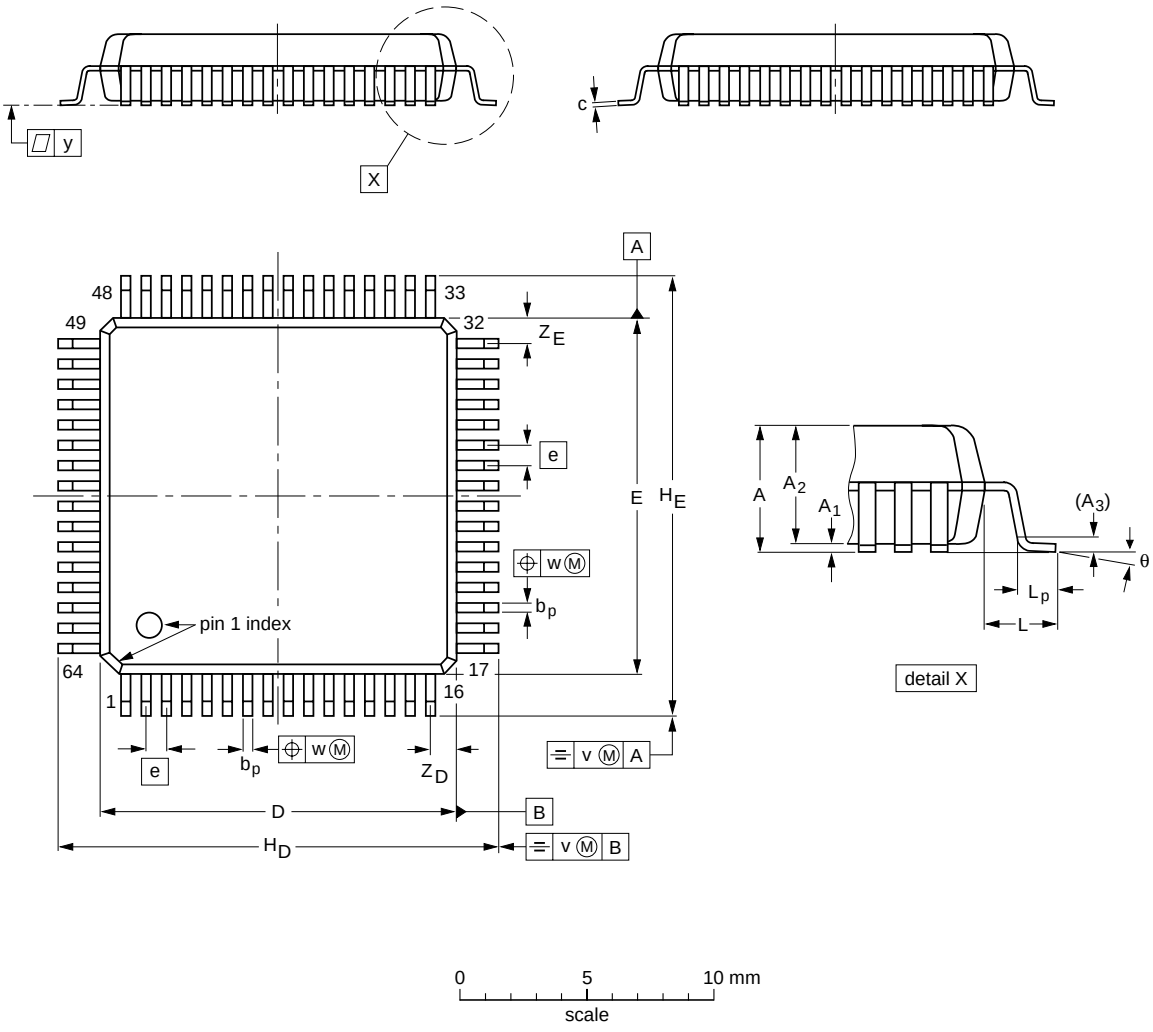


Fig.37 Typical application diagram.

(1) For crystal oscillator see Figs 3 and 4.
(2) For n = 8 applications an additional resistor (value tbf) should be added between I_{ref} (pin 18) and ground.

14 PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm **SOT393-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.00	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.60	1.03 0.73	0.16	0.16	0.10	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT393-1		MS-022				~~96-05-21~~ 97-08-04

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

15.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

15.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

18 PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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