Z89138/ Z89139 (ROMLESS)

VOICE PROCESSING CONTROLLERS

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z89138	24	256	47	4.5V to 5.5V
Z89139		256	47	4.5V to 5.5V

Note: *General-Purpose

- Watch-Dog Timer and Power-On Reset
- Improved Low-Power STOP Mode
- On-Chip Oscillator that Accepts a Crystal or External Clock Drive
- Improved Global Power-Down Mode
- Low-Power Consumption - 200 mW (typical)
- Two Comparators
- RAM and ROM Protect
- On-Board Oscillator for 32.768 kHz Real-Time Clock
- Clock Speeds of 20.48 or 29.49 MHz
- 16-Bit Digital Signal Processor (DSP)
- 6K Word DSP Program ROM
- 512 Words On-Chip DSP RAM
- 8-Bit A/D Converter with up to 16 kHz Sample Rate
- 10-Bit PWM D/A Converter
- Six Vectored, Prioritized Z8 Interrupts
- Three Vectored, Prioritized DSP Interrupts
- Two DSP Timers to Support Different A/D and D/A Sampling Rates
- IBM® PC-Based Development Tools
- Developer's Toolbox for T.A.M. Applications

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GENERAL DESCRIPTION

The Z89138/Z89139 is a fully integrated, dual processor controller designed for voice processing applications. The I/O control processor is a Z8® MCU with 24 KB of program memory, two 8-bit counter/timers, and up to 47 I/O pins. The DSP is a 16-bit processor with a 24-bit ALU and accumulator, 512x16 bits of RAM, single cycle instructions, and 6K words of program ROM. The chip also contains a half-flash 8-bit A/D converter with up to a 16 kHz sample rate and a 10-bit PWM D/A converter. The sampling rates for the converters are programmable. The precision of the 8-bit A/D can be extended by resampling the data at a lower rate in software. The Z8 and DSP processors are coupled by mailbox registers and an interrupt system. DSP or Z8 programs can be directed by events in each other's domain.

The Z89139 is the ROMless version of the Z89138. However, the on-chip DSP is not ROMless.

Notes: All Signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

GENERAL DESCRIPTION (Continued)

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Z8 Core Processor

The on-chip Z8 is Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripheral and I/O circuits. The Z8 offers a flexible I/O scheme, an efficient register and address space structure and a number of ancillary features, which makes it ideally suited for high-volume processing, peripheral controllers, and consumer applications.

For applications demanding powerful I/O capabilities, the Z89138 provides 47 pins dedicated to input and output. These I/O lines are grouped into six ports. Each port is configurable under software control to provide timing, status signals and parallel I/O with or without handshake.

Four basic memory resources for the Z8 are available to support a wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File. The Z8 core processor is supported by an efficient register file that allows any of 256 on-board data and control registers to be either the source and/or the destination of almost any instruction. This unique architecture eliminates traditional microprocessor Accumulator bottlenecks and permits rapid content switching.

The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The Expanded Register File consists of mailbox registers, WDT mode register, DSP Control register, Stop-Mode Recovery register, Port Configuration register, and the control and data registers for Port 4 and Port 5. Some of these registers are shared with the DSP.

To unburden the software from supporting real-time problems such as counting/timing and data communication, the Z8 offers two on-chip counter/timers with a large number of user-selectable modes.

Watch-Dog Timer and Stop-Mode Recovery features are software driven by setting specific bits in control registers.

STOP and HALT instructions support reduced power operation. The low-power Stop Mode allows parameter information to be stored in the register file if power fails. An external capacitor or battery will retain device memory and power the 32 kHz timer.

DSP Coprocessor

The DSP coprocessor is a second generation, 16-bit two's- complement CMOS Digital Signal Processor (DSP). Most instructions, including multiply and accumulate, are accomplished in a single clock cycle. The processor contains two on-chip data RAM blocks of 256 words, a 6K word program ROM, 24-bit ALU, 16x16 multiplier, 24-bit Accumulator, shifter, six-level stack, three vectored interrupts and two inputs for conditional program jumps. Each RAM block contains a set of four pointers which can be incremented or decremented automatically to affect hardware looping without software overhead. The data RAMs can be simultaneously addressed and loaded to the multiplier for a true single-cycle scalar multiply.

Four external DSP registers are mapped into the expanded register file of the Z8. Communication between the Z8 and the DSP occurs through those common registers that form the mailbox registers.

The analog output is generated by a 10-bit resolution Pulse Width Modulator (PWM). The PWM output is a digital signal with CMOS output levels. The output signal has a resolution of 1 in 1024 with a sampling rate of 16 kHz (XTAL = 20.48 MHz). The sampling rate can be changed under software control and can be set at 10 and 16 kHz. The dynamic range of the PWM is from 0 to 4V.

An 8-bit resolution half-flash A/D converter is provided. The conversion is conducted with a sampling frequency of 16 kHz. (XTAL = 20.48 MHz) in order to provide oversampling. The input signal is 4V peak to peak.

Two additional timers (Timer2 and Timer3) have been added to support different sampling rates for the A/D and D/A converters. These timers are free-running counters that divide the crystal frequency to the appropriate sampling of frequency. Two DSP I/O pins: DSP0, DSP1 are provided for application.

PIN DESCRIPTION

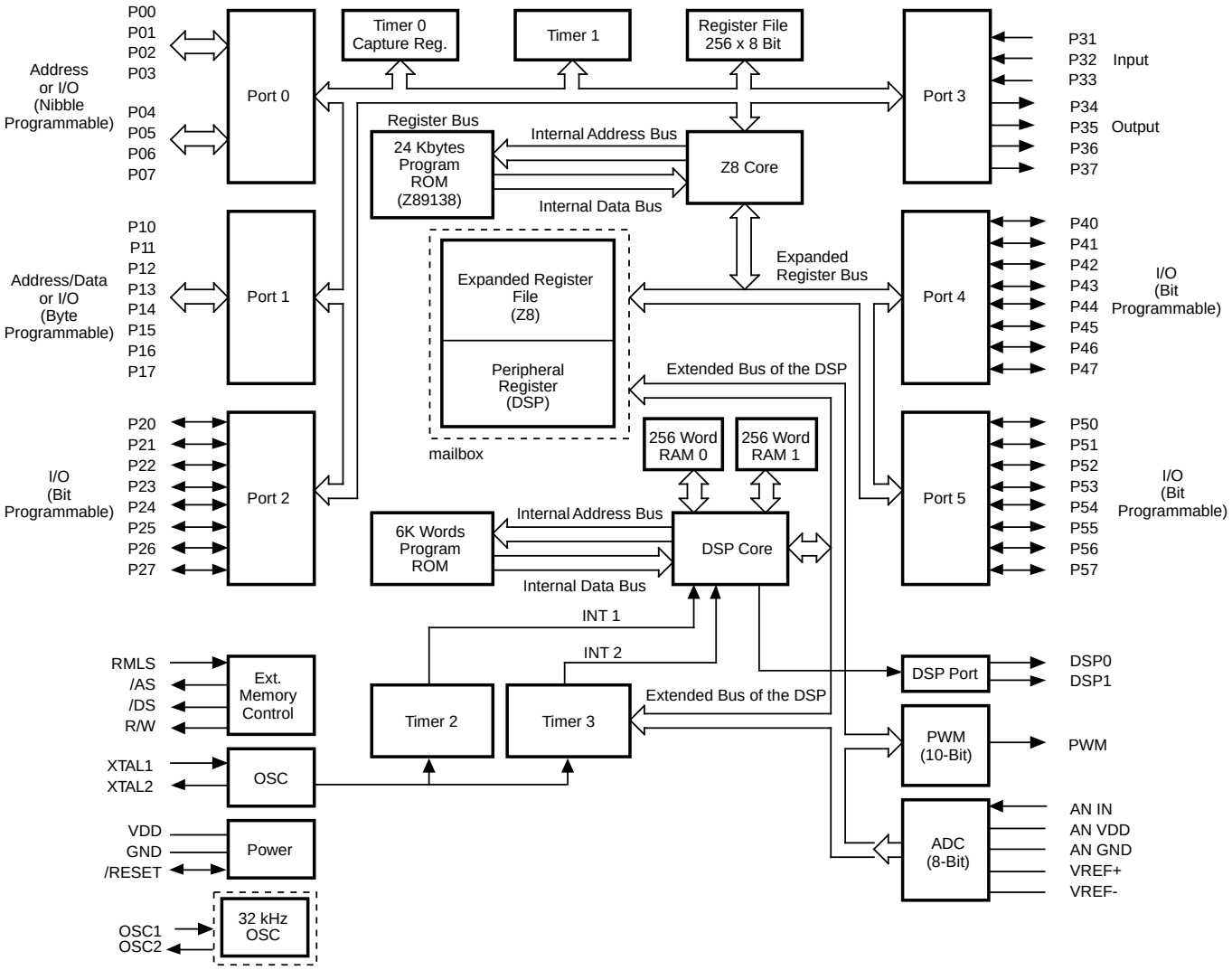


Figure 1. Z89138/139 Functional Block Diagram

PIN DESCRIPTION (Continued)

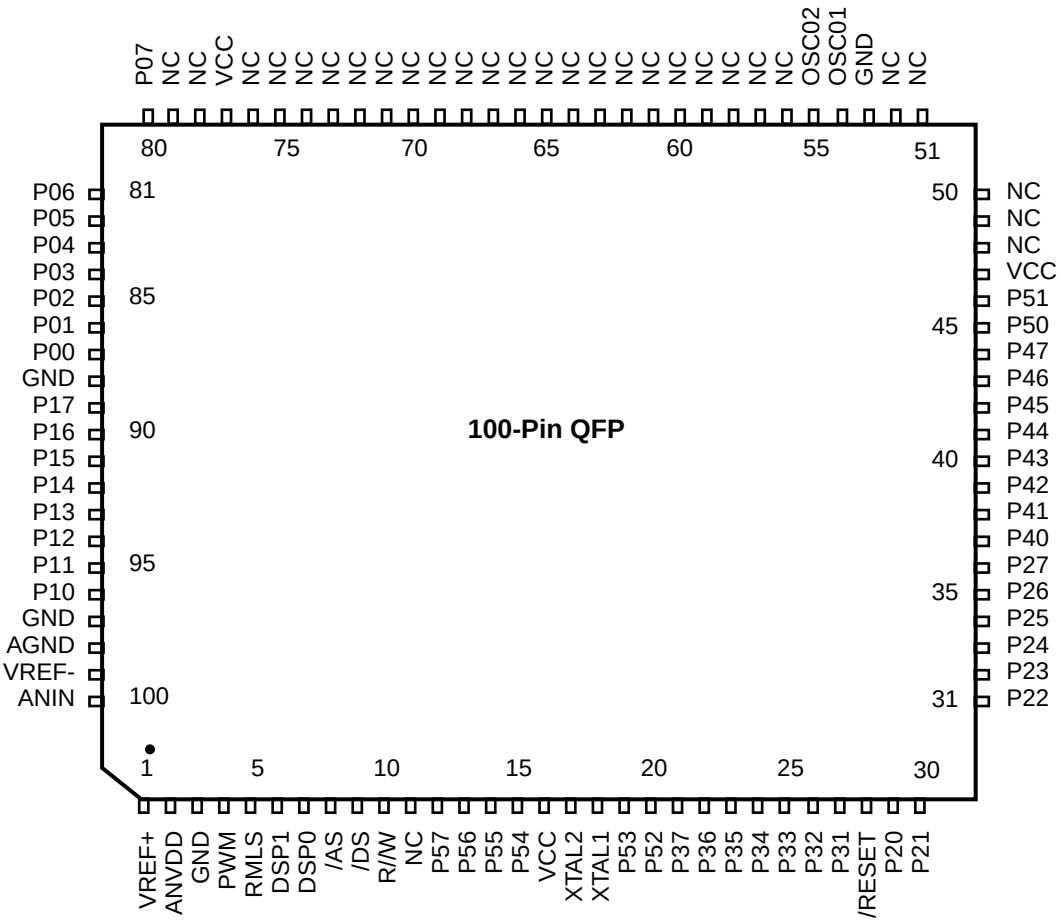


Figure 2. Z89138 100-Pin QFP Pin Configuration

Table 1. Z89138 100-Pin QFP Pin Identification

I/O Port Symbol	Pin Number	Direction	Function
GND	3, 53, 88, 97		Digital Ground
V_{CC}	16, 47, 77		Digital V_{CC} = +5V
VREF+	1	Input/Output	Analog Voltage Ref+
ANV_{DD}	2		Analog V_{DD}
PWM	4	Output	PWM Output
RMLS	5	Input	Control Input
DSP1-0	6, 7	Output	DSP User Output 1, 0
/AS	8	Output	Address Strobe
/DS	9	Output	Data Strobe
R//W	10	Output	Read/Write
NC	11		No Connection
P57-P54	12-15	Input/Output	Port 5 Bit 7-4
XTAL2	17	Output	Crystal Output (20.48 or 29.49 MHz)
XTAL1	18	Input	Crystal Input (20.48 or 29.49 MHz)
P53-P52	19, 20	Input/Output	Port 5 Bit 3-2
P37-P34	21-24	Output	Port 3 Bit 7-4
P33-P31	25-27	Input	Port 3 Bit 3-1
/RESET	28	Input/Output	Reset
P20-P27	29-36	Input/Output	Port 2, Bit 0-7
P40-P47	37-44	Input/Output	Port 4, Bit 0-7
P50-P51	45, 46	Input/Output	Port 5, Bit 0-1
NC	48-52		No Connection
OSC1	54	Input	Crystal Input (32.768 kHz)
OSC2	55	Output	Crystal Output (32.768 kHz)
NC	56-76		No Connection
NC	78, 79		No Connection
P07-P00	80-87	Input/Output	Port 0, Bit 7-0
P17-P10	89-96	Input/Output	Port 1, Bit 7-0
ANGND	98		Analog GND
VREF-	99	Input	Analog Voltage Ref-
ANIN	100	Input	Analog Input

PIN DESCRIPTION (Continued)

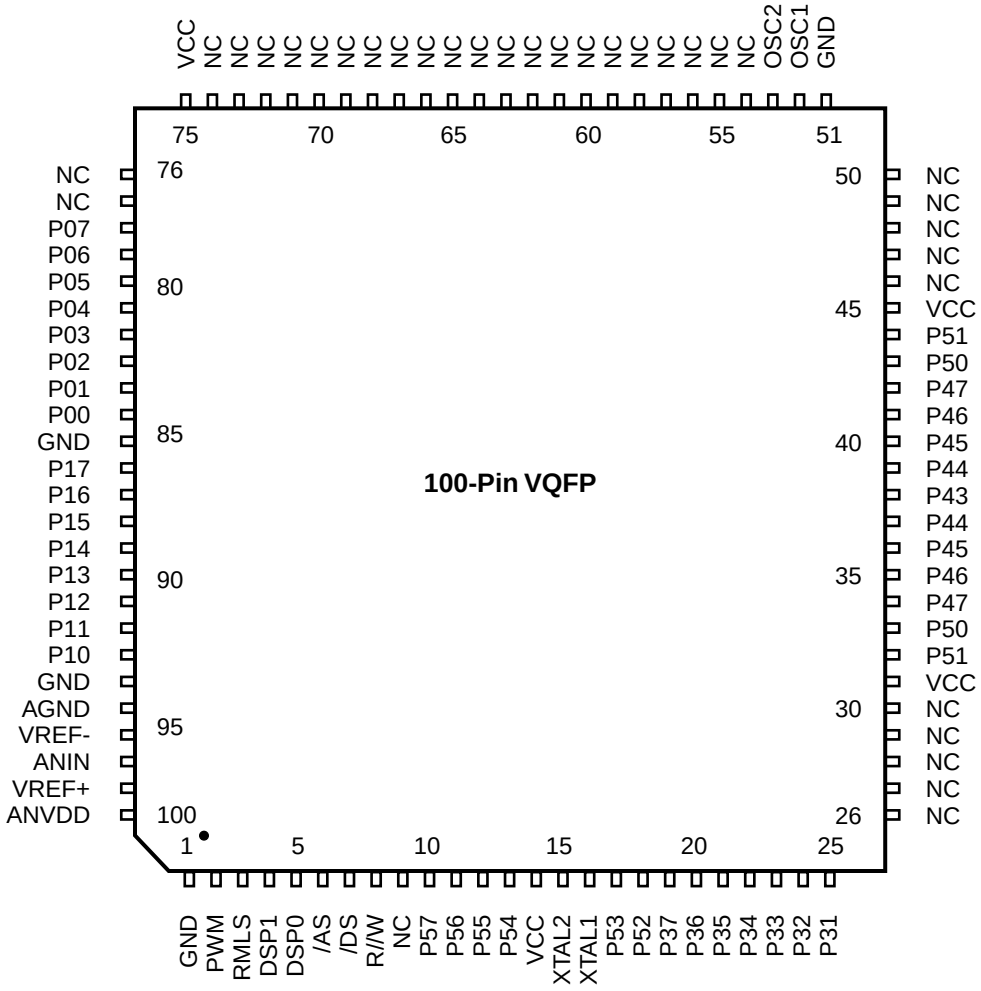


Figure 3. Z89138 100-Pin VQFP Pin Configuration

Table 2. Z89138 100-Pin VQFP Pin Identification

I/O Port Symbol	Pin Number	Direction	Symbol
GND	1, 51, 86, 95		Digital Ground
V_{CC}	14, 45, 75		Digital VCC = +5V
VREF+	99	Input/Output	Analog Voltage Ref+
ANV_{DD}	100		Analog VDD
PWM	2	Output	PWM Output
RMLS	3	Input	Control Input
DSP1-0	4, 5	Output	DSP User Output 1, 0
/AS	6	Output	Address Strobe
/DS	7	Output	Data Strobe
R//W	8	Output	Read/Write
NC	9		No Connection
P57-P54	10-13	Input/Output	Port 5 Bit 7-4
XTAL2	15	Output	Crystal Output (20.48 or 29.49 MHz)
XTAL1	16	Input	Crystal Input (20.48 or 29.49 MHz)
P53-P52	17, 18	Input/Output	Port 5 Bit 3-2
P37-P34	19-22	Output	Port 3 Bit 7-4
P33-P31	23-25	Input	Port 3 Bit 3-1
/RESET	26	Input/Output	Reset
P20-P27	27-34	Input/Output	Port 2, Bit 0-7
P40-P47	35-42	Input/Output	Port 4, Bit 0-7
P50-P51	43, 44	Input/Output	Port 5, Bit 0-1
NC	46-50		No Connection
OSC1	52	Input	Crystal Input (32.768 kHz)
OSC2	53	Output	Crystal Output (32.768 kHz)
NC	54-74		No Connection
NC	76, 77		No Connection
P07-P00	78-85	Input/Output	Port 0, Bit 7-0
P17-P10	87-94	Input/Output	Port 1, Bit 7-0
ANGND	96		Analog GND
VREF-	97	Input	Analog Voltage Ref-
ANIN	98	Input	Analog Input

PIN DESCRIPTION (Continued)

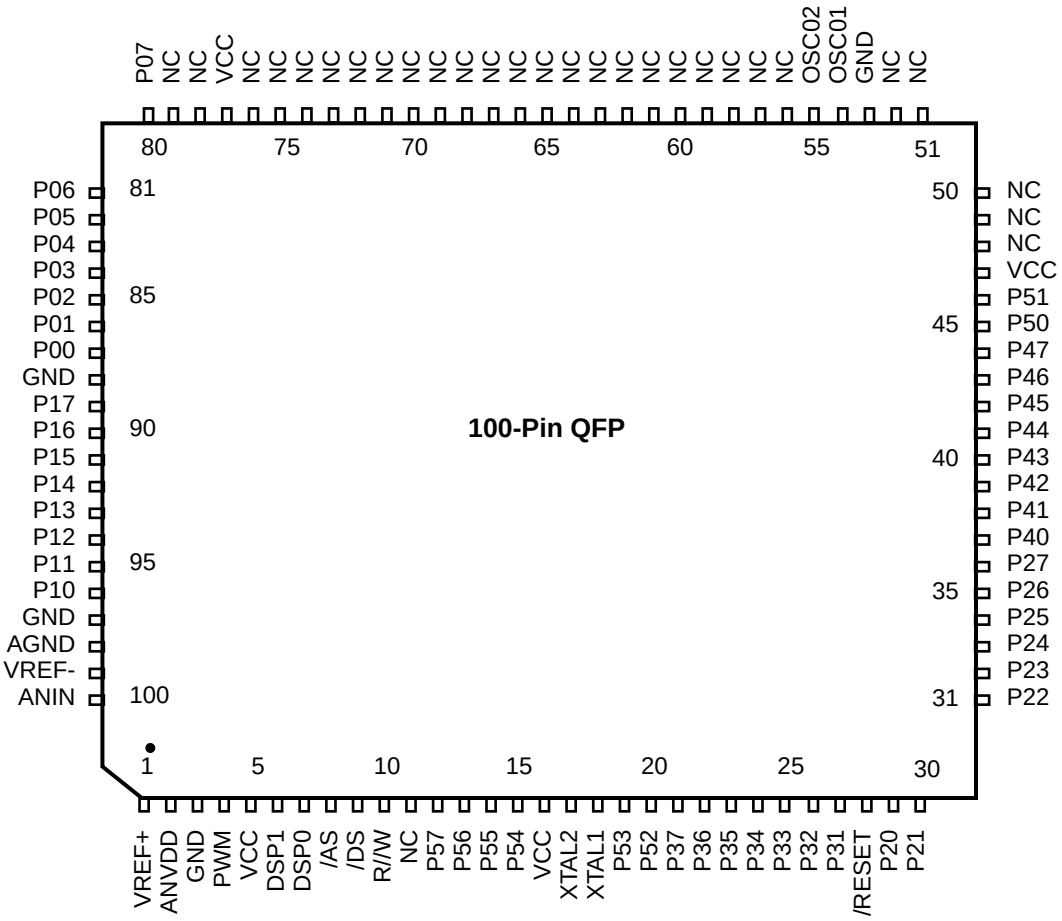


Figure 4. Z89139 100-Pin QFP Pin Configuration

Table 3. Z89139 100-Pin QFP Pin Identification

I/O Port Symbol	Pin Number	Direction	Function
GND	3, 53, 88, 97		Digital Ground
V_{CC}	5, 16, 47, 77		Digital V_{CC} = +5V
VREF+	1	Input/Output	Analog Voltage Ref+
ANV_{DD}	2		Analog V_{DD}
PWM	4	Output	PWM Output
DSP1-0	6, 7	Output	DSP User Output 1, 0
/AS	8	Output	Address Strobe
/DS	9	Output	Data Strobe
R//W	10	Output	Read/Write
NC	11		No Connection
P57-P54	12-15	Input/Output	Port 5 Bit 7-4
XTAL2	17	Output	Crystal Output (20.48 or 29.49 MHz)
XTAL1	18	Input	Crystal Input (20.48 or 29.49 MHz)
P53-P52	19, 20	Input/Output	Port 5 Bit 3-2
P37-P34	21-24	Output	Port 3 Bit 7-4
P33-P31	25-27	Input	Port 3 Bit 3-1
/RESET	28	Input/Output	Reset
P20-P27	29-36	Input/Output	Port 2, Bit 0-7
P40-P47	37-44	Input/Output	Port 4, Bit 0-7
P50-P51	45, 46	Input/Output	Port 5, Bit 0-1
NC	48-52		No Connection
OSC1	54	Input	Crystal Input (32.768 kHz)
OSC2	55	Output	Crystal Output (32.768 kHz)
NC	56-76		No Connection
NC	78-79		No Connection
P07-P00	80-87	Input/Output	Port 0, Bit 7-0
P17-P10	89-96	Input/Output	Port 1, Bit 7-0
ANGND	98		Analog GND
VREF-	99	Input	Analog Voltage Ref-
ANIN	100	Input	Analog Input

PIN DESCRIPTION (Continued)

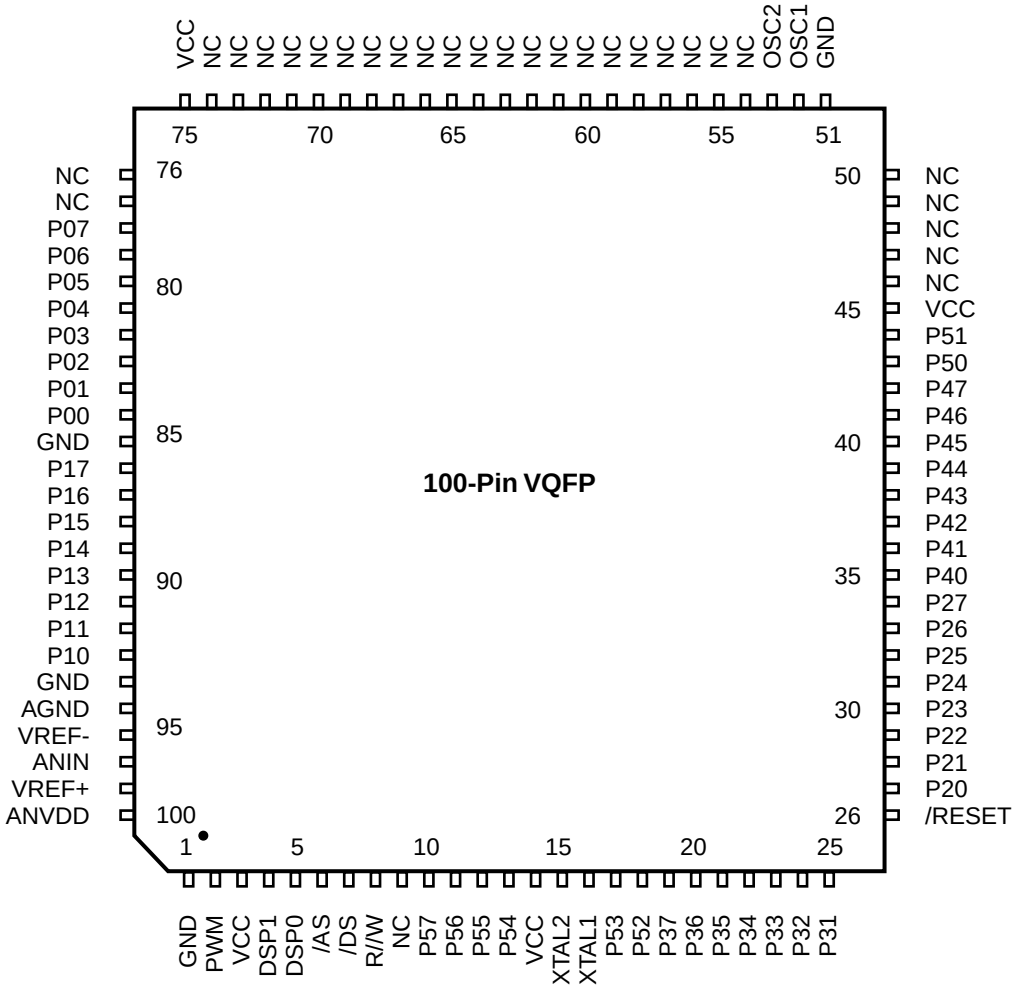


Figure 5. Z89139 100-Pin VQFP Pin Configuration

Table 4. Z89139 100-Pin VQFP Pin Identification

I/O Port Symbol	Pin Number	Direction	Function
GND	1, 51, 86, 95		Digital Ground
V_{CC}	3, 14, 45, 75		Digital V_{CC} = +5V
VREF+	99	Input/Output	Analog Voltage Ref+
ANV_{DD}	100		Analog VDD
PWM	2	Output	PWM Output
DSP1-0	4, 5	Output	DSP User Output 1, 0
/AS	6	Output	Address Strobe
/DS	7	Output	Data Strobe
R//W	8	Output	Read/Write
NC	9		No Connection
P57-P54	10-13	Input/Output	Port 5 Bit 7-4
XTAL2	15	Output	Crystal Output (20.48 or 29.49 MHz)
XTAL1	16	Input	Crystal Input (20.48 or 29.49 MHz)
P53-P52	17, 18	Input/Output	Port 5 Bit 3-2
P37-P34	19-22	Output	Port 3 Bit 7-4
P33-P31	23-25	Input	Port 3 Bit 3-1
/RESET	26	Input/Output	Reset
P20-P27	27-34	Input/Output	Port 2, Bit 0-7
P40-P47	35-42	Input/Output	Port 4, Bit 0-7
P50-P51	43, 44	Input/Output	Port 5, Bit 0-1
NC	46-50		No Connection
OSC1	52	Input	Crystal Input (32.768 kHz)
OSC2	53	Output	Crystal Output (32.768 kHz)
NC	54-74		No Connection
NC	76, 77		No Connection
P07-P00	78-85	Input/Output	Port 0, Bit 7-0
P17-P10	87-94	Input/Output	Port 1, Bit 7-0
ANGND	96		Analog GND
VREF-	97	Input	Analog Voltage Ref-
ANIN	98	Input	Analog Input

ABSOLUTE MAXIMUM RATINGS

Sym	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C

Notes:
*Voltage on all pins with respect to GND.
†See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 6).

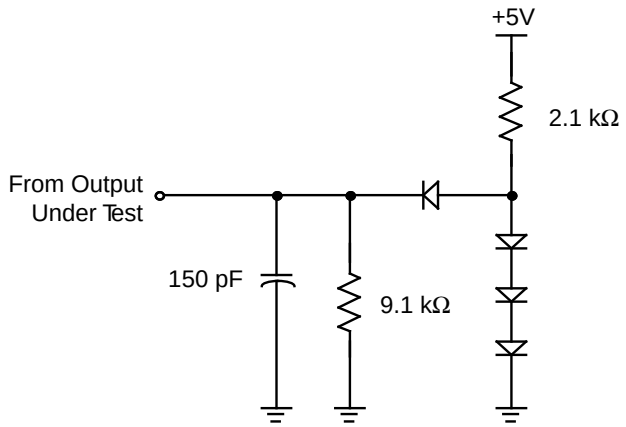


Figure 6. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note 1	T_A = 0°C to +55°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC}	Supply Current	5.0V		65	40	mA	
I_{CC1}	Halt Mode Current	5.0V		20	6	mA	
I_{CC2}	Stop Mode Current	5.0V		20	6	µA	See Note 2
V_{MAX}	Max Input Voltage	5.0V		7			
V_{CH}	Clock Input High Voltage	5.0V	0.9 V_{CC}	V_{CC} +0.3	2.5	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	5.0V	GND –0.3	0.1 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	5.0V	0.7 V_{CC}	V_{CC} +0.3	2.5	V	
V_{IL}	Input Low Voltage	5.0V	GND –0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltage	5.0V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA
V_{OL1}	Output Low Voltage	5.0V		0.4	0.1	V	I_{OL} = +4.0 mA
V_{OL2}	Output Low Voltage	5.0V		1.2	0.3	V	I_{OL} = +12 mA, 3 Pin Max
V_{RH}	Reset Input High Voltage	5.0V	.8 V_{CC}	V_{CC}	2.1	V	
V_{RI}	Reset Input Low Voltage	5.0V	GND –0.3		0.2 V_{CC}	1.7	
V_{OFFSET}	Comparator Input Offset	5.0V			25	10	mV
	Voltage						
I_{IL}	Input Leakage	5.0V	–10		10	10	µA
I_{OL}	Output Leakage	5.0V	–10		10	10	µA
I_{IR}	Reset Input Current	5.0V			–55	–30	µA

Notes:
1. 5.0V ±0.5V
2. When a 32 kHz crystal is used, additional value must be added to the STOP Mode current ICC2. The sum will be 200 µA/max, 150 µA/typical.

DC ELECTRICAL CHARACTERISTICS

Z89138 A/D Converter

			T_A = 0° C to +55°C						
Sym	**Parameter**	**V_{DD}**	**Min**	**Max**	**Units**	**Conditions**			
I_{IL}	Input Leakage Analog Input	5.5V		1.00	µA	ANV_{DD}	=	5.50	V
						V_{IN}	=	0.00	V
						V_{REFH}	=	5.50	V
						V_{REFL}	=	0.00	V
I_{IH}	Input Leakage Analog Input	5.5V		2.00	µA	ANV_{DD}	=	5.50	V
						V_{IN}	=	5.50	V
						V_{REFH}	=	5.50	V
						V_{REFL}	=	0.00	V
I_{VREFH}	Input Current	5.5V		1.00	mA	V_{IN}	=	5.50	V
						V_{REFL}	=	0.00	V
						ANV_{DD}	=	5.50	V
I_{VREFL}	Input Current	5.5V		2	µA	V_{IN}	=	5.50	V
						V_{REFL}	=	5.50	V
						ANV_{DD}	=	5.50	V
I_{VEFL}	Input Current	5.5V		–2.00	mA	V_{IN}	=	0.00	V
						V_{REFH}	=	5.50	V
						ANV_{DD}	=	0.00	V
I_{VREFL}	Input Current	5.5V		2	µA	V_{IN}	=	0.00	V
						V_{REFH}	=	5.50	V
						ANV_{DD}	=	5.50	V

DC ELECTRICAL CHARACTERISTICS

21 Other Non-Regular I/O

			T_A = 0° C to +55°C			
Sym	**Parameter**	**V_{DD}**	**Min**	**Max**	**Units**	**Conditions**
I_{IRH}	Input Current ROMless Pin	5.5V		6.00	µA	V_{IN} = 5.50 V
I_{IR1}	Input Current ROMless Pin	5.5V		6.00	µA	V_{IN} = 0.00 V
I_{IR}	Input Current ROMless Pin During Reset Active	5.5V		1.00	mA	V_{IN} = 5.50 V
I_{IHX2}	Input Current XTAL2 pin in STOP Mode	5.5V		1.00	µA	V_{IN} = 0.00 V
I_{ILX2}	Input Current XTAL2 Pin in STOP Mode	5.5V		1.00	µA	V_{IN} = 5.50 V
I_{IHX1}	Input current XTAL1 Pin	5.5V		30	µA	V_{IN} = 0.00 V
I_{ILX1}	Input Current XTAL1 Pin	5.5V		30	µA	V_{IN} = 5.50 V
V_{OLXR}	Output Low Voltage XTAL2 Reset Inactive	5.5V		1.20	V	I_{OL} = 4.00 mA
V_{OLX}	Output Low Voltage XTAL2 Reset Inactive	5.5V		0.60	V	I_{OL} =1.00 mA
V_{OHXR}	Output High Voltage XTAL2 Reset Inactive	5.5V	4.00		V	I_{OH} = 4.00 mA
I_{VOHX}	Output High Voltage XTAL2 Reset Inactive	5.5V	4.00		V	I_{OH} =1.00 mA
I_{IH}	Input Current P31, P32, P33	5.5V		1.00	µA	V_{IN} = 5.50 V
I_{IL}	Input Current P31, P32, P33	5.5V		1.00	µA	V_{IN} = 0.00 V

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

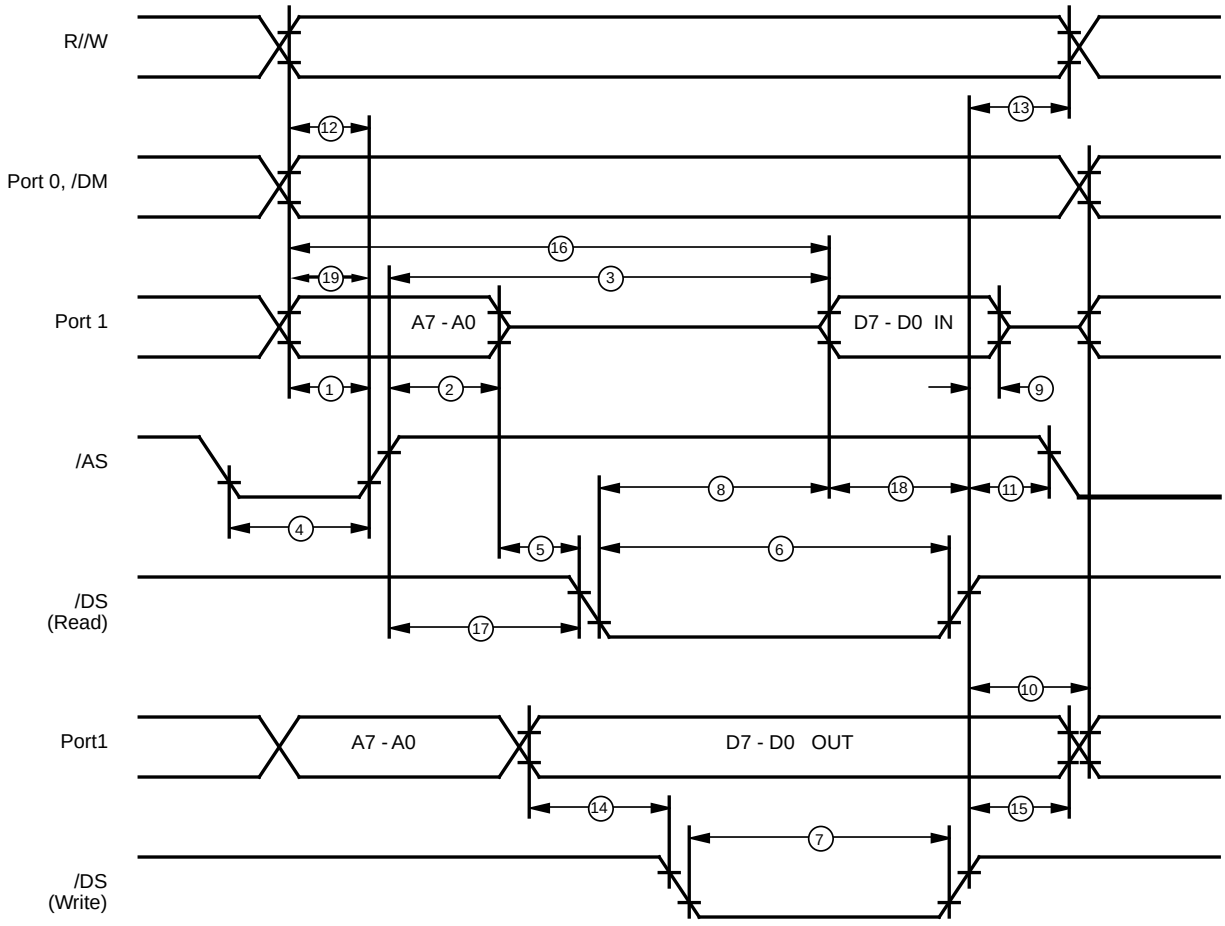


Figure 7. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

			V_{CC}	T_A= 0°C to +55°C			
No	**Symbol**	**Parameter**	**Note [4]**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS Rise Delay	5.0V	25		ns	2,3
2	TdAS(A)	/AS Rise to Address Float Delay	5.0V	35		ns	2,3
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	5.0V		150	ns	1,2,3
4	TwAS	/AS Low Width	5.0V	35		ns	2,3
5	TdAZ(DS)	Address Float to /DS Fall	5.0V	0		ns	
6	TwDSR	/DS (Read) Low Width	5.0V	125		ns	1,2,3
7	TwDSW	/DS (Write) Low Width	5.0V	75		ns	1,2,3
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	5.0V		90	ns	1,2,3
9	ThDR(DS)	Read Data to /DS Rise Hold Time	5.0V	0		ns	2,3
10	TdDS(A)	/DS Rise to Address Active Delay	5.0V	40		ns	2,3
11	TdDS(AS)	/DS Rise to /AS Fall Delay	5.0V	35		ns	2,3
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	5.0V	25		ns	2,3
13	TdDS(R/W)	/DS Rise to R//W Not Valid	5.0V	35		ns	2,3
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	5.0V	40		ns	2,3
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	5.0V	25		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid	5.0V		180	ns	1,2,3
17	TdAS(DS)	/AS Rise to /DS Fall Delay	5.0V	48		ns	2,3
18	TdDI(DS)	Data Input Setup to /DS Rise	5.0V	50		ns	1,2,3
19	TdDM(AS)	/DM Valid to /AS Fall Delay	5.0V	20		ns	2,3

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle dependent characteristics table.
4. 5.0V ±0.5 V.

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

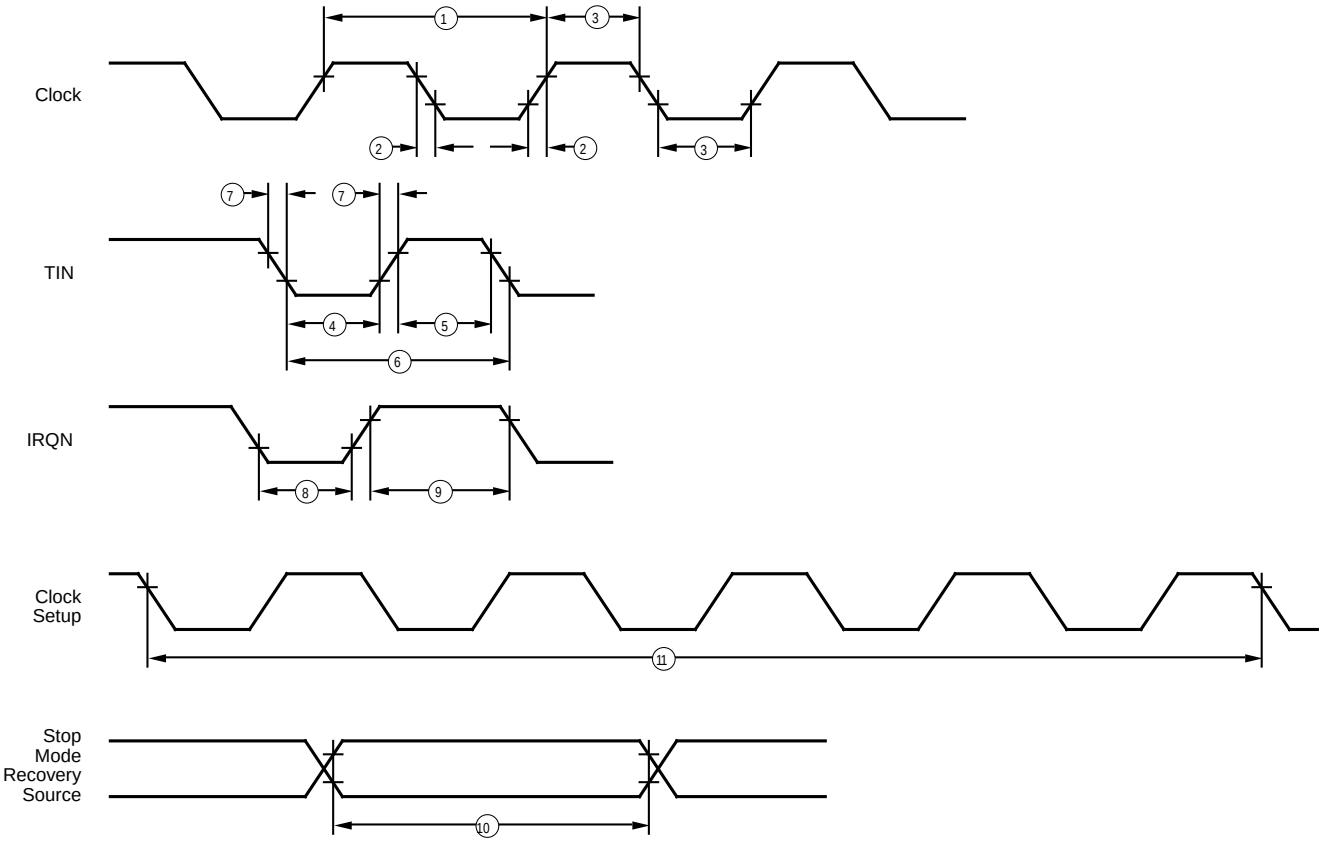


Figure 8. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table

			V_{CC}	T_A= 0°C to +55°C			
No	**Sym**	**Parameter**	**Note 5**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	5.0V	48.83		ns	1, 6
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		6	ns	1
3	TwC	Input Clock Width	5.0V	17		ns	1,7
4	TwTinL	Timer Input Low Width	5.0V	70		ns	
5	TwTinH	Timer Input High Width	5.0V	3TpC			1
6	TpTin	Timer Input Period	5.0V	8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	5.0V		100	ns	1
8a	TwIL	Int. Request Low Time	5.0V	70		ns	1,2
8b	TwIL	Int. Request Low Time	5.0V	3TpC			1
9	TwIH	Int. Request Input High Time	5.0V	3TpC			1
10	Twsm	Stop-Mode Recovery Width Spec	5.0V	12		ns	1
11	Tost	Oscillator Start-up Time	5.0V	5TpC			3
12	Twdt	Watch-Dog Timer	5.0V	5		ms	D1 = 0, D0 = 0 [4]
			5.0V	15		ms	D1 = 0, D0 = 1 [4]
			5.0V	25		ms	D1 = 1, D0 = 0 [4]
			5.0V	100		ms	D1 = 1, D0 = 1 [4]

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. SMR-D5 = 0
4. Reg. WDT
5. 5.0V ±0.5 V
6. For 29.49 MHz, it will be 30.53 ns.
7. For 29.49 MHz, it will be 9 ns.

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Diagrams

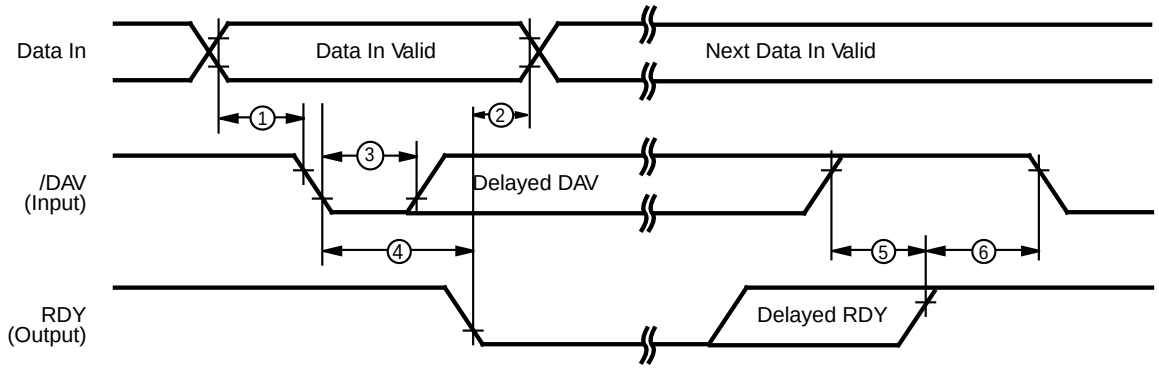


Figure 9. Input Handshake Timing

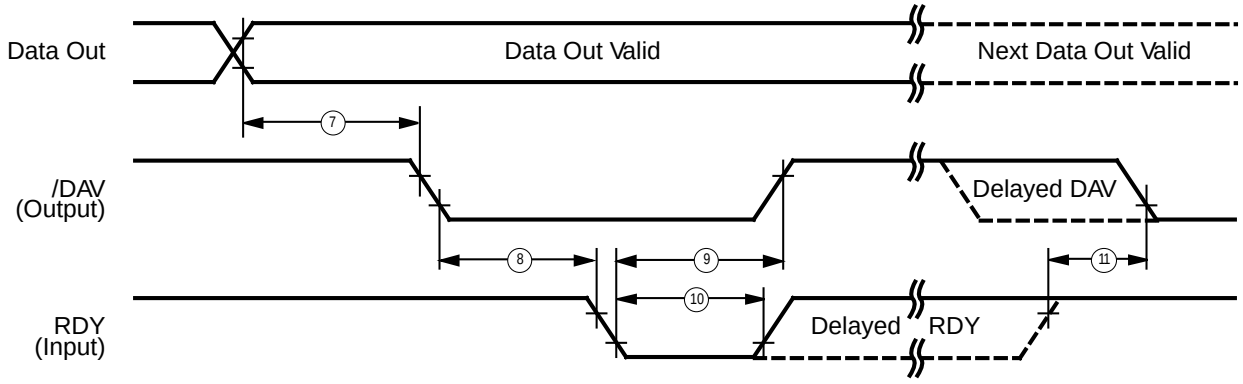


Figure 10. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note	T_A= 0°C to +55°C Min	Max	Units	Data Direction
1	TsDI(DAV)	Data In Setup Time	5.0V	0		ns	IN
2	ThDI(RDY)	RDY to Data Hold Time	5.0V	0		ns	IN
3	TwDAV	Data Available Width	5.0V	40		ns	IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0V		70	ns	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	5.0V		40	ns	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	5.0V	0		ns	IN
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay	5.0V	TpC		ns	OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0V	0		ns	OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0V		70	ns	OUT
10	TwRDY	RDY Width	5.0V	40		ns	OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0V		40	ns	OUT

Note: 5.0V ±0.5V

PIN FUNCTIONS

/RESET (input, active Low). This pin initializes the MCU. Reset is accomplished either through Power-On Reset (POR), Watch-Dog Timer (WDT) reset, Stop-Mode Recovery, or external reset. During POR and WDT Reset, the internally generated reset signal is driving the reset pin Low for the POR time. Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions. A /RESET will reset both the Z8 and the DSP.

For the Z8: After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. Program execution begins at location 000CH (hexadecimal), 5-10 TpC cycles after /RESET is released. The Z8 does not reset WDT, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

For the DSP: After POR, the DSP is in RUN mode. The Z8 controls the DSP commands to HALT, RUN or RESET. When the DSP is in HALT mode, it cannot be woke up with WDT or SMR.

RMLS ROMless (input, active High). This pin, when connected to VDD, disables the internal Z8 ROM. (Note that, when pulled Low to GND, the device functions normally as the ROM version.) The DSP cannot be configured as ROMless. This pin is only available on the Z89138.

R//W Read/Write (output, write Low). The R//W signal defines the signal flow when the Z8 is reading or writing to an external program or data memory. The Z8 is reading when this pin is High and writing when this pin is Low.

/AS Address Strobe (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

/DS Data Strobe (output, active Low). Data Strobe is activated once for each external memory transfer. For read operations, data must be available prior to the trailing edge of /DS. For write operations, the falling edge of /DS indicates that output data is valid.

XTAL1 Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or an external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, or LC network to the on-chip oscillator output.

DSP0 (output). DSP0 is a general-purpose output pin connected to bit 6 of the Analog Control Register (DSP EXT4). This bit has no special significance and can be used to output data by writing to bit 6 of the ACR.

DSP1 (output). DSP1 is a general-purpose output pin connected to bit 7 of the Analog Control Register (DSP EXT4). This bit has no special significance and can be used to output data by writing to bit 7 of the ACR.

PWM Pulse Width Modulator (Output). The PWM is a 10-bit resolution D/A converter. This output is a digital signal with CMOS output levels.

AN_{IN} (input). Analog input for the A/D converter.

ANV_{DD}. Analog power supply for the A/D converter.

VREF+ (input). Reference voltage (High) for the A/D converter.

V_{DD}. Digital power supply for the Z89138.

GND. Digital ground for the Z89138.

OSC1 Oscillator 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network to the on-chip oscillator input.

OSC2 Oscillator 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network to the on-chip oscillator output.

NC No Connect. For the 100-pin QFP package, pins 63 through 76, and pins 78 and 79 should be tied to Ground. Other NC pins must float.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and the output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction to Port 0 of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble.

The Auto Latch on Port 0 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after reset.)

Port 0 is set in the high-impedance mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R//W (Figure 11).

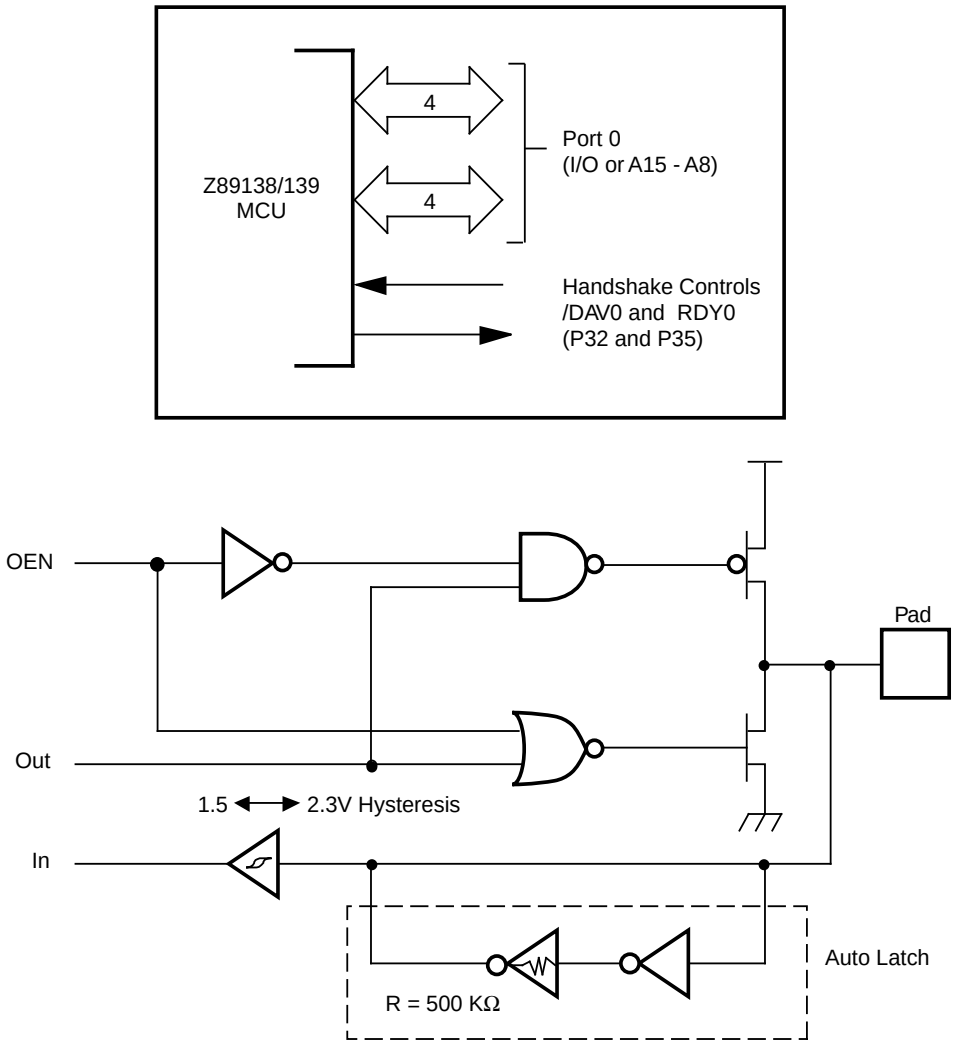


Figure 11. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS compatible port (Figure 12). It has multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output drivers are push-pull.

Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). Memory locations greater than 24575 (Z89138) (in ROM mode) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the Z89138/139 to share common resources in multiprocessor and DMA applications.

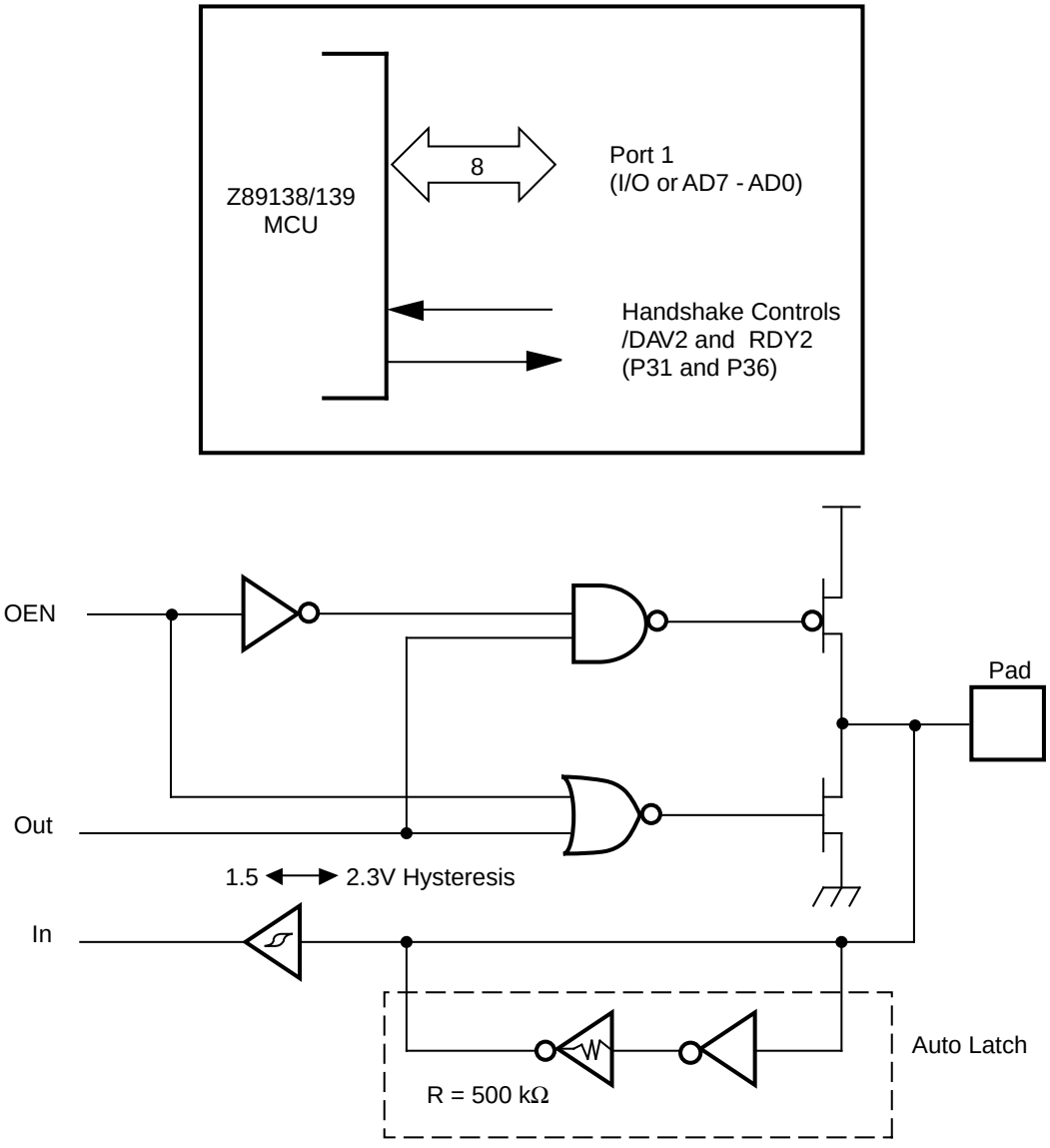


Figure 12. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines are configured under software control independently as inputs or outputs. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain.

Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 13).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

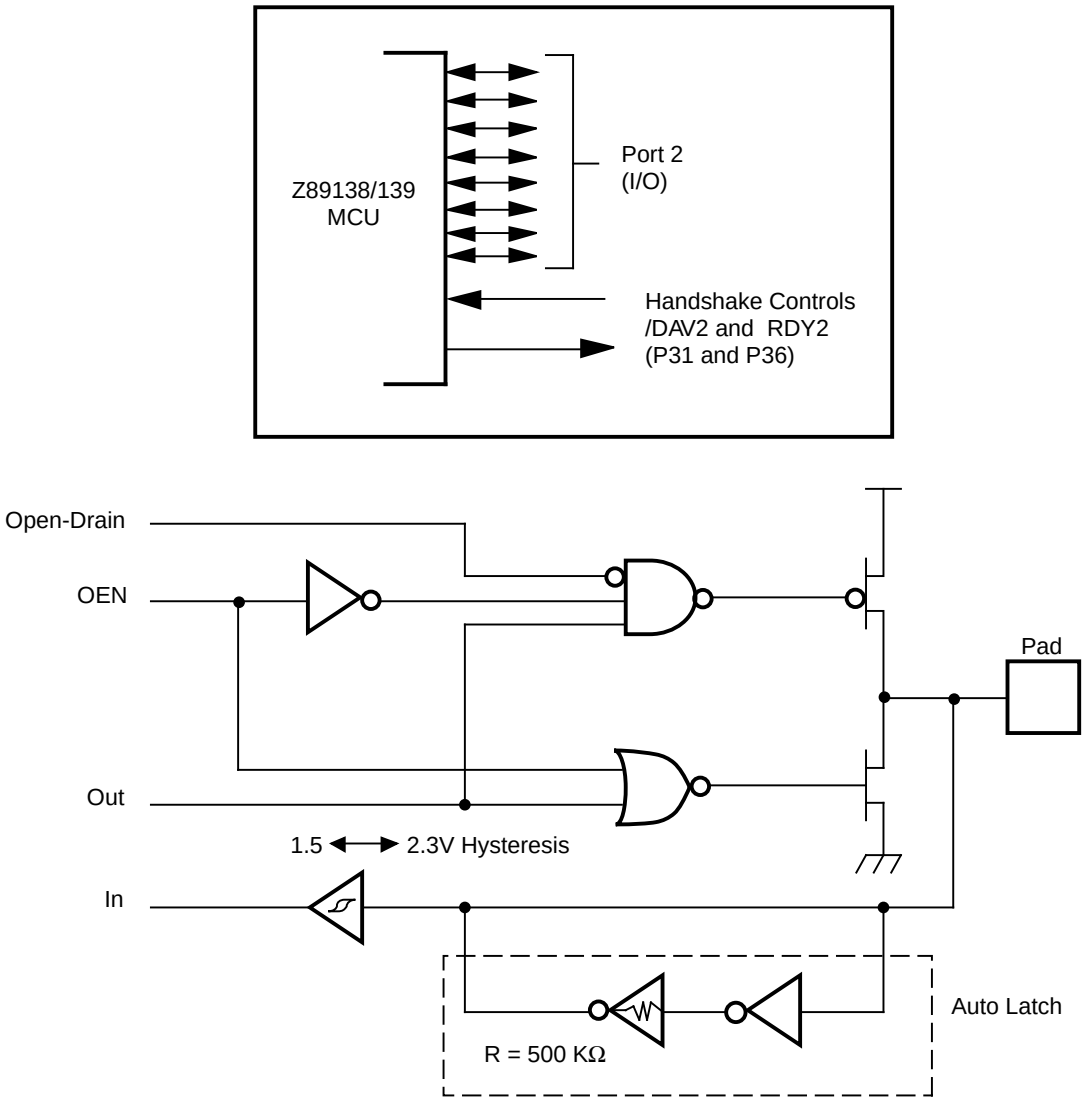


Figure 13. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P31). Port 3 is a 7-bit, CMOS compatible port with three fixed inputs (P33-P31) and four fixed outputs (P37-P34). It is configured under software control for input/output, counter/timers, interrupt, and port handshakes. Pins P31, P32, and P33 are standard CMOS inputs; outputs are push-pull.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming bit 1 of the Port 3 Mode Register. Port 3, pin 3 is a falling edge interrupt input. P31 and P32 are programmable as rising, falling or both edge-triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to counter/timer1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); three external interrupt request signals (IRQ3-IRQ1); timer input and output signals (T_{IN} and T_{OUT}) (Figure 14).

Comparator Inputs. Port 3, pins P31 and P32 all have a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In analog mode, P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source.

Table 5. Port 3 Pin Assignments

Pin	I/O	CTC1	AN IN	Int.	P0 HS	P1 HS	P2 HS	EXT
P31	IN	T_{IN}	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT					R/D		DM
P35	OUT				R/D			
P36	OUT	T_{OUT}					R/D	
P37	OUT							

Notes:
HS = Handshake Signals
D = DAV
R = RDY

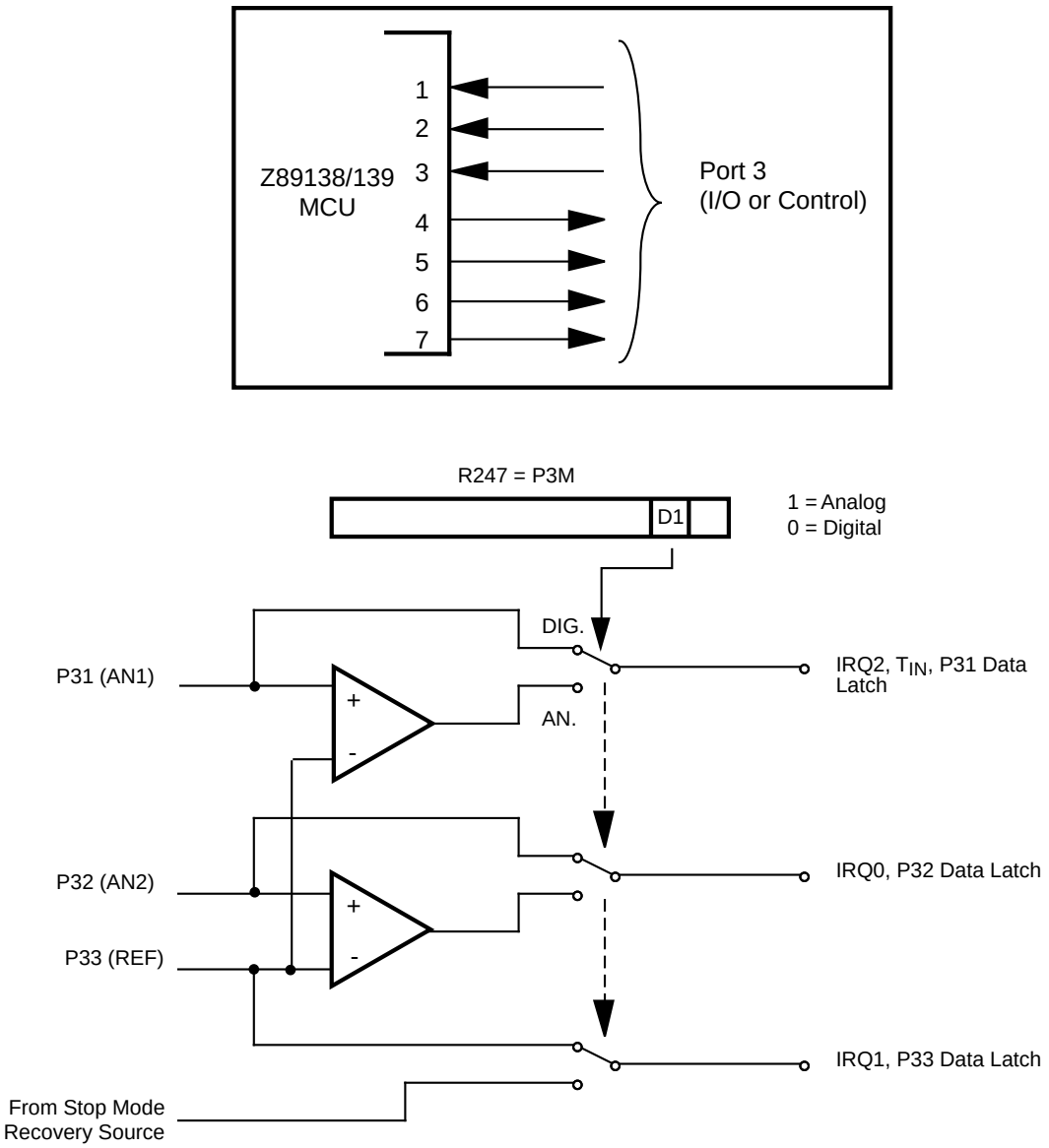


Figure 14. Port 3 Configuration

PIN FUNCTIONS (Continued)

Port 4 (P47-P40). Port 4 is an 8-bit, bidirectional, CMOS compatible I/O port (Figure 15). These eight I/O lines are configured under software control independently as inputs or outputs. Port 4 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain.

Port 4 is a bit programmable general-purpose I/O port. The control registers for Port 4 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 4 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

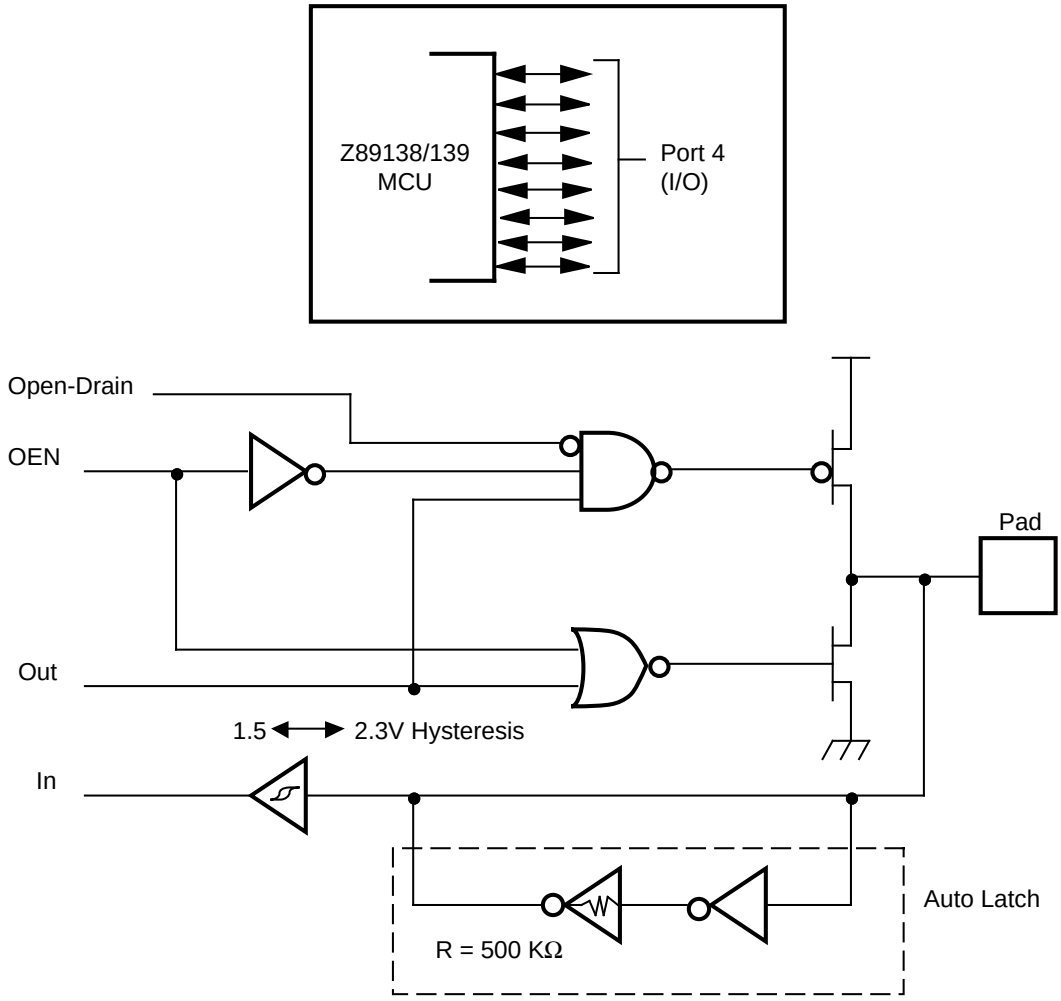


Figure 15. Port 4 Configuration

Port 5 (P53-P50). Port 5 is a 4-bit, bidirectional, CMOS compatible I/O port (Figure 16). These four I/O lines are configured under software control independently as inputs or outputs. Port 5 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain.

Port 5 is a bit programmable general-purpose I/O port. The control registers for Port 5 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 5 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

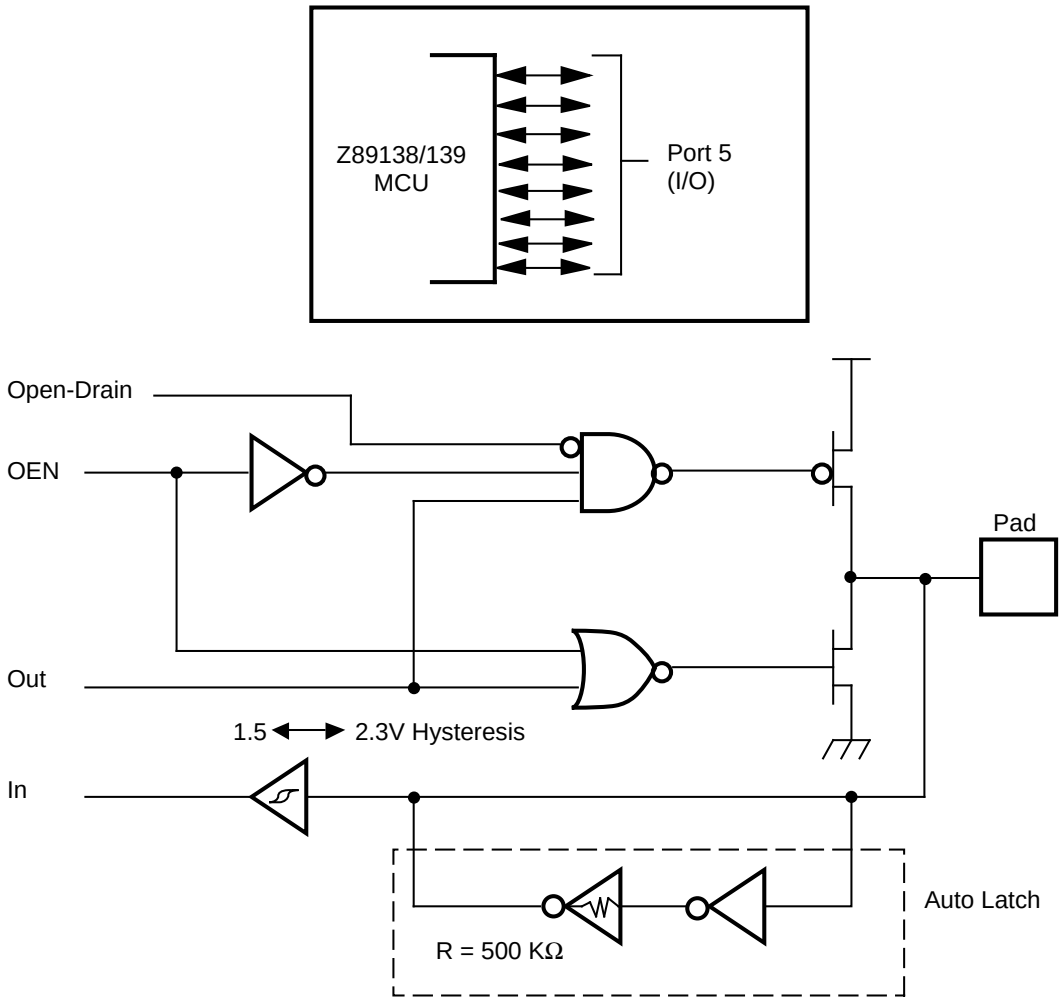


Figure 16. Port 5 Configuration

Z8 FUNCTIONAL DESCRIPTION

The Z8 core of the Z89138/139 incorporates special functions to enhance the Z8's application in a variety of voice-processing applications.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- External Reset

Program Memory. The Z8 addresses up to 24 KB of internal program memory and 40 KB external memory (Figure 17). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors which correspond to the five user interrupts and one DSP interrupt. Byte 12 to byte 24575 consist of on-chip mask-programmed ROM. At addresses 24576 and greater the Z8 executes external program memory. In ROMless mode, the Z8 will execute external program memory beginning at byte 12 and continuing through byte 65535.

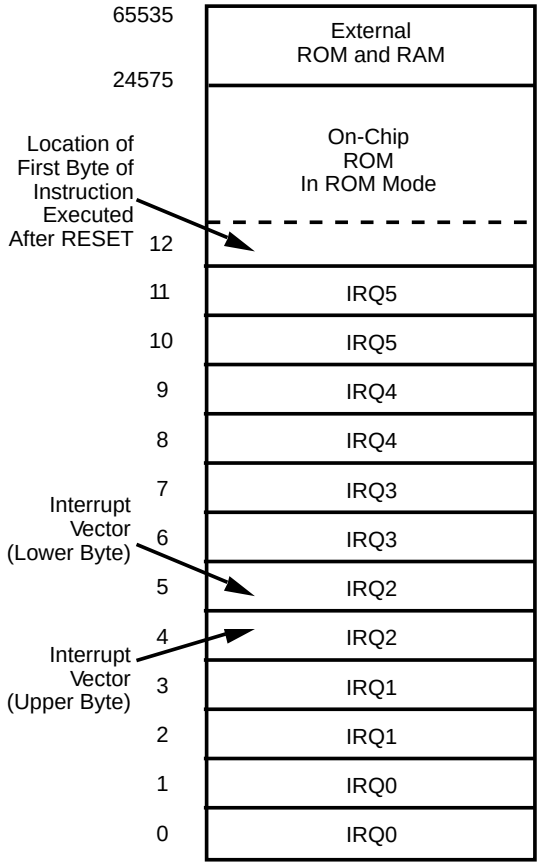


Figure 17. Program Memory

ROM Protect. The 24 KB of internal program memory for the Z8 is mask programmable. A ROM protect feature prevents "dumping" of the ROM contents of Program Memory by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions. The ROM Protect option is mask-programmable, to be selected by the customer at the time the ROM code is submitted.

Data Memory (/DM). In ROM Mode, the Z8 can address up to 40 KB of external data memory beginning at location 24576 (Figure 18). In ROMless mode, the Z8 can address the full 64 KB of external data memory beginning at location 12. External data memory can be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on Port 34, is used to distinguish between data and program memory space. The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory (Figure 18).

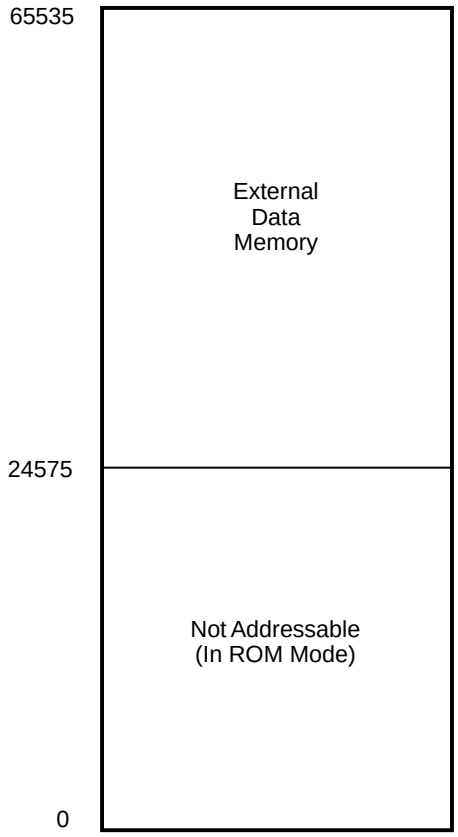


Figure 18. Data Memory Map

Register File. The standard Z8 register file consists of four I/O port registers, 236 general-purpose registers, and 15 control and status registers (R0-R3, R4-R239, and R241-R255, respectively). The instructions access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 19). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group (Figure 20).

Note: Register Group E (Registers EF-E0) is only accessed through a working register and indirect addressing modes.

RAM Protect. The upper portion of the Z8's RAM address spaces 80H to EFH (excluding the control registers) is protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates the RAM Protect from the internal ROM code by loading a bit D6 in the IMR register to either a 0 (OFF) or a 1 (ON). A 1 in D6 indicates RAM Protect enabled.

Stack. The Z8's external data memory or the internal register file is used for the stack. The 16-bit Stack Pointer (R255-R254) is used for the external stack which can reside only from 24576 to 65535 in ROM mode or 0 to 65535 in ROMless mode. An 8-bit Stack Pointer (R255) is used for the internal stack residing within the 236 general-purpose registers (R239-R4). SPH can be used as a general-purpose register when using internal stack only.

Expanded Register File. The register file on the Z8 has been expanded to allow for additional system control registers and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space has been implemented as 16 banks of 16 register groups per bank (Figure 20). These register banks are known as the ERF (Expanded Register File). Bits 7-4 of register RP (Register Pointer) select the working register group. Bits 3-0 of register RP select the Expanded Register bank (Figure 21).

The SMR register, WDT Register, control and data registers for Port 4 and Port 5, and the DSP control register are located in Bank F of the Expanded Register File. Bank B of the Expanded Register File consists of the Mailbox Interface through which the Z8 and the DSP communicate. The rest of the Expanded Register is not physically implemented and is open for future expansion.

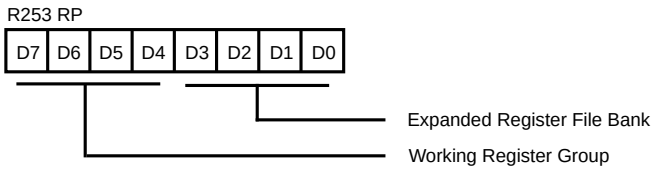


Figure 19. Register Pointer Register

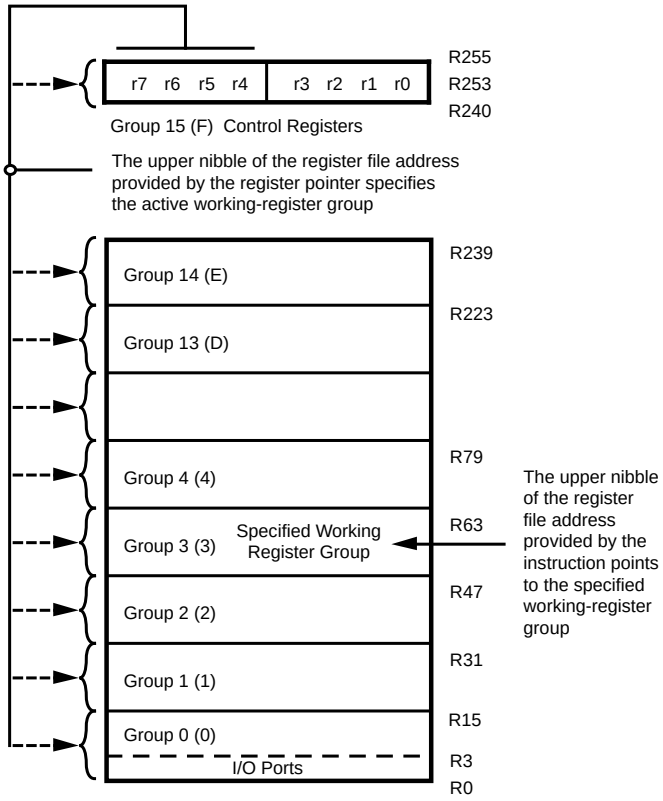


Figure 20. Register Pointer

Z8 FUNCTIONAL DESCRIPTION (Continued)

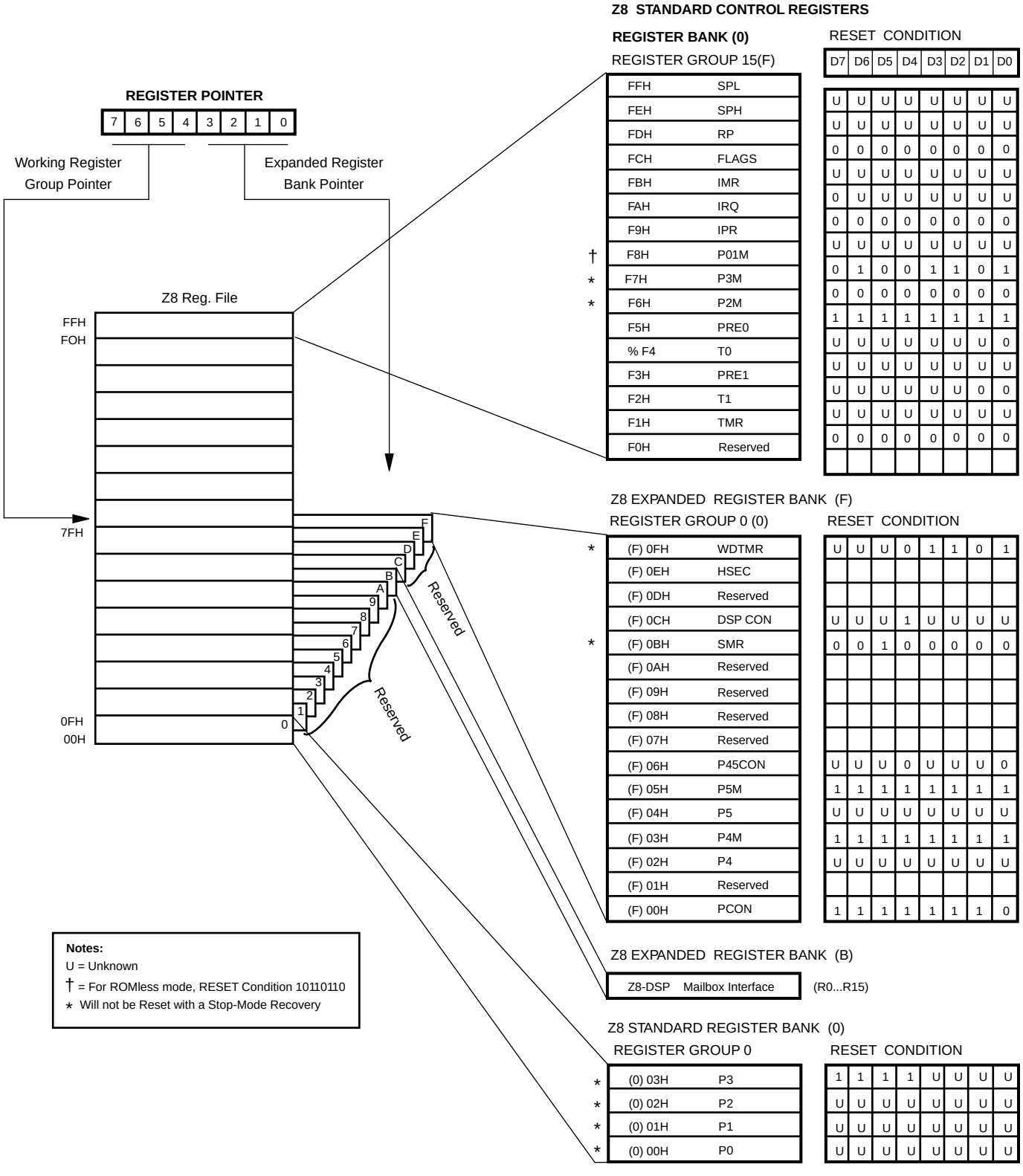


Figure 21. Expanded Register File Architecture

Interrupts. The Z8 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 22). The six sources are divided as follows; three sources are claimed by Port 3 lines P33-P31, two by counter/timers, and one by the DSP (Table 6). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

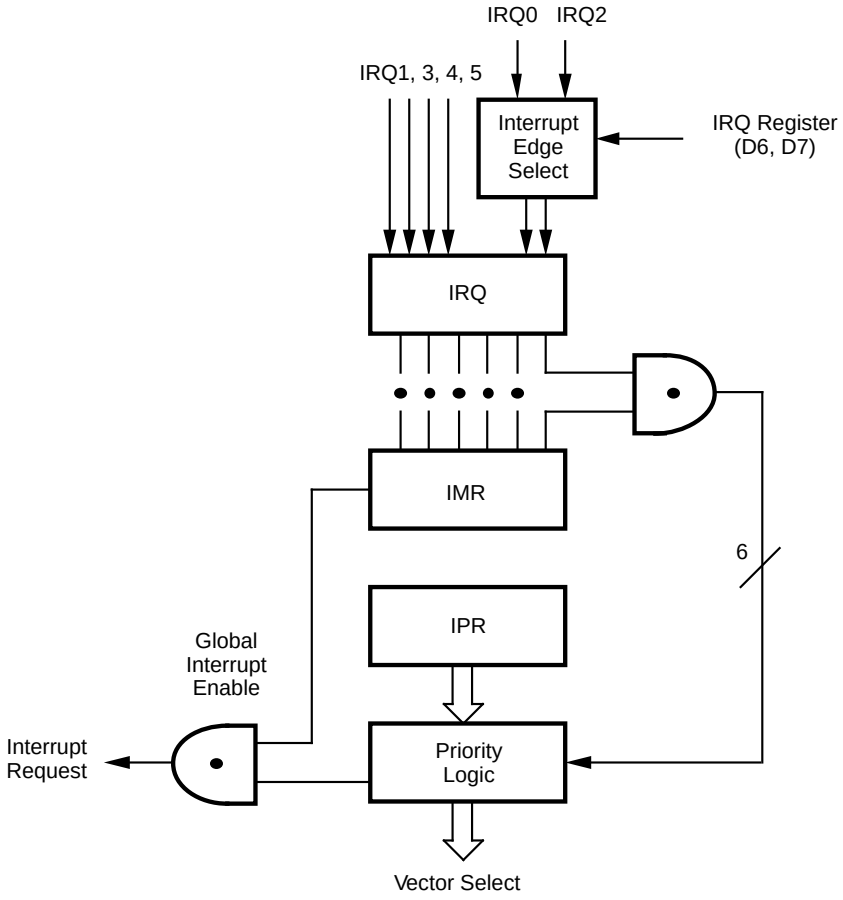


Figure 22. Interrupt Block Diagram

Table 6. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, P32, AN2	0, 1	External (P32), Programmable Rise or Fall Edge Triggered
IRQ1	/DAV1, P33	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, P31, TIN, AN2	4, 5	External (P31), Programmable Rise or Fall Edge Triggered
IRQ3	IRQ3	6, 7	Internal (DSP activated), Fall Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

Z8 FUNCTIONAL DESCRIPTION (Continued)

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, pushes the Program Counter and Status Flags to the stack, and then branches to the program memory vector location reserved for that interrupt.

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register can be polled to determine which of the interrupt requests needs service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6 . The configuration is shown in Table 7.

Table 7. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z89138/139 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 20.48 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The system clock (SCLK) is one half the crystal frequency.

The crystal is connected across XTAL1 and XTAL2 using capacitors from each pin to Ground (Figure 23).

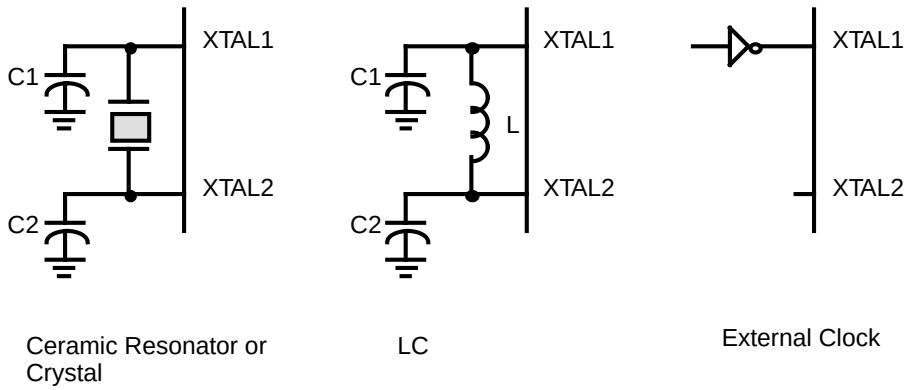


Figure 23. Oscillator Configuration

Counter/Timers. There are two 8-bit programmable counter/timers (T1,T0), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources. However, the T0 prescaler is driven by the internal clock only (Figure 24).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (0 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input via Port 31. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

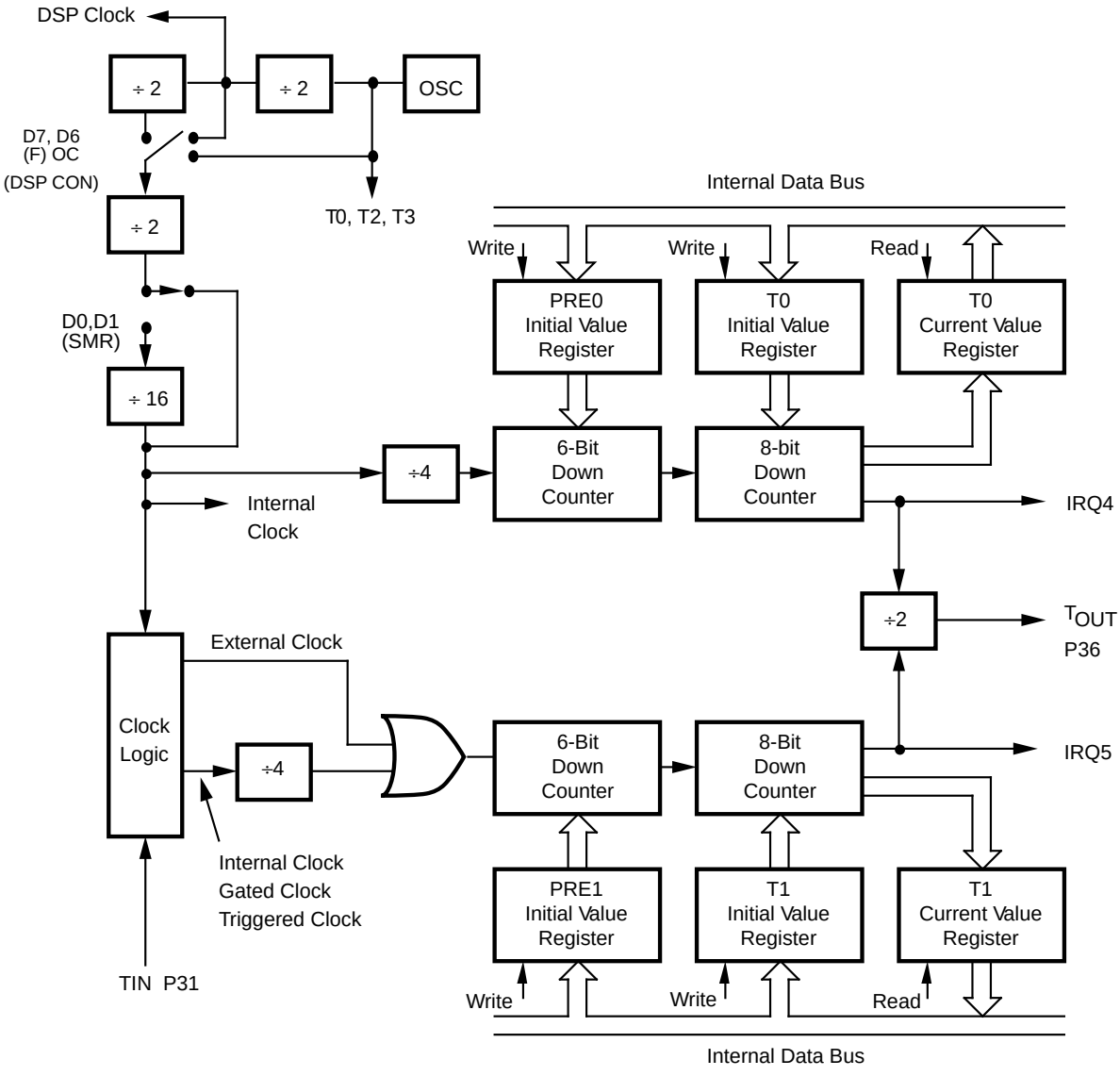


Figure 24. Counter/Timer Block Diagram

Z8 FUNCTIONAL DESCRIPTION (Continued)

Port Configuration Register (PCON). The PCON register configures the comparator output on Port 3. The PCON register (Figure 25) is located in the Expanded Register File at Bank F, location 00H.

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35, and a 0 releases the Port to its standard I/O configuration.

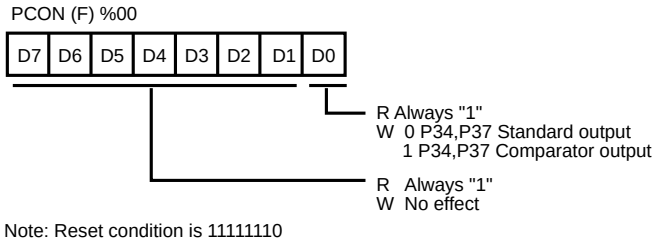


Figure 25. Port Configuration Register (PCON)

Port 4 and 5 Configuration Register (P45CON). The P45CON register configures Port 4 and Port 5, individually, to open-drain or push-pull active. This register is located in the Expanded Register File at Bank F, location 06H.

Port 4 Open-Drain (D0). Port 4 can be configured as an open-drain by resetting this bit (D0 = 0) or configured as push-pull active by setting this bit (D0 = 1). The default value is 1.

Port 5 Open-Drain (D4). Port 5 can be configured as an open-drain by resetting this bit (D4 = 0) or configured as push-pull active by setting this bit (D4 = 1). The default value is 1.

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows VCC and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status;
2. Stop-Mode Recovery (if D5 of SMR=1);
3. WDT time-out.

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation. It reduces the standby current to 20 μA or less. The STOP Mode is terminated by a reset only, either by WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate Sleep instruction. For example:,

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 26). All bits are Write-Only except bit 7, which is Read-Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR is located in Bank F of the Expanded Register group at address 0BH.

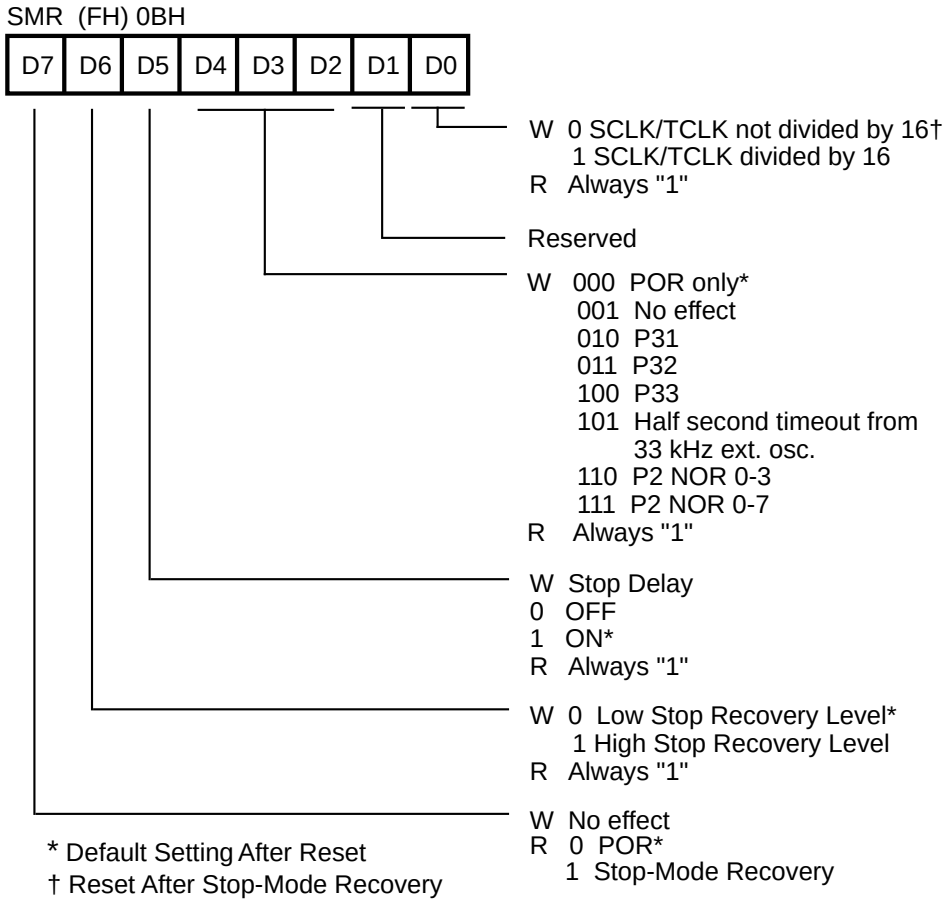


Figure 26. Stop-Mode Recovery Register (SMR)

Z8 FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources counter/timers and interrupt logic).

Stop-Mode Recovery Source (D4-D2). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Figure 27 and Table 8).

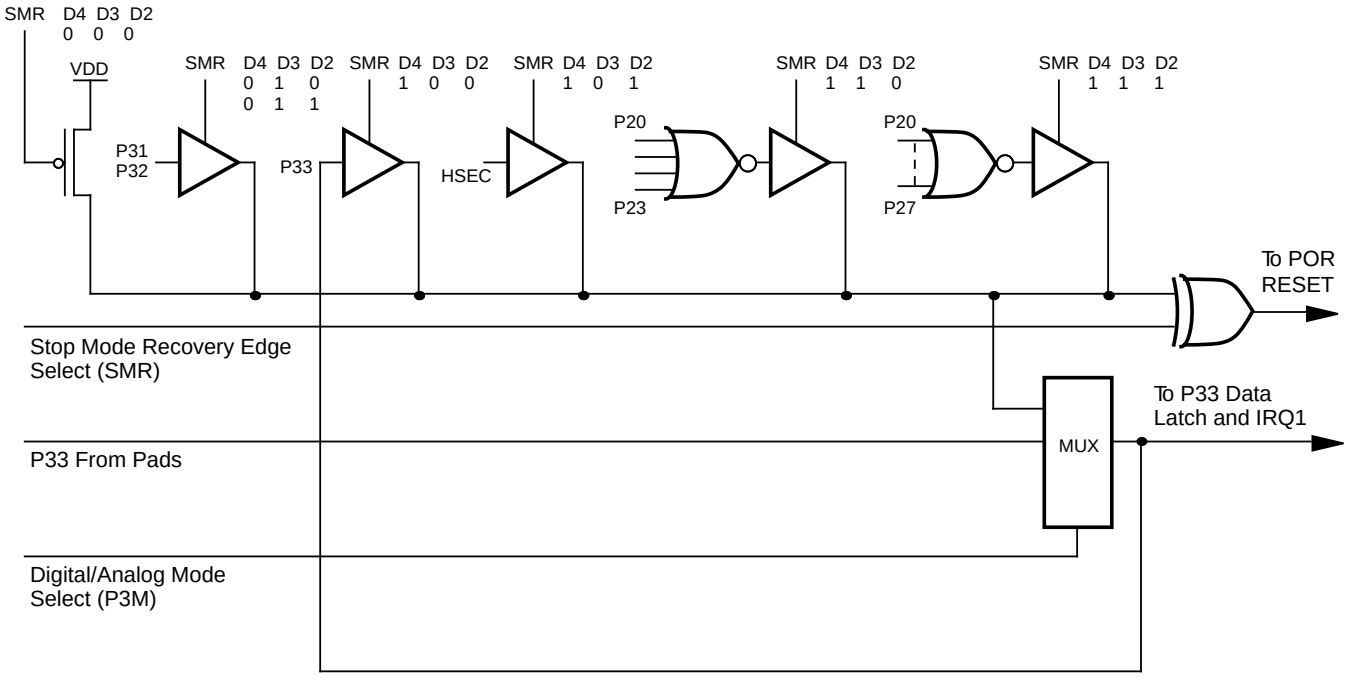


Figure 27. Stop-Mode Recovery Source

Table 8. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	No effect
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	HSEC
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). When Low, this bit disables the 5 ms /RESET delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop-Mode Recovery source is kept active for at least 5 TpC.

Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z89138/139 from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Table 8).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT /RESET. This bit is Read-Only. It is used to distinguish between a cold or warm start.

DSP Control Register (DSPCON). The DSPCON register controls various aspects of the Z8 and the DSP. It can configure the internal system clock (SCLK) or the Z8, /RESET, and HALT of the DSP, and control the interrupt interface between the Z8 and the DSP (Table 9).

Table 9. DSP Control Register (F) OCH [Read/Write]

Field DSPCON (F)0CH	Position	Attrib	Value	Label
Z8_SCLK	76------	R/W	00 01 1x	(OSC/8) (OSC/4) (OSC/2)
DSP_Reset	--5-----	R		Return “0”
		W	0	No effect
			1	Reset DSP
DSP_Run	---4----	R/W	0	Halt_DSP
			1	Run_DSP
Reserved	----32--	W		No effect
		R		Return “0”
				No effect
DSP_INT2	------1-	R		FB_DSP_INT2
		W	1	Set DSP_INT2
			0	No effect
Z8_IRQ3	-------0	R		FB_Z8_IRQ3
		W	1	Clear IRQ3
			0	No effect

Z8 IRQ3 (D0). When read, this bit indicates the status of the Z8 IRQ3. The Z8 IRQ3 is set by the DSP by writing to D9 of DSP External Register 4 (ICR). By writing a 1 to this bit, Z8 IRQ3 is Reset.

DSP INT2 (D1). This bit is linked to DSP INT2. Writing a 1 to this bit sets the DSP INT2. Reading this bit indicates the status of the DSP INT2.

DSP RUN (D4). This bit defines the HALT Mode of the DSP. If this bit is set to 0, then the DSP clock is turned off to minimize power consumption. After this bit is set to 1, then the DSP will continue code execution from where it was halted. After a hardware reset, this bit is reset to 1.

DSP RESET (D5). Setting this bit to 1 will reset the DSP. If the DSP was in HALT Mode, this bit is automatically preset to 1. Writing a 0 has no effect.

Z8 SCLK (D7-D6). These bits define the SCLK frequency of the Z8. The oscillator can be divided by 8, 4, or 2. After a reset, both bits default to 00.

Z8 FUNCTIONAL DESCRIPTION (Continued)

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 28). The WDTMR register is accessible only within 64 Z8 clock cycles after POR.

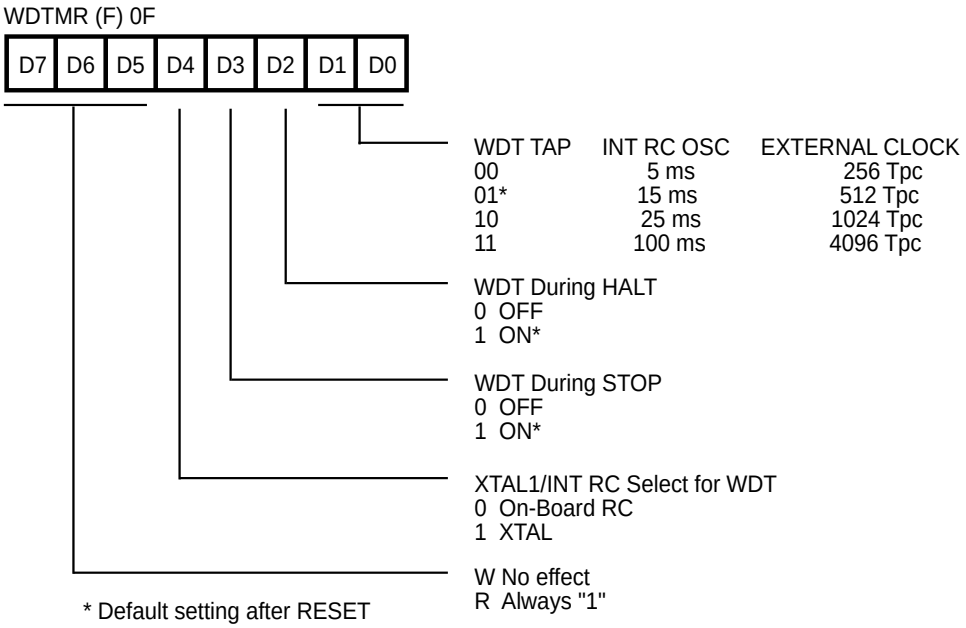


Figure 28. Watch-Dog Timer Mode Register

Half-Second Timer Status Register (HSEC). The half-second timer status register (Figure 29) is a free-running timer clocked by the external 32.768 kHz crystal. In normal operation mode, every half-second, the timer will time-out and set bit 0 (D0) of the HSEC register to 1. The user can reset this bit for real timing. In Stop mode, this timer can be used as a Stop-Mode Recovery source. Every half-second, the timer will recover the Stop mode and bit 0 of the HSEC register will be set to 1. Therefore, in STOP Mode, the user can keep real time.

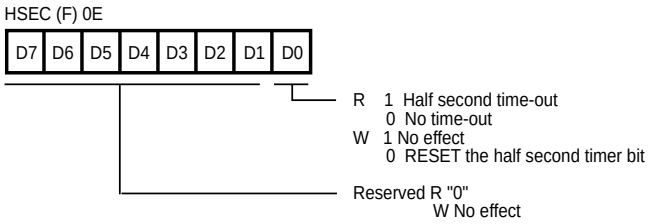


Figure 29. Half-Second Timer Status Register

WDT Time Select (D0, D1). These bits selects the WDT time period. The configuration is shown in Table 10.

Table 10. WDT Time Select

D1	D0‘	Time-out of Internal RC OSC	Time-out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle.
Tolerance = ±10%

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0 which selects the RC oscillator.

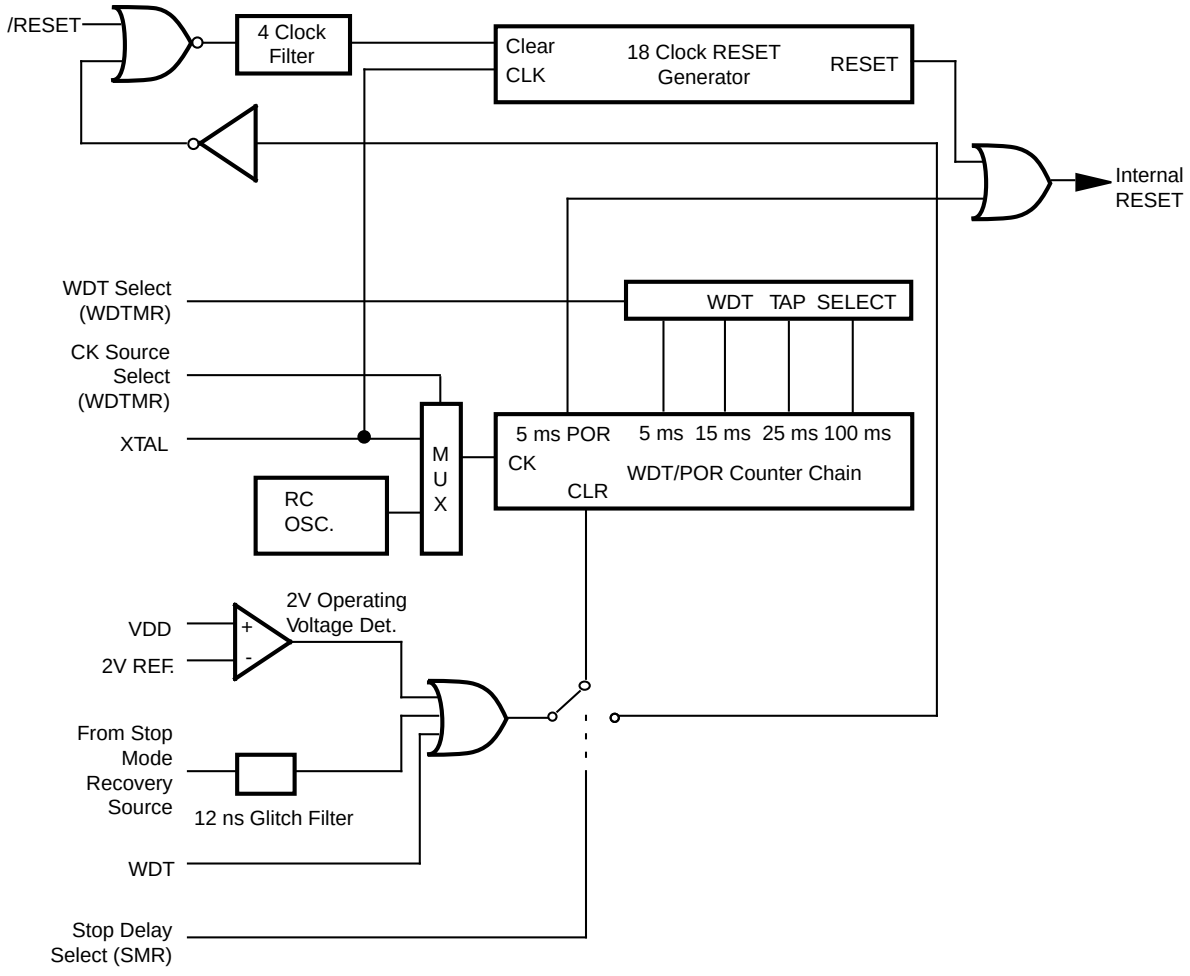


Figure 30. Resets and WDT

DSP REGISTERS DESCRIPTION

General. The DSP is a high-performance second generation CMOS Digital Signal Processor with a modified Harvard-type architecture with separate program and data ports. The design has been optimized for processing power and saving silicon space.

Registers. The DSP has eight internal registers and seven external registers. The external registers are for the A/D and D/A converters, and the mailbox and interrupt interfacing between DSP to the Z8. External registers are accessed in one machine cycle, the same as internal registers.

DSP Registers

There are 15 internal and extended 16-bit registers which are defined in Table 11.

Table 11. DSP Registers

Register	Attribute	Register Definition
BUS	Read	Data-Bus
X	Read/Write	X Multiplier Input, 16-Bit
Y	Read/Write	Y Multiplier Input, 16-Bit
A	Read/Write	Accumulator, 24-Bit
SR	Read/Write	Status Register
SP	Read/Write	Stack Pointer
PC	Read/Write	Program Counter
P	Read	Output of MAC, 24-Bit
EXT0	Read	Z8 ERF Bank B, Register 00-01 (from Z8)
	Write	Z8 ERF Bank B, Register 08-09 (to Z8)
EXT1	Read	Z8 ERF Bank B, Register 02-03 (from Z8)
	Write	Z8 ERF Bank B, Register 0A-0B (to Z8)
EXT2	Read	Z8 ERF Bank B, Register 04-05 (from Z8)
	Write	Z8 ERF Bank B, Register 0C-0D (to Z8)
EXT3	Read	Z8 ERF Bank B, Register 06-07 (from Z8)
	Write	Z8 ERF Bank B, Register 0E-0F (to Z8)
EXT4	Read/Write	DSP Interrupt Control Register
EXT5	Read	A/D Converter
	Write	D/A Converter
EXT6	Read/Write	Analog Control Register

EXT3-EXT0 (External Registers 3-0). These are the Mailbox Registers used by the DSP and Z8 to communicate. These four 16-bit registers correspond to the eight outgoing and eight incoming 8-bit registers in Bank B of the Z8's Expanded Register File.

EXT4 (DSP Interrupt Control Register (ICR)). This register controls the interrupts in the DSP as well as the interrupts in common between the DSP and the Z8. It is accessible by the DSP only, except for bit F and bit 9.

EXT5 (D/A and A/D Data Register). This register is used by both D/A and A/D converters. The D/A converter is loaded by writing to this register, while the A/D converter is addressed by reading from this register. The Register EXT5 is accessible only by the DSP.

EXT6 (Analog Control Register). This register controls the D/A and A/D converters. It is a read/write register accessible only by the DSP.

DSP Z8 Mail Box

To receive information from the DSP, the Z8 uses eight incoming registers which are mapped in the Z8 extended Register File (Bank B, 08 to 0F). The DSP treats these as four 16-bit registers that correspond to the eight incoming Z8 registers (Figure 31).

The Z8 can supply the DSP with data through eight outgoing registers mapped into both the Z8 Expanded Register File (Bank B, Registers 00 to 07) and the external register interface of the DSP. These registers are Read/Write and can be used as general-purpose registers of the Z8. The DSP can only read information from these registers. Since the DSP uses a 16-bit data format and the Z8 an 8-bit data format, eight outgoing registers of the Z8 correspond to four DSP registers. The DSP can only read information from the outgoing registers.

Both the outgoing registers and the incoming registers share the same DSP address (EXT3-EXT0).

Note: The Z8 can read and write to ERF Bank B R00-R07, Registers 08-0F are Read-Only from the Z8.

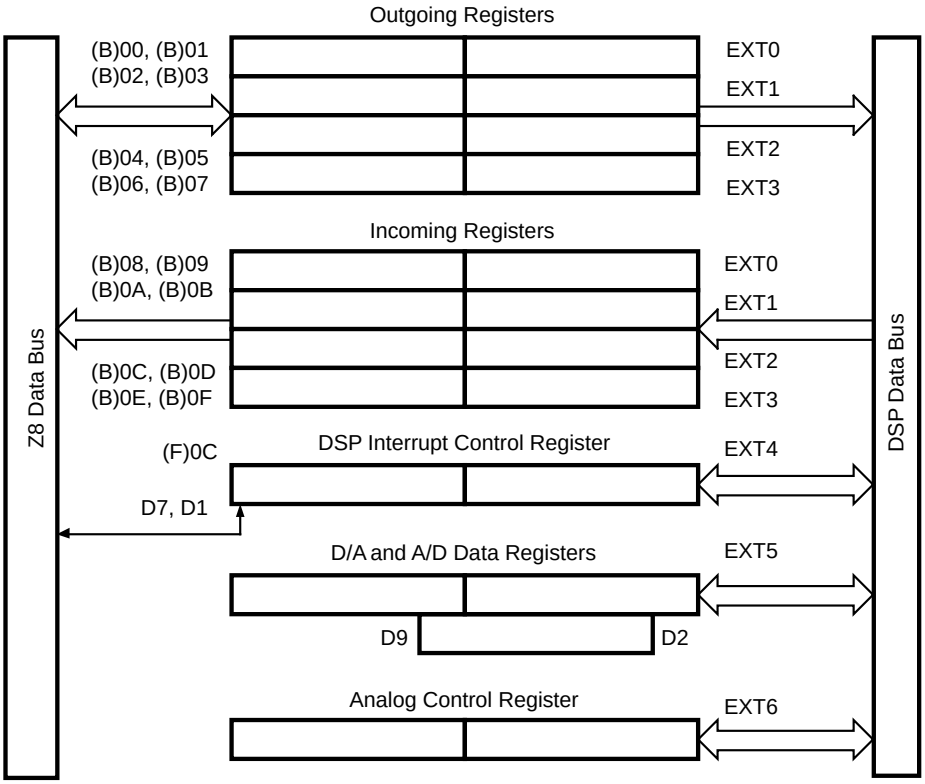


Figure 31. Z8-DSP Interface

Table 12. Z8 Outgoing Registers (Read-Only from DSP)

Field	Position	Attrib	Value	Label
Outgoing [0] (B)00	76543210	R/W	%NN	(B)00/DSP_ext0_hi
Outgoing [1] (B)01	76543210	R/W	%NN	(B)01/DSP_ext0_lo
Outgoing [2] (B)02	76543210	R/W	%NN	(B)02/DSP_ext1_hi
Outgoing [3] (B)03	76543210	R/W	%NN	(B)03/DSP_ext1_lo
Outgoing [4] (B)04	76543210	R/W	%NN	(B)04/DSP_ext2_hi
Outgoing [5] (B)05	76543210	R/W	%NN	(B)05/DSP_ext2_lo
Outgoing [6] (B)06	76543210	R/W	%NN	(B)06/DSP_ext3_hi
Outgoing [7] (B)07	76543210	R/W	%NN	(B)07/DSP_ext3_lo

DSP REGISTERS DESCRIPTION (Continued)

Table 13. Z8 Incoming Registers (Write-Only from DSP)

Field	Position	Attrib	Value	Label
Incoming [8] (B)08	76543210	R	%NN	DSP_ext0_hi
		W		No Effect
Incoming [9] (B)09	76543210	R	%NN	DSP_ext0_lo
		W		No Effect
Incoming [a] (B)0A	76543210	R	%NN	DSP_ext1_hi
		W		No Effect
Incoming [b] (B)0B	76543210	R	%NN	DSP_ext1_lo
		W		No Effect
Incoming [c] (B)0C	76543210	R	%NN	DSP_ext2_hi
		W		No Effect
Incoming [d] (B)0D	76543210	R	%NN	DSP_ext2_lo
		W		No Effect
Incoming [e] (B)0E	76543210	R	%NN	DSP_ext3_hi
		W		No Effect
Incoming [f] (B)0F	76543210	R	%NN	DSP_ext3_lo
		W		No Effect

Table 14. DSP Incoming Registers

Field	Position	Attrib	Value	Label
DSP_ext0	fedcba9876543210	R	%NNNN	(B)00, (B)01
Mail Box		W		(B)08, (B)09
DSP_ext1	fedcba9876543210	R	%NNNN	(B)02, (B)03
Mail Box		W		(B)0A, (B)0B
DSP_ext2	fedcba9876543210	R	%NNNN	(B)04, (B)05
Mail Box		W		(B)0C, (B)0D
DSP_ext3	fedcba9876543210	R	%NNNN	(B)06, (B)07
Mail Box		W		(B)0E, (B)0F

DSP Interrupts

The DSP processor has three interrupt sources (INT2, INT1, INT0) (Figure 32). These sources have different priority levels (Figure 33). The highest priority, the next lower and the lowest priority level are assigned to INT2, INT1 and INT0, respectively (Figure 34). The DSP does not allow interrupt nesting (interrupting service routines that are currently being executed). When two interrupt requests occur simultaneously the DSP starts servicing the interrupt with the highest priority level.

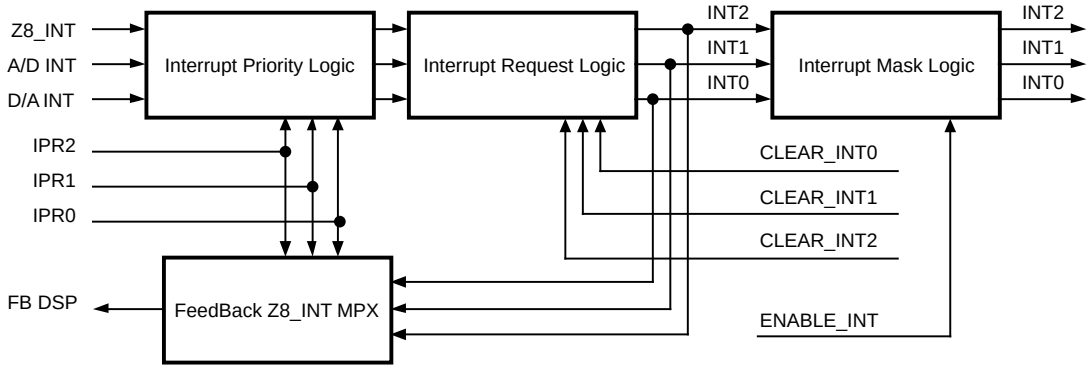


Figure 32. DSP Interrupts

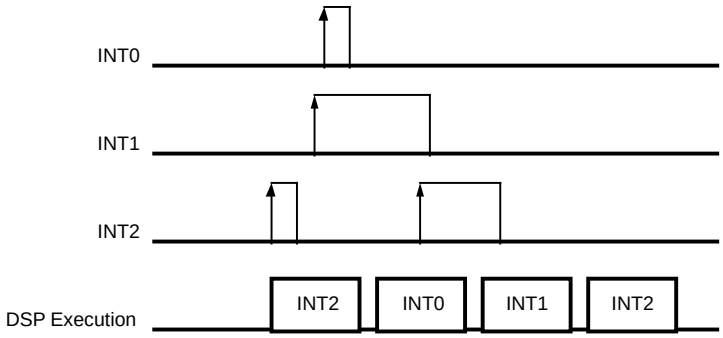


Figure 33. DSP Interrupt Priority Structure

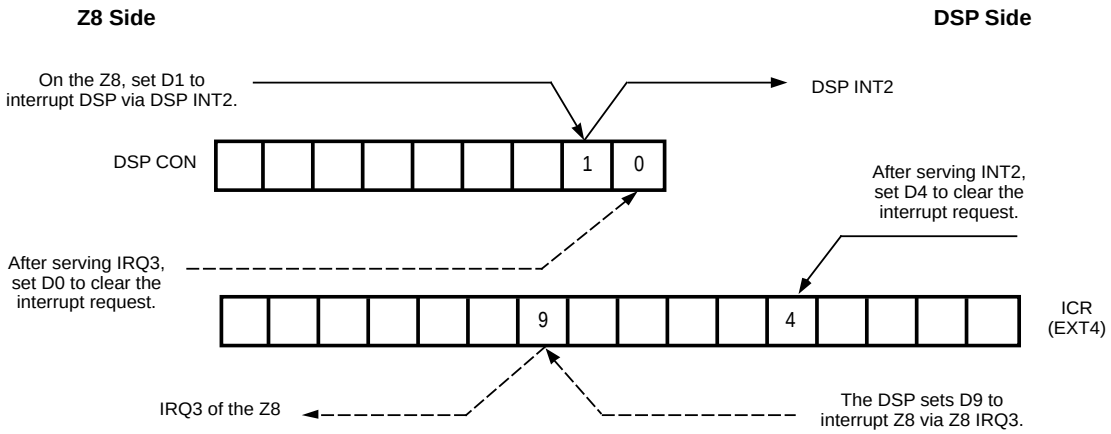


Figure 34. Interprocessor Interrupts Structure

DSP REGISTERS DESCRIPTION (Continued)

Table 15. EXT4 DSP Interrupt Control Register (ICR) Definition

Field	Position	Attrib	Value	Label
DSP_IRQ2	f---------------	R	1	Set_IRQ2
			0	Reset_IRQ2
	f---------------	W		No effect
DSP_IRQ1	-e--------------	R	1	Set_IRQ1
			0	Reset_IRQ1
	-e--------------	W		No effect
DSP_IRQ0	--d-------------	R	1	Set_IRQ0
			0	Reset_IRQ0
	--d-------------	W		No effect
DSP_MaskINT2	---c------------	R/W	1	Enable_INT2
			0	Disable_INT2
DSP_MaskINT1	----b-----------	R/W	1	Enable_INT1
			0	Disable_INT1
DSP_MaskINT0	-----a----------	R/W	1	Enable_INT0
			0	Disable_INT0
Z8_IRQ3	------9---------	R		Return "0"
	------9---------	W	1	Set_Z8_IRQ3
			0	Reset_Z8_IRQ3
DSPintEnable	-------8--------	R/W	1	Enable
			0	Disable
DSP_IPR2	--------7-------	R/W	Binary	IPR2
DSP_IPR1	---------6------	R/W	Binary	IPR1
DSP_IPR0	----------5-----	R/W	Binary	IPR0
Clear_IRQ2	-----------4----	R		Return "0"
	-----------4----	W	1	Clear_IRQ2
			0	Has_no_effect
Clear_IRQ1	------------3---	R		Return "0"
	------------3---	W	1	Clear_IRQ1
			0	No effect
Clear_IRQ0	-------------2--	R		Return "0"
	-------------2--	W	1	Clear_IRQ0
			0	No effect
Reserved	--------------10	W		No effect "0"
		R		

Interrupt Control Register (ICR). The ICR is mapped into EXT4 of the DSP (Table 15). The bits are defined as follows:

DSP_IRQ2 (Z8 Interrupt). This bit is read by both Z8 and DSP and is set only by writing to the Z8 expanded Register File (Bank F, ROC, bit 0). This bit asserts IRQ2 of the DSP and is cleared by writing to the Clear_IRQ2 bit.

DSP_IRQ1 (A/D Interrupt). This bit is read by the DSP only and is set when valid data is present at the A/D output register (conversion done). This bit asserts IRQ1 of the DSP and is cleared by writing to the Clear_IRQ1bit.

DSP_IRQ0 (D/A Interrupt). This bit is read by DSP only and is set by Timer3. This bit assists IRQ0 of the DSP and is cleared by writing to the Clear_IRQ0 bit.

DSP_MaskIntX. These bits are accessed by the DSP only. Writing a 1 to these locations allows the INT to be serviced, while writing a 0 masks off the corresponding INT.

Z8_IRQ3. This bit can be read by both the Z8 and the DSP but can only be set by the DSP. Addressing this location accesses bit D3 of the Z8 IRQ register, hence, this bit is not implemented in the ICR. During the interrupt service routine executed on the Z8 side, the User must reset the Z8_IRQ3 bit by writing a 1 to bit D0 of the DSPCON.

The hardware of the Z89138/139 automatically resets Z8_IRQ3 bit three instructions of the Z8 after 1 is written to its location in register bank 0F. This delay provides the timing synchronization between the Z8 and the DSP sides during interrupts. In summary, the interrupt service routine of the Z8 for IRQ3 should be finished by:

```
LD      ;       RP,#%0F
OR      ;       r12,#%01
POP     ;       RP
IRET    ;
```

DSP Enable_INT. Writing a 1 to this location enables global interrupts of the DSP while writing 0 disables them. A system Reset globally disables all interrupts.

DSP_IPRX. This three-bit group defines the Interrupt Selection logic as shown in Table 16.

Clear_IRQX. These bits are accessed by the DSP only. Writing a 1 to these locations resets the corresponding DSP_IRQX bits to 0. Clear_IRQX are virtual bits and are not implemented.

Table 16. DSP Interrupt Selection

DSP_IPR[2-0] 2 1 0	Z8_INT is switched to	A/D_INT is switched to	D/A_INT is switched to
0 0 0	INT2	INT1	INT0
0 0 1	INT1	INT2	INT0
0 1 0	INT2	INT0	INT1
0 1 1	INT1	INT0	INT2
1 0 0	INT0	INT2	INT1
1 0 1	INT0	INT1	INT2
1 1 0	Reserved	Reserved	Reserved
1 1 1	Reserved	Reserved	Reserved

DSP Analog Data Registers

The D/A conversion is DSP driven by sending 10-bit data to the EXT5 of the DSP. The six remaining bits of EXT5 are not used (Figure 35).

A/D supplies 8-bit data to the DSP through the register EXT5 of the DSP. From the 16 bits of EXT5, only bits 2 through 9 are used by the A/D (Figure 36). Bits 0 and 1 are padded with zeroes.

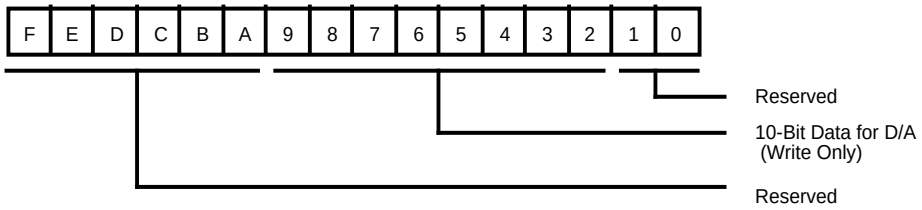


Figure 35. EXT5 Register D/A Mode Definition

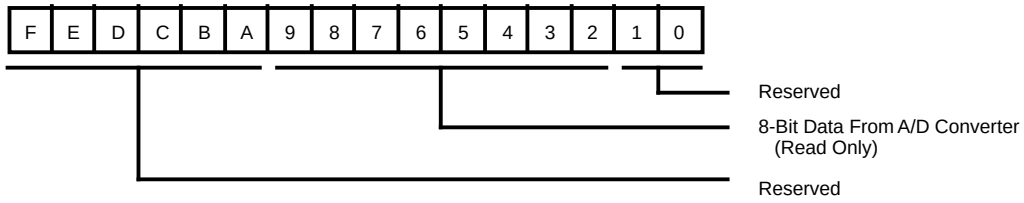


Figure 36. EXT5 Register A/D Mode Definition

ANALOG CONTROL REGISTER (ACR)

The Analog Control register is mapped to register EXT6 of the DSP (Table 17). This read/write register is accessible by the DSP only.

The 16-bit field of EXT6 defines modes of both the A/D and the D/A. The High Byte configures the D/A while the Low Byte controls the A/D mode.

Table 17. EXT6 Analog Control Register (ACR)

Field	Position	Attrib	Value	Label	20.48 MHz	29.49 MHz*
MPX_DSP_INT0	f---------------	R/W	1	P26		
			0	Timer3		
Reserved	-edcba----------	R		Return “0”		
		W		No effect		
Reserved	------9---------	R		Return “1”		
		W		No effect		
D/A_SamplingRate	-------8--------	R/W	0		16 kHz	8.04 kHz
			1		10 kHz	9.6 kHz
DSP_port (DSP1, DSP0)	--------76------	R/W		User-defined DSP outputs		
Enable A/D	----------5-----	R/W	1	A/D Enabled		
			0	A/D Disabled		
ConversionDone	----------4----	W		No effect		
		R	1	Done		
			0	Not Done		
StartConversion	------------3---	R/W	1	Start		
			0	Wait Timer		
Reserved	-------------2--	R		Return “0”		
		W		No effect		
20/29 MHz Select	--------------1-	R/W	1	29.49 MHz*		
			0	20.48 MHz†		
A/D_SamplingRate	---------------0	R/W	1		16 kHz	16 kHz
			0		8 kHz	9.6 kHz

Notes:
* Default value
† Optional feature

DSP IRQ0. This bit defines the source of the DSP IRQ0 interrupt.

D/A_Sampling Rate. This field defines the sampling rate of the D/A output. It changes the period to Timer3 interrupt and the maximum possible accuracy of the D/A Sampling Rate (Table 18).

Table 18. D/A Data Accuracy

D/A_Sampling Rate	Sampling Rate	
Bit 8	20.48 MHz	29.49 MHz
0	16 kHz	8.04 kHz
1	10 kHz	9.6 kHz

DSP0. DSP0 is a general-purpose output pin connected to Bit 6. This bit has no special significance and can be used to output data by writing to bit 6.

DSP1. DSP1 is a general-purpose output pin connected to Bit 7. This bit has no special significance and can be used to output data by writing to bit 7.

Enable A/D. Writing a 0 to this location disables the A/D converter, a 1 will enable it. A hardware reset forces this bit to 0.

Conversion Done. This Read-Only flag indicates that the A/D conversion is complete. Upon reading EXT5 (A/D data), the Conversion Done flag is cleared.

Start A/D Conversion. Writing a 1 to this location immediately starts one conversion cycle. If this bit is reset to 0 the input data is converted upon successive Timer2 time-outs. A hardware reset forces this bit to 1.

A/D_Sampling Rate. This field defines the sampling rate of the A/D. It changes the period of Timer2 interrupt (Table 19).

Table 19. A/D Sampling Rate

A/D_Sampling Rate	Sampling Rate	
Bit 0	20.48 MHz	29.49 MHz
1	16 kHz	16 kHz
0	8 kHz	9.6 kHz

DSP TIMERS

Timer2 is a free running counter that divides the XTAL frequency (20.48 MHz) to support different sampling rates for the A/D converter. The sampling rate is defined by the Analog Control Register. Upon reaching the end of a count, the timer generates an interrupt request to the DSP.

Analogous to Timer2, Timer3 generates the different sampling rates for the D/A converter. Timer3 also generates an interrupt request to the DSP upon reaching its final count value (Figure 37).

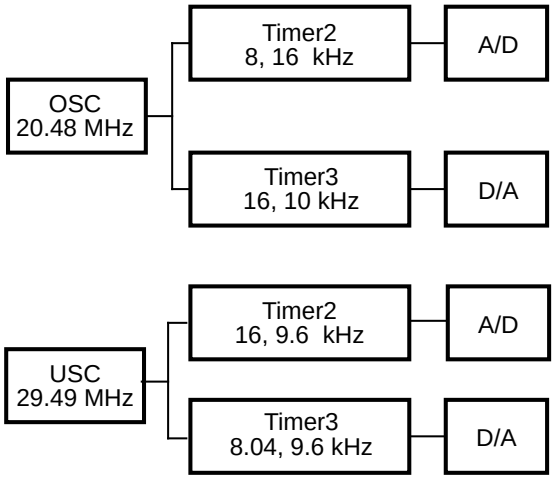


Figure 37. Timer2 and Timer3

Pulse Width Modulator (PWM)

The PWM supports two different sampling rates (10 and 16 kHz), according to the settings of bit 8 of the ACR. The output of the PWM can be assigned to logic 1 only during the active region (which is 4/5 of the output signal period). The output will be at logic 0 for the rest of the time. An exception occurs in 10 kHz PWM, where the active region covers the whole output signal period (Figure 39). The active region is divided into 1024 time slots. In each of these time slots, the output can be set to logic 1 or logic 0.

In order to increase the effective sampling rate, the PWM employs a special technique of distributing the “logic 1” period over the active region.

The 10-bit PWM data is divided into two parts: the upper five bits (High_Val) and the lower five bits (Low_Val). The 1024 time slots in the active region are divided into 32 equal groups, with 32 time slots in each group. The first slot of each of the 32 groups represents Low_Val, while High_Val is represented by the remaining 31 time slots in each group.

For example, a value of %13a is loaded into PWM data register EXT 5:

%13a = 01 0011 1010B = 314

High_Val = 01001B = 9

Low_Val = 11010B = 26

26 out of 32 groups will then have their first slots set to logic 1. The remaining one slot in each group has nine time slots set to logic 1.

For 10 kHz PWM, the effective output frequency is 10K x 32 = 320 kHz. Figure 40 illustrates the waveform by using a 6-bit PWM data (3-bit High_Val and 3-bit Low_Val).

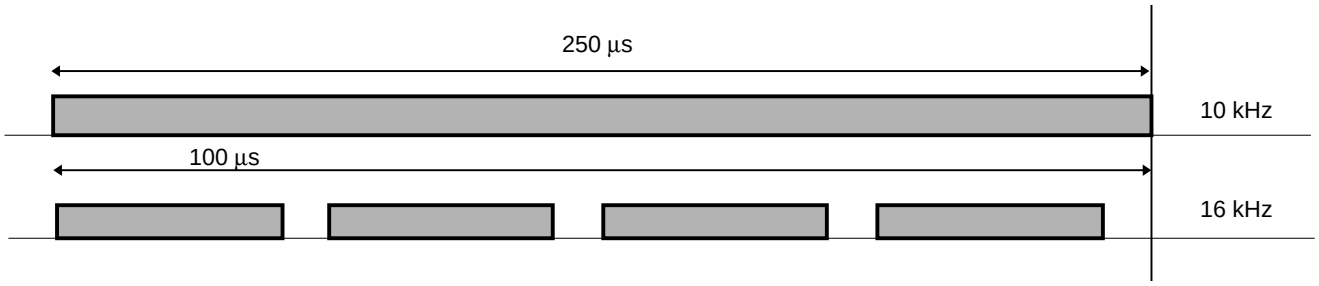


Figure 38. PWM Waveform (shaded area shows the active region)

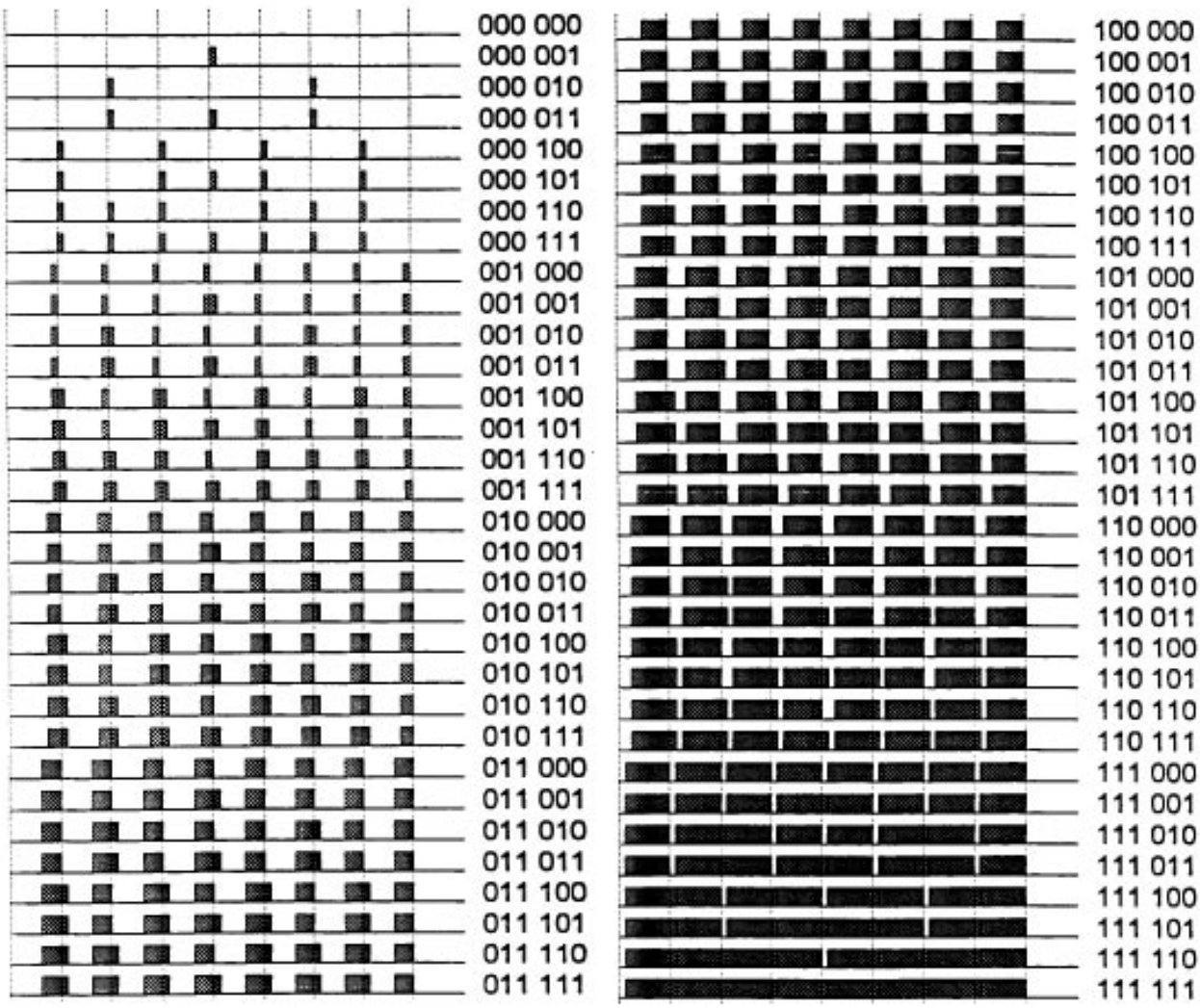


Figure 39. PWM Waveform of the Active Region (for a 6-bit PWM data)

A/D CONVERTER (ADC)

Analog to Digital Converter

The A/D converter is an 8-bit half flash converter which uses two reference resistor ladders for its upper four bits (MSBs) and lower four bits (LSBs) conversion (Figure 40). Two reference voltage pins, VREF+ (High) and VREF- (Low), are provided for external reference voltage supplies. During the sampling period, the converter is auto-zeroed before starting the conversion time depending on the external clock frequency and the selection of the A/D sampling rate (Figure 40). The sampling rates are 10 or 16 kHz (XTAL = 20.48 MHz) in order to provide oversampling. The rates are software controlled by the ACR (DSP External Register 6). Timer2 supports the ADC. The maximum conversion time is 2 µs.

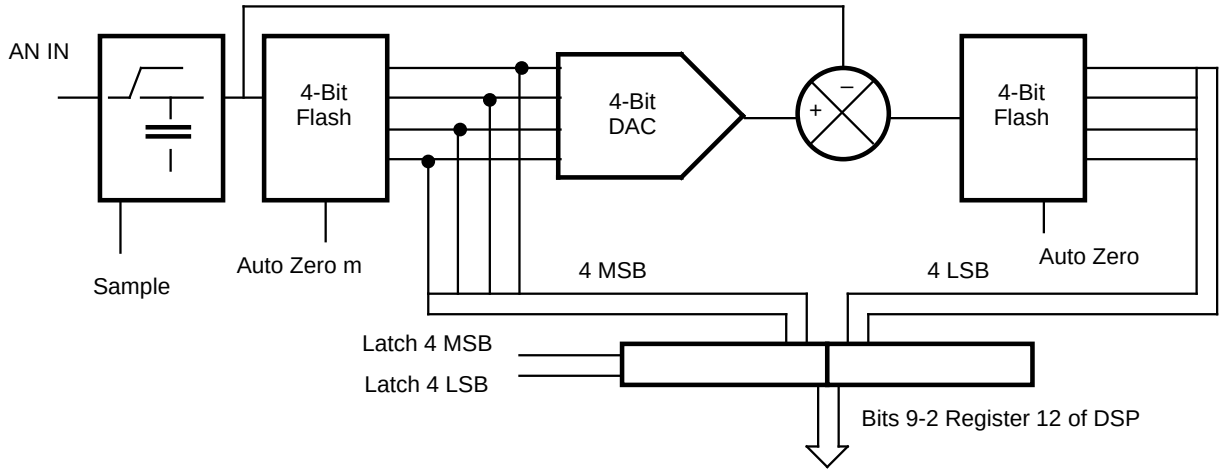
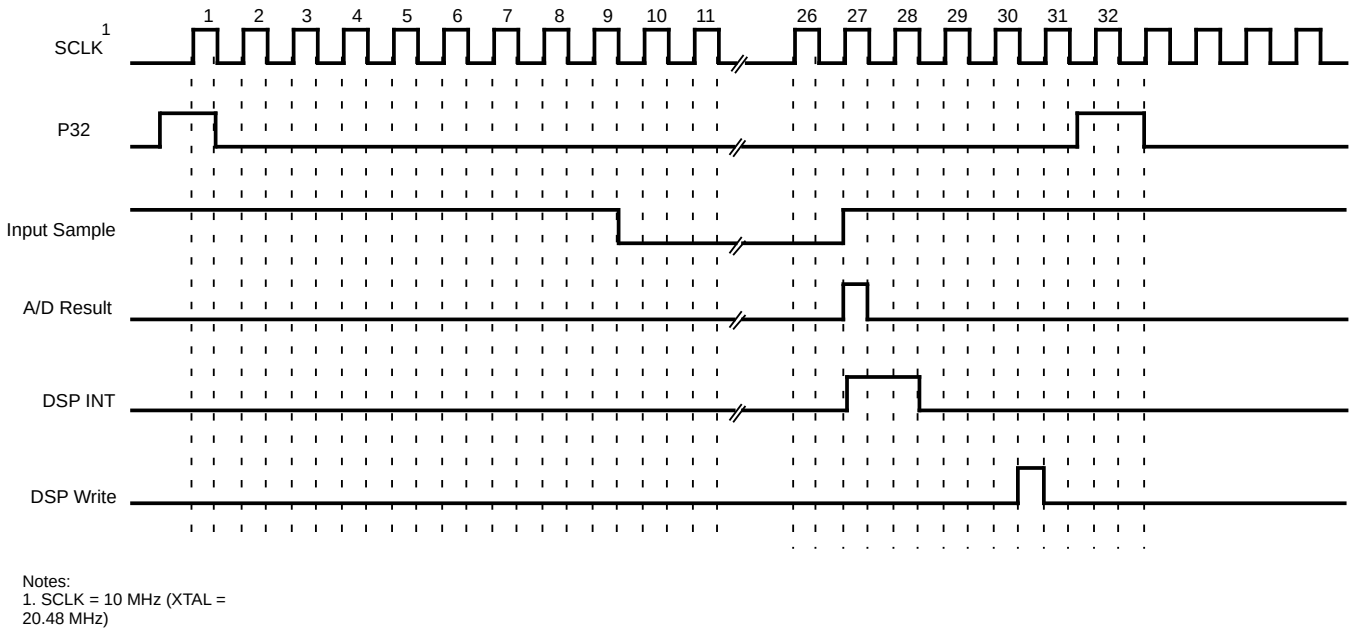


Figure 40. A/D Converter

Conversion begins by writing to the appropriate bit in the Analog Control Register (ACR). The start commands are implemented in such a way as to begin a conversion at any time. If a conversion is in progress and a new start command is received, then the conversion in progress is aborted and a new conversion initiated. This allows the programmed values to be changed without affecting a conversion in progress. The new values take effect only after a new start command is received.

The ADC can be disabled (for low power) or enabled by an analog Control Register bit.

Though the ADC functions for a smaller input voltage and voltage reference, the noise and offsets remain constant over the specified electrical range. The errors of the converter will increase and the conversion time can also take slightly longer due to smaller input signals.



Notes:
1. SCLK = 10 MHz (XTAL = 20.48 MHz)

Figure 41. ADC Timing Diagram

Figure 42 shows the input circuit of the ADC. When conversion starts, the analog input voltage from the input is connected to the MSB and LSB flash converter inputs as shown in the Input Impedance CKT diagram. Shunting 31 parallel internal resistances of the analog switches and simultaneously charging 31 parallel 1 pF capacitors is equivalent to a 400 Ohms input impedance in parallel with a 31 pF capacitor. Other input stray capacitance adds about 10 pF to the input load. Input source resistances up to 2 kOhms can be used under normal operating conditions without any degradation of the input settling time. For larger input source resistance, longer conversion cycle times can be required to compensate the input settling time problem. V_{REF} is set using the V_{REF} + pin.

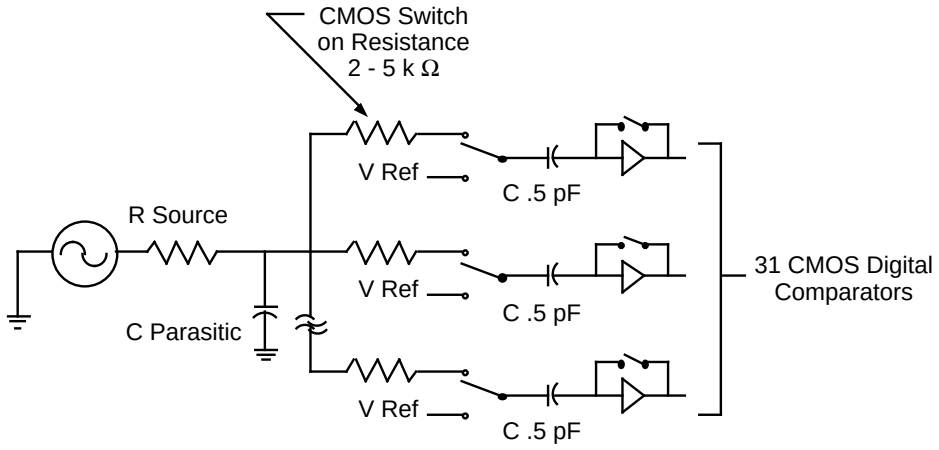


Figure 42. Input Impedance of ADC

Z8 EXPANDED REGISTER FILE REGISTERS

Expanded Register Bank B

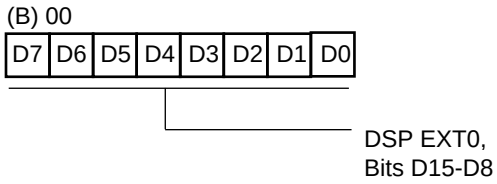


Figure 43. Outgoing Register to DSP EXT0 (High Byte) (B) 00H [Read/Write]

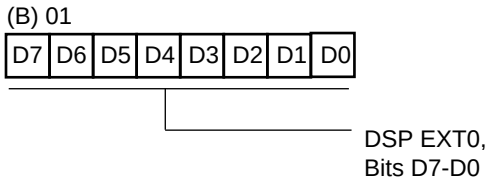


Figure 44. Outgoing Register to DSP EXT0 (Low Byte) (B) 01H [Read/Write]

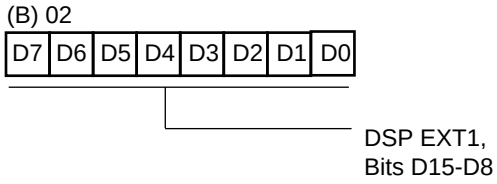


Figure 45. Outgoing Register to DSP EXT1 (High Byte) (B) 02H [Read/Write]

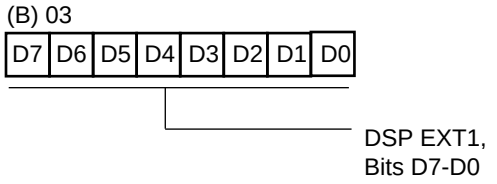


Figure 46. Outgoing Register to DSP EXT1 (Low Byte) (B) 03H [Read/Write]

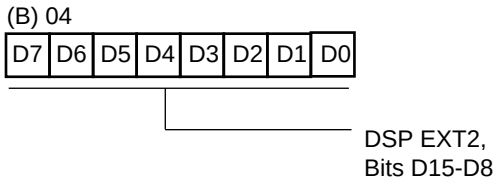


Figure 47. Outgoing Register to DSP EXT2 (High Byte) (B) 04H [Read/Write]

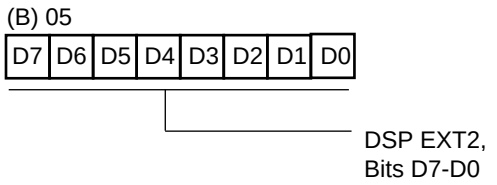


Figure 48. Outgoing Register to DSP EXT2 (Low Byte) (B) 05H [Read/Write]

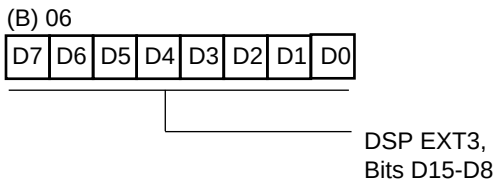


Figure 49. Outgoing Register to DSP EXT3 (High Byte) (B) 06H [Read/Write]

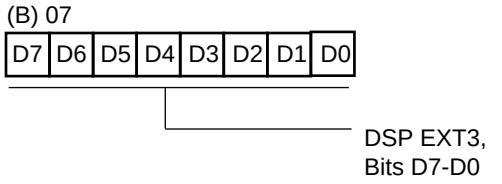


Figure 50. Outgoing Register to DSP EXT3 (Low Byte) (B) 07H [Read/Write]

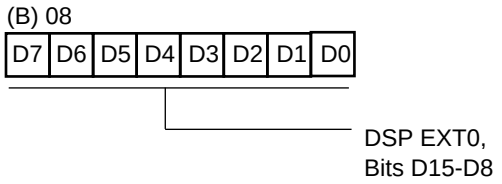


Figure 51. Incoming Register from DSP EXT0 (High Byte) (B) 08H [Read-Only]

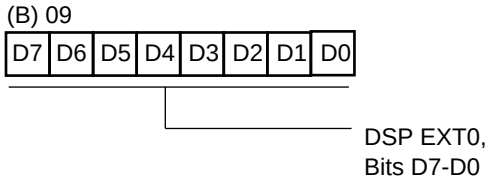


Figure 52. Incoming Register from DSP EXT0 (Low Byte) (B) 09H [Read-Only]

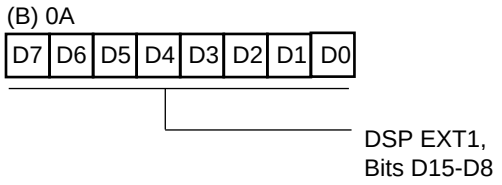


Figure 53. Incoming Register from DSP EXT1 (High Byte) (B) 0AH [Read-Only]

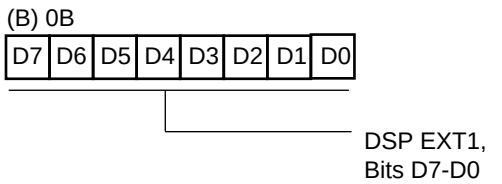


Figure 54. Incoming Register from DSP EXT1 (Low Byte) (B) 0BH [Read-Only]

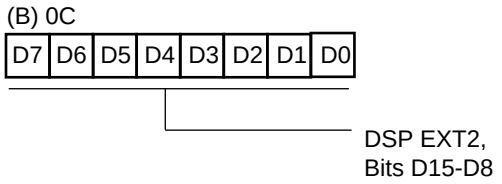


Figure 55. Incoming Register from DSP EXT2 (High Byte) (B) 0CH [Read-Only]

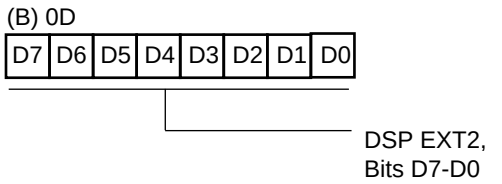


Figure 56. Incoming Register from DSP EXT2 (Low Byte) (B) 0DH [Read-Only]

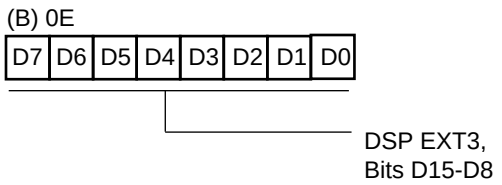


Figure 57. Incoming Register from DSP EXT3 (High Byte) (B) 0EH [Read-Only]

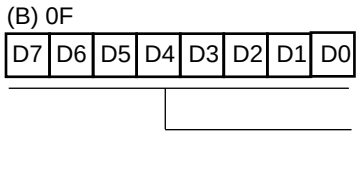
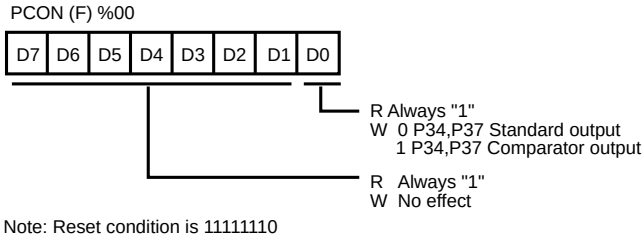


Figure 58. Incoming Register from DSP EXT3 (Low Byte) (B) 0FH [Read-Only]

Expanded Register Bank F



Note: Reset condition is 11111110

Figure 59. Port Configuration Register (PCON) (F) 00H [Write-Only]

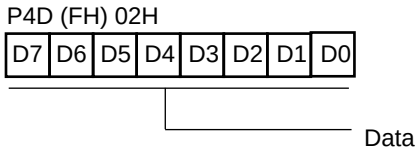


Figure 60. Port 4 Data Register (F) 02H [Read/Write]

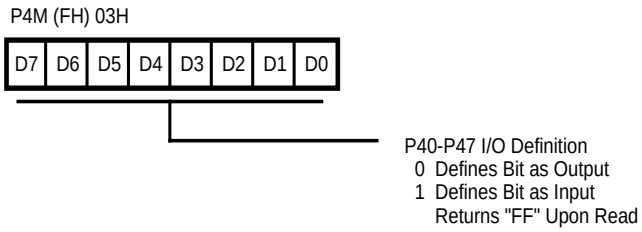


Figure 61. Port 4 Mode Register (F) 03H [Write-Only]

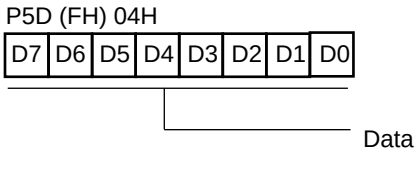


Figure 62. Port 5 Data Register (F) 04H [Read/Write]

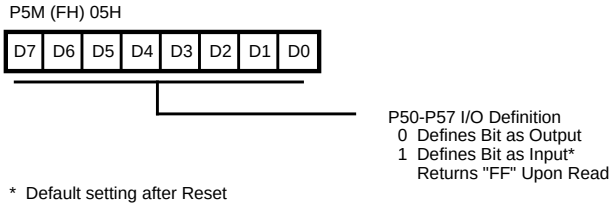


Figure 63. Port 5 Mode Register (F) 05H [Write-Only]

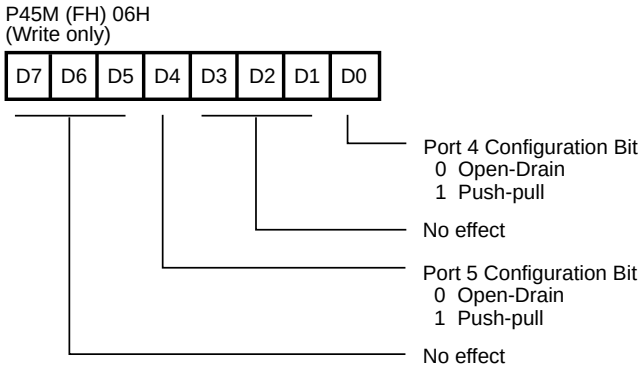


Figure 64. Port 4 and 5 Configuration Register (F) 06H [Write-Only]

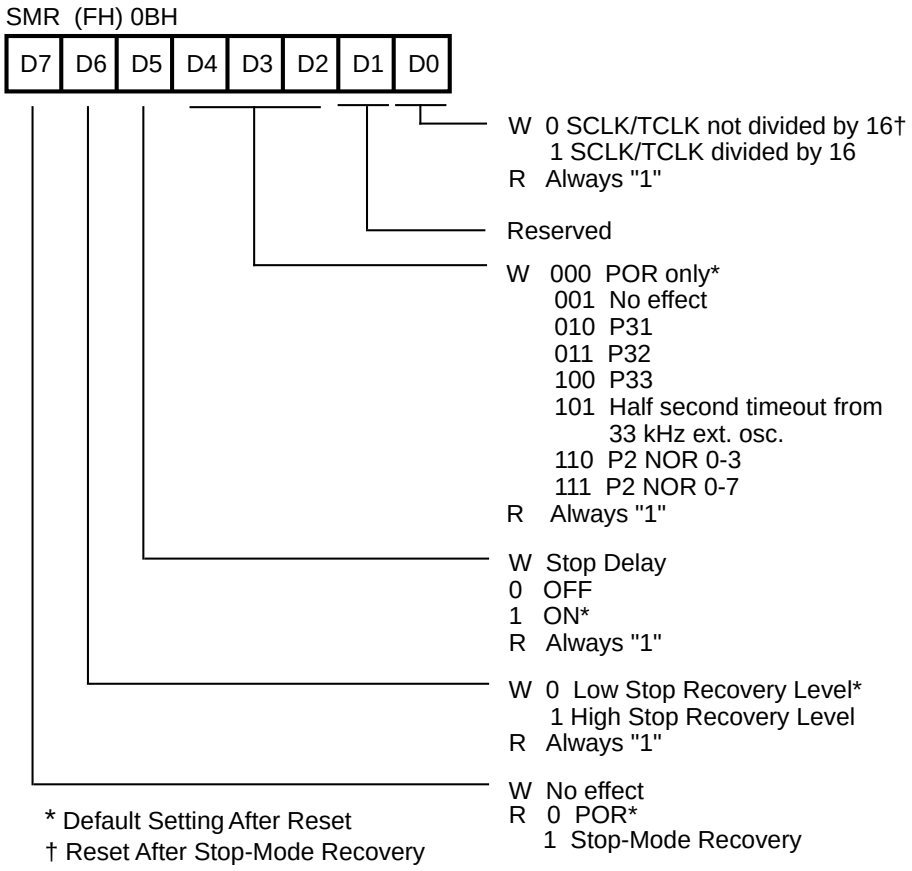


Figure 65. Stop-Mode Recovery Register (SMR)
(F) 0BH [Read/Write]

Table 20. DSP Control Register (F) 0CH [Read/Write]

Field DSPCON (F) 0CH	Position	Attributes	Value	Label
Z8_SCLK	76------	R/W	00	OSC/8
			01	OSC/4
			1x	OSC/2
DSP_Reset	--5-----	R		Return “0”
		W	0	No effect
			1	Reset DSP
DSP_Run	---4----	R/W	0	Halt_DSP
			1	Run_DSP
Reserved	----32--		xx	
				Return “0”
				No effect
IntFeedback	------1-	R		FB_DSP_INT2
		W	1	Set DSP_INT2
			0	No effect
	-------0	R		FB_Z8_IRQ3
		W	1	Clear IRQ3
			0	No effect

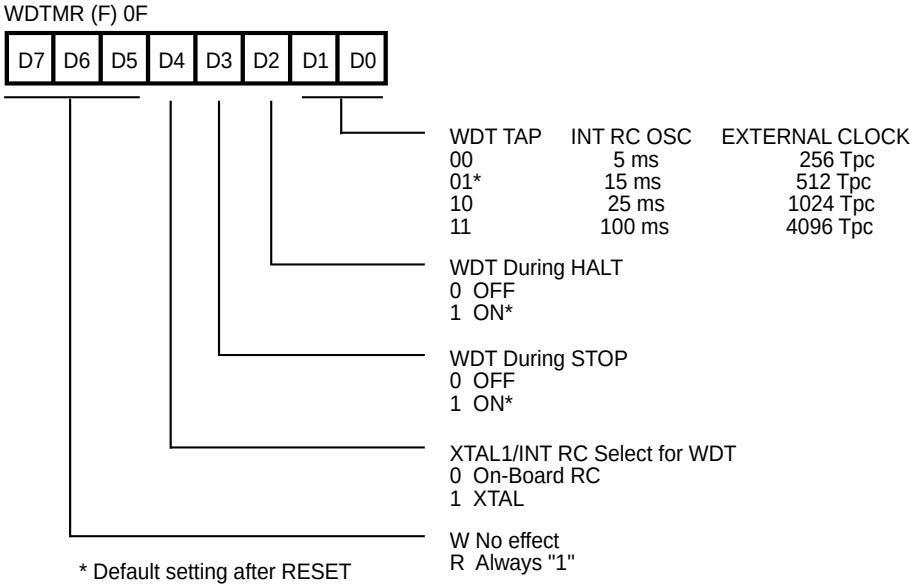


Figure 66. Watch-Dog Timer Mode Register (F) 0FH [Read/Write]

Z8 CONTROL REGISTERS

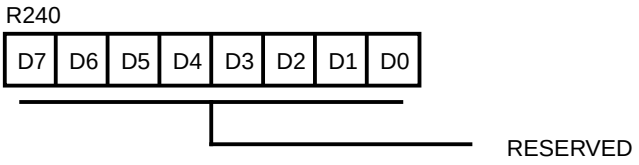


Figure 67. Reserved (F0H)

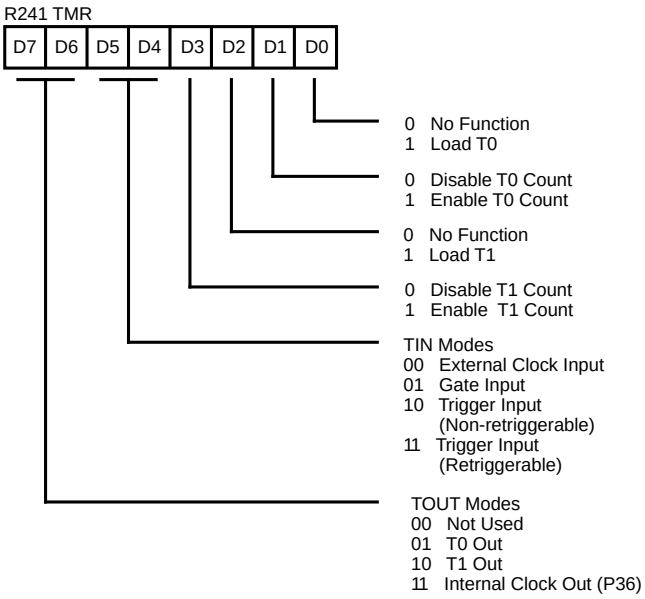


Figure 68. Timer Mode Register (F1H: Read/Write)

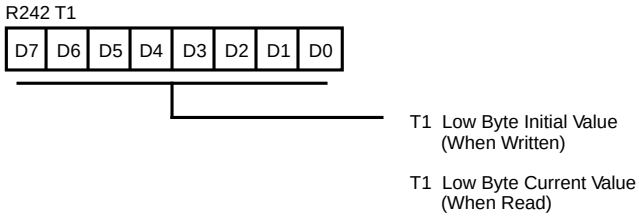


Figure 69. Counter/Timer 1 Register (F2H: Read/Write)

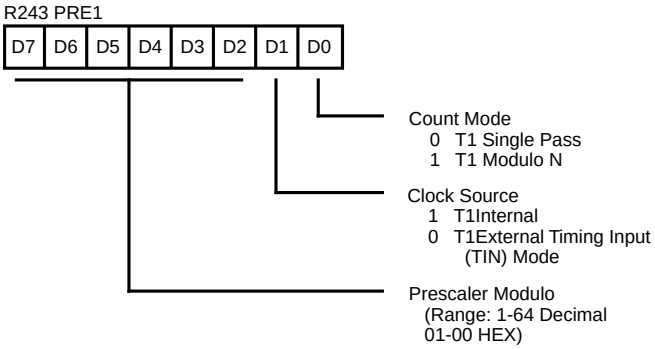


Figure 70. Prescaler 1 Register (F3H: Write-Only)

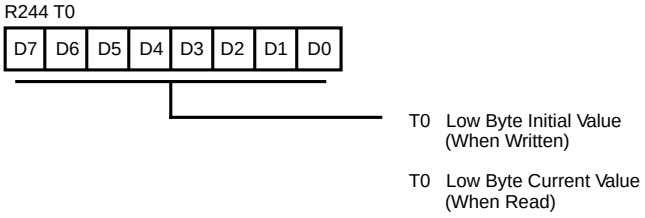


Figure 71. Counter/Timer 0 Register (F4H: Read/Write)

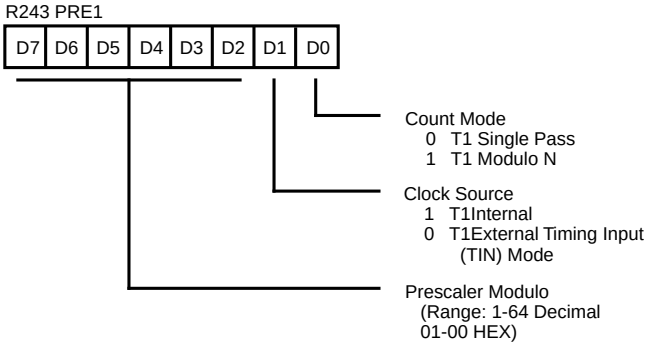


Figure 72. Prescaler 0 Register (F5H: Write-Only)

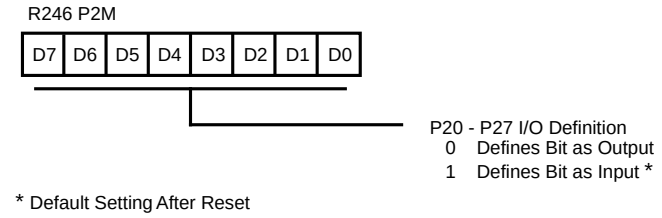


Figure 73. Port 2 Mode Register (F6H: Write-Only)

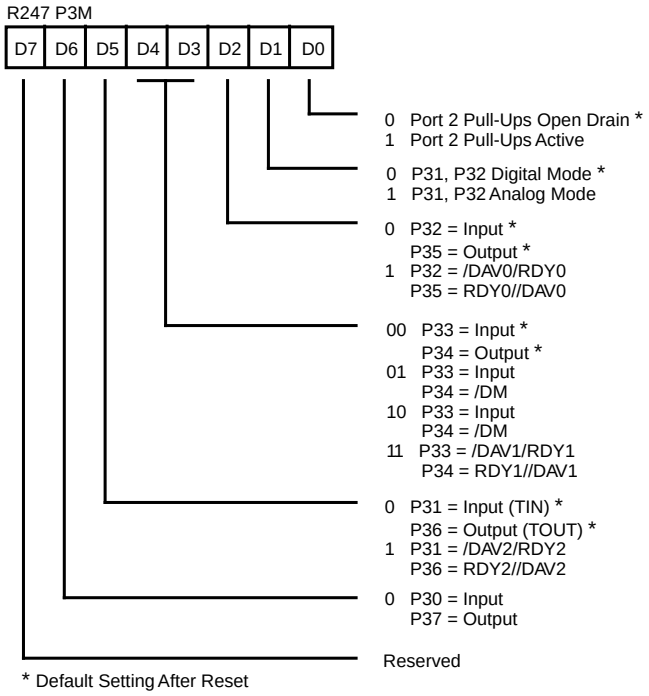


Figure 74. Port 3 Mode Register (F7H: Write-Only)

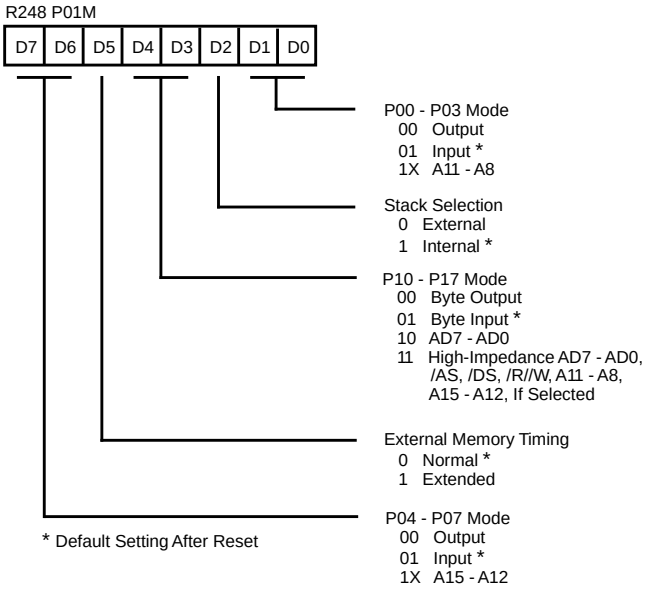


Figure 75. Port 0 Mode Register (F8H: Write-Only)

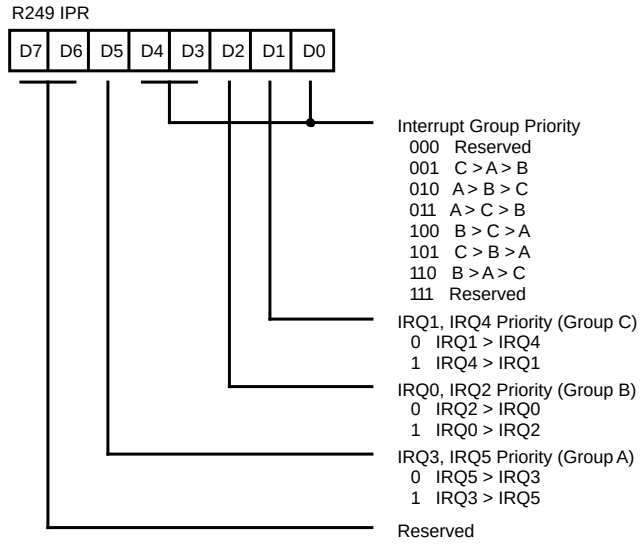


Figure 76. Interrupt Priority Register (F9H: Write-Only)

Z8 CONTROL REGISTERS (Continued)

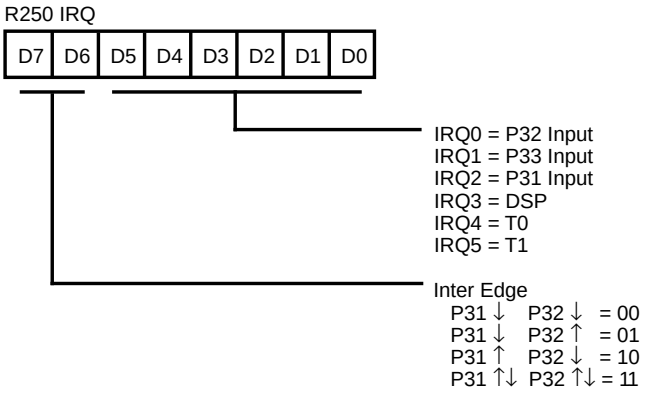


Figure 77. Interrupt Request Register (FAH: Read/Write)

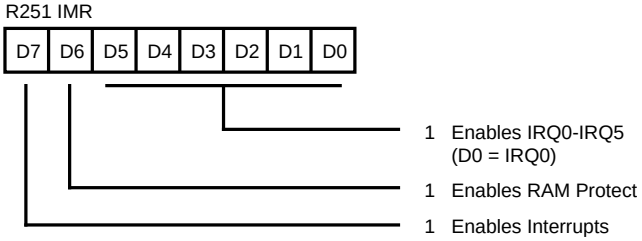


Figure 78. Interrupt Mask Register (FBH: Read/Write)

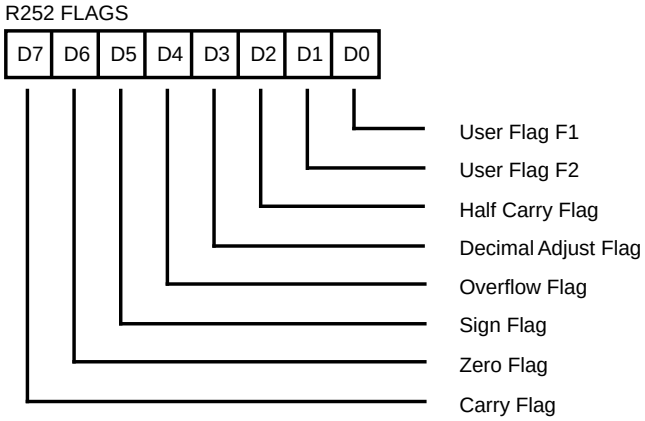


Figure 79. Flag Register (FCH: Read/Write)

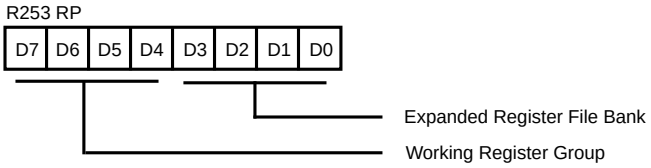


Figure 80. Register Pointer (FDH: Read/Write)

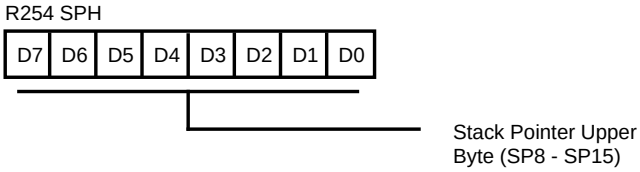


Figure 81. Stack Pointer High (FEH: Read/Write)

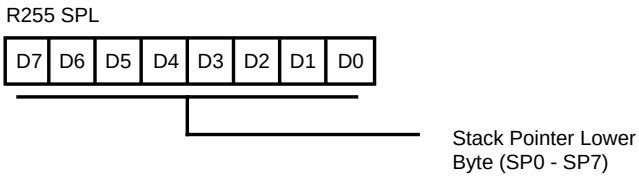
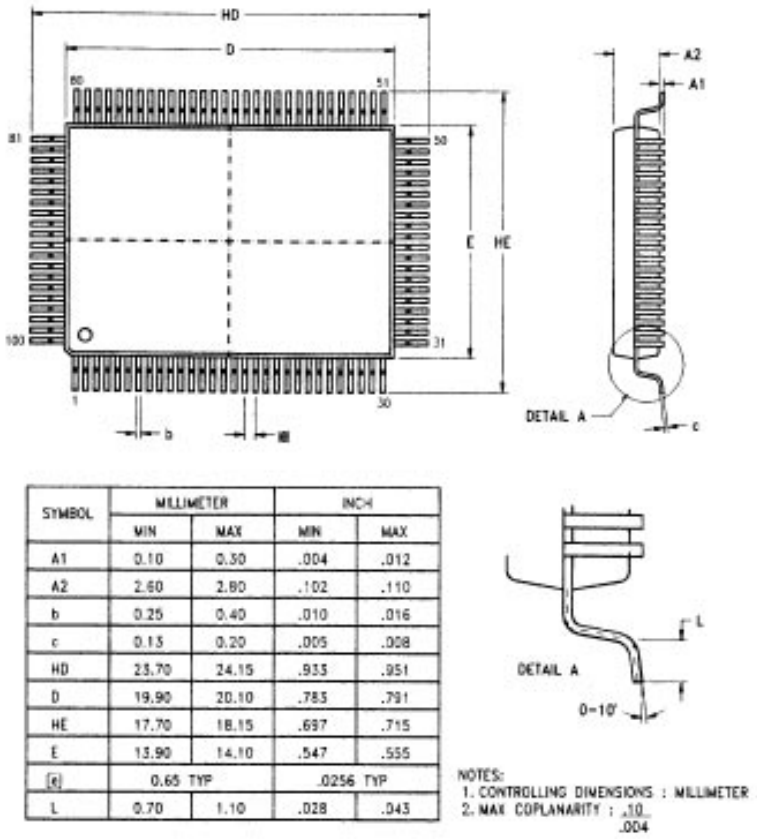


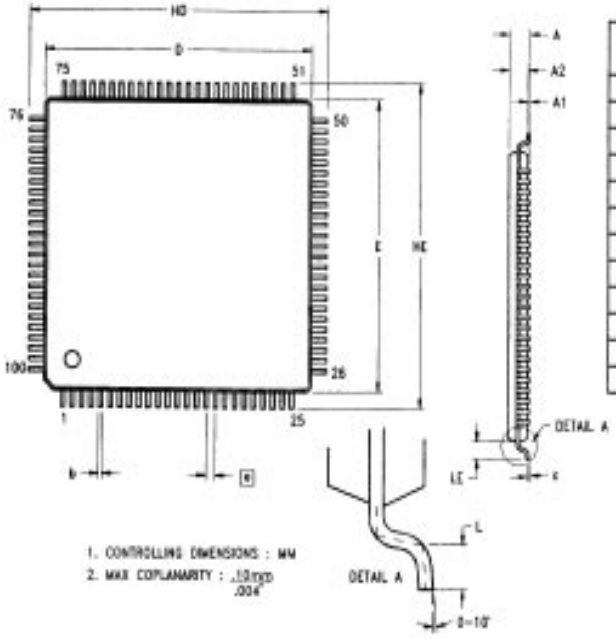
Figure 82. Stack Pointer Low (FFH: Read/Write)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.50	.004	.012
A2	2.60	2.80	.102	.110
b	0.25	0.40	.010	.016
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.65 TYP		.0256 TYP	
L	0.70	1.10	.028	.043

Figure 83. 100-Pin QFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.006	.010
c	0.10	0.20	.004	.008
HD	15.85	16.15	.624	.636
D	13.90	14.10	.547	.555
HE	15.85	16.15	.624	.636
E	13.90	14.10	.547	.555
e	0.50 TYP		.0197 TYP	
L	0.35	0.65	.014	.026
LE	0.90	1.10	.035	.043

Figure 84. 100-Pin VQFP Package Diagram

ORDERING INFORMATION

Z89138 (20 MHz)		Z89138 (29 MHz)	
100-Pin QFP	**100-Pin VQFP**	**100-Pin QFP**	**100-Pin VQFP**
Z8913820FSC	Z8913820ASC	Z8913829FSC	Z8913829ASC

Z89139 (20 MHz)		Z89139 (29 MHz)	
100-Pin QFP	**100-Pin VQFP**	**100-Pin QFP**	**100-Pin VQFP**
Z8913920FSC	Z8913920ASC	Z8913929FSC	Z8913929ASC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

CODES

Packages
F = Quad Flatpack (QFP)
A = Very Small Quad Flatpack (VQFP)

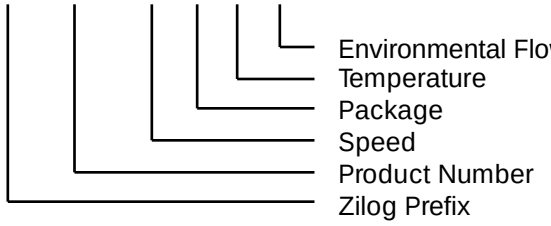
Speeds
20 = 20.48 MHz
29 = 29.49 MHz

Temperature
S = 0°C to + 55°C

Environmental
C = Plastic Standard

Example:

Z 89138 20 F S C is a Z89138, 20.48 MHz, QFP, 0°C to +55°C, Plastic Standard Flow



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