300-MHz, 2.5-Ω, Dual SPDT Analog Switches

DESCRIPTION

The DG787 are dual SPDT analog switches which operate from 1.8 V to 5.5 V single rail power supply. They are design for audio, video, and USB switching applications.

The devices have 2.5 Ω on-resistance and 300 MHz 3 dB bandwidth. 0.2 Ω on-resistance matching and 1 Ω flatness make the device high linearity. The devices are 1.6 V logic compatible within the full operation voltage range.

These switches are built on a sub-micron high density process that brings low power consumption and low voltage performance.

The switch is package in MSOP 10 package.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. DG787 is offered in a MSOP package. The MSOP package uses 100 % matte tin device termination and is represented by the lead (Pb)-free "-E3" suffix. Both the matte tin device terminations meet all JEDEC standards for reflow and MSL ratings.

FEATURES

- 1.8 V to 5.5 V operation
- 2.5 Ω at 2.7 V R_{ON}
- 300 MHz - 3 dB bandwidth
- ESD per MIL-STD-883 method 3015.7 > 2 kV
- Latch-up current 200 mA (JESD 78)
- 1.6 V logic compatible
- Compliant to RoHS directive 2002/95/EC
- Halogen-free according to IEC 61249-2-21 definition

Pb-free
RoHS COMPLIANT
HALOGEN FREE

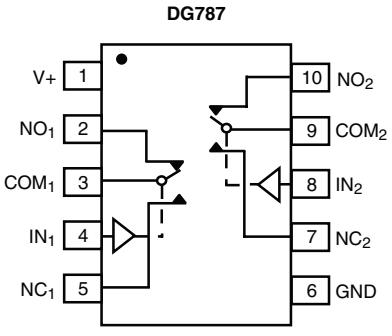
BENEFITS

- Space saving MSOP-10 package
- High linearity
- Low power consumption
- High bandwidth
- Full rail signal swing range

APPLICATIONS

- Cellular phones
- MP3
- Media players
- Modems
- Hard drives
- PCMCIA

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View

TRUTH TABLE		
Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	MSOP-10	DG787DQ-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (NO, NC, COM)		± 100	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature	(D Suffix)	- 65 to 150	°C
ESD per MIL-STD-883 Method 3015.7		> 2	kV
Power Dissipation (Packages)[c]	MSOP-10[d]	320	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. Refer to IPC/JEDEC (J-STD-020).
c. All leads welded or soldered to PC board.
d. Derate 4.0 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS V+ = 3 V

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.7 V to 3.6 V, V_{IN} = 0.5 V or 1.4 V[e]		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Analog Switch								
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}			Full	0		V+	V
On-Resistance[d]	R_{ON}	V+ = 2.7 V, I_{NO}, I_{NC} = 10 mA	V_{COM} = 1.5 V	Room Full		2.5	3.5 3.8	Ω
R_{ON} Flatness[d]	R_{ON} Flatness		V_{COM} = 1, 1.5, 2 V	Room		0.52	1.0	
On-Resistance Match Between Channels[d]	$\Delta R_{DS(on)}$		V_{COM} = 1.5 V	Room			0.25	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 3 V/0.3 V		Room Full	- 1 - 20		1 20	nA
	$I_{COM(off)}$			Room Full	- 1 - 20		1 20	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V		Room Full	- 1 - 20		1 20	
Digital Control								
Input High Voltage[d]	V_{INH}			Full	1.4			V
Input Low Voltage	V_{INL}			Full			0.5	
Input Capacitance	C_{in}			Full		5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+		Full	1		1	µA

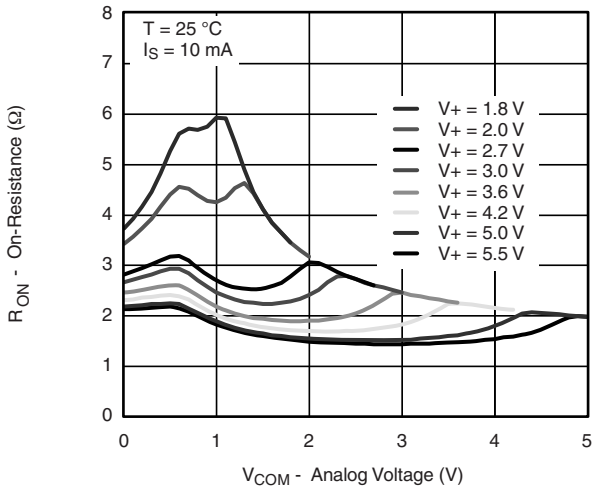
SPECIFICATIONS V+ = 3 V								
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 2.7 V to 3.6 V, V_{IN} = 0.5 V or 1.4 V[e]		**Temp.[a]**	**Limits - 40 °C to 85 °C Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Dynamic Characteristics								
Turn-On Time	t_{ON}	V+ = 2.7 V, V_{NO} or V_{NC} = 1.5 V R_L = 300 Ω, C_L = 35 pF		Room Full		21	51 52	ns
Turn-Off Time	t_{OFF}			Room Full		15	45 46	
Break-Before-Make Time	t_d			Full	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 2.0 V, R_{GEN} = 0 Ω		Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 74		dB
			f = 10 MHz	Room		- 54		
Crosstalk[d]	X_{TALK}		f = 1 MHz	Room		- 76		
			f = 10 MHz	Room		- 56		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz		Room		12		pF
	$C_{NC(off)}$			Room		12		
Channel-On Capacitance[d]	$C_{NO(on)}$			Room		40		
	$C_{NC(on)}$			Room		40		
Power Supply								
Power Supply Current	I+	V_{IN} = 0 or V+		Room Full			1.0 1.0	µA

SPECIFICATIONS V+ = 5 V

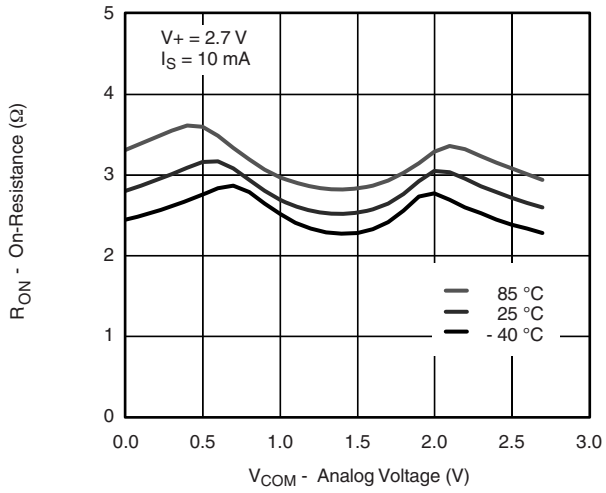
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 4.2 V to 5.5 V, V_{IN} = 0.8 V or 2.0 V[e]		Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Analog Switch								
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}			Full	0		V+	V
On-Resistance[d]	R_{ON}	V+ = 4.2 V, I_{NO}, I_{NC} = 10 mA	V_{COM} = 3.5 V	Room Full		2.2	2.9 3.1	Ω
R_{ON} Flatness[d]	R_{ON} Flatness		V_{COM} = 1, 2, 3.5 V	Room		0.53	1.0	
On-Resistance Match Between Channels[d]	$\Delta R_{DS(on)}$		V_{COM} = 3.5 V	Room			0.25	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5.5 V, V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V		Room Full	- 1 - 20		1 20	nA
	$I_{COM(off)}$			Room Full	- 1 - 20		1 20	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V		Room Full	- 1 - 20		1 20	
Digital Control								
Input High Voltage[d]	V_{INH}			Full	2.0			V
Input Low Voltage	V_{INL}			Full			0.8	
Input Capacitance	C_{in}			Full		5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+		Full	1		1	µA
Dynamic Characteristics								
Turn-On Time	t_{ON}	V+ = 4.2 V, V_{NO} or V_{NC} = 3.0 V, R_L = 300 Ω, C_L = 35 pF		Room Full		15	45 46	ns
Turn-Off Time	t_{OFF}			Room Full		12	42 43	
Break-Before-Make Time	t_d			Full	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 2.0 V, R_{GEN} = 0 Ω		Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF	f = 1 MHz	Room		- 74		dB
			f = 10 MHz	Room		- 54		
Crosstalk[d]	X_{TALK}		f = 1 MHz	Room		- 78		
			f = 10 MHz	Room		- 56		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz		Room		12		pF
	$C_{NC(off)}$			Room		12		
Channel-On Capacitance[d]	$C_{NO(on)}$			Room		40		
	$C_{NC(on)}$			Room		40		
Power Supply								
Power Supply Current	I+	V_{IN} = 0 or V+		Room Full			1.0 1.0	µA

Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V testing, not production tested.

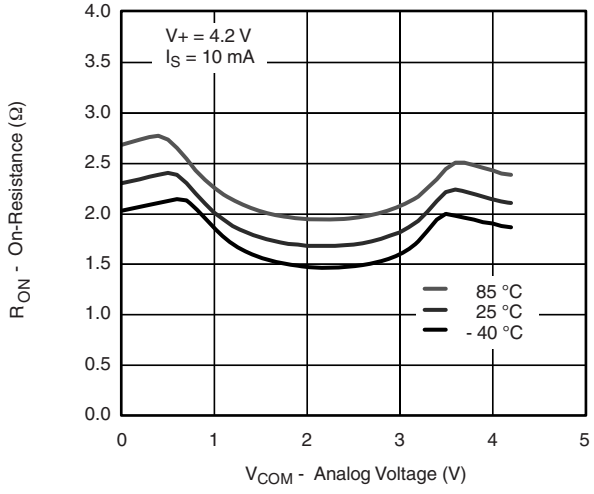
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



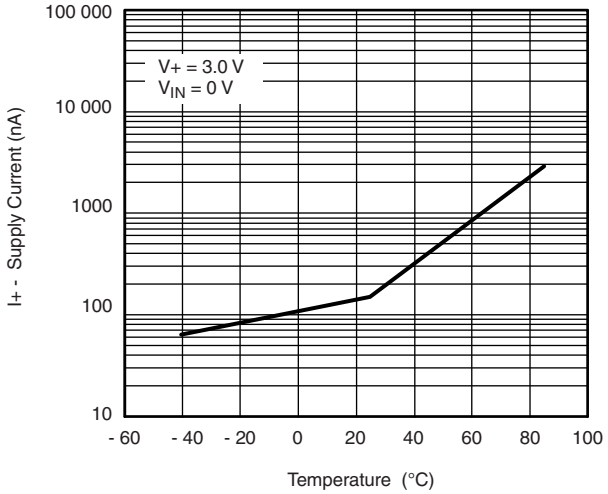
R_{ON} vs. V_{COM} and Single Supply Voltage



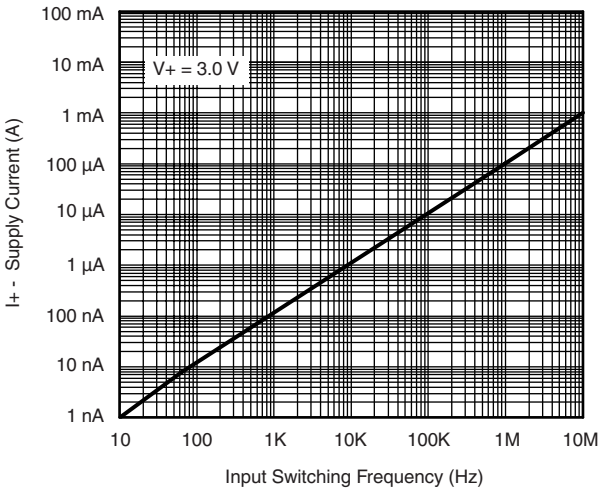
R_{ON} vs. Analog Voltage and Temperature



R_{ON} vs. Analog Voltage and Temperature

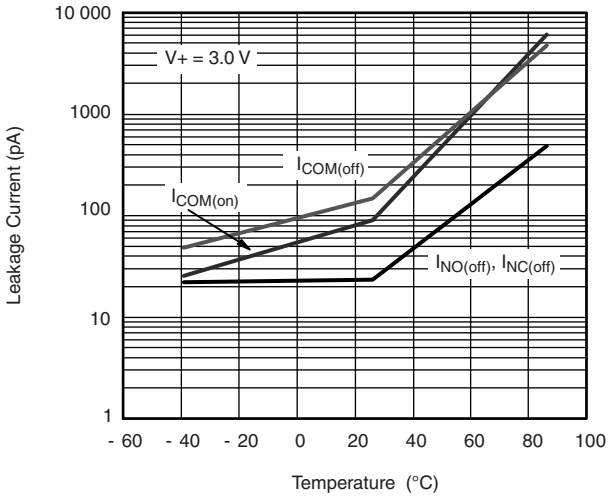


Supply Current vs. Temperature

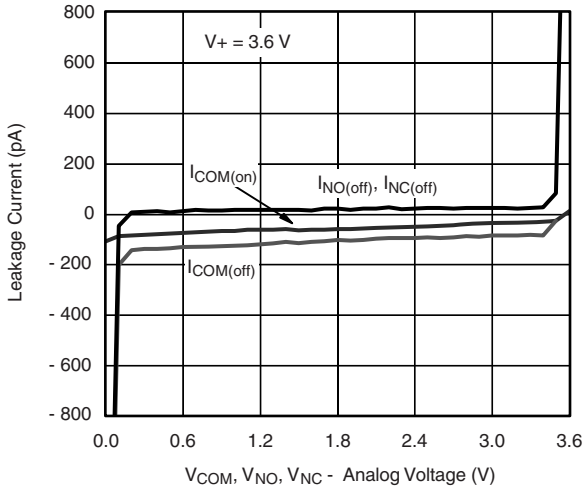


Supply Current vs. Input Switching Frequency

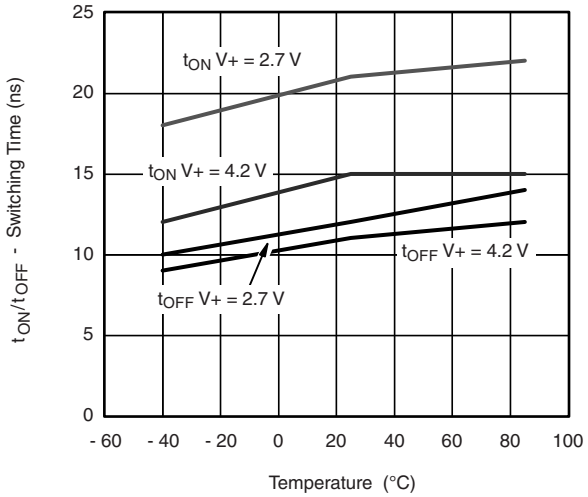
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



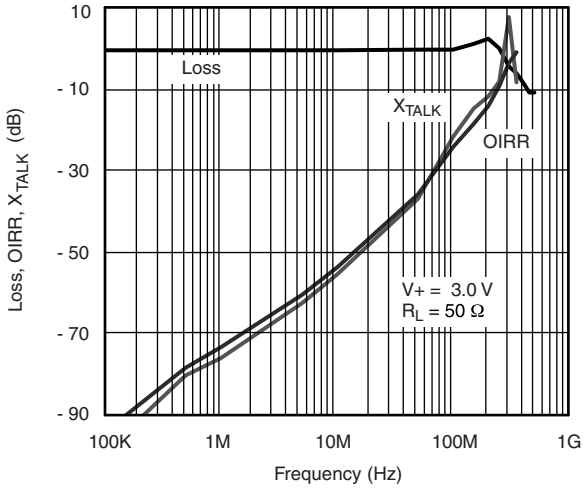
Leakage Current vs. Temperature



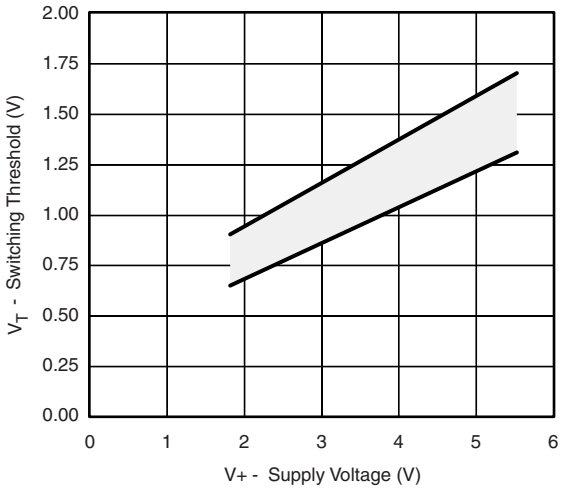
Leakage vs. Analog Voltage



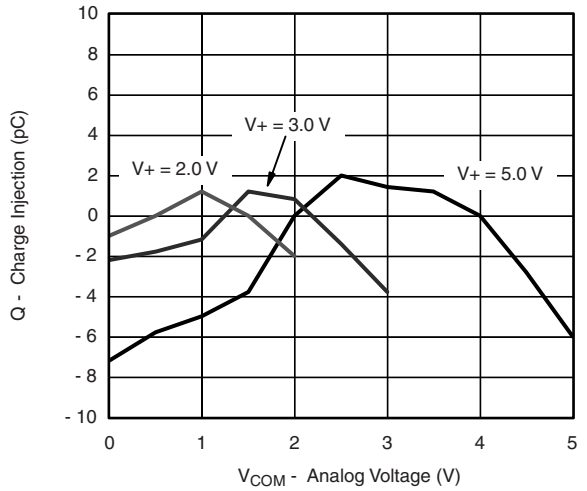
Switching Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

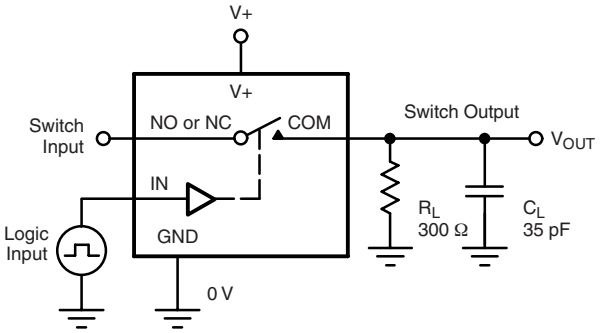


Switching Threshold vs. Supply Voltage



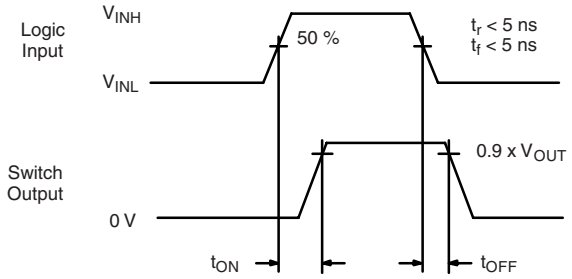
Charge Injection vs. Analog Voltage

TEST CIRCUITS



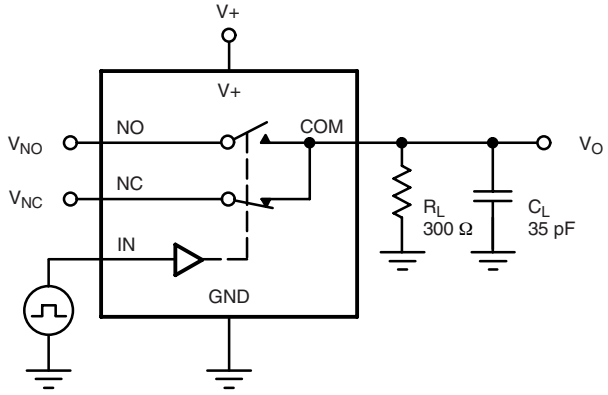
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

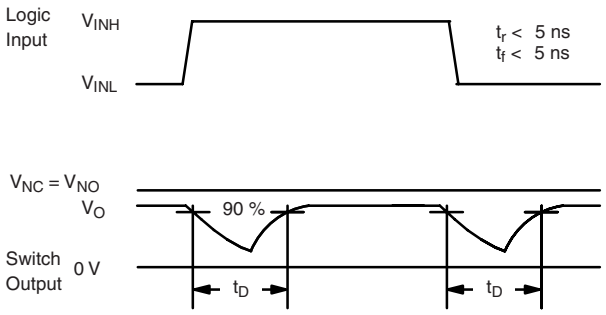
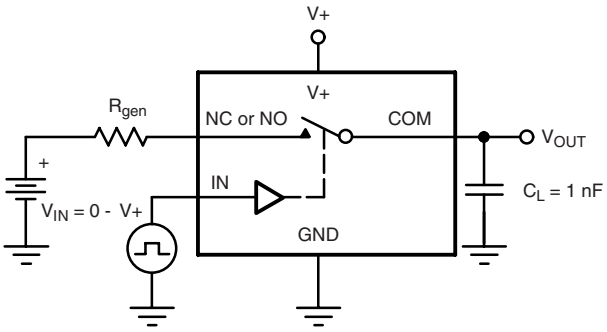
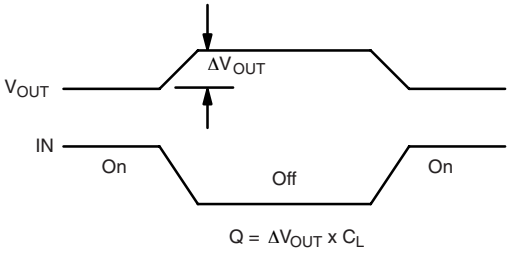


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

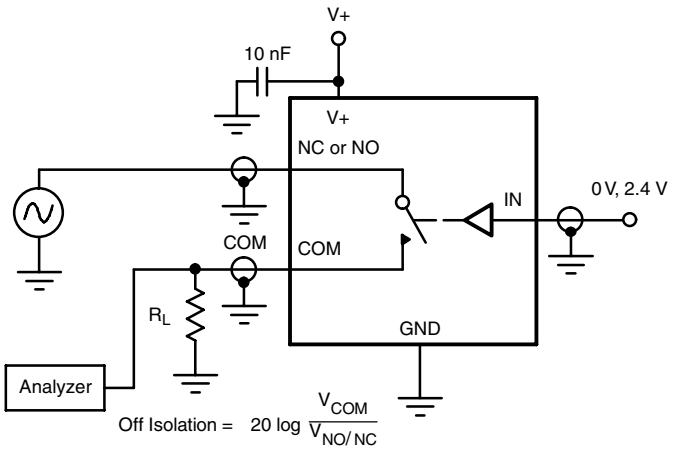


Figure 4. Off-Isolation

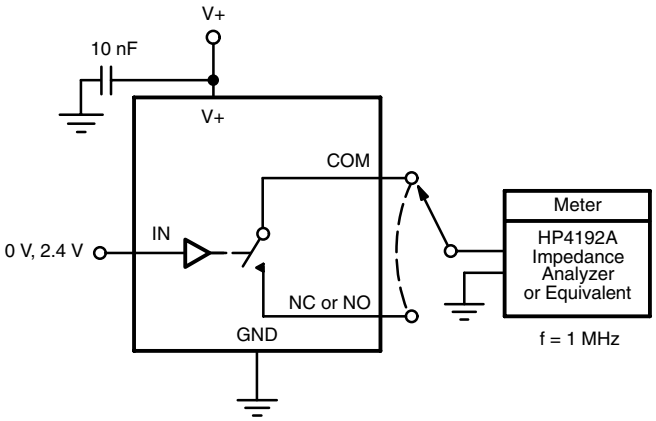
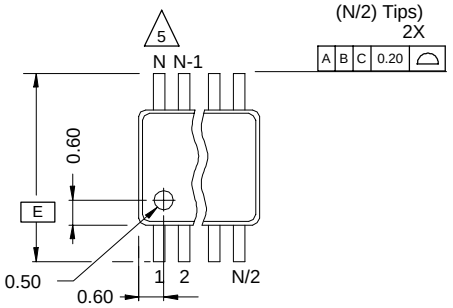


Figure 5. Channel Off/On Capacitance

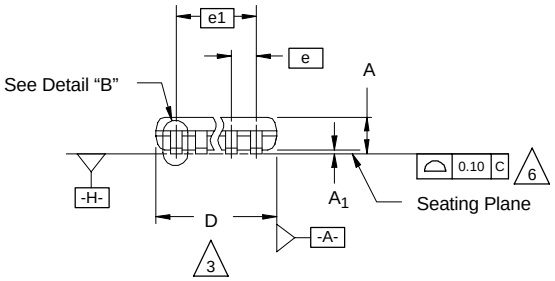
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65369.

MSOP: 10-LEADS

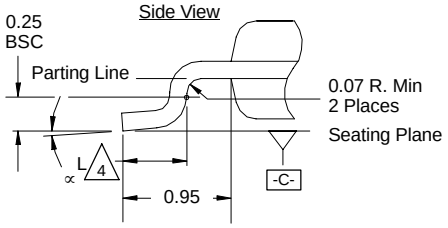
JEDEC Part Number: MO-187, (Variation AA and BA)



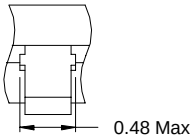
Top View



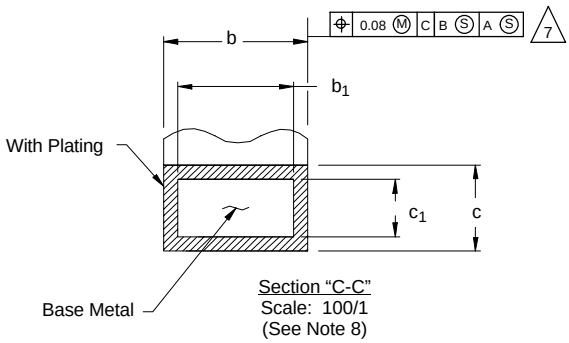
Side View



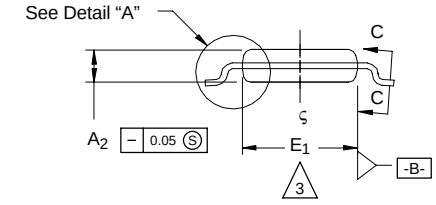
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 10L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.17	-	0.27	8
b_1	0.17	0.20	0.23	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.50 BSC			
e_1	2.00 BSC			
L	0.40	0.55	0.70	4
N	10			5
∝	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
DWG: 5867

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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.