Video Memory / FIFO

HD FRAME MEMORY

Features

- Memory densities: 15, 30, 60Mbit
- 150MHz Max clock rate
- Independent Read and Write ports:
  - Supports simultaneous read/write operations
  - Enables buffering across clock domains
- Operating Modes:
  - Single-channel FIFO w/ Asynchronous I/O
  - Dual independent FIFOs w/ Asynchronous I/O
- Flexible Write/Read Pointer Manipulation
  - W/R address pointer Clear/Set
  - W/R address pointers can be overridden in real-time using external 24bit address port
  - TRS detection for auto-clearing of Write pointer
  - W/R memory access Enable/Disable
  - Input enable control (Write Masking) for freeze frame control
- Selectable I/O V_{DD} = 1.8V, 2.5V, 3.3V
- Selectable Core V_{DD} = 1.8V, 2.5V, 3.3V
- 172 ball FBGA package (15 x 15 x 1.4mm)
- Depth expansion is supported for Multi-frame HDTV, Multiframe SDTV, and other formats:
  - Seamless address space is maintained with up to 12 cascaded devices
- Near-Full/Empty Flags With Programmable Thresholds
- Collide Flag alerts User of W/R pointer crossings
- I²C Serial Microprocessor Interface
- Output Enable Control (Data Skipping)
- JTAG Boundary Scan - IEEE 1149.1

LF4460 - 60Mbit
Selectable Memory Organization
• 7,761,600 x 8-bit
• 6,209,280 x 10-bit
• 5,174,400 x 12-bit
• 3,880,800 x 16-bit
• 3,104,640 x 20-bit
• 2,587,200 x 24-bit

LF4430 - 30Mbit
Selectable Memory Organization
• 3,880,800 x 8-bit
• 3,104,640 x 10-bit
• 2,587,200 x 12-bit
• 1,940,400 x 16-bit
• 1,552,320 x 20-bit
• 1,293,600 x 24-bit

LF4415 - 15Mbit
Selectable Memory Organization
• 1,940,400 x 8-bit
• 1,552,320 x 10-bit
• 1,293,600 x 12-bit
• 970,200 x 16-bit
• 776,160 x 20-bit
• 646,800 x 24-bit

Applications

- Frame buffer for common HD formats (720p, 1080i, 1080p)
- HDTV / SDTV Frame Synchronization
- HDTV Display Buffer
- Time Base Correction (TBC)
- Freeze-Frame Buffer
- Picture-in-Picture (PIP) Buffer
- Frame Rate Conversion
- Security Camera Systems
- Field-Based or Frame-Based Comb Filtering
- HD Video Capture & Editing Systems
- Deep Data Buffering
- Image Manipulation (Rotation, Zoom)
- Test Pattern Generation
- Motion Detection or Frame-to-Frame Correlation

PRELIMINARY INFORMATION

LF4430 Overview

Memory Organization

Imagine a full-frame HDTV frame buffer solution in a single, tiny chip. Add a simple, easy to use SRAM interface and complex addressing capability on-chip - and you have a LOGIC Devices HD Frame Memory. The LF44xx Video Memory family supports all SDTV/HDTV video formats and range from 15 to 60Mbit densities with configurable memory organizations and parallel word-widths. Independent (asynchronous) clock domains on the device's data I/O ports enable synchronization and rate matching. Since reads are non-destructive, a given data value written into the memory core may be read as many times as desired. Applications requiring additional depth may cascade devices for depth expansion.

Addressing Flexibility

In addition to memory organization flexibility, the LF44xx family simplifies memory addressing tasks. Timing reference signals (TRS) on an incoming video signal can be detected and used to provide an auto-clear on the Write pointer/address for simplified frame-sync applications. Write or Read pointers can be forced (in real-time) to any location within the entire address space using an external 24bit address port. Full-time Write or Read address manipulation using the external address port enables such applications as image rotation, Region-of-Interest extraction, or Picture-in-Picture (PIP).

Simple Configuration & Control

Devices are configured by simply tying off static control pins. If a more complex memory implementation is required, access to application specific functions/features are provided through 8bit configuration words programmed via a standard I²C serial interface.

MODE control pins define memory organization, I/O word width, and number of unique FIFO channels. Combinations of MODE settings range from 8 to 24bit I/O in single or dual FIFO configurations.

LF44xx Functional Block Diagram

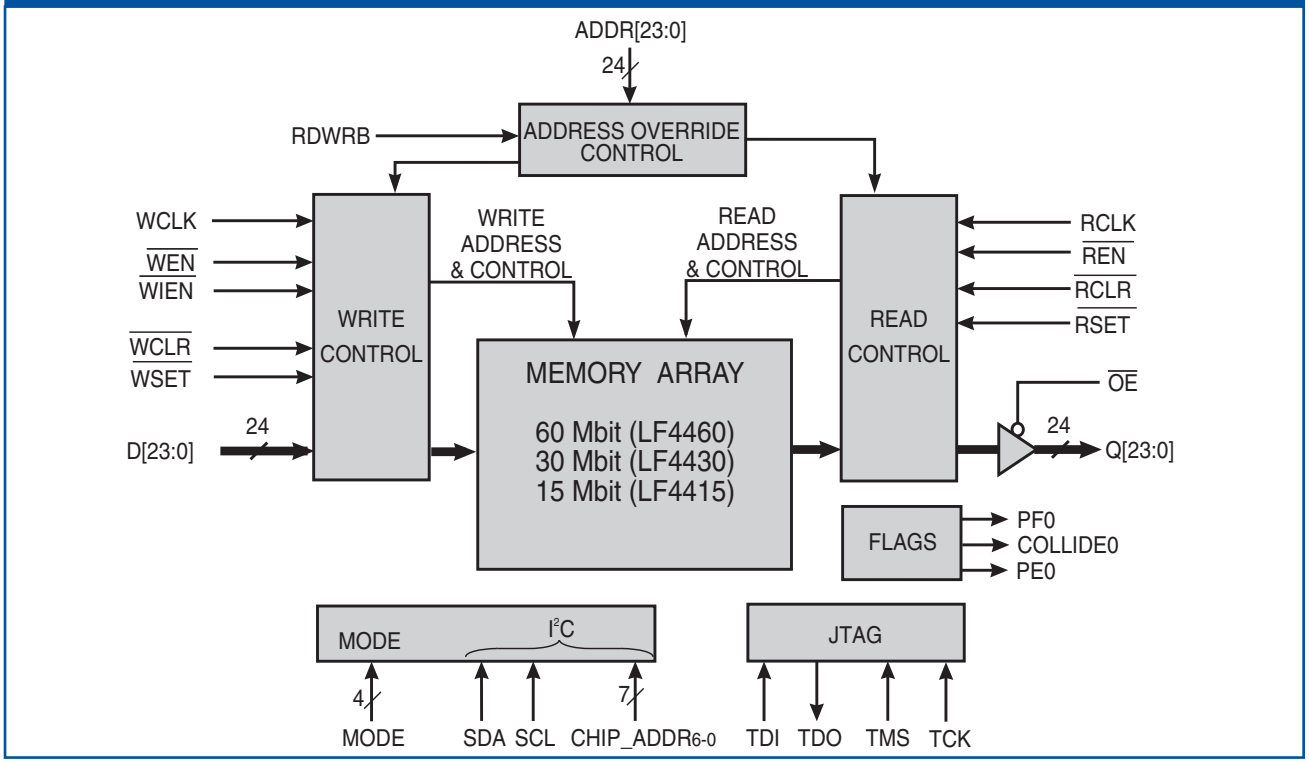


Figure 1. Single-Channel FIFO Configuration

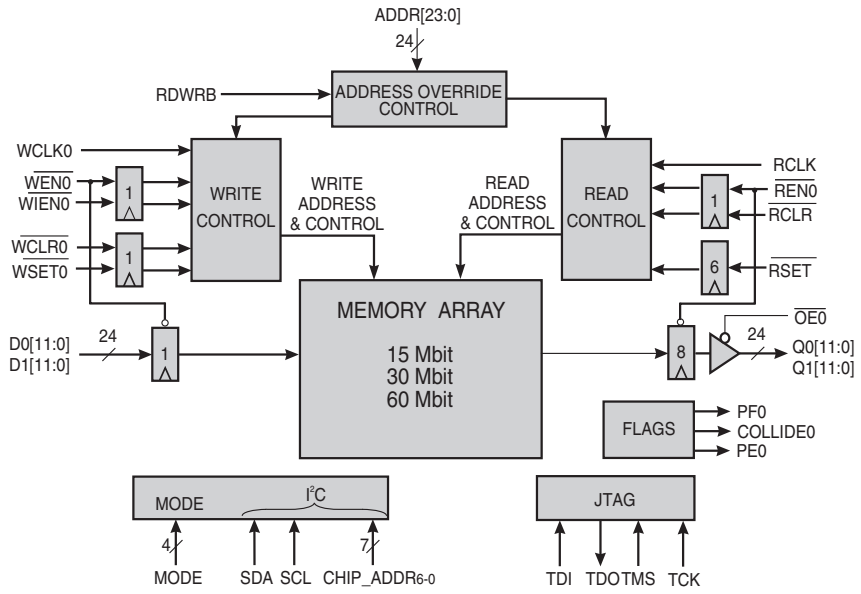
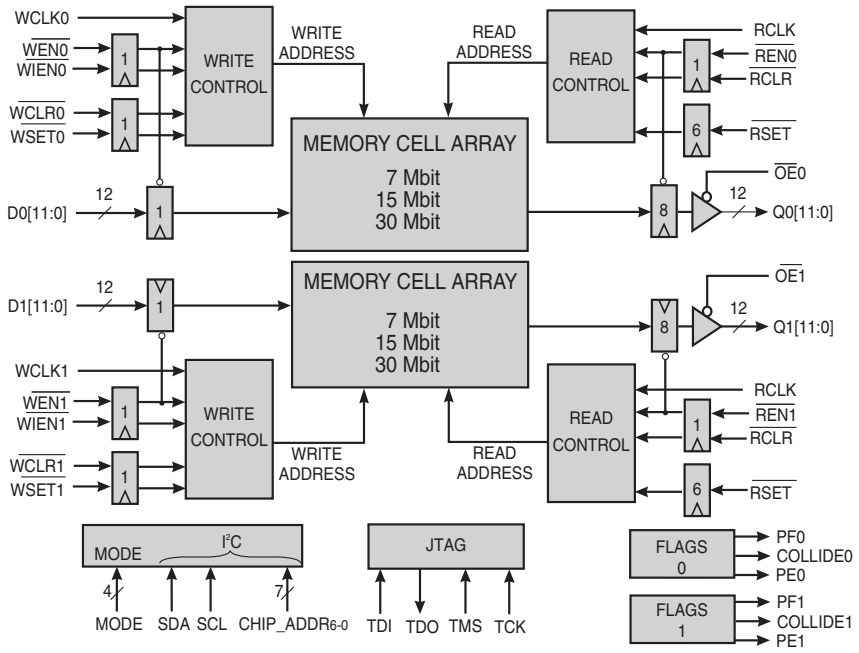


Figure 2. Dual Independent FIFOs Configuration



Operating Modes

Single-Channel Mode

Single-Channel FIFO Configuration (MODE = 0xxx) The LF44xx memory can be organized as a single channel deep FIFO (from 8 to 24bits wide), with independent read and write ports and clocks to allow for fully independent/asynchronous operation. This mode is ideal for rate matching, frame synchronization, and image manipulation applications.

Dual-Channel Mode

Dual Independent FIFOs Configuration (MODE = 11xx) Dual-channel mode is designed for applications requiring independent control of two FIFOs in one device. Each channel of the LF44xx operates as an independent FIFO with the exceptions of A) both channels share a common read clock RCLK and B) memory access using an external address port is not possible. Each channel input, control, or output is identified by its suffix “0” or “1”. (Ex: D0, WEN0 versus D1, WEN1, etc...)

FIFO Addressing

Buffering/synchronization applications often require sequential FIFO addressing, where the read pointer chases the write pointer across the memory address space. The first data sample (or pixel) of a frame of data is generally referenced to address zero in memory. This is implemented by clearing the write pointer (bringing WCLR0 LOW) on the first sample of each frame of data written into memory. Upon requesting a frame of data from memory starting with address zero (pixel 0), the read pointer is cleared (by bringing RCLR0 LOW). The LF4430 write and read address pointers increment automatically through the memory address space, and memory writes/reads are enabled, when WEN0 and REN0 are LOW respectively.

External Address Port

For applications requiring arbitrary access to memory addresses, a 24bit external address port is provided. This 24bit address port provides access to the entire memory space on a cycle by cycle basis and can be used to override the Write or Read sequential FIFO address pointers. The write address is forced to the value defined by the 24bit external address port by bringing WSET0 LOW (assuming ADSEL is LOW). The read pointer is forced to the value defined by the 24bit external address port by bringing RSET LOW (assuming RDWR is HIGH). The external address can be updated each write or read cycle, depending on which port is being addressed, to enable such applications as image rotation, PIP, region of interest extraction, etc. Once the write or read address pointer override is to be terminated (bringing WSET0 or RSET back HIGH), the write or read address pointer resumes sequential increment sequence starting at the last address overriden by the address port (see Address Control table).

2-D Addressing

The LF44xx memory can be mapped as a linear address space (sequential FIFO addressing from say 0 to FFFF) or as a 2-D address space (as an image is addressed - using rows and columns). 2-D address mapping simplifies complex address manipulation requirements that exist in video and image processing. In order to access the memory using a 2-D address space, the external 24bit address port defines a 12bit row and column address for writing or reading. See Control Registers 0 and 1.

Auto TRS Decode & Pointer Clear

Timing Reference Signals (TRS) from the incoming video stream are automatically detected and continuously monitored. The field (‘F’) or vertical blanking (‘V’) bits in the TRS sequence can be programmed to auto-clear the write address pointer to zero. This is useful in synchronization applications by relieving the designer of routing SYNC signals from the upstream decoder, deserializer, or processor to the FIFO Write address controls.

Empty/Full Flags

If the read and write address pointers collide, the COLLIDE0 flag will be brought HIGH, to alert the host. The programmable almost-full (PF) and almost-empty (PE) flags provide advance warning of pointer collisions. They are triggered when the R/W pointers are within user-specified “fullness” or “emptiness” thresholds. Thresholds are set by the user and can be written into configuration registers (see registers 0D-18), and are defaulted to 1/80th for PE and 79/80th for PF. For example, if the flags are defaulted to the 1/80 and 79/80 thresholds, flag PE0 will go HIGH whenever the read pointer lags behind the write pointer by less than 1/80 of the memory space, and flag PF0 will go HIGH whenever the read pointer leads the write pointer by this amount. (See LF4430 Flag application note)

LF4415 (15Mbit) Memory Organization

Figure 3 - LF4415 (15Mbit) Memory Organization Control

# FIFO Channels	Memory Organization	MODE	Description
1	8 x 1,940,400	000x	8bit wide 15Mbit single-channel FIFO
1	10 x 1,552,320	0010	10bit wide 15Mbit single-channel FIFO
1	12 x 1,293,600	0011	12bit wide 15Mbit single-channel FIFO
1	16 x 970,200	100x	16bit wide 15Mbit single-channel FIFO
1	20 x 776,160	1010	20bit wide 15Mbit single-channel FIFO
1	24 x 646,800	1011	24bit wide 15Mbit single-channel FIFO
2	(2x) 8 x 970,200	110x	Two independent 8bit wide 7Mbit FIFOs
2	(2x) 10 x 776,160	1110	Two independent 10bit wide 7Mbit FIFOs
2	(2x) 12 x 646,800	1111	Two independent 12bit wide 7Mbit FIFOs

Figure 4 - External Address Port Configuration*

RDRW	Address Override	Description
0	Write	External address port (ADDR) overrides WRITE address when WSET0 = LOW
1	Read	External address port (ADDR) overrides READ address when RSET = LOW

*Only Single Channel Modes are capable of using the External Address port (ADDR)

Figure 5 - Single Channel FIFO I/O Mapping

I/O Word	D1/Q1[11:0]												D0/Q0[11:0]											
Width	11	10	9	8	7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0
8													I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	----	----	----	----
10													I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	----	----
12													I/O_{11}	I/O_{10}	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
16	I/O_{15}	I/O_{14}	I/O_{13}	I/O_{12}	I/O_{11}	I/O_{10}	I/O_9	I/O_8	----	----	----	----	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	----	----	----	----
20	$I/O1_9$	I/O_{18}	I/O_{17}	I/O_{16}	I/O_{15}	I/O_{14}	I/O_{13}	I/O_{12}	I/O_{11}	I/O_{10}	----	----	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	NC	NC
24	I/O_{23}	I/O_{22}	I/O_{21}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{17}	I/O_{16}	I/O_{15}	I/O_{14}	I/O_{13}	I/O_{12}	I/O_{11}	I/O_{10}	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0

LF4430 (30Mbit) Memory Organization

Figure 3 - LF4430 (30Mbit) Memory Organization Control

# FIFO Channels	Memory Organization	MODE	Description
1	8 x 3,880,800	000x	8bit wide 30Mbit single-channel FIFO
1	10 x 3,104,640	0010	10bit wide 30Mbit single-channel FIFO
1	12 x 2,587,200	0011	12bit wide 30Mbit single-channel FIFO
1	16 x 1,940,040	100x	16bit wide 30Mbit single-channel FIFO
1	20 x 1,552,320	1010	20bit wide 30Mbit single-channel FIFO
1	24 x 1,293,600	1011	24bit wide 30Mbit single-channel FIFO
2	(2x) 8 x 1,940,040	110x	Two independent 8bit wide 15Mbit FIFOs
2	(2x) 10 x 1,552,320	1110	Two independent 10bit wide 15Mbit FIFOs
2	(2x) 12 x 1,293,600	1111	Two independent 12bit wide 15Mbit FIFOs

Figure 4 - External Address Port Configuration*

RDRW	Address Override	Description
0	Write	External address port (ADDR) overrides WRITE address when WSET0 = LOW
1	Read	External address port (ADDR) overrides READ address when RSET = LOW

*Only Single Channel Modes are capable of using the External Address port (ADDR)

Figure 5 - Single Channel FIFO I/O Mapping

I/O Word	D1/Q1[11:0]												D0/Q0[11:0]											
Width	11	10	9	8	7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0
8													I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	----	----	----	----
10													I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	----	----
12													I/O_{11}	I/O_{10}	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
16	I/O_{15}	I/O_{14}	I/O_{13}	I/O_{12}	I/O_{11}	I/O_{10}	I/O_9	I/O_8	----	----	----	----	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	----	----	----	----
20	$I/O1_9$	I/O_{18}	I/O_{17}	I/O_{16}	I/O_{15}	I/O_{14}	I/O_{13}	I/O_{12}	I/O_{11}	I/O_{10}	----	----	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	NC	NC
24	I/O_{23}	I/O_{22}	I/O_{21}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{17}	I/O_{16}	I/O_{15}	I/O_{14}	I/O_{13}	I/O_{12}	I/O_{11}	I/O_{10}	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0

LF4460 (60Mbit) Memory Organization

Figure 3 - LF4460 (60Mbit) Memory Organization Control

# FIFO Channels	Memory Organization	MODE	Description
1	8 x 7,761,600	000x	8bit wide 60Mbit single-channel FIFO
1	10 x 6,209,280	0010	10bit wide 60Mbit single-channel FIFO
1	12 x 5,174,400	0011	12bit wide 60Mbit single-channel FIFO
1	16 x 3,880,800	100x	16bit wide 60Mbit single-channel FIFO
1	20 x 3,104,640	1010	20bit wide 60Mbit single-channel FIFO
1	24 x 2,587,200	1011	24bit wide 60Mbit single-channel FIFO
2	(2x) 8 x 3,880,800	110x	Two independent 8bit wide 30Mbit FIFOs
2	(2x) 10 x 3,104,640	1110	Two independent 10bit wide 30Mbit FIFOs
2	(2x) 12 x 2,587,200	1111	Two independent 12bit wide 30Mbit FIFOs

Figure 4 - External Address Port Configuration*

RDRW	Address Override	Description
0	Write	External address port (ADDR) overrides WRITE address when WSET0 = LOW
1	Read	External address port (ADDR) overrides READ address when RSET = LOW

*Only Single Channel Modes are capable of using the External Address port (ADDR)

Figure 5 - Single Channel FIFO I/O Mapping

I/O Word	D1/Q1[11:0]												D0/Q0[11:0]											
Width	11	10	9	8	7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0
8													I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	----	----	----	----
10													I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	----	----
12													I/O_{11}	I/O_{10}	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
16	I/O_{15}	I/O_{14}	I/O_{13}	I/O_{12}	I/O_{11}	I/O_{10}	I/O_9	I/O_8	----	----	----	----	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	----	----	----	----
20	$I/O1_9$	I/O_{18}	I/O_{17}	I/O_{16}	I/O_{15}	I/O_{14}	I/O_{13}	I/O_{12}	I/O_{11}	I/O_{10}	----	----	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	NC	NC
24	I/O_{23}	I/O_{22}	I/O_{21}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{17}	I/O_{16}	I/O_{15}	I/O_{14}	I/O_{13}	I/O_{12}	I/O_{11}	I/O_{10}	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0

Device Configuration

Programming the LF44xx

Most LF44xx applications will not require the internal configuration registers to be modified from their default settings. If access to a special-purpose mode/feature is required, an I²C serial interface is provided. Once written, the updated 8bit configuration modify the working circuitry only after writing an update command to Register 03F. (See note at the end of this section).

Serial MPU Interface

The standard two-wire interface is composed of an SCL clock pin and a bi-directional SDA data pin. When inactive, SDA and SCL are forced HIGH by external pull up resistors.

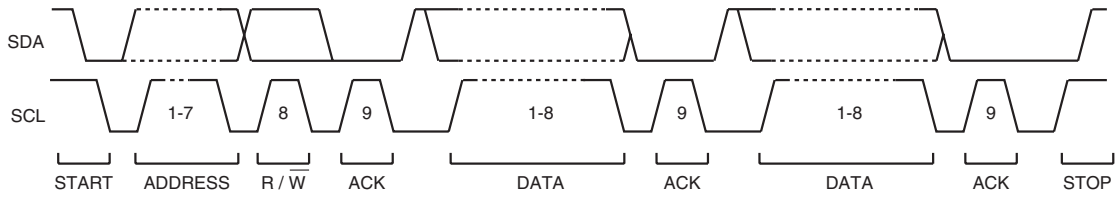
Data transmission is achieved over the SDA pin and must remain constant during the logical HIGH portion of the SCL clock pulse. The level of SDA, while SCL is HIGH, is interpreted as the appropriate bit value as will be shown later. Changing the data on SDA must only occur when SCL is low, because any changes to SDA while SCL is HIGH is interpreted as a start or stop request, which are shown in Figure 7 with an example data transfer in Figure 8.

The first operation to begin programming the LF4430 through the serial interface, is to send a start signal. When the interface is inactive, a HIGH to LOW transition must be sent on SDA while SCL is HIGH, notifying all connected devices (slaves) to expect a data transmission. When transferring data, the MSB of the eight bit sequence is the first bit to be transmitted to or from the master or slave. The first byte of data to be transmitted on SDA must consist of the 7-bit base address of the slave, along with an 8th READ/WRITE bit as the LSB, which describes the direction of the data transmission. The slave whose 7-bit CHIP_ADDR6-0, matches the 7-bit base address sent on SDA, will send an acknowledgement back to the master by bringing SDA LOW on the 9th SCL pulse.

During a write operation, if the slave does not send an acknowledgment back to the master device, SDA is left high which forces the master to generate a stop signal. In contrast, during a read operation, if there is no acknowledgement back from the master device, the LF44xx interprets this as if it were the end of the data transmission, and leaves SDA high, allowing the master to generate its stop signal.

Figure 7 - I²C Start and Stop Signals

Figure 8 - Initiation and Data Transfer (to consecutive registers) on I²C Bus



Device Configuration

There are four operations that can be performed between the master and the slave. They are: Write to consecutive registers, write to a single control register, read from consecutive registers and read from a single register. To write to consecutive control registers, a start signal and base address must be sent with the R/W bit as described above. After the acknowledgment back from the appropriate slave, the 8-bit address of the target control register must be written to the slave with the R/W bit LOW. The slave then acknowledges by setting SDA LOW. The data byte to be written into the register can now be transferred on SDA. The slave then acknowledges by pulling SDA LOW on the next positive going pulse of SCL. The first control register address loaded into the LF4430 is considered as the beginning address for consecutive writes, and automatically increments to the next higher address space. Therefore after the acknowledgement, the data byte to configure register (first address + 1) can now be transferred from master to slave. At any point a stop signal can be given to end the data transfer. To write to a single control register, the same technique can be applied adding a stop signal after the first data write.

To read from consecutive control registers, the master must again give the start signal followed by a base address with the R/W bit = 0, as if the master wants to write to the slave. The appropriate slave then acknowledges. The master will then transfer the target register address to the slave and wait for an acknowledge. The master will then give a repeated start signal to the slave, along with the base address and R/W bit this time HIGH signifying a read and wait for an acknowledge. The user must write to the LF44xx to select the appropriate initial target register. Otherwise the starting position of the read is uncertain. Once the LF44xx acknowledges, the next byte of data on SDA is the contents of the addressed register sent from the device. If the master acknowledges, the LF44xx will send the next higher register's contents on the following byte of data. To read from only one register is the same procedure as for consecutive reading with a stop signal following the transfer of the register's contents.

****NOTE: UPDATE COMMAND REQUIRED**
After updating any of the configuration registers, Register 03F must be written with all zeros to modify the working registers.

Depth Expansion

Depth Expansion Mode
Multiple devices can be cascaded for depth expansion - deepening the address space by 2x, 3x, etc. The address space is extended for every additional device that is cascaded. Depth expansion is implemented by tying together input data, controls, and outputs of all devices. Only one device drives the shared output bus at a time. All bus contention, addressing, and inter-chip control is handled internally. No additional external circuitry is required.

Each device in an expansion of N devices is responsible for 1/N of the address space. That is, each device writes and/or reads based on common W/R pointer locations and its position in the expansion. Configuration Register C[3:0] (BASE_ADDR) is used to define each device's position in the chain of devices.

Depth expansion is supported in single-channel mode only. The configuration registers of each device must be programmed identically, depending on mode/function, except for Register C. Register C defines which region of the 24bit address space the particular device is responsible for. Within Register C, there is a 4bit BASE_ADDR and 4bit NUM_DEV word. BASE_ADDR determines the region of address space each device controls, and NUM_DEV defines how many devices are tied together. Register C effectively is programmed as "Chip n of N".

Detailed Signal Definitions

Power

***VCC_{INT}* - Internal Core Power Supply (+1.8V, +2.5V or +3.3V)**
VCCint is auto-regulated to an internal core VCC. All VCCint pins must be connected.

***VCC_O* - Output Driver Power Supply (+1.8V, +2.5V or +3.3V)**
VCCo is auto-regulated to an internal I/O driver VCC.. All VCCo power pins must be connected.

Clocks

WCLK0 - Write Clock 0
Data present on D0/D1 is latched and write pointer(s) are incremented on the rising edge of WCLK0 when WEN0 is LOW. In dual-channel modes (MODE=x1xx), WCLK0 services input port D0 only.

WCLK1 - Write Clock 1
In dual-channel modes (MODE=x1xx), data present on D1[11-0] is latched on the rising edge of WCLK1 when WEN1 is LOW. In single-channel modes (MODE=x0xx), WCLK1 is ignored and can be tied LOW unless used as an 'ADDR' external address bit (See ADDR descr.).

RCLK - Read Clock
Data is read from memory, read pointer(s) are incremented, and data is presented on its respective output port (Qx[11-0]) on a rising edge of RCLK when RENx and OEx is LOW.

Data Input Ports

D0[11-0] / D1[11-0] - Data Input Ports 0 / 1
D0/D1 is a 24-bit registered data input port. Please refer to Figure 5/6/7 on page 5/6/7 respectively. For any single-channel configuration, including data widths of 16bits and higher, a combined D0/D1 input port is enabled, with data latched on the rising edge of WCLK0. For data widths of 12bits or less, use D0[11-0]. For two independent FIFOs, D0 services channel 0 and D1 services channel 1. In dual-channel modes (MODE=x1xx), D1[11-0] is the 12-bit registered data input port for Channel 1. In this case D0 is is latched on the rising edge of WCLK0 and D1[11-0] is latched on the rising edge of WCLK1. Bit 11 is the MSB in all modes. Any unused data input pins should be tied LOW.

I^2C Interface

SDA - Serial Data I/O
SDA is the standard bidirectional data pin of a two-wire serial microprocessor interface. External pullup is required on both SDA and SCL pins.

SCL - Serial Clock Input
SCL is a standard two-wire serial microprocessor interface clock pin. Since this part cannot be the master on a two-wire serial microprocessor interface, SCL functions as a dedicated input.

Address Port

ADDR23-0 - External Read/Write Address Port
ADDR is a 24-bit input port for real-time Write or Read address override (single channel mode). The ADDR23-0 port shares input pins unused in single-channel mode. See Table 1 below. This address can be mapped as a linear 24bit address (default) or as a 2-D address with row/column components. For 2-D addresses ADDR11-0 defines the X/Column-coordinate and ADDR23-12 specifies the Y/Row-coordinate. For 2-D addressing, see the description of ROW_LENGTH. ADDR defines the write address if RDWR=0 (ADDR is latched by a WCLK0 rising edge). ADDR defines the read address if RDWR=1 (ADDR is latched by a WCLK0 rising edge). See Registers 0 and 1.

Table 1 - External Address ADDR[23:0] Mapping

Linear	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pins	WIEN1	WEN1	ADDR21	ADDR20	ADDR19	ADDR18	ADDR17	ADDR16	REN1	COLLID1	PE1	PF1	ADDR11	ADDR10	ADDR9	ADDR8	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	WCLR1	WSET1	WCLK1
2-D	11	10	9	8	7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0
	Y / Row Address												X / Column Address											

Detailed Signal Definitions

Mode Control Pins

MODE - Memory Organization DEfinition
The 4-bit MODE setting defines the memory organization in terms of depth, width, and number of unique FIFO channels. See figures on page 5/6/7.

RDWRB - External Address Read/ Write pointer Override Control
When RDWRB is LOW, the external address ADDR defines the WRITE pointer - latched by bringing WSET0 LOW. When RDWRB is HIGH, the external address ADDR defines the READ pointer - latched by bringing RSET LOW. See Figure 4 on page 5.

W/R Pointer Contol Pins

WCLR0 - Write Pointer Clear 0
A LOW on WCLR0 clears the write address pointer to zero. When WCLR0 is brought LOW, a rising edge of WCLK0 will write the current value on D0 to address 0 in memory . When WCLR0 is HIGH, the write pointer auto-increments sequentially (unless WSET0 is brought LOW). WCLR0 may be programmed to be edge-triggered, clearing the write pointer for a single cycle following a falling WCLR0 edge, after which a sequential increment resumes. When active-LOW triggered, a LOW on WCLR0 forces the write pointer to zero until brought HIGH. WCLR0 is only effective if WEN0 is LOW. In dual-channel modes (MODE=x1xx), WCLR0 affects only the Channel 0 write pointer.

WCLR1- Write Pointer Clear 1
A LOW on WCLR1 clears the write address pointer to zero. WCLR1 may be programmed to be edge-triggered, clearing the write pointer for a single cycle following a falling WCLR1 edge, after which a sequential increment resumes. When active-LOW triggered, a LOW on WCLR1 forces the write pointer to zero until brought HIGH. In single-channel modes (MODE=x0xx), tie WCLR1 LOW - unless used as an ADDR external address bit (See ADDR descr.).

WSET0 - Write Pointer Set 0
When WSET0 is brought LOW, a rising edge of WCLK0 writes the data on D0[11:0] to the address specified by the RDWR address control. WSET0 may be programmed to be edge-triggered, in which case it ‘sets’ or ‘jumps’ the write pointer for only one clock cycle following a falling edge on WSET0, after which auto incrementing resumes. When active-LOW triggered, a LOW on WSET0 overrides the write pointer until it is brought HIGH. For prolonged address overrides, programming WSET0 to be active LOW triggered while holding WSET0 LOW provides a continuous write pointer override. WSET0 is effective only when WEN0 is LOW and WCLR0 is HIGH.

WSET1 - Write Pointer Set 1
In single-channel mode, WSET1 should be tied LOW. In dual-channel mode, WSET1 controls the Channel 1 write pointer as WSET0 controls the Channel 0 write pointer. WSET1 may be programmed to be edge-triggered, in which case it ‘sets’ or ‘jumps’ the write pointer for only one clock cycle following a falling edge on WSET1, after which auto incrementing resumes. When active-LOW triggered, a LOW on WSET1 overrides the write pointer until it is brought HIGH. WSET1 is effective only when WEN1 is LOW and WCLR1 is HIGH. In single-channel modes (MODE=x0xx), tie WSET LOW - unless used as an ADDR external address bit (See ADDR descr.).

RSET - Read Address Pointer Set
When a RSET is brought LOW, a rising edge of RCLK reads the address specified by the external address port (assuming WCLR1/ADSEL is HIGH). RSET may be programmed to be edge-triggered, in which case it ‘sets’ the read pointer for only one clock cycle following a falling edge on RSET, after which auto incrementing resumes. When active-LOW triggered, a LOW on RSET overrides the read pointer until it is brought HIGH. For prolonged address overrides, programming RSET to be active LOW triggered while holding RSET LOW provides a continuous read pointer override. RSET is effective only when RENx is LOW during the previous cycle and RCLR is HIGH. RSET cannot be brought LOW while WSETx or are LOW.

Detailed Signal Definitions

EDGE - Edge/Level Sensitivity Triggering for Address 'SET' Control
The EDGE pin controls whether WSETx, WSETx, RSETx are level or negative-edge triggered. When level-sensitive, the appropriate pointer is overridden as long as the WSETx/RSETx pin is LOW. When falling edge sensitive, a falling edge on one of the WSETx/RSETx pins triggers a single cycle of address override (to the value on the 24bit ADDR external address). Individual sensitivity control over any SET and CLR pin is possible by modifying Register A which overrides the settings preset by EDGE. The table below outlines the EDGE pin settings.

Figure 9 - 'Set' Trigger Control

EDGE	WSET0	WSET1	RSET
0	Edge	Edge	Level
1	Level	Level	Edge

RCLR - Read Address Pointer Clear
RCLR clears the read pointer. When RCLR is brought LOW, a rising edge of RCLK will read from address 0 in memory . When RCLR is HIGH, the read pointer auto-increments sequentially unless RSET is brought LOW. RCLR may be programmed to be edge-triggered, in which case it clears the read pointer for only one clock cycle following a falling edge on RCLR, after which auto incrementing resumes. When active-LOW triggered, a LOW on RCLR forces the read pointer to zero until it is brought HIGH. RCLR is only effective if REN0 is LOW. In dual-channel mode, RCLR clears both Channel 0 & 1 read pointers. The read enables RENx must be LOW on the previous cycle to clear their respecitve read pointers.

WEN0 - Write Enable 0
WEN0 enables/disables memory write accesses and write pointer auto-incrementing. D0 data is written into memory and the write address pointer is incremented on the rising edge of WCLK0 when WEN0 is LOW.

WEN1 - Write Enable 1
In dual-channel mode, WEN1 enables/disables Channel-1 memory write accesses and write pointer auto-incrementing. D1 data is written into memory and the write address pointer is incremented on the rising edge of WCLK1 when WEN1 is LOW. In single-channel mode, WEN1 should be tied LOW - unless used as an ADDR external address bit (See ADDR descr.).

WIEN0 - Memory Write Enable 0 (Write Masking)
WIEN0 is used to disable writing into memory independent of the write pointer increment. A LOW on WIEN0 enables writing, while a HIGH on WIEN0 disables writing. The write address pointer is incremented by WEN0 regardless of WIEN0. WIEN0 can be used to mask data from being written to memory while the write pointer freely increments. Unless writes to memory are to be masked, simply tie WIEN0 LOW and let WEN0 handle memory/pointer enabling.

WIEN1 - Memory Write Enable 1 (Write Masking)
In dual-channel mode, WIEN1 is used to disable writing into channel-1 memory. A LOW on WIEN1 enables writing, while a HIGH on WIEN1 disables writing. The write address pointer is incremented by WEN1 regardless of WIEN1. WIEN1 can be used to mask data from being written to memory while the write pointer remains free running (incrementing). Unless writes to memory are to be masked, simply tie WIEN1 LOW and let WEN1 handle memory/pointer enabling. In single-channel mode, tie WIEN1 LOW - unless used as an ADDR external address bit (See ADDR descr.).

Detailed Signal Definitions

$\overline{\text{REN0}}$ - Read Enable 0
REN0 enables/disables memory read accesses and read pointer auto-incrementing. Data is read from memory and the read address pointer is incremented on the rising edge of RCLK when REN0 is LOW. An additional 8 RCLK cycles, with REN0 LOW, are required for the memory contents to appear on Q0[11-0].

REN1 - Read Enable 1
In dual-channel mode, REN1 enables/disables memory read accesses and read pointer auto-incrementing. Data is read from memory and the read address pointer is incremented on the rising edge of RCLK when REN1 was LOW for the previous rising edge of RCLK. An additional 8 RCLK cycles, with REN1 LOW, are required for the memory contents to appear on Q1[11-0]. In single-channel mode, tie REN1 LOW - unless used as an ADDR external address bit (See ADDR descr.).

Global Reset

RESET - Global Reset
Bringing RESET LOW upon power-up ensures that the read/write pointers are cleared and configuration registers loaded to their default states. An internal power-on reset makes this pin *optional*. RESET is active low and will hold all state machines in their clear statess until it is released HIGH. When applying this global reset, at least one rising edge of both WCLKx and RCLK should capture a LOW on the RESET signal.

Cascade Control

CHIP_ADDR6-0 - Chip Address (CA6-0)
CHIP_ADDR6-0 determines the LF4430's address on the two-wire microprocessor bus. Each LF4430 chip's 7-bit two-wire serial microprocessor interface address is equal to its CHIP_ADDR6-0.

Output Tri-state Control

OE0 - Output Enable 0
When OE0 is LOW, Q0[11-0] is enabled and driven as an output. When OE0 is HIGH, Q0[11-0] is placed in a high-impedance state. Depending on WIDTH settings, unused Q0/Q1 bits are automatically tristated. Flag outputs are not affected by OE0.

OE1 - Output Enable 1
With data widths over 12bits, OE1 should be tied to OE0. When OE1 is LOW, Q1[11-0] is enabled and driven as an output. When OE1 is HIGH, or in any single-channel mode with a data width of 12bits or less, Q1[11-0] is automatically tristated. Depending on WIDTH settings, unused Q0/Q1 bits are automatically tristated. Flag outputs are not affected by OE1.

Data Output Ports

Q0[11-0] / Q1[11-0] - Data Output Port 0/1
Q0/Q1 is a 24-bit registered data output port. Please see Figure 5/6/7 on page 5/6/7 for memory and I/O organization. For any single-channel configuration, including data widths of 16bits and higher, data is read from a combined Q0/Q1 output port, with data updated on the rising edge of RCLK when REN0 is LOW. For data widths of 12bits or less, data is read out on Q0[11-0]. For two independent FIFOs, Q0 services channel 0 and Q1 services channel 1. Depending on WIDTH settings, unused output bits from Q0/Q1 are automatically tri-stated.

Flag Outputs

PF0 / PF1 - Programmable Almost Full Flag 0 & 1
PF0 / PF1 goes HIGH (active) when the write pointer is more than (MAX_depth - (FullThresh)) locations ahead of the read pointer. FulThresh0 and FulThres1 are user programmable threshold values for channel 0 and 1 respectively and are written into Registers 13-15 and 16-18. See Excel File in the 'Video Memory Application Notes' area on www.logicdevices.com for specific threshold values. PF0 is updated on the rising edge of WCLK0. In Dual-Channel mode, PF1 is updated on the rising edge of WCLK1 and is tristated in dual channel mode. In single-channel modes, PF1 must be tied off unless used as an external address it (refer to ADDR discussion).

PE0 / PE1 - Programmable Almost Empty Flag 0 & 1
PE0 / PE1 goes HIGH (active) when the write pointer is less than or equal to (MAX_depth - (EmpThresh*X*)) locations ahead of the read pointer. EmpThresh0 and EmpThresh1 are user programmable threshold values for channel 0 and 1 respectively and are written into Registers 0D-0F and 10-12. See Excel File in the 'Video Memory Application Notes' area on www.logicdevices.com for specific threshold values. PE0 and PE1 are updated on the rising edge of RCLK. In single-channel modes, PE1 must be tied off unless used as an external address it (refer to ADDR discussion)

COLLIDE0 - Memory Read/Write Pointer Collision Flag 0
COLLIDE0 is activated (HIGH) when the write/read address pointers collide/coincide. By monitoring the partial full/empty flags, the user can determine the direction of approach, i.e., read pointer catching up with write (FIFO empty) or write pointer catching up with read (FIFO full). COLLIDE0 is updated on the rising edge of RCLK.

COLLIDE1 - Memory Read/Write Pointer Collision Flag 1
In dual-channel mode, COLLIDE1 is activated (HIGH) when the write/read address pointers collide/coincide. By monitoring the partial full/empty flags, the user can ascertain the direction of approach, i.e., read pointer catching up with write (FIFO empty) or write pointer catching up with read (FIFO full). COLLIDE1 is updated on the rising edge of RCLK. In single-channel modes, COLLIDE1 must be tied off unless used as an external address it (refer to ADDR discussion).

JTAG

TDI - JTAG input data
TDI is the input data pin when using JTAG.

TDO - JTAG output data
TDO is the output data pin when using JTAG.

TMS - JTAG Tap controller input
TMS controls the state of the tap controller.

TCK - JTAG clock
TCK is the used supplied clock of JTAG. It controls the flow of data and latches input data on the rising edge.

Address Control

Figure 7 - Write Address Pointer Control

RESET	WCLK	WEN	WCLR	WSET	RDWR[1]	ADDR	D11-0	PrevAdd	Addr.	Description
0	↑	X	X	X	X	X	X	X	0000	Master reset - write/read pointers are cleared
1	↑	0	1	1	X	X	D1	0000	0001	Increment write pointer - write D1 to addr. 1
1	↑	0	0	1	X	X	D2	0001	0000	Clear write pointer - write D2 to addr. 0
1	↑	0	1	1	X	X	D3	0000	0001	Increment write pointer - write D3 to addr. 1
1	↑	1	1	1	X	X	XXX	0001	0001	Halt write pointer - no write operation
1	↑	1	1	1	X	X	XXX	0001	0001	Halt write pointer - no write operation
1	↑	0	1	1	X	X	D4	0001	0002	Increment write pointer - write D4 to addr 2
1	↑	0	1	1	X	X	FFF	0002	0003	Increment write pointer - write FFF to addr 3 (begin EAV/SAV)
1	↑	0	1	1	X	X	000	0003	0004	Increment write pointer - write 000 to addr 4
1	↑	0	1	1	X	X	000	0004	0005	Increment write pointer - write 000 to addr 5
1	↑	0	1	1	X	X	XYZ	0005	0006	Increment write pointer - write XYZ to addr 6
1	↑	0	1	1	X	X	D5	0006	0004	Write pointer cleared (assuming falling F-bit detected - Register 9[7])[2]
1	↑	0	1	1	X	X	D6	0004	0005	Increment write pointer - write D6 to addr. 1
1	↑	0	1	0	0	An	D7	0005	An	Ext. Addr. Port address override - write D7 to addr. “An” **
1	↑	0	1	0	0	Am	D8	An	Am	Ext. Addr. Port address override - write D8 to addr. “Am” **
1	↑	0	1	1	X	X	D9	Am	Am+1	Increment write pointer - write D9 to addr “Am+1”

NOTES:

1. Overriding the Write address is only possible during Single-Channel modes. Holding WSET0 LOW for multiple cycles allows multi-cycle or ‘full-time’ Write address override - with the address capable of changing every cycle

2. Upon detecting a falling F-bit in the TRS preamble (assuming Register 9[7] is set), the write pointer is cleared - with the beginning of the TRS preamble referenced to address zero. The ‘FFF’ word is written to address 0000, the first ‘000’ word is written to address 0001, etc. The first active sample is therefore written to address 0004.

Address Control

Figure 8 - Read Address Pointer Control

RESET	RCLK	REN	RCLR	RSET	RDWRB[1]	ADDR	PrevAdd	IntAdd	Description[2]
0	↑	X	X	X	X	X	X	0000	Master reset - write/read pointers are clearedMaster reset
1	↑	0	1	1	X	X	0000	0000	REN pipelined by 1 RCLK cycle
1	↑	1	1	1	X	X	0000	0001	Increment read pointer - read from addr 1
1	↑	0	1	1	X	X	0001	0001	Halt read pointer - no output register update- no read operation
1	↑	0	1	1	X	X	0001	0002	Increment read pointer - read from addr 2
1	↑	0	1	0	1	An	0002	An	Override read pointer to Ext. Addr. Port - read from addr. An
1	↑	0	1	0	1	Am	An	Am	Override read pointer to Ext. Addr. Port - read from addr. Am
1	↑	0	1	1	X	X	Am	Am+1	Increment read pointer - read from addr Am+1
1	↑	0	0	1	X	X	Am+1	0000	Clear read pointer - read from addr 0
1	↑	--	1	1	X	X	0000	1	Increment read pointer - read from addr 1

NOTES:

1. Overriding the Read address is only possible in Single-Channel modes. Holding RSET LOW for multiple cycles allows multi-cycle or 'full-time' Read address override - with the address capable of changing every cycle

2. An additional 8 rising RCLK edges are required for the Memory contents to appear on Qx[11:0]

Configuration Registers

Figure 9 - 8bit Configuration Register Map

Address	Register Name(s)	Description
0	ROW_LENGTH [11:8]	Defines row length for 2-D row/column addressing
1	ROW_LENGTH [7:0]	Defines row length for 2-D row/column addressing
2	---	Reserved
3	---	Reserved
4	---	Reserved
5	---	Reserved
6	---	Reserved
7	---	Reserved
8	----	Reserved
9	TRS_DETECT, TRS_TRIGGER	Defines the detection and use of embedded video TRS information
A	PTR_CNTRL	Defines falling-edge or level sensitivty of individual pointer control pins
B	----	Reserved
C	BASE_ADDR, NUM_CASC	Defines depth expansion characteristics
D	EMPTY_THRESH_0 [21:16]	Defines ‘almost-empty’ threshold for programmable empty flag PE0
E	EMPTY_THRESH_0 [15:8]	Defines ‘almost-empty’ threshold for programmable empty flag PE0
F	EMPTY_THRESH_0 [7:0]	Defines ‘almost-empty’ threshold for programmable empty flag PE0
10	EMPTY_THRESH_1 [17:16]	Defines ‘almost-empty’ threshold for programmable empty flag PE1
11	EMPTY_THRESH_1 [15:8]	Defines ‘almost-empty’ threshold for programmable empty flag PE1
12	EMPTY_THRESH_1 [7:0]	Defines ‘almost-empty’ threshold for programmable empty flag PE1
13	FULL_THRESH_0 [21:16]	Defines ‘almost-full’ threshold for programmable full flag PF0
14	FULL_THRESH_0 [15:8]	Defines ‘almost-full’ threshold for programmable full flag PF0
15	FULL_THRESH_0 [7:0]	Defines ‘almost-full’ threshold for programmable full flag PF0
16	FULL_THRESH_1 [17:16]	Defines ‘almost-full’ threshold for programmable full flag PF1
17	FULL_THRESH_1 [15:8]	Defines ‘almost-full’ threshold for programmable full flag PF1
18	FULL_THRESH_1 [7:0]	Defines ‘almost-full’ threshold for programmable full flag PF1
3F	REG_UPDATE	Updates and activates modified configuration registers

Configuration Register Definitions

Register 0, 1

2-D Data Row Length

Register 0,1 = ROW_LENGTH[11:0] - for 2-D Cartesian address mapping

The memory can be addressed using the external 24bit address port either as a 2-Dimensional Cartesian address (in terms of row/column coordinates) or simple linear address (such as 0 to FFFFFF). As a 2-D address, the lower 12bits of ADDR port defines the X/Column component and the upper 12bits define the Y/Row component See table below. If 2-D addressing is desired** and the line/row length of the data array is 'N', ROW_LENGTH[11:0] must be loaded as 'N'. When linear addressing is required, the ADDR port acts as a 24bit linear address. Setting ROW_LENGTH to 0 causes the incoming address to be interpreted simply as a linear address (or equivalently, a Cartesian address with 4095 pixels per line).

Register 0 = ROW_LENGTH[11:8] (DEFAULT= 0000)

3:0 = ROW_LENGTH[11:8]	Most significant 4 bits of the 12bit ROW_LENGTH

Register 1 = ROW_LENGTH[7:0] (DEFAULT= 00000000)

7:0 = ROW_LENGTH[7:0]	Least significant 8 bits of the 12bit ROW_LENGTH

24bit External Address Mapping

	ADDR[23:12]	ADDR[11:0]
2-D Addresses (non-zero row_length)	Y / Column Address	X / Row Address
24bit Linear Address (row_length of 0)	ADDR[23:0]	

**Application Example) An application requires the LF4430 to store a full frame of standard def D1 video and requires 2-D address mapping (accessing memory locations based on a row/column address defined by the 24bit external address port). The video in this example has 1716 samples per line. ROW_LENGTH should be set to 1716 decimal = 6B4 hex. In order to address Line 255 and Column 511 of the frame, Q1 = 0FF and D1 = 1FF.

Register 2 - 8

Registers 2, 3, 4, 5, 6, 7, 8 = RESERVED

Configuration Register Definitions

Register 9

Detect & Use Embedded TRS Pre-amble

Register 9 [7:6] = TRS_DETECT[1:0] - Detect & Act on Embedded TRS EAV (a)

00	disable auto-TRS sync detection ***(DEFAULT)***
01	V-bit of embedded TRS EAV **CLEARs** current write pointer. See Register 9[5:4].
10	F-bit of embedded TRS EAV **SETs** current write pointer to value set by ADDR
11	F-bit of embedded TRS EAV **CLEARs** current write pointer. See Register 9[5:4].

TRS Trigger Control

Register 9 [5] = TRS_TRIGGER _B - TRS Trigger Control, Chnl B (ONLY for DUAL-CHANNEL)

0	use only falling F/V bit in TRS - FRAME SYNC; otherwise ignore ***(DEFAULT)***
1	use both rising and falling F/V bits in TRS

Register 9 [4] = TRS_TRIGGER - TRS Trigger Control, Chnl A

0	use only falling F-bit in EAV - FRAME SYNC; otherwise ignore ***(DEFAULT)***
1	use both rising and falling F-bit in EAV - FIELD SYNC

Register 9 [3:0] = Reserved [LOAD '0000' IF MODIFYING REG 9]

Register A

Register A [7:6] = Reserved [LOAD '00' IF MODIFYING REG A]

Write/Read Pointer Trigger Control

Register A [5:0] PTR_CNTRL - Individual W/R Pointer Trigger Control

A [5] RSET	0 = Falling edge triggered ***(DEFAULT)***, 1 = Active LOW
A [4] RCLR	0 = Falling edge triggered ***(DEFAULT)***, 1 = Active LOW
A [3] BSET	0 = Falling edge triggered ***(DEFAULT)***, 1 = Active LOW
A [2] BCLR	0 = Falling edge triggered ***(DEFAULT)***, 1 = Active LOW
A [1] ASET	0 = Falling edge triggered ***(DEFAULT)***, 1 = Active LOW
A [0] ACLR	0 = Falling edge triggered ***(DEFAULT)***, 1 = Active LOW

Trigger Control bit = 0: Each falling edge on the corresponding control pin (control signal must still fall within setup/hold spec to associated CLK) overrides memory address counter for exactly one clock cycle, after which normal memory address incrementing immediately resumes.

Trigger Control bit = 1: The corresponding 'active LOW' control pin continuously overrides the memory address counter as long as it is held LOW. Memory address incrementing resumes when the pin is returned HIGH.

NOTE: In Single-Channel modes (MODE=x0xx), the following trigger control pairs must be set the same: WSET0 / WSET1 along with WCLR0 / WCLR0.

Configuration Register Definitions

Register B

Register B [7:0] = Reserved

Register C

Register C [7:4] = BASE_ADDR[3:0] - position of chip in depth expansion; BASE_ADDR[3:0] must not exceed NUM_DEV[3:0]

Depth Expansion: Chip Position

0000:	single-chip operation OR device 1 of N ***(DEFAULT)***
0001:	device 2 of N
.....	device n of N

Register C [3:0] = NUM_CASC_DEV[3:0] - number of devices tied together* for a concatenated address space. (ignore unless performing Depth Expansion)

Depth Expansion: # of Devices

0000:	single device ***(DEFAULT)*** - no depth expansion
0001:	2x depth - two devices; sequential R/W addresses, modulo 7,761,600 (8bit mode)
...	...
1100:	12x depth - twelve devices; sequential R/W addresses, modulo 23,284,800 (8bit mode)

*Note limits on number of possible device connections (related to WIDTH control):

8bit data: 4 or less LF4430s (W = 00)

10bit data: 5 or less LF4430s (W = 01)

12bit data: 6 or less LF4430s (W = 1x)

Register D, E, F

Register D [7:6] Reserved [LOAD '00' IF MODIFYING REG D]

Registers D, E, F = EMPTY_THRESH_0[21:0] - PE0 Programmable threshold for the Partially Empty Flag behavior

EmptyThresh0 is a 22bit constant used to define the emptiness threshold for the PE0 flag. The default is 1/80th of the total memory space in single channel mode. ***See Excel file on logicdevices.com Application Notes area for setting this threshold***. In single channel and cascade modes, the EmptyThresh0 applies. In dual channel mode, this threshold only applies to channel 0's PE flag.

Programamble Empty Flag 0 Definition

Register D= EMPTY_THRESH_0 [21:16] (DEFAULT= 00000)

5:0=EMPTY_THRESH_0 [21:16]	Most significant 6 bits of the 22bit EmptyThresh0

Register E = EMPTY_THRESH_0 [15:8] (DEFAULT= 00000000)

7:0=EMPTY_THRESH_0 [15:8]	Middle byte of the 22bit EmptyThresh0

Register F = EMPTY_THRESH_0 [7:0] (DEFAULT= 00000000)

7:0=EMPTY_THRESH_0 [7:0]	Least significant byte of the 22bit EmptyThresh0

Configuration Register Definitions

Register 10, 11, 12

Programmable Empty Flag 1 Definition

Register 10 [7:2] Reserved [LOAD as '000000' IF MODIFYING REG 10]

Register 10,11,12 = EMPTY_THRESH_1[17:0] - PE1 Programmable threshold for the Partially Empty Flag behavior

EmptyThresh1 is a 18bit constant used to define the emptiness threshold for the PE1 flag. The default is 1/80th of the total memory space of channel 0. In single channel and cascade modes, this threshold is ignored. In dual channel mode, this threshold applies to channel 1's PE flag.

Register 10= EMPTY_THRESH_1[17:16] (DEFAULT= 00)

5:0=EMPTY_THRESH_1[17:16]	Most significant 2 bits of the 18bit EmptyThresh1

Register 11 = EMPTY_THRESH_1[15:8] (DEFAULT= 00000000)

7:0=EMPTY_THRESH_1[15:8]	Middle byte of the 18bit EmptyThresh1

Register 12 = EMPTY_THRESH_1[7:0] (DEFAULT= 00000000)

7:0=EMPTY_THRESH_1[7:0]	Least significant byte of the 18bit EmptyThresh1

Register 13, 14, 15

Programmable Full Flag 0 Definition

Register 13 [7:6] Reserved [LOAD AS '00' IF MODIFYING REG 13]

Register 13,14,15 = FULL_THRESH_0[21:0] - PF0 Programmable threshold for the Partially Full Flag behavior

FullThresh0 is a 22bit constant used to define the fullness threshold for the PF0 flag. The default is 79/80th of the total memory space in single channel mode. In single channel and cascade modes, this threshold applies. In dual channel mode this threshold only applies to channel 0's PF flag.

Register 13= FULL_THRESH_0 [21:16] (DEFAULT= 00000)

5:0=FULL_THRESH_0 [21:16]	Most significant 6 bits of the 22bit FullThresh0

Register 14 = FULL_THRESH_0 [15:8] (DEFAULT= 00000000)

7:0=FULL_THRESH_0 [15:8]	Middle byte of the 22bit FullThresh0

Register 15 = FULL_THRESH_0 [7:0] (DEFAULT= 00000000)

7:0=FULL_THRESH_0 [7:0]	Least significant byte of the 22bit FullThresh0

Configuration Register Definitions

Register 16, 17, 18

Programmable Full Flag 1 Definition

Register 16 [7:2] Reserved [LOAD AS '000000' IF MODIFYING REG 16]

Register 16,17,18 = FULL_THRESH_1[17:0] - PF1 Programmable threshold for the Partially Full Flag behavior

FullThresh1is a 18 bit constant used to define the fullness threshold for the PF0 flag. The default is 79/80th of the total memory space of channel 1. In single channel and cascade modes, this threshold is ignored. In dual channel mode this threshold applies only to channel 1's PF flag.

Register 16= FULL_THRESH_1[17:16] (DEFAULT= 00)

5:0=FULL_THRESH_1[17:16]	Most significant 2 bits of the 18bit FullThresh1

Register 17 = FULL_THRESH_1[15:8] (DEFAULT= 00000000)

7:0=FULL_THRESH_1[15:8]	Middle byte of the 18bit FullThresh1

Register 18 = FULL_THRESH_1[7:0] (DEFAULT= 00000000)

7:0=FULL_THRESH_1[7:0]	Least significant byte of the 18bit FullThresh1

Register 3F

Working Register Update

Register 3F [7:0] = REG_UPDATE - Modified Register Update/Activation - LOAD as '00000000'

***NOTE**: After modifying any of the configuration registers, register 3F must be written with all zeros.*
Writing all ZEROS to Register 3F is *REQUIRED to update the device's operation.*

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
VCC_{INT} , Internal supply voltage with respect to ground	–0.5V to + 4.0V
VCC_O, Output drivers supply voltage with respect to ground	–0.5V to + 4.0V
Signal applied to high impedance output	–0.5V to + 3.3V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Characteristic	Mode	Temperature Range	Supply Voltage
VCC_{INT}	Commerical	0°C to +70°C	$1.71V \leq VCC_{INT} \leq 3.60V$
VCC_O	Commerical	0°C to +70°C	$1.71V \leq VCC_O \leq 3.60V$
VCC_{INT}	Industrial	-40°C to +85°C	$1.71V \leq VCC_{INT} \leq 3.60V$
VCC_O	Industrial	-40°C to +85°C	$1.71V \leq VCC_O \leq 3.60V$

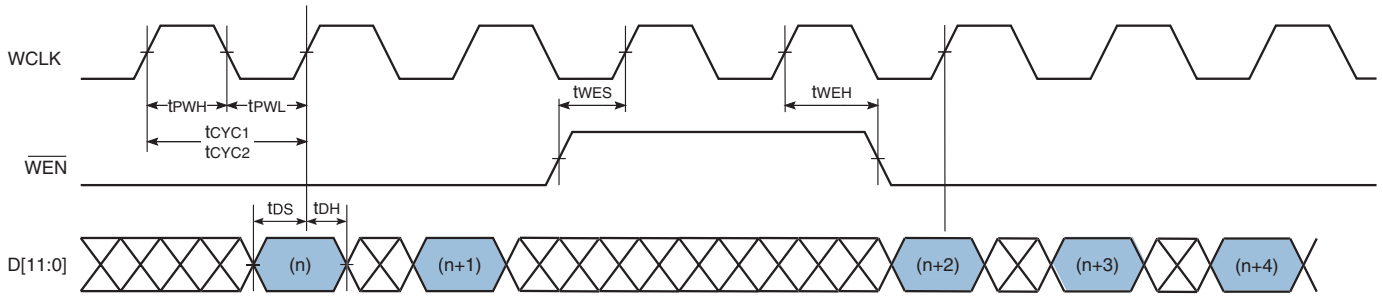
ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH1}	Output High Voltage	V_{CCo} = 3.3V, I_{OH} = -4 mA	2.4			V
V_{OL1}	Output Low Voltage	V_{CCo} = 3.3V, I_{OL} = 4 mA			0.4	V
V_{IH1}	Input High Voltage	V_{CCo} = 3.3V	2.0			V
V_{IL1}	Input Low Voltage	V_{CCo} = 3.3V, (Note 3)			0.8	V
V_{OH2}	Output High Voltage	V_{CCo} = 1.8V, $I_{OH\ MAX}$ = -4 mA	1.6			V
V_{OL2}	Output Low Voltage	V_{CCo} = 1.8V, $I_{OL\ MAX}$ = 4 mA			0.2	V
V_{IH2}	Input High Voltage	V_{CCo} = 1.8V	1.3			V
V_{IL2}	Input Low Voltage	V_{CCo} = 1.8V, (Note 3)			0.36	V
I_{Ix}	Input Current	With Internal Pull-up - JTAG & I2C pins			TBD	µA
I_{Ix}	Input Current	All other pins			TBD	µA
I_{OZ}	Output Leakage Current	Ground $\leq V_{OUT} \leq V_{CC}$ (Note 12)			TBD	µA
I_{CC1a}	V_{CCint} Current, Dynamic	150MHz, 16, 20 or 24-bit full-time addr. override			420	mA
I_{CC1b}	V_{CCint} Current, Dynamic	150MHz, 8,10 or 12-bit full-time addr. override			230	mA
I_{CC1c}	V_{CCint} Current, Dynamic	150MHz, 16, 20 or 24-bit FIFO addressing			100	mA
I_{CC1d}	V_{CCint} Current, Dynamic	150MHz, 8, 10 or 12-bit FIFO addressing			60	mA
I_{CC2}	V_{CCint} Current, Quiescent	150MHz,			35	mA
I_{CC3}	V_{CCo} Current, Dynamic	V_{CCo} =1.96V (Note 6)			116	mA
I_{CC4}	V_{CCo} Current, Quiescent	V_{CCo} =1.96V			90	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			7	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			7	pF
Θ_{JA}	Thermal Resistance	Junction to Ambient (15 x 15mm FBGA)		25		°C/W

Switching Characteristics
Commercial Operating Range (0°C to +70°C) Notes 9, 10 (ns)

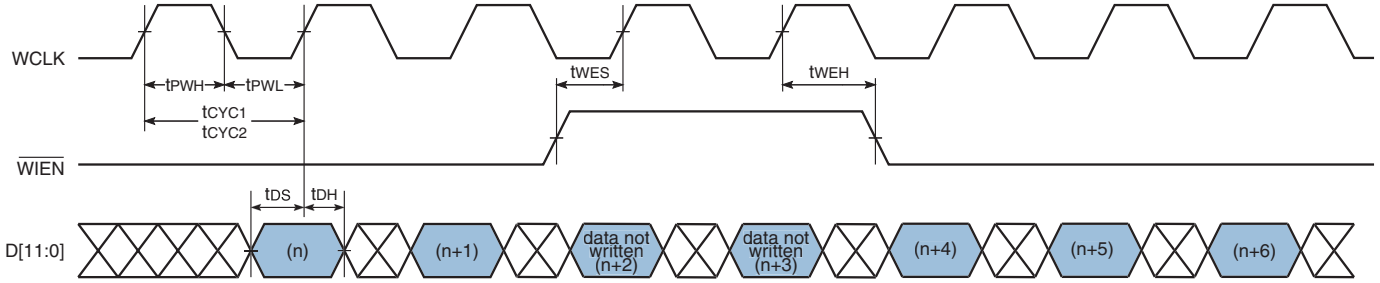
		LF4415		LF4430		LF4460	
		150MHz		150MHz		150MHz	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{CYC1}	Cycle Time 1 (WCLKx,RCLK)	6.6		6.6		6.6	
t_{PWH}	Clock Pulse Width High (WCLKx,RCLK)	TBD		TBD		TBD	
t_{PWL}	Clock Pulse Width Low (WCLKx,RCLK)	TBD		TBD		TBD	
t_{DS}	Setup Time, Data Inputs (Dx)	TBD		TBD		TBD	
t_{DH}	Hold Time, Data Inputs (Dx)	TBD		TBD		TBD	
t_{WES}	Write Enable Setup Time (WENx)	TBD		TBD		TBD	
t_{WEH}	Write Enable Hold Time (WENx)	TBD		TBD		TBD	
t_{RES}	Read Enable Setup Time (RENx)	TBD		TBD		TBD	
t_{REH}	Read Enable Hold Time (RENx)	TBD		TBD		TBD	
t_{RWS}	R/W Set/Clr Setup Time (WCLRx,WSETx,RSET,RCLR)	TBD		TBD		TBD	
t_{RWH}	R/W Set/Clr Hold Time (WCLRx,WSETx,RSET,RCLR)	TBD		TBD		TBD	
t_D	Access Time		TBD		TBD		TBD
t_F	Clock to Programmable Flags (PEx,PFx,COLLIDEx)		TBD		TBD		TBD
t_{DIS}	Tri-state Output Disable Delay		TBD		TBD		TBD
t_{ENA}	Tri-state Output Enable Delay		TBD		TBD		TBD

Figure 10 - Write Cycle Timing - Write Enable



NOTE: $\overline{WIEN}$ = LOW

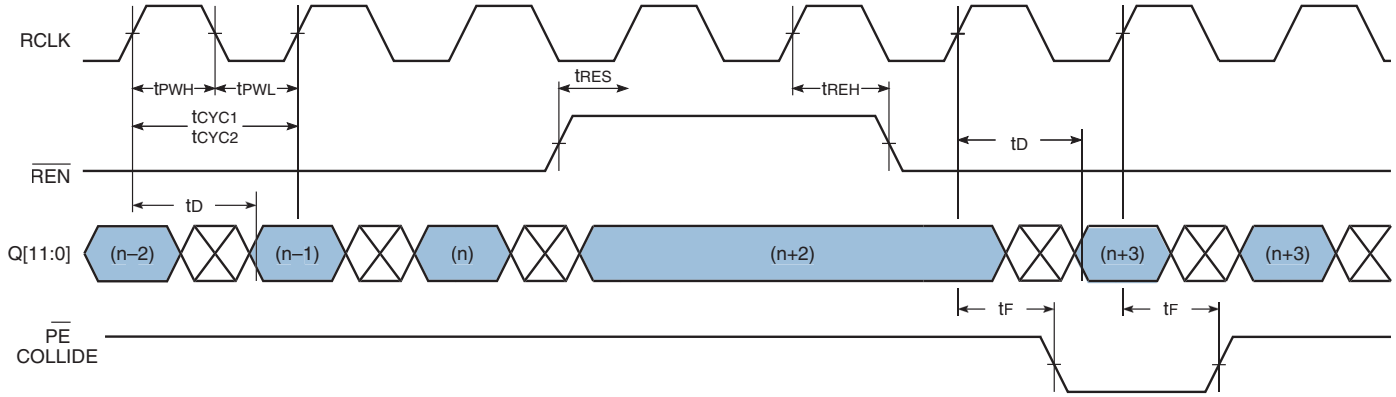
Figure 11 - Write Cycle Timing - Write Masking



$\overline{WEN}$ = LOW

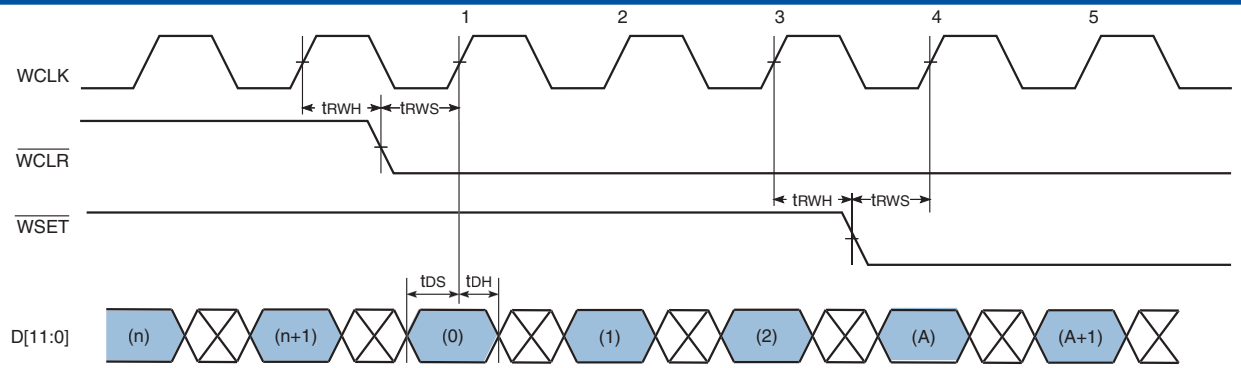
NOTE: While bringing WIEN HIGH disables writes into memory, the write pointer continues to increment if WEN is LOW

Figure 12 - Read Cycle Timing



$\overline{OE}$ = LOW

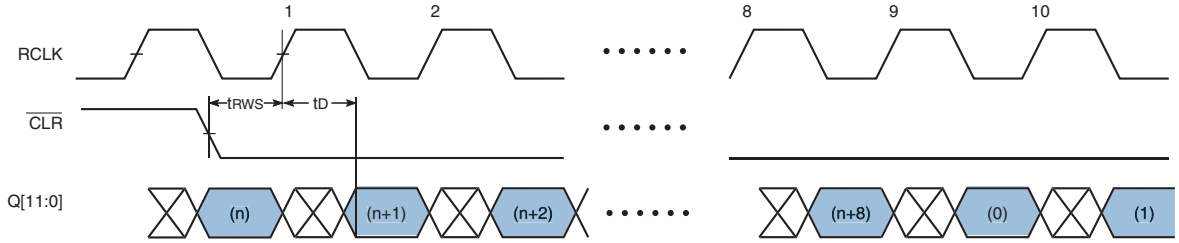
Figure 13 - Write Pointer 'Clear' and 'Set' Timing



$\overline{WEN}$ = LOW
CLR and SET both programmed to be falling edge sensitive

* Rising Edge 1: Clears Write Pointer and latches data on D to be written in address 0
* Rising Edge 4: Sets Write Pointer to Address A (based on WADDR) and latches data on D to be written in Address A

Figure 14 - Read Pointer 'Clear' Timing

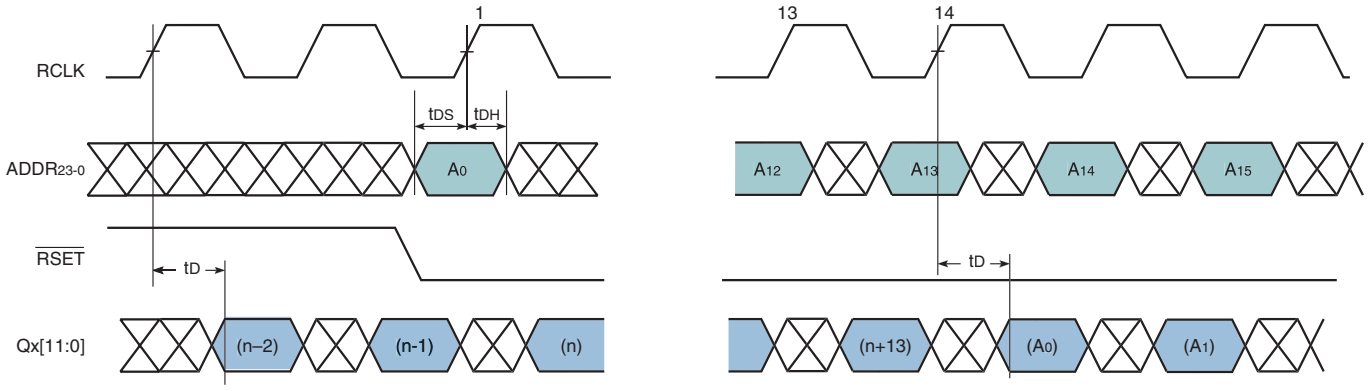


$\overline{REN}$ = LOW

NOTE: CLR programmed as being falling edge sensitive

It takes 9 REN-enabled rising edges of RCLK (including the edge that latches a LOW on CLR) to pass the contents of address 0 to the Q port.

Figure 15 - Read Pointer Full-Time Override using 24bit External Address

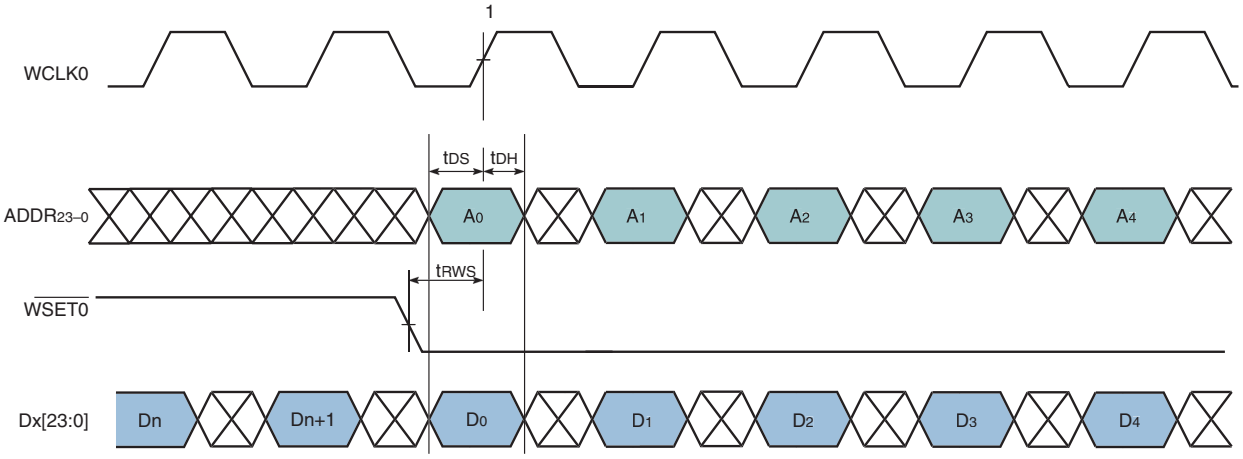


$\overline{OE}$ = LOW $\overline{REN}$x = LOW RDWR = HIGH MODE=x0xx

NOTE: RSET programmed to be active LOW (full-time read address override)

NOTE: It takes 14 rising edges of RCLK upon setting/jumping the Read pointer
(to the 24bit Address "A0" on ADDR) for the contents of location A0 to be dumped onto Q

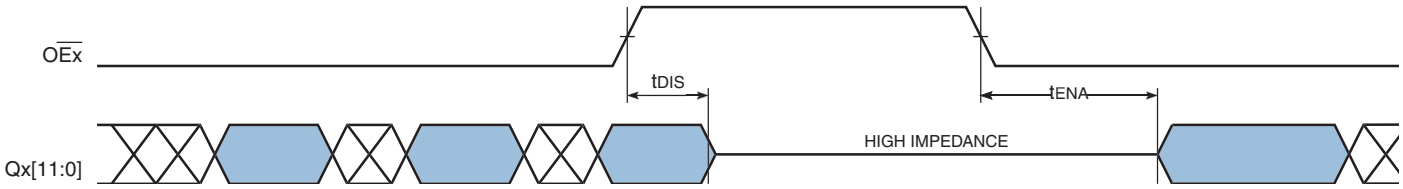
Figure 16 - Write Pointer Override using 24bit External Address Port



$\overline{WEN}$= LOW RDWR = LOW MODE= x0xx

NOTE:
- WSET programmed to be active LOW (full-time write pointer override
- D0 will be written to Address 0, D1 to Address 1, etc...

Figure 17 - Output Enable and Disable



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at TDBV.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. I/O Ring supply power for a given application can be approximated by:

$$\frac{NCV^2F}{2}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with 30 output pins driving 10pF loads, while toggling at an average of 30% of the 150MHz clock rate at 1.96V. This number will change depending on VCCo level. The 10pF load is estimate of trace and downstream pin capacitance.

7. These parameters are guaranteed but not 100% tested.

8. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{dis} test), and input levels of nominally 0 to 3.0V(when using 3.3V IO voltage). Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used (when using 3.3V IO voltage). Parasitic capacitance is 30 pF minimum, and may be distributed.

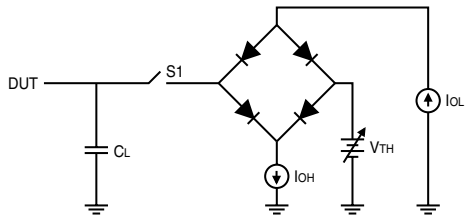
9. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

10. For the t_{ena} test, the transition is measured to the 50% crossing point with datasheet loads. For the t_{dis} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±datasheet loads. The balancing voltage, V_{th}, is set at VCCo min for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

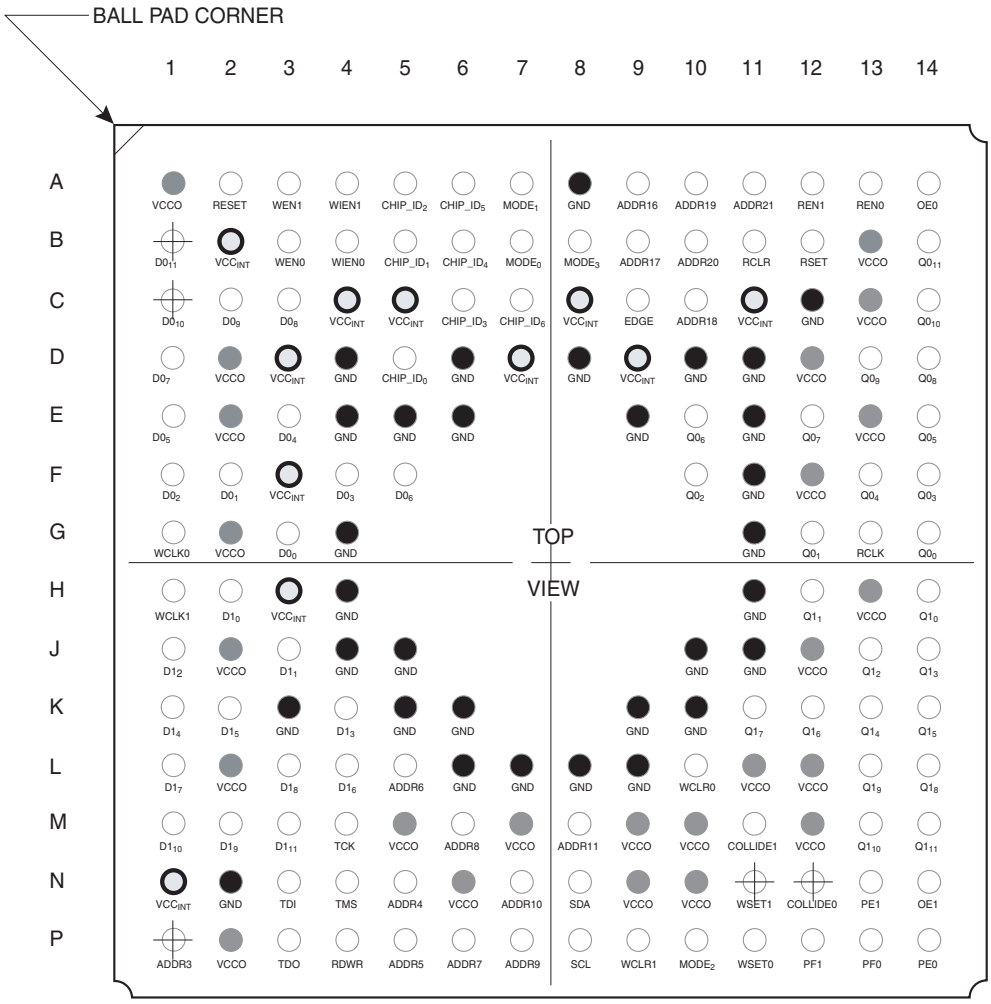
11. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

Notes

FIGURE A. OUTPUT LOADING CIRCUIT



Pin Configuration and Ordering Information



172 Ball FBGA (Refer to Mechanical Drawing MD-BG2)

Ordering Information

Speed (MHz)	Ordering Code	Package Type	Operating Range
150	LF44xxBC-150	15 x 15 x 1.4 FBGA	Commercial 0°C to +70°C
150	LF44xxBI-150	15 x 15 x 1.4 FBGA	Industrial -40°C to +85°C

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Document History Page

DOCUMENT TITLE: LF44XX VIDEO MEMORY / FIFO DATASHEET			
Rev.	ECN #	Issue Date	Description of Change
A	C00040	1/29/08	Initiate