Programmable Linear Hall IC with Advanced Diagnostics for Safety-Critical Applications

FEATURES AND BENEFITS

- High-speed analog, A-to-D converter (ADC), and digital architectures, enabling user-selectable bandwidth for speed-sensitive applications
  - □ 4-phase chopper stabilization, which minimizes offset drift across temperature range
  - □ 16-bit, high update rate ADC
- Automotive AEC-Q100 qualified
- Exceptional stability throughout lifetime and across temperature changes
  - □ Factory-configured using multisegment temperature compensation to give a flat baseline across operating temperature range
  - □ Customer configurability for 1st and 2nd order sensitivity and 1st order offset compensation across temperature range
  - □ Integrated feedback coil compensates for drift throughout product lifetime

Continued on the next page…

PACKAGE:

3-pin SIP (suffix UC)

Not to scale

DESCRIPTION

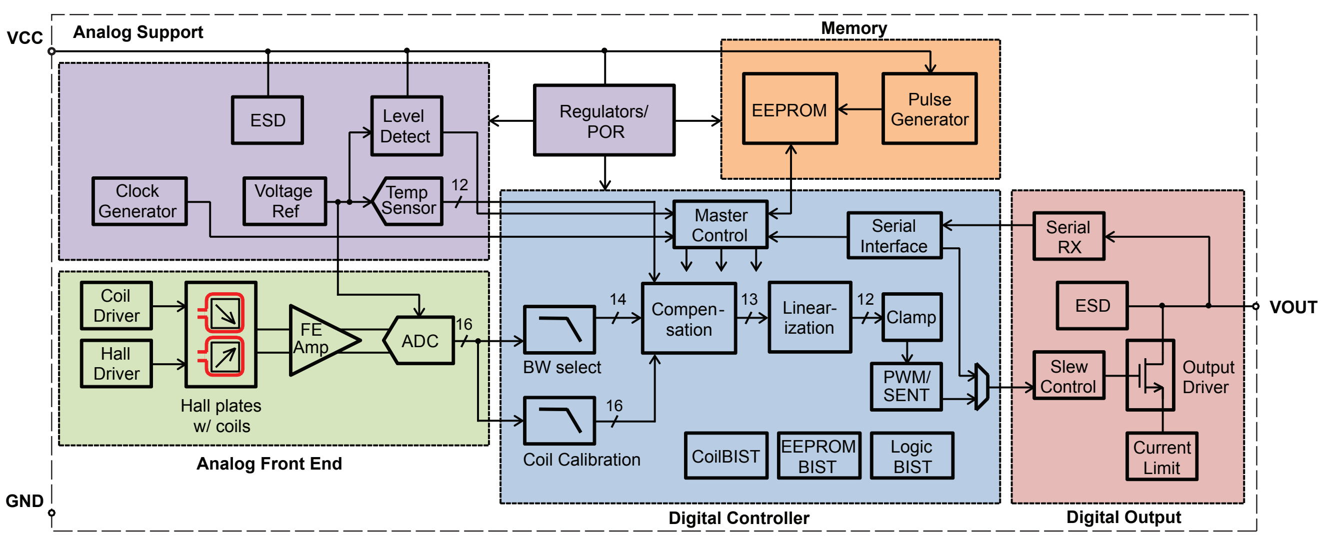
The A1342 device is a high-precision, programmable Hall-effect linear sensor integrated circuit (IC) with an open-drain output, for both automotive and nonautomotive applications. The signal path of the A1342 provides flexibility through external programming that allows the generation of an accurate, and customized, output from an input magnetic signal.

The A1342 is an especially configurable and robust solution for the most demanding linear field sensor applications. The BiCMOS, monolithic IC incorporates a Hall sensing element, precision temperature-compensating circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element, a small-signal high-gain amplifier, proprietary dynamic offset cancellation circuits, advanced output linearization circuitry, and advanced diagnostics. The A1342 provides an unmatched level of customer-programmable options.

A key feature of the A1342 is its ability to produce a highly linear device output for nonlinear input magnetic fields. To achieve this, the device features 16-segment customer-programmable linearization, where a unique linearization coefficient factor is applied to each segment. Linearization coefficients are stored in a look-up table in EEPROM.

The A1342 has two configurable output options: SENT or PWM. In addition to SAEJ2716, the A1342 includes two additional proprietary SENT options: SSENT and ASENT. Both protocols enable bus configurations with up to four devices on one SENT line to reduce system costs. SSENT provides sequential

Continued on the next page…



Functional Block Diagram

Description (continued)

access to the sensors connected to the same line. SSENT provides a very low overhead method to maximize the sensor bandwidth on this single SENT line, minimizing impact on system performance. ASENT provides random access to all the sensors on the common SENT line. Both protocols allow individual sensors on the same line to enter diagnostic mode while the other sensors continue to respond to queries, allowing for the highest diagnostic coverage while maintaining 100% availability of the sensor solution.

The A1342 is available in a through-hole, lead (Pb) free 3-pin SIP package (UC suffix), with 100% matte-tin leadframe plating.

Features and Benefits (continued)

- Wide operating flexibility to meet any application:
  - □ Input field range up to ±1500 G
  - □ Rail to negative rail offset configurability
  - □ High-precision, full output range high and low clamps
  - □ Integrated linearization allows for flexible output waveform translation and compensation for nonlinear magnetic inputs
  - □ Integrated capacitors offer extremely robust ESD performance and enhanced EMC performance
- Advanced diagnostic-focused features enabling easier system-level ASIL compliance
  - □ Full data path validation through active front-end stimulation with internal magnetic coil; this method validates all relevant transistors for device operation
  - □ Logic Built-In Self Test (LBIST) on-demand to validate the digital subsystem
  - □ Large suite of configurable fault monitors provide system level fault detection, including:
    - ♦ Overvoltage or undervoltage
    - ♦ Overtemperature
    - ♦ Magnetic Field Out of Range detection
    - ♦ Broken wire detection
- Flexible output protocols with up to 12-bit resolution and configurable error notifications
  - □ Digital open-drain output allows for flexible output voltage levels
  - □ PWM (Pulse-Width-Modulated) output with diagnostic output mode to identify fault conditions
  - □ SENT (Single Edge Nibble Transmission) compliant output with configurable reporting of error conditions and other diagnostic information
  - □ Proprietary Fast SENT provides increased data rates to support high-bandwidth applications
  - □ Device-shared SENT protocol as SSENT (Sequential SENT) and ASENT (Addressable SENT) allows user to connect up to four devices on the same output line for faster communication.
  - □ Enhanced EMC tuning through programmable fall-time configurability
- Integrated EEPROM enables a high level of configurability and product traceability
  - □ Customer-reserved area allows on-board storage of unique lot and date code information
  - □ Robust EEPROM with Single Error Correction and Double Error Detection (SECDED) capability
  - □ Integrated charge pump allows in-application programming without any requirement for high voltages to be supplied to the device during programming

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SELECTION GUIDE

Part Number	Packing [1]
A1342LUCTN-T	4000 pieces per 13-in. reel

[1] Contact Allegro™ for additional packing options

Table of Contents

Functional Block Diagram 1
Specifications 4
Absolute Maximum Ratings 4
Thermal Characteristics 4
Pinout Diagram and Terminal List 4
Operating Characteristics 5
Magnetic Characteristics 7
Accuracy Characteristics 8
Programmable Characteristics 9
Application Information 10
Signal Path 11
Compansation Block 11
Linearization 12
Post-Linearization Trim 14
Clamp 14
Diagnostic Conditions 15
Diagnostic Modes 15
Diagnostic Configuration 15
Analog Signal Path 15
BIST 16
ADC Overflow 17
Undervoltage Detection and Reset 17
Broken Ground Detection 17
EEPROM Diagnostics 17
Linear Output Protocols 18
PWM Output Mode (outmsg_mode = 0) 18
SENT Output Modes 20
Message Structure 20
Optional Short Serial Message 21
Data Nibble Format 21
Checksum (CRC) Nibble 22
Output Driver Fall Time Selection 22
SAEJ2716 SENT and TSENT 24
SSENT Addressing Protocol 27
SSENT Function Pulses 28
ASENT Addressing Protocol 30
ASENT Function Pulses 31
Serial Communication 31
Programming Information 32
Serial Interface Message Structure 35
Read and Write Transmission 36
CRC 36
Customer Factory Access 37
Customer Memory Lock 37
EEPROM Margin Checking 37
Memory Address Map 38
Programmable Parameter Reference 43
Package Outline Drawing 47

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

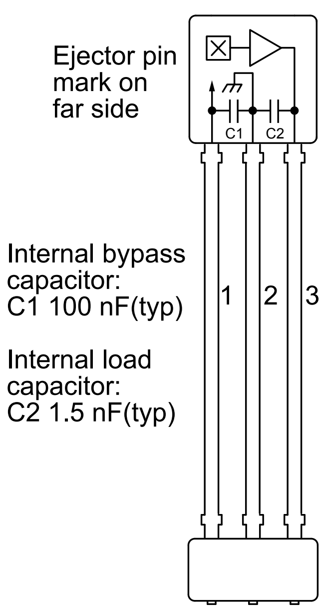
Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		20	V
Reverse Supply Voltage	V_{RCC}		–16	V
Forward Supply Current	I_{CC}		30	mA
Reverse Supply Current	I_{RCC}		–30	mA
Forward Output Voltage	V_{OUT}		20	V
Reverse Output Voltage	V_{ROUT}		–1	V
Output Short-Circuit Current	$I_{OUTSC(SINK)}$	V_{CC} to V_{OUT}, 4.5 V < V_{CC} < 5.5 V	–20	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	1-layer PCB with copper limited to solder pads	201	°C/W

[1] Additional thermal information available on the Allegro website.

PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package UC, 3-Pin SIP Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCC	Input power supply [2]
2	GND	Ground
3	VOUT	Output signal

[2] Allegro offers LDOs well-suited for regulated sensor applications. For available devices, visit www.allegromicro.com/en/Products/Regulators-And-Lighting/Single-Output-Regulators, or contact your local Allegro sales representative.

ALLEGRO microsystems
Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPERATING CHARACTERISTICS: Valid T_A and V_{CC}, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	Compensation coil off	–	–	10	mA
Peak Supply Current	$I_{CC(pk)}$	Compensation coil on	–	–	16	mA
Reverse Supply Current	I_{RCC}	V_{CC} = –16 V, T_A = 25°C	–3	–	–	mA
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	I_{CC} = 13 mA, compensation coil off, T_A = 25°C	20	–	–	V
Chopping Frequency	f_C	T_A = 25°C, compensation coil off	–	128	–	kHz
		T_A = 25°C, compensation coil on	–	64	–	kHz
Oscillator Frequency	f_{OSC}	T_A = 25°C	6963	8192	9421	kHz
Undervoltage Detection Threshold	$V_{CC(UV)LOW}$	V_{CC} falling, see Figure 1	4	–	4.35	V
	$V_{CC(UV)HIGH}$	V_{CC} rising, see Figure 1	4.05	–	4.4	V
Power-On-Reset Threshold	$V_{CC(POR)LOW}$	V_{CC} falling, see Figure 1	3.4	–	3.8	V
	$V_{CC(POR)HIGH}$	V_{CC} rising, see Figure 1	3.5	–	3.9	V
Overvoltage Detection Threshold	$V_{CC(OV)LOW}$	V_{CC} falling, see Figure 1	6.6	–	7.4	V
	$V_{CC(OV)HIGH}$	V_{CC} rising, see Figure 1	6.7	–	7.6	V
High-Voltage Threshold	$V_{CC(HV)LOW}$	V_{CC} falling, see Figure 1	15	–	–	V
	$V_{CC(HV)HIGH}$	V_{CC} rising, see Figure 1	–	–	17	V
OUTPUT CHARACTERISTICS						
Bandwidth [1]	BW	bw_sel_c = 0	–	40	–	Hz
		bw_sel_c = 1	–	160	–	Hz
		bw_sel_c = 2	–	680	–	Hz
		bw_sel_c = 3	–	3000	–	Hz
		bw_sel_c = 4-7	–	7400	–	Hz
Noise (Peak-to-Peak) [2]	$OUT_{N(PK-PK)}$	bw_sel_c = 0, T_A = 25°C, coil_freq = 0, coilcomp_dis = 0, bw_sel_comp_c = 0	–	0.32	–	G
		bw_sel_c = 1, T_A = 25°C, coil_freq = 0, coilcomp_dis = 0, bw_sel_comp_c = 0	–	0.50	–	G
		bw_sel_c = 2, T_A = 25°C, coil_freq = 0, coilcomp_dis = 0, bw_sel_comp_c = 0	–	0.93	–	G
		bw_sel_c = 3, T_A = 25°C, coil_freq = 0, coilcomp_dis = 0, bw_sel_comp_c = 0	–	1.74	–	G
		bw_sel_c = 4, T_A = 25°C, coil_freq = 0, coilcomp_dis = 0, bw_sel_comp_c = 0	–	2.85	–	G
Output Leakage Current	I_{OUT}	Output voltage ≤ 5.5 V, output FET off	–	–	100	µA
Output Load Resistance	$R_{L(PULLUP)}$	Output current ≥ –10 mA	1.2	–	–	kΩ
Output Saturation Voltage	$V_{OUT(Sat)LOW}$	Output current = –4.7 mA, V_{CC} = 5 V, Output FET on	–	–	0.35	V
Output Current Limit	I_{LIMIT}	Output FET on, T_A = 25°C	20	30	50	mA
Output Zener Clamp Voltage	V_{ZOUT}	T_A = 25°C, output current = –3 mA	20	–	–	V
Internal Load Capacitor [3]	C_{LI}	T_A = 25°C	–	1.5	–	nF
External Load Capacitor	C_{LX}		–	–	4.7	nF

Continued on the next page…

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPERATING CHARACTERISTICS (continued): Valid T_A and V_{CC}, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Response Time [4]	t_{resp}	bw_sel_c = 4-7	–	0.15	–	ms
		bw_sel_c = 3	–	0.25	–	ms
		bw_sel_c = 2	–	0.69	–	ms
		bw_sel_c = 1	–	2.4	–	ms
		bw_sel_c = 0	–	9.3	–	ms
Power-On Time [4]	t_{PO}	bw_sel_c = 4-7	–	0.6	–	ms
		bw_sel_c = 3	–	0.75	–	ms
		bw_sel_c = 2	–	1.25	–	ms
		bw_sel_c = 1	–	3.7	–	ms
		bw_sel_c = 0	–	13	–	ms
Output Jitter, PWM [1]	PWM_{JIT}	outmsg_mode = 0, SENT_PWM_RATE < 2 kHz	–1	–	1	LSB
		outmsg_mode = 0, SENT_PWM_RATE ≥ 2 kHz	–3	–	3	LSB
Output, Integral Nonlinearity	INL	outmsg_mode = 0, SENT_PWM_RATE < 2 kHz	–	±0.5	–	%FSO
Maximum Output Resolution [5]	OUT_{RES}	T_A = 25°C, outmsg_mode = 1-5	–	12	–	bit
		T_A = 25°C, outmsg_mode = 0, SENT_PWM_RATE ≤ 2 kHz	–	12	–	bit
PWM Carrier Frequency [6]	f_{PWM}		–15	–	15	%

[1] Determined from design characterization; not tested in production.
[2] Noise (Peak-to-Peak) calculated as 6 sigma (6 standard deviations) from characterization of a small sample of devices. Conversion of noise from gauss to LSB can be done by: Noise (G) × Sensitivity (LSB/G) = Noise (LSB)
[3] Capacitor internal to device package between VOUT and GND. Capacitor specifications are determined by the manufacturer.
[4] Defined as time before magnetic data is 90% of the settled value.
[5] When outmsg_mode = 0, the maximum output resolution decreases to 11 – n (bits) for SENT_PWM_RATE = 2 kHz × 2^n.
[6] PWM carrier frequency accuracy is % of the programming target. See programmable parameter reference for PWM carrier frequency programming options.

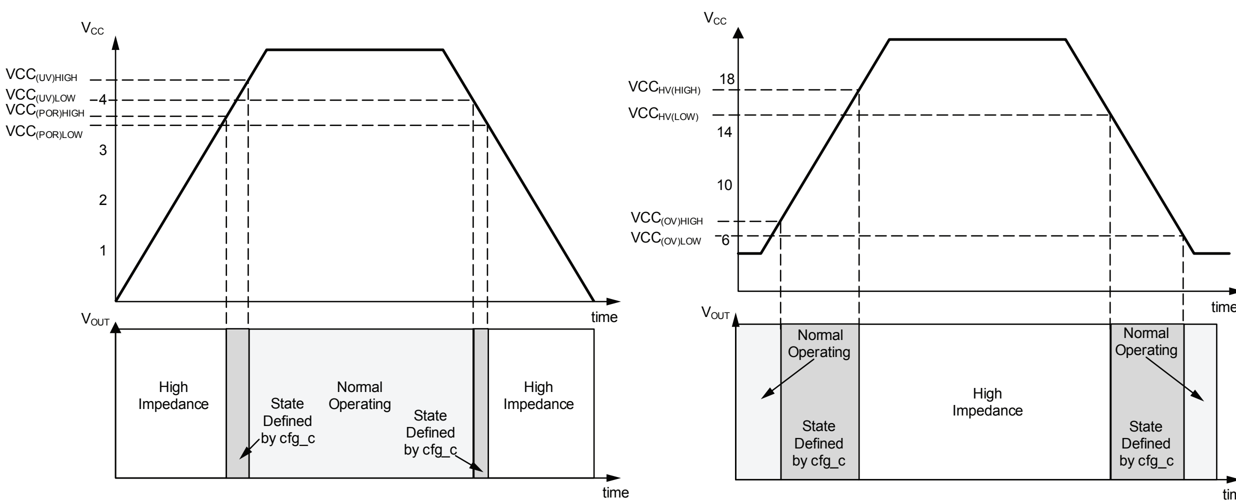


Figure 1: V_{CC} Thresholds and Resultant Output States

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

MAGNETIC CHARACTERISTICS: Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1][2]
Input Field Range	B_{IN}		–1500	–	1500	G
Initial Sensitivity	$SENS_{INIT}$		–	0.0333	–	%FSO/G
Initial Quiescent Output	QO_{INIT}		–	50	–	%FSO
Initial Output Clamp	$OUT_{CLP(L)INIT}$	clampl = 0, outmsg_mode = 1-5	–	0	–	LSB
		clampl = 0, outmsg_mode = 0	–	2	–	%D
	$OUT_{CLP(H)INIT}$	clamph = 0, outmsg_mode = 1-5	–	4095	–	LSB
		clamph = 0, outmsg_mode = 0	–	98	–	%D

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] *FSO* means Full Scale Output. See Definitions of Terms section.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ACCURACY CHARACTERISTICS: Valid at T_A and V_{CC}, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1,2]
Lifetime Sensitivity Drift	$\Delta SENS_{LIFE}$	Variation on final programmed Sensitivity value; T_A = 25°C coilcomp_dis = 0; shift after AEC-Q100 grade 0 qualification testing; measured at T_A = 25°C	–	<±1.5	–	%
		Variation on final programmed Sensitivity value; T_A = 25°C coilcomp_dis = 1; shift after AEC-Q100 grade 0 qualification testing; measured at T_A = 25°C	–	<±2.5	–	%
Sensitivity Drift Due To Package Hysteresis	$\Delta SENS_{PKG}$	Variation on final programmed Sensitivity value; measured at T_A = 25°C after temperature cycling from 25°C, coilcomp_dis = 0	–	<±0.5	–	%
		Variation on final programmed Sensitivity value; measured at T_A = 25°C after temperature cycling from 25°C, coilcomp_dis = 1	–	<±2.0	–	%
Sensitivity Drift Over Temperature[1]	$\Delta SENS$	25°C ≤ T_A ≤ 150°C, coil compensation on	–1.5	–	1.5	%
		–40°C ≤ T_A ≤ 25°C, coil compensation on	–2	–	2	%
		25°C ≤ T_A ≤ 150°C, coil compensation off	–1	–	1	%
		–40°C ≤ T_A ≤ 25°C, coil compensation off	–1.5	–	1.5	%
Quiescent Output Drift[2]	ΔQO	SENS = $SENS_{INIT}$	–1.32	–	1.32	G

[1] Does not include drift over lifetime and package hysteresis.
[2] Quiescent Output Drift scales with Sensitivity.

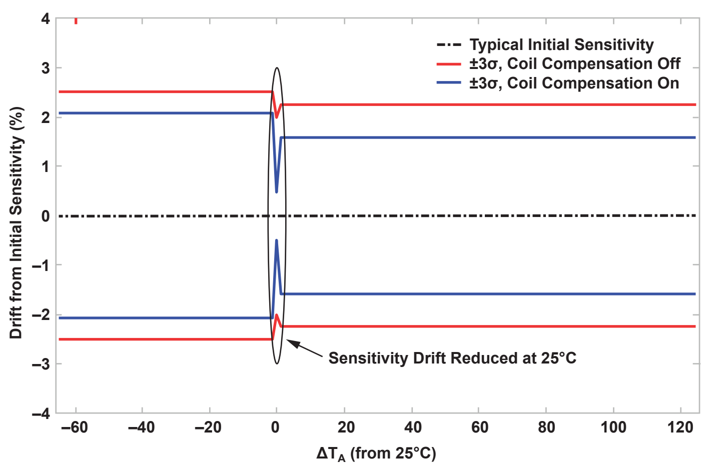


Figure 2: Typical Initial Sensitivity Drift Due To Temperature and Package Hysteresis

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PROGRAMMABLE CHARACTERISTICS: Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
SENSITIVITY						
Output Sensitivity Trim Range [2]	SENS		0.5	–	48	–
Bits Sensitivity Trim, Coarse	Bit (SENSM_C)		–	3	–	bit
Sensitivity Coarse Trim Range [3]	SENSM_C		1	–	32	–
Bits Sensitivity Trim, Fine	Bit (SENS_C)		–	11	–	bit
Sensitivity Fine Trim Range [4]	SENS_C		0.5	–	1.5	–
Bits Sensitivity Polarity	Bit (POL)		–	1	–	bit
OFFSET (QUIESCENT OUTPUT)						
Bits Quiescent Output Trim, Fine	Bit (QO_C)		–	16	–	bit
Customer Quiescent Output Fine Trim Range	QO_C		–32768	–	32767	LSB
CLAMPS (HIGH AND LOW OUTPUT CLAMPS)						
Bits Output Low Clamp	Bit ($OUT_{CLP(LOW)}$)		–	12	–	bit
Output Low Clamp Range	$OUT_{CLP(LOW)}$		0	–	4095	LSB
Bits Output High Clamp	Bit ($OUT_{CLP(HIGH)}$)		–	12	–	bit
Output High Clamp Range	$OUT_{CLP(HIGH)}$		0	–	4095	LSB
TEMPERATURE COMPENSATION						
Bits 1st Order Sensitivity TC	Bit (SENSTC1)	senstc1_hot_c, senstc1_cld_c	–	11	–	bit
1st Order Sensitivity TC Range	SENSTC1	25°C < T_A ≤ 150°C	–0.391	–	0.391	% / °C
		–40°C ≤ T_A < 25°C	–0.781	–	0.781	% / °C
Bits 2nd Order Sensitivity TC	Bit (SENSTC2)	senstc2_hot_c, senstc2_cld_c	–	10	–	bit
2nd Order Sensitivity TC Range	SENSTC2	25°C < T_A ≤ 150°C	–1.5	–	1.5	m% / °C²
		–40°C ≤ T_A < 25°C	–6	–	6	m% / °C²
Bits 1st Order Offset TC	Bit (QOTC)	qotc_hot_c, qotc_cld_c	–	12	–	bit
1st Order Offset TC Range	QOTC	25°C < T_A ≤ 150°C	–32	–	31.98	LSB / °C
		–40°C ≤ T_A < 25°C	–64	–	63.97	LSB / °C

Continued on the next page…

PROGRAMMABLE CHARACTERISTICS (continued): Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
LINEARIZATION						
Linearization Positions			–	17	–	data point
Bits Linearization Coefficients	Bits (LIN_{COEF})		–	12	–	bit
Bits Post Linearization Sensitivity Trim	Bits (PLIN_SENS)		–	12	–	bit
Post Linearization Sensitivity Trim Range	PLIN_SENS (RANGE)		–	±1	–	–
Bits Post Linearization Offset Trim	Bits (PLIN_QVO)		–	12	–	bit
Post Linearization Offset Trim Range	PLIN_QVO (RANGE)		–2048	–	2047	LSB
Bit Linearization Output Polarity	Bits (POL_{OUT})		–	1	–	bit
Bit Linearization Input Polarity	Bits (POL_{IN})		–	1	–	bit

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] The Initial Sensitivity is adjustable by the Sensitivity Trim Coarse and Fine parameters. When reducing the initial Sensitivity check the input field is within the range specified by B_{IN}.
[3] Sensitivity Coarse Trim is a multiplier to the initial Sensitivity with step sizes defined by the sensm parameter. Refer to the Programmable Parameter Reference section for more information.
[4] Sensitivity Fine Trim is a multiplier applied to the initial Sensitivity after the Sensitivity Coarse Trim with step sizes defined by the sens_c parameter. Refer to the Programmable Parameter Reference section for more information.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION

Signal Path

The A1342 contains a Hall-effect transducer that produces a signal proportional to the magnetic flux density perpendicular to the face of the package, referred as the applied magnetic flux density. The output of the Hall transducer is then amplified and digitized. The resulting signal is a signed digital value that can be scaled, offset, and compensated to achieve a desired output. The advanced digital parameters allow for a large range of input signals to be adjusted for the application. This results in the A1342 being highly flexible and accurate for applications with challenging sensing requirements. The following sections give an overview of digital signal path blocks and the corresponding transfer functions.

COMPENSATION BLOCK

The compensation block contains adjustments to the Sensitivity and Offset. This includes compensation for input signal changes over the operating temperature range. First, the Sensitivity Trim Block multiplies the signal by a temperature-dependant gain (or attenuation) factor. The correction is segmented into two regions: hot and cold, where hot indicates ambient temperatures greater or equal to 25 °C, and cold indicates ambient temperatures lesser or equal to 25 °C. Each segmented region also contains 1st and 2nd order Sensitivity temperature compensation.

Note:
The hot Sensitivity temperature compensation is independent of the cold region.

Equations 1 and 2 show the transfer function of the Sensitivity Trim Block.

$$Y_1 = B_{IN} \cdot SENS_{INIT} \cdot POL\_C \cdot SENSM\_C \cdot SENS\_C \cdot \left[1 + \left(\left(\frac{SENSTC2\_HOT\_C}{1000}\right) \cdot \Delta T_A + SENSTC1\_HOT\_C\right) \cdot \frac{\Delta T_A}{100}\right] \quad (1)$$

$$Y_1 = B_{IN} \cdot SENS_{INIT} \cdot POL\_C \cdot SENSM\_C \cdot SENS\_C \cdot \left[1 + \left(\left(\frac{SENSTC2\_CLD\_C}{1000}\right) \cdot \Delta T_A + SENSTC1\_CLD\_C\right) \cdot \frac{\Delta T_A}{100}\right] \quad (2)$$

NOTE:
Included in the transfer function shown in Equations 1 and 2 is the conversion from the applied magnetic input to a digital value, $B_{IN} \times SENS_{INIT}$.

The output of the Sensitivity Trim Block, Y_1, is a 17-bit signed integer.

The Offset Trim Block adds a temperature-dependent factor to the input signal. The offset factor is segmented into two region: hot and cold, as defined in the Sensitivity Trim Block. Each segment contains 1st order Offset temperature compensation. Equations 3 and 4 show the transfer functions of the Offset Trim Block. The output, Y_2, is a 13-bit signed integer and is the value passed out of the Compensation Block.

$$Y_2 = Y_1 + QO\_C + QOTC\_HOT\_C \times \Delta T_A \quad (3)$$

$$Y_2 = Y_1 + QO\_C + QOTC\_CLD\_C \times \Delta T_A \quad (4)$$

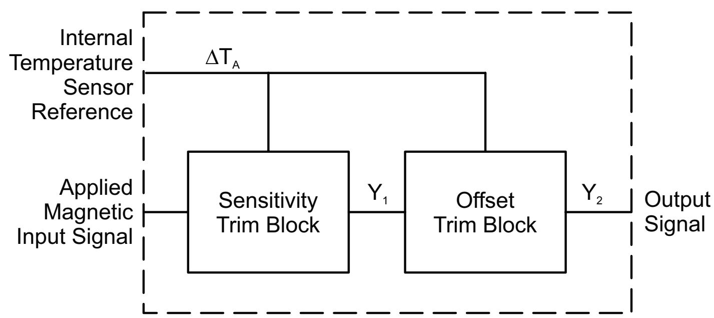


Figure 3: Compensation Block

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 1: Compensation Block Parameters

Variable	Description	Programmable Parameter (Memory Location)	Units
POL_C	Determines the sensitivity polarity. The default polarity is increasing with output with increasing applied south magnetic flux density.	pol_c (Register sens_trim_c 0x3 [15])	NA
SENSM_C	Coarse Sensitivity multiplier	sensm_c (Register sens_trim_c 0x3 [14:12])	NA
SENS_C	Fine Sensitivity multiplier	sens_c (Register sens_trim_c 0x3 [10:0])	NA
SENSTC2_HOT_C	2nd order Sensitivity temperature compensation for $T_A \geq 25°C$	senstc2_hot_c (Register senstc2_c 0x5 [9:0])	$m\%/°C^2$
SENSTC1_HOT_C	1st order Sensitivity temperature compensation for $T_A \geq 25°C$	senstc1_hot_c (Register senstc1_c 0x4 [10:0])	%/°C
SENSTC2_CLD_C	2nd order Sensitivity temperature compensation for $T_A \leq 25°C$	senstc2_cld_c (Register senstc2_c 0x5 [21:12])	$m\%/°C^2$
SENSTC1_CLD_C	1st order Sensitivity temperature compensation for $T_A \leq 25°C$	senstc1_cld_c (Register senstc1_c 0x4 [22:12])	%/°C
ΔT_A	Change in ambient temperature, equal the ambient temperature, T_A, minus 25°C.	NA	°C
QO_C	Fine quiescent output adjustment	qo_c (Register qo_trim_c 0x6 [15:0])	LSB
QOTC_HOT_C	1st order quiescent output temperature drift compensation.	qotc_hot_c (Register qotc_c 0x7 [11:0])	LSB/°C
QOTC_CLD_C	1st order quiescent output temperature drift compensation.	qotc_cld_c (Register qotc_c 0x7 [23:12])	LSB/°C
$SENS_{INIT}$	Initial Sensitivity	NA	LSB/G
B_{IN}	Applied magnetic flux density	NA	G

LINEARIZATION

The Linearization block passes the output from the compensation block through a piecewise-linear transfer described by 17 points, which define 16 line segments. The *x*-coordinates of these points are programmable and are stored as 12-bit words in a table in memory, LIN_C. Corresponding y-coordinates are fixed and are equally spaced over the output range. For proper operation, table increasing entries, i.e., $x_0 \leq x_1 \leq x_2 \leq ... \leq x_{16}$ should be satisfied. If not satisfied, the output is undefined. Adjacent table entries can be equal. The linearization algorithm will not produce output values in between the *y*-coordinates that correspond to identical adjacent table entries; these output values are skipped. Thus jumps in the transfer function can be realized. Additionally, two more segments are implemented above and below the normal 12-bit output range to facilitate use of all 16 linearization segments without output clipping. Output points in these two segments are linearly extrapolated from the two points nearest each end of the linearization table.

The linearization algorithm incorporates two modes, linearization mode (Lin Mode) and binning mode (Bin Mode).

Linearization Mode (Lin Mode)

Figure 4 shows an example transfer function which is monotonically increasing. Adjacent points form line segments; input values between are linearly interpolated to find intermediate values. Input values smaller than the first table entry are extrapolated using the points (x_0,−2048) and (x_1, −1792), down to a minimum output value of −2304. Input values larger than the last table entry are extrapolated using the points (x_{15},+1792) and (x_{16},+2048), up to a maximum output value of +2304. The output of the Linearization Algorithm Block, Y_3, is a 13-bit signed integer.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

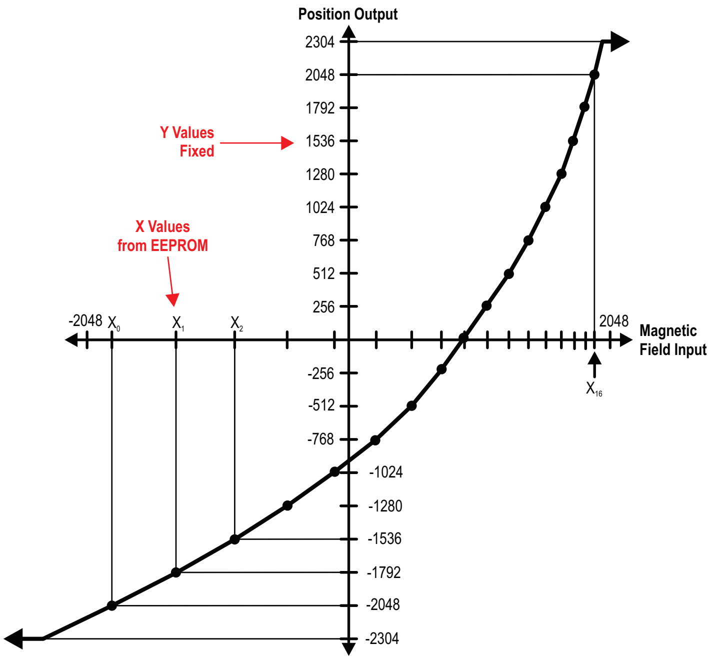


Figure 4: Monotonically Increasing Linearization Transfer Function

Linearization Binning Mode (Bin Mode)

When the bin_mode_c parameter, address lin8_c 0x12 [13], is set, the linearization algorithm does not interpolate between points, but instead produces the output corresponding to the nearest linearization table entry less than or equal to the input value. This transfer function is useful for applications that require distinguishing between several different input ranges. For example, see Figure 5, because $x_2 = x_3 = x_4$ and corresponding output points are −1536, −1280 and −1024 respectively, input values just below $x_2 = x_3 = x_4$ produce an output of −1792 (output corresponding to x_1) and inputs just above or equal to $x_2 = x_3 = x_4$ produce an output of −1024. Intermediate values are skipped. Thus the linearization table functions like a series of comparators with 12-bit programmable thresholds.

Note:
The input values below the lowest table entry produce an output value of −3072, while input values above the highest table entry produce an output value of +2048.

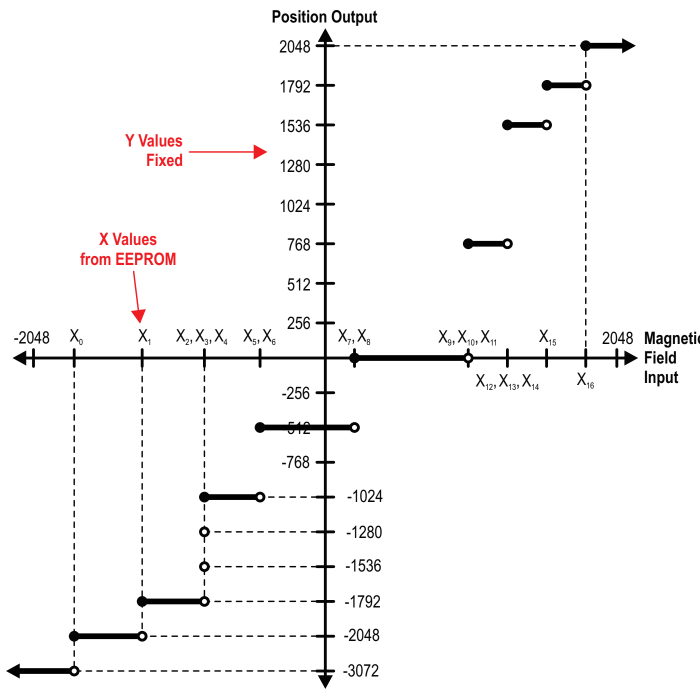


Figure 5: Bin Mode Transfer Function Containing Jumps (Identical Adjacent Table Entries)

The Linearization coefficients and corresponding parameters are stored in following memory locations.

Table 2: Linearization Algorithm Block Parameters

Coefficient/Parameter	Description	Memory Location	Units
$x_0, x_2, \ldots x_{14}, x_{16}$	Even Linearization Coefficients	lin0_c … lin8_c	LSB
$x_1, x_3, \ldots x_{13}, x_{15}$	Odd Linearization Coefficients	lin0_c … lin7_c	LSB
lint_e	Set to logic 1 to enable the Linearization table.	lin8_c 0x12 [12]	NA
lint_bin_e	Set to logic 1 to enable linearization binning mode.	lin8_c 0x12 [13]	NA
lint_out_inv	Set to logic 1 to Invert output of linearization block	lin8_c 0x12 [14]	NA
lint_in_inv	Set to logic 1 to Invert input of linearization block	lin8_c 0x12 [15]	NA

POST-LINEARIZATION TRIM

An additional gain and offset trim stage is available in the linearization block. This can be used to attenuate and gain the signal to maintain usage of all 17 linearization points when using an output range that is not full-scale. Equation 5 shows the transfer function for the Post Linearization. The output of the Post Linearization Block, Y_4, is a 12-bit signed integer and is the output of the Linearization Block.

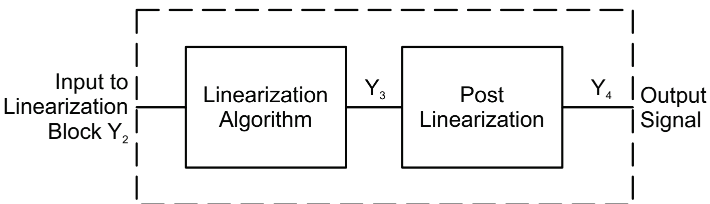


Figure 6: Linearization Block

$$Y_4 = Y_3 \times (1 + PLIN\_SENS) + PLIN\_QVO \qquad (5)$$

CLAMP

The clamp block limits the output to a programmable range set by the parameters clamph and clampl, register clamp_c 0x8. Clamps are programmable throughout the full output range. If the input to the clamp block is greater than the value set by clamph the output is limited to the upper clamp value. Similarly, if the input to the clamp block is less than the value set by clampl the output is limited to the lower clamp value. If the lower clamp exceeds the upper clamp the output is undefined.

Note:
The input to the clamp block is a 12 bit signed value (-2048 to +2047) and is changed to a 12 bit unsigned value (0 to 4095) before comparing to the upper and lower clamp values.

Equations 6 and 7 show the transfer functions for the clamp block. The output of the Clamp Comparison is a 12-bit unsigned integer and is passed to the output block at a fixed frequency of 16 kHz.

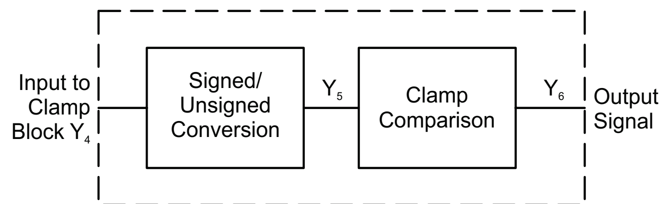


Figure 7: Clamp Block

$$Y_5 = Y_4 + 2048$$

$$\textit{(conversion from signed to unsigned)} \qquad (6)$$

$$\text{if } (Y_5 > OUT_{CLP(HIGH)}), \text{ then } Y_6 = OUT_{CLP(HIGH)}$$

$$\text{else if } (Y_5 < OUT_{CLP(LOW)}), Y_6 = OUT_{CLP(LOW)}$$

$$\text{else } Y_6 = Y_5 \qquad (7)$$

Table 3: Post-Linearization Trim Memory Parameters

Variable	Step Size	Min.	Max.	Description	Parameter (Memory Location)	Units
PLIN_SENS	2^{-11}	−1	+1	Customer post-linearization sensitivity adjustment	plin_sens, (post_lin_c 0x13 [11:0])	NA
PLIN_QVO	1	−2048	+2047	Customer post-linearization offset adjustment	plin_qvo, (post_lin_c 0x13 [23:12])	LSB

Table 4: Clamp Block Parameters

Variable	Description	Programmable Parameter (Memory Location)	Units
CLAMPH	Determines the upper clamp value	clamph (Register clamp_c 0x8 [11:0])	LSB
CLAMPL	Determines the lower clamp value	clampl (Register clamp_c 0x8 [23:12])	LSB

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Diagnostic Conditions

DIAGNOSTIC MODES

The A1342 contains features specifically designed to reduce nondetectable fault conditions and improve system-level ASIL (Automotive Safety Integrity Level) performance. The diagnostic features provide ability to diagnose errors of the main signal path, including the analog signal path (Hall sensor and amplifiers), the ADC, and the digital processing. The A1342 also contains features to diagnose broken wire or open circuit conditions. A description of the broken wire fault conditions are listed in Table 5.

DIAGNOSTIC CONFIGURATION

The A1342 contains EEPROM parameters to configure the diagnostic modes and output behavior. The EEPROM register, cfg_c, contains configurable parameters to enable or disable the Overvoltage Detection, Undervoltage Detection, BIST Error, Signal Out of Range, and Analog Signal Path Error (CoilBIST). In addition the output behavior in response to the error conditions is configurable. By default the device outputs a diagnostic error signal that is decoded by either the PWM or SENT message. Alternatively, the output behavior in response to the error conditions can be set to a high-impedance state (see Table 7).

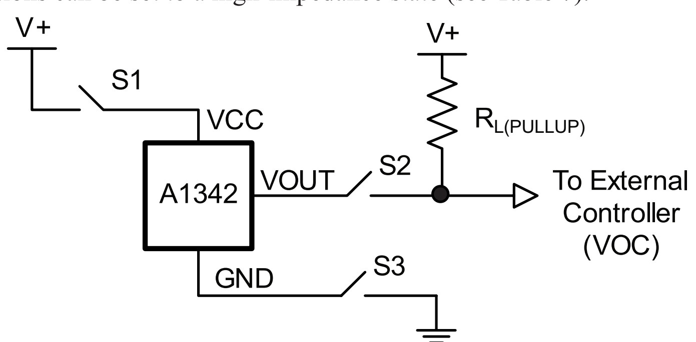


Figure 8: Diagnostic Application Circuit

ANALOG SIGNAL PATH

Errors in the analog signal path are diagnosed using an integrated active coil compensation circuit, CoilBIST. When enabled (coil_freq < 3), an active coil provides a known diagnostic input magnetic field to the Hall sensor circuit. The diagnostic input runs passively during normal operation and does not interfere with the response to external magnetic input. The analog signal path is time-shared between the diagnostic input and the external input at a rate of approximately 128 kHz. The CoilBIST signal detection circuit monitors the signal path at rate of approximately 8 kHz by comparing the diagnostic signal to an internal reference. In the event the analog signal path deviates by more than 10%, V_{OUT} is forced to a state defined by the EEPROM register cfg_c. Setting the parameter coilbist_dis = 1 prevents the analog signal path monitoring from reporting detected errors on the output.

The active coil also provides compensation to reduce Sensitivity drift from lifetime and package stress influences. This feature results in a highly stable Sensitivity over multiple temperature excursions. A programmable bit, coilcomp_dis, is available to disable the compensation while retaining the diagnostic features.

The active coil compensation feature requires an increase of the supply current, I_{CC}, to generate the internal diagnostic magnetic input. The coil compensation on-time is fixed at approximately 16 ms, while the off-time is determined by the EEPROM parameter coil_freq. When the coil compensation is on, the supply current increases by approximately 4 mA. See Table 6 for available coil compensation off time settings. Note, setting coil_freq to a value of 1 or 2 may increase Noise. Setting coil_freq to a value of 3 disables the active coil compensation and diagnostic features during normal operation, while this may reduce noise.

Table 5: Broken Wire Detection Conditions

Description	Circuit	S1	S2	S3	VOUT	VOC
Broken VCC	Figure 8	OPEN	CLOSED	CLOSED	High Impedance	VCC
Broken VOUT	Figure 8	CLOSED	OPEN	CLOSED	Low Impedance	VCC
Broken Ground	Figure 8	CLOSED	CLOSED	OPEN	High Impedance	VCC

NOTE: For proper diagnostic detection the device output clamps should be programmed to appropriate levels. Typical levels are 10% FSO for clamp low and 90% FSO for clamp high.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 6: Coil Compensation On/Off Time

coil_freq [1] (0x09 bits 14:13)	Typical Coil Compensation On-Time (ms)	Typical Coil Compensation Off-Time (ms)	Typical Average I_{CC} Increase Due to Coil Compensation (mA)	CoilBIST Response Time (ms)
0	16	0	4	10
1	16	16	2	26
2	16	4080	0.015625	4090
3	0	16	NA	After BIST Request

[1] Setting coil_freq = 1 or 2 may increase noise. Setting coil_freq = 3 may decrease noise but increase Lifetime Sensitivity Drift.

BIST

The A1342 also has a BIST (Built-In Self Test) feature to check for logic errors in the digital processing circuitry. The BIST feature is configurable with options to disable or enable on request. The options are configured by customer-programmable EEPROM bits in the cfg_c register. When set for enable on request, the BIST runs in response to a request by an external controller. Diagnostic request will be different based on the output protocol. When the output protocol is PWM or SENT, the controller must hold the output low for two consecutive messages to trigger a BIST. In the case when output protocol is TSENT, to request the device perform a BIST, the external controller must hold the output low for a period of time, t_{dreq}, during the Data Nibbles of the output after the SCN nibble (see Table 8, Figure 11, and Figure 15), and then release the output to a high-impedance state. For SSENT and ASENT, the F_DIAG function pulse should be used to trigger a BIST request.

Alternatively, the BIST can execute in response to a write command from the serial communication interface. To request the device perform a BIST using the serial communication interface, a write command is used to set parameter lbist_run = 1 in register lbist_crtl_c (see Figure 28). The LBIST test takes approximately 10 ms to complete.

After the BIST request is received, the Output remains in a high-impedance state while the internal BIST executes. If the parameter lbist_ack is set, the first output message contains a BIST signature value (LBIST Ack) indicating whether or not an error is detected during the digital logic test. If the parameter coilbist_ack is set, the first output message contains the coil diagnostic value (ABIST Ack) from the CoilBIST. If both lbist_ack and coilbist_ack are set, the first output message is the LBIST Ack followed by the second output message ABIST Ack. The ABIST Ack message is only valid when coil_freq = 3. For more information on CoilBIST when using coil_freq < 3, see Diagnostic Conditions: Analog Signal Path. If there are no errors detected, the next output message after the acknowledge messages contains the normal output response. Alternatively, the LBIST Ack and ABIST Ack are returned in register lbist_ctrl_c. Should an error be detected, the output remains in a high-impedance state after the acknowledge messages are transmitted. See Table 7, Diagnostic Summary Table, for more information on the output in response to a diagnosed error.

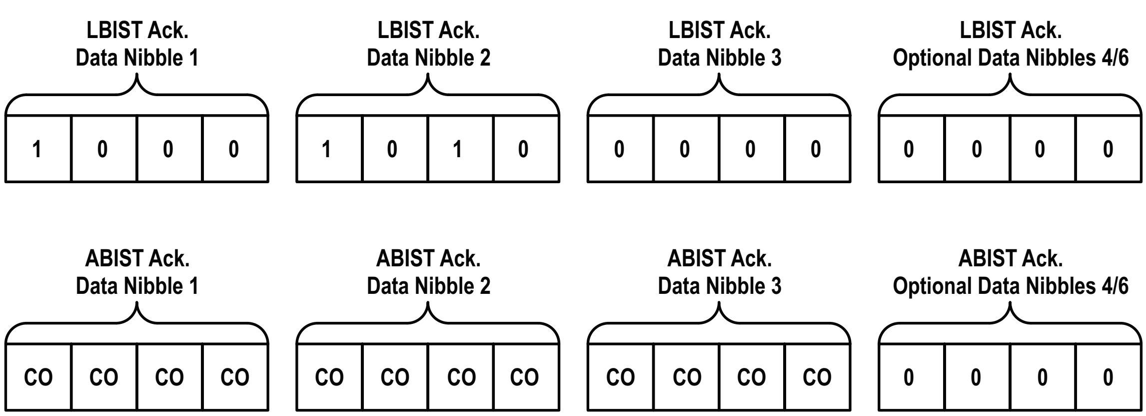


Figure 9: Acknowledgment Signatures for BIST (no errors detected)

(CO = Calibrated Output, valid when coil_freq = 3)

SIGNAL OUT OF RANGE

Included in the A1342 is a diagnostic feature, Signal Out of Range, to detect erroneous clamping of digital signal path as a result of external magnetic input signals. This feature also checks that the magnetic input does not exceed internal ADC range. The output responds to a Signal Out of Range diagnostic according to the settings in the EEPROM register, cfg_c and Table 7.

UNDERVOLTAGE DETECTION AND RESET

The A1342 contains circuitry to detect a condition when the supply voltage drops below the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{CC(UV)HIGH} – V_{CC(UV)LOW}$. As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} drops below $V_{CC(UV)LOW}$, VOUT is forced to a state defined by the EEPROM register, cfg_c. When V_{CC} returns above $V_{CC(UV)HIGH}$, VOUT returns to its normal operating state. If V_{CC} drops below the internal reset level, $V_{CC(POR)LOW}$, the output is forced to a high-impedance state. When V_{CC} returns above the rising reset level, $V_{CC(POR)HIGH}$, the output responds according to the undervoltage detection. The output will not respond with normal data until a delay of t_{PO} after a reset event.

OVERVOLTAGE DETECTION

The A1342 contains circuitry to detect a condition when the supply voltage rises above the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{CC(OV)HIGH} – V_{CC(OV)LOW}$. As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} rises above $V_{CC(OV)HIGH}$, V_{OUT} is forced to a state defined by the EEPROM register, cfg_c. When V_{CC} returns below $V_{CC(OV)LOW}$, V_{OUT} returns to its normal operating state.

The overvoltage detection is only enabled when the EEPROM lock bit is set. If the EEPROM lock bit is not set, and V_{CC} increases above $V_{CC(OV)HIGH}$, the device will enter programming mode and the output is forced to a high-impedance state. If V_{CC} rises above the high-voltage threshold, $V_{CC(HV)HIGH}$, the output is forced to a high-impedance state.

OVERTEMPERATURE DETECTION

The A1342 contains circuitry to detect a condition when the ambient temperature is greater than 160°C, which is outside of the operating range of the part. This will cause the output to respond according to the settings in the EEPROM register, cfg_c and Table 7.

BROKEN GROUND DETECTION

The A1342 contains circuitry to detect a condition when the ground connection is disconnected. When the ground connection is severed, the digital output driver turns off, forcing the output to a high-impedance state.

EEPROM DIAGNOSTICS

The A1342 contains EEPROM with error checking and correction, ECC. The ECC corrects for a single EEPROM bit error without effecting device performance. The ECC also detects a dual bit EEPROM error and triggers an internal fault signal and forces the output to a high-impedance state. Upon a read of EEPROM with no errors, bits 0 through 25 will return the requested EEPROM contents and bits 26 through 31, the six MSBs of the EEPROM register, will return as all zeros. When a corrected single bit error is detected, bit 28 of the read response will return high, indicating the single bit error. When a dual bit error is detected, a read of EEPROM will have bit 29 set high indicating the dual bit error.

Table 7: Diagnostic Summary Table

Diagnostic Detection	Conditions	V_{OUT} (PWM) diag_mode = 0	V_{OUT} (SENT) diag_mode = 0	V_{OUT} (PWM) diag_mode = 1 [1]	diag_reg_c (binary)	SENT Data Nibble #4 and #5 (sent_data_cfg = 1) (binary)
Overvoltage Condition	Overvoltage detection is enabled, diagnostic output is set for advanced output flag, and device lock is set, ovd_dis = 0, dev_lock = 5.	½ carrier frequency 60% DC	See SENT, SCN nibble bit 1 = 1	High impedance	XXX1 XXXX	XXXX 1XXX
Undervoltage Condition [2]	Undervoltage detection is enabled, and diagnostic output is set for advanced output flag, uvd_dis = 0.	½ carrier frequency 40% DC	See SENT, SCN nibble bit 1 = 1	High impedance	XXXX 1XXX	XXX1 XXXX
CoilBIST (Analog Signal Path) Error	CoilBIST enabled and diagnostic output is set for advanced output flag, coilbist_dis = 0, coil_freq < 3.	½ carrier frequency 30% DC	See SENT, SCN nibble bit 0 = 1	High impedance	XXXX X1XX	XX1X XXXX
BIST Error	lbist_dis = 0	High impedance	High impedance	High impedance	XXXX XX1X	NA (High Impedance)
Overtemperature Condition	Overtemperature detection is enabled and diagnostic output is set for advanced output flag, otmp_dis = 0.	½ carrier frequency 70% DC	See SENT, SCN nibble bit 1 = 1	High impedance	XX1X XXXX	XXXX X1XX
Signal Out of Range, Low	Signal Out of Range detection is enabled, and diagnostic output is set for advanced output flag, oor_dis = 0.	½ carrier frequency 80% DC	See SENT, SCN nibble bit 1 = 1	High impedance	X1XX XXXX	XXXX XX1X
Signal Out of Range, High	Signal Out of Range detection is enabled, and diagnostic output is set for advanced output flag, oor_dis = 0.	½ carrier frequency 90% DC	See SENT, SCN nibble bit 1 = 1	High impedance	1XXX XXXX	XXXX XXX1
EEPROM Fault (2 bit error detection)		High impedance	High impedance	High impedance	XXXX XXX1	NA (High Impedance)

[1] diag_mode = 1 is not supported when V_{OUT} is configured for SENT protocol.
[2] An Overvoltage Condition will cause the device to enter Programming Mode which will result in the output being in a high-impedance state when dev_lock does not equal 5.

Linear Output Protocols

The A1342 operating output is a digital voltage signal that transfers information proportionally to the applied magnetic input signal. Few customer-selectable options are provided for output signal formatting: pulse-width-modulated (PWM), and variations of single-edge nibble transmission encoding scheme (SENT, SAEJ2716).

Note:

The device response to the applied magnetic field is on the OUT pin. However, that pin is also used to transmit and receive data in response to a serial programming commands, during which the normal output operation is suppressed. Refer to the Programming Serial Interface section for more information. The EEPROM is described in the EEPROM Structure section. The output falling edge slew rate is adjustable using the outdrv_sel parameter. Adjusting this can improve EMC performance by reducing high-frequency currents. This parameter can also increase the output fall time and result in longer minimum pulse durations for serial communication or SENT transmission.

PWM OUTPUT MODE (outmsg_mode = 0)

PWM involves converting the output voltage amplitude to a series of constant-frequency binary pulses, with the percentage of the of high portion of the pulse varied in direct proportion to the applied magnetic field.

The PWM output mode is configured by setting the following parameters in EEPROM:

- PWM option is EEPROM programmable (for programming parameters, see EEPROM Structure section)
- sent_pwm_rate sets the PWM carrier frequency based on the values in Table 14

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

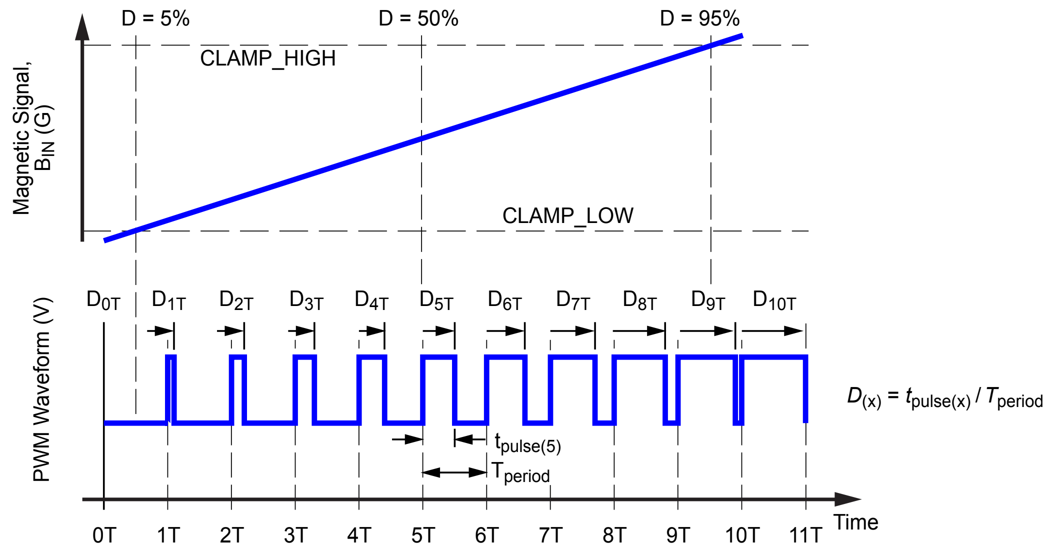


Figure 10: PWM Mode Duty-Cycle-Based Waveform

PWM mode outputs a duty-cycle-based waveform that can be read by the external controller as a cumulatively changing continuous voltage.

Initiation of the BIST is done through the external controller request and explained in Table 8 and Figure 11.

Table 8: External BIST Request and SENT Trigger Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Trigger Pulse Width	t_{trg}	Trigger pulse for TSENT operation; see SSENT and ASENT sections for F_OUTPUT pulse durations	1.8	–	–	μs
Synchronization Pulse Delay [1]	t_{dsync}		7	–	524	tick
SENT Output Trigger Signal	$V_{SENTtrig(L)}$	V_{OUT} falling, T_A = 25°C	–	–	1.39	V
	$V_{SENTtrig(H)}$	V_{OUT} rising, T_A = 25°C	2.3	–	–	V
SENT Output Trigger Signal Hysteresis	$V_{SENTtrig(HYST)}$	T_A = 25°C	–	300	–	mV
External BIST Request Pulse Width	t_{dreq}	PWM	2	–	–	frame rate [2]
		SENT Modes	15	–	–	tick
BIST Delay	t_{diag}	Delay for device to execute internal BIST	10	–	20	ms

[1] t_{dsync} can increase from 7 ticks to preserve a minimum time of approximately 70 μs from the falling edge of the trigger to the start of the SCN nibble.
[2] The frame rate is determined by the sent_pwm_rate parameter.
[3] When in Trigger SENT Output mode the external controller must pull the output low after tdsync and before the first data nibble in the SENT frame, for a time of t_{dreq}, to initiate a BIST request.

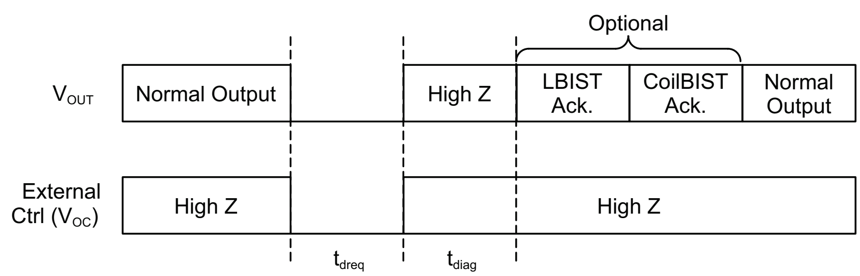


Figure 11: External BIST Request with PWM or Synchronous SENT Output Mode

SENT OUTPUT MODES

The SENT output mode converts the input magnetic signal to a binary value mapped to the Full Scale Output, FSO, range of 0 to 4095, shown in Figure 12. This data is inserted into a binary pulse message, referred to as a frame, that conforms to the SENT data transmission specification (SAEJ2716 JAN2010). Certain parameters for configuration of the SENT messages can be set in EEPROM.

The SENT output modes are selected by setting the following parameters in EEPROM:

- SAE J2716 SENT with enhancement options (outmsg_mode = 1)
- Triggered SENT – TSENT (outmsg_mode = 2) – User defines sampling and data retrieving.
- Sequential SENT – SSENT – User requests data from multiple devices on the SENT line in sequential order (outmsg_mode = 4 for short_trigger and outmsg_mode = 3 for long_trigger). Short and long trigger modes can be differentiated on the length and number of host function/request pulses.
- Addressable SENT – ASENT – User requests data from any device on the SENT line in any order. (outmsg_mode = 7, 6, or 5)
- Additional configuration parameters in register 0x14, out_cfg_c.

MESSAGE STRUCTURE

A SENT message is a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval
- The low interval, SENT_FIXED, is defined as 5 SENT ticks. The high interval contains information and is variable in duration to indicate the data payload of the nibble.

The duration of a nibble is denominated in clock ticks. The period of a tick is set by sent_pwm_rate parameter as in Table 14. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The nibbles of a SENT message are arranged in the following required sequence (see Figure 13):

1. Synchronization and Calibration: flags the start of the SENT message
2. Status and Communication: provides A1342 status and the format of the data
3. Data: magnetic field and optional data
4. CRC: error checking
5. Pause Pulse: sets timing relative to A1342 updates

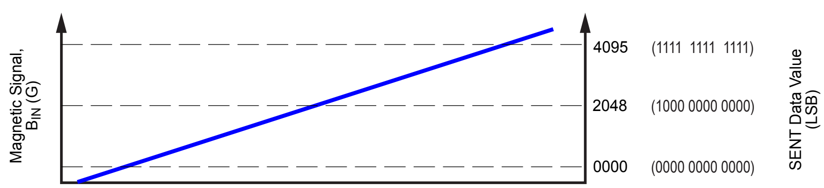


Figure 12: SENT Mode Output
SENT mode outputs a digital value that can be read by the external controller

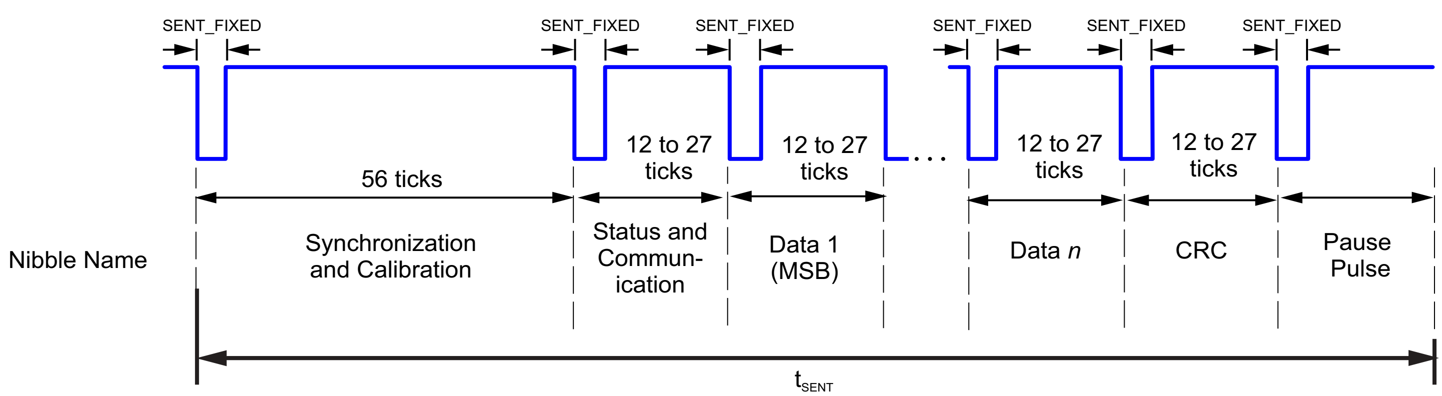


Figure 13: General Format for SENT Message Frame

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPTIONAL SHORT SERIAL MESSAGE

The A1342 SENT output supports an optional mode to transmit additional data. The slow serial mode, enables transmission of additional data by encoding information in the Status and Communication (SCN) nibbles. The encoded data is captured over several transmissions and is then decoded to indicate additional short serial message data. For more details on the short serial message please refer to the SENT SAEJ2716 specification.

The slow serial mode is enabled when the EEPROM parameter sent_slow_ser_dis = 0. Following a reset, the first message transmitted is 0, following in order of the message ID until message 4, and then repeating. Table 10 identifies the data sent with each message ID. The CRC for the Short Serial Message is derived for the Message ID and data, and is the same checksum algorithm used for the SENT CRC.

Table 9: Short Serial Message Format in SENT Status and Communication Nibble

SCN Bit (For the values of bits 0 and 1 please see Table 7: Diagnostic Summary)	Nibble #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Bit 3 (Start Bit)	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 2 (Serial Data)	Message ID				Data								CRC			

Table 10: SENT Slow Serial Data

Message ID	Data
0	Error status from the parameter diag_reg_c located in register err_status_c, 0x45 bits [23:16]. {EEPROM DBE, LBIST, Coil Measurement Monitor, Undervoltage, Overvoltage, Overtemperature, Signal out of range low, Signal out of range high}
1	8-bit temperature value from internal temperature sensor. Values are saturated to ±128°C, and 3 LSBs are rounded to nearest degree
2	id_c[7:0] (Customer ID, EEPROM 0x2)
3	id_c[15:8] (Customer ID, EEPROM 0x2)
4	id_c[23:16] (Customer ID, EEPROM 0x2)

In the case of SSENT and ASENT mode, SCN bits 2 and 3 can be selected to label the address of the sensor on the shared SENT line (sen_no_smsg =1 and sent_slow_ser_dis = 1, gives ID in SCN).

DATA NIBBLE FORMAT

The A1342 SENT output supports options for the message data nibble format. The data nibble format is determined by the EEPROM parameter sent_data_cfg. The options for either a minimum 3 or maximum 6 nibbles of data is defined in Table 11. Where:

- magout[11:0]: 12-bit magnetic output data.
- count[11:0]: SENT frame count. The counter increments once for every frame that is sent up to the maximum count. At the next count, after the maximum, the counter starts again at 0. The maximum count is 15 and 4095 for sent_data_cfg = 1 and sent_data_cfg = 2 respectively.
- temp_out[11:0]: 12-bit signed output from the internal temperature sensor. Ambient temperature (°C) = 12-bit signed temperature value / 8 (LSB / °C) + 25.
- diag[7:0] Diagnostic flags, EEPROM, LBIST, CoilBist, Undervoltage, Overvoltage, Overtemperature, Signal out of range low, and Signal out of range high.

Table 11: SENT Data

sent_data_cfg	Data Nibble #1	Data Nibble #2	Data Nibble #3	Data Nibble #4	Data Nibble #5	Data Nibble #6	# of Nibbles
0	mag_out [11:8]	mag_out[7:4]	mag_out[3:0]	–	–	–	3
1	mag_out [11:8]	mag_out[7:4]	mag_out[3:0]	diag[7:4]	diag[3:0]	count[3:0]	6
2	mag_out[11:8]	mag_out[7:4]	mag_out[3:0]	count[11:8]	count[7:4]	count[3:0]	6
3	mag_out[11:8]	mag_out[7:4]	mag_out[3:0]	temp_out [11:8]	temp_out [7:4]	temp_out [3:0]	6

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

CHECKSUM (CRC) NIBBLE

The CRC consists of 4 bits derived from the data nibbles only. The CRC is calculated using the polynomial $x^4 + x^3 + x^2 + 1$ with a seed of 4’b0101. For the shared SENT protocols, SSENT and ASENT, there is an option that SCN is included into the CRC nibble (sen_crc_has_scn = 1, includes SCN into CRC).

OUTPUT DRIVER FALL TIME SELECTION

User is allowed to change the fall time of the output digital signal using the EEPROM parameter outdrv_sel. See Table 12 below.

Table 12: Code vs C_{LOAD} for outdrv_sel

Function	Output Signal Configuration Sets configuration of the output signal slew-rate control. Sets the ramp rate on the gate of the output driver, thereby changing slew rate at the output.	
Syntax	Field width: 3 bits	
Related Commands	–	
Values	Code	Fall Time (Typical), see Figure 14: Test Circuit (µs) C_{LI} = 1.5 nF, C_{LX} = 0
	0 (Default)	0.11
	1	0.18
	2	0.27
	3	0.35
	4	0.70
	5	1.24
	6	2.42
	7	3.55
Options	–	
Examples	–	

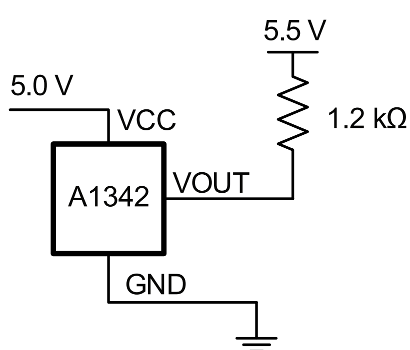


Figure 14: Fall Time Test Circuit

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 13: Message Frame Section Definitions

Section	Description
SYNCHRONIZATION AND CALIBRATION	
Function	Provide the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section, for ease of distinction by the external controller.
Syntax	Nibbles: 1 Quantity of ticks: 56 Quantity of bits: 1
STATUS AND COMMUNICATION	
Function	Provides the external controller with the status of the A1342 and indicates the format and contents of the Data section.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 Quantity of bits: 4 1:0 Device status (see Table 20) 3:2 Message serial data protocol (sent_slow_ser_dis)
DATA	
Function	Provides the external controller with data selected by the sent_data_cfg parameter.
Syntax	Nibbles: 3 to 6 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4 (each nibble)
CRC	
Function	Provides the external controller with cyclic redundancy check (CRC) data for certain error detection routines applied to the Data nibbles and to the Status information.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4
PAUSE PULSE	
Function	Additional time can be added at the end of a SENT message frame to ensure all message frames are of appropriate length.
Syntax	Nibbles: NA Quantity of ticks: Quantity of bits: NA
TRIGGER PULSE	
Function	(Optional) Allow the external controller to determine when to transmit data
Syntax	Nibbles: NA Output must be held low a minimum of 1.8 μs after the pause pulse.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SAEJ2716 SENT AND TSENT

The A1342 SENT output is configurable for four (4) transmission modes, Internal Synchronous Mode, External Trigger Mode (TSENT), SSENT or ASENT. The transmission modes are configured by setting the parameter outmsg_mode.

When configured for Internal Synchronous Mode, outmsg_mode = 1, the SENT output transmits continuously, while in normal operating conditions. The SENT message frame rate is correlated to the internal update rate of the device (see Figure 16). The pause pulse is extended to correlate with the next available sample.

When configured for External Trigger Mode, outmsg_mode = 2, the SENT output transmits when requested by the external controller (see Figure 17). The pause pulse is extended until the next trigger pulse.

The external controller initiates a trigger pulse by holding the output pin low. The data sample is latched at the next internal update, 128 kHz, after the falling edge of the trigger pulse. The SENT frame is transmitted when external controller releases the output, the rising edge of the trigger pulse. After the rising edge of the trigger pulse the output remains high for minimum of seven SENT tick times before going low to initiate the start of the SENT synchronization pulse. For the fastest SENT rates, the start of the SENT synchronization pulse may be delayed longer than seven ticks to allow enough time for signal processing of the latched data. This is done to preserve a minimum time of 70.4 µs from the falling edge of the trigger pulse to end of the sync pulse, required for internal signal processing.

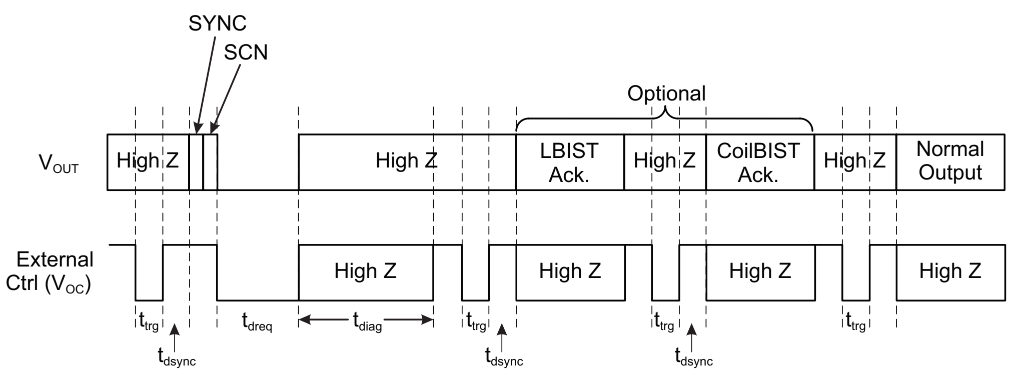


Figure 15: External BIST Request with Triggered SENT Output Mode

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

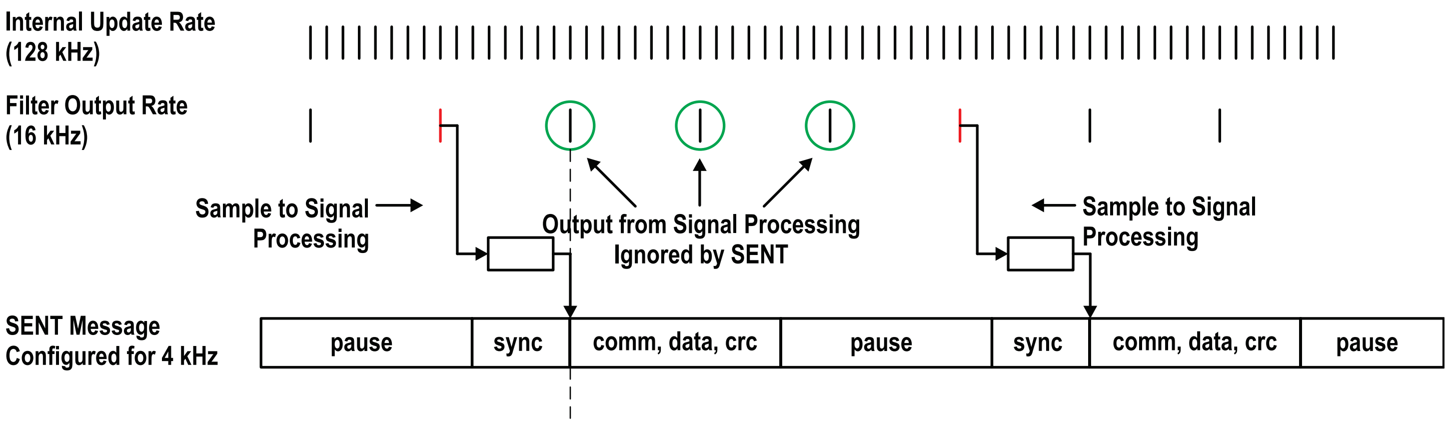


Figure 16: SENT Synchronization with Output Data and Internal Synchronous Mode

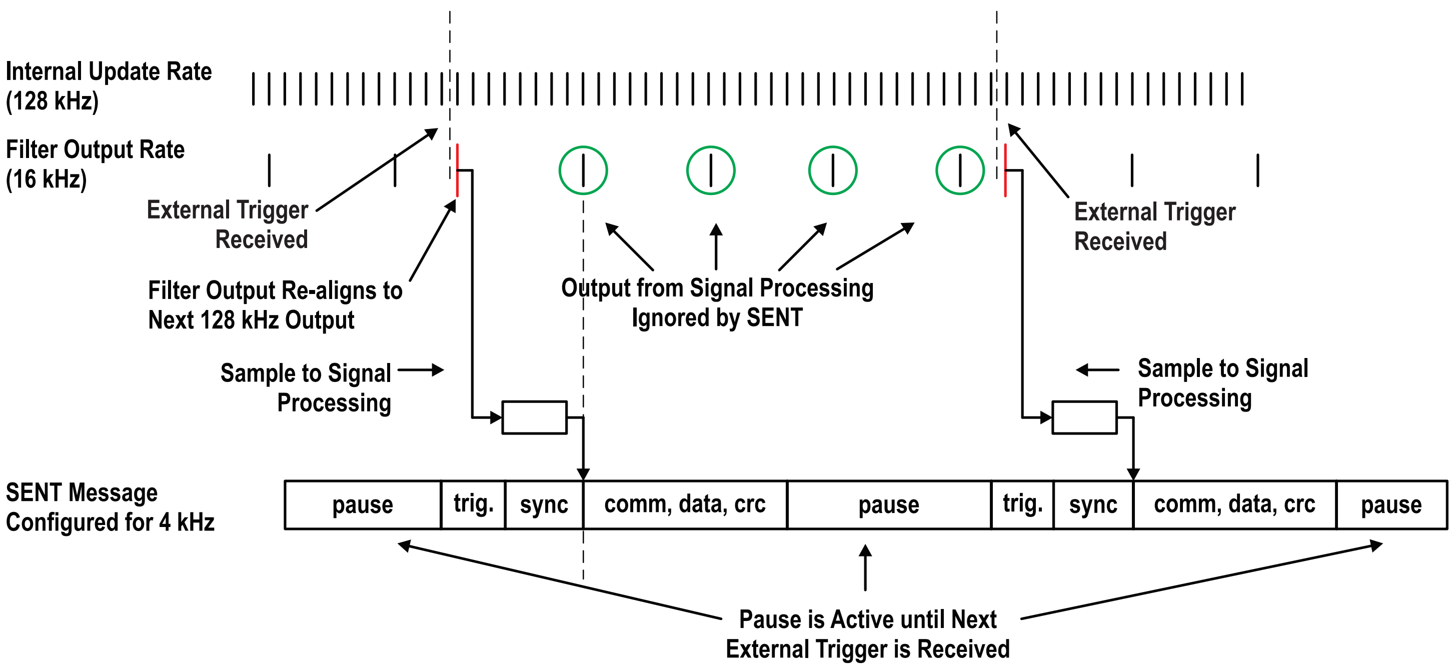


Figure 17: SENT Synchronization with Output Data and External Trigger Mode

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 14: SENT Frame Rate

PWM/SENT Code	ASENT/SSENT	TSENT/SENT	PWM
	Tick Time (µs) [1]	Tick Time (µs) [1]	f_{PWM} (Hz) [2]
0	0.12	3.05	125
1	0.12	3.05	167
2	0.24	3.05	250
3	0.37	3.05	333
4	0.49	14.77	500
5	0.61	9.64	667
6	0.73	7.32	800
7	0.85	6.10	1000
8	0.98	4.76	1333
9	1.10	3.54	1600
10	1.22	2.44	2000
11	1.34	1.71	2667
12	1.46	1.22	4000
13	1.59	0.85	5333
14	1.71	0.61	8000
15	1.83	0.61	16000
16	1.95	–	–
17	2.08	–	–
18	2.20	–	–
19	2.32	–	–
20	2.44	–	–
21	2.56	–	–
22	2.69	–	–
23	2.81	–	–
24	2.93	–	–
25	3.05	–	–
26	3.17	–	–
27	3.30	–	–
28	3.42	–	–
29	3.54	–	–
30	3.66	–	–
31	3.78	–	–

[1] The combination of C_{LI} and output pull-up resistor may prevent use of some tick times due to increased output rise time.
[2] f_{PWM} frequencies of 2000 Hz or greater may reduce output resolution.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SSENT ADDRESSING PROTOCOL

The SSENT protocol requires Sensors on the bus to be polled in sequential order, meaning increasing, consecutive, and rotating order by SensorID starting with SensorID 0. The Slot for a Sensor is the time at which that Sensor is expected to respond to an AddressingPulse and other Sensors are expected to not respond.

Each Sensor independently maintains a SlotCounter that is incremented each time the Sensor detects an AddressingPulse. This SlotCounter becomes the SlotNumber, which is used by the Sensor to decide which Sensor is being polled by the Host. The SlotCounter is compared to the SensorID, and if they match, that Sensor responds with the SENT Frame, and all other Sensors do not respond, although they increment their own SlotCounter. If the SlotCounter is incremented past the total number of Sensors on the bus (C_MAX_SENSOR option), the SlotCounter is returned to 0. Each Sensor must be programmed consistently with the total number of Sensors so they all roll over to 0 at the same count. Sensors do not increment their SlotCounter on a BroadcastPulse.

The SSENT protocol relies on each Sensor maintaining the exact same SlotNumber by counting the AddressingPulses. In order to synchronize all Sensors to the same SlotNumber, the SSENT protocol has a broadcast F_SYNC pulse that is used by the Host to force all Sensors to reset their SlotCounter to 0.

In order to reduce the burden on the Host, and also to improve detection and recovery from BusContention or system errors affecting the SENT bus, the SSENT protocol has the following configuration options that can be selected.

- C_SLOT_MARKING (cfg_slot_marking, 0x14). When enabled, each Sensor will wait a different length of time following an AddressingPulse, based on their SensorID. This leaves the SENT bus in a high state for a varying duration before the Sensor pulls the line low to begin the SENT Frame. All Sensors on the bus (including the addressed Sensor) measure this time to interpret the SensorID of the transmitting sensor. By comparing this to the SlotCounter, each Sensor can recognize if an unexpected Sensor responded to the AddressingPulse. By default, the Sensor would then drop Offline, since it cannot be known which Sensor is out of sync. This option increases the overhead on the bus and therefore reduces the maximum rate at which Sensors can be polled. SlotMarking increases the polling time of a Sensor by the SlotMarking time for that Sensor. All sensors on a bus must be configured with the same choice for this option.

Table 15: Slot Marking Delay Times for SSENT

SensorID	Delay Time Ticks (Nominal)
0	7
1	18
2	36
3	62

Note:
It is not recommended using the slot marking option under a tick time of 1.2 µs since delay time associated with the Sensor ID might be too short for the sensor to process and give out the new sample.

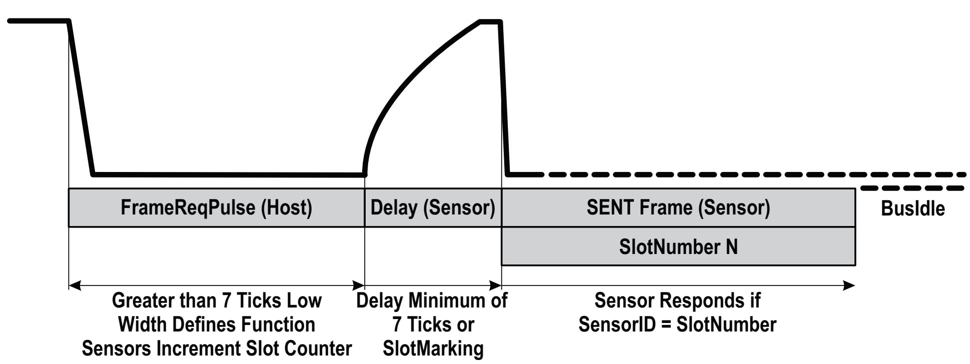


Figure 18: SSENT Sensor Addressing

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

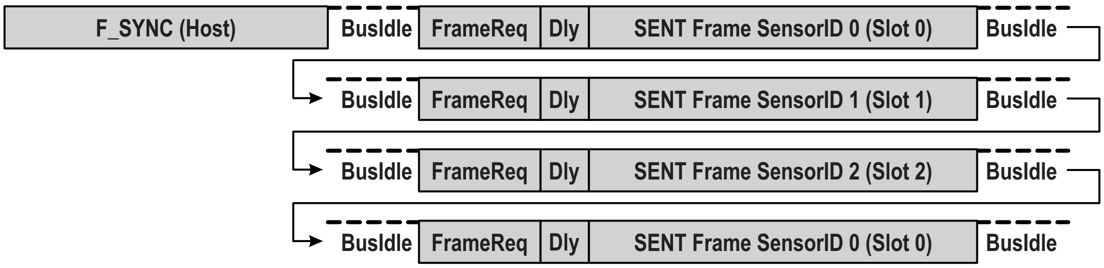


Figure 19: SSENT Sensor Addressing – No Slot Marking (3 Sensors on Bus)

- C_SLOT_SYNC (cfg_slot_synch, 0x14). When enabled in conjunction with C_SLOT_MARKING, a Sensor that is in BusSync for a reason other than BusContention will load its SlotCounter with the measured SlotNumber from the first AddressingPulse that does not have a Timeout. A Sensor would normally be Offline as a result of powering up, reset, or diagnostics. As long as any Sensor is Online and responding, this allows all other Sensors that are Offline to automatically synchronize their SlotCounter and begin responding correctly to future AddressingPulses targeting that Sensor. If all Sensors are offline, though, the Host must detect that no Sensor responds, and issue the F_SYNC function.
- C_POR_OFFLINE (cfg_por_offline,0x14). When enabled, a Sensor will stay Offline until the Host issues F_SYNC, or one of the other synchronization options takes effect (C_SLOT_SYNC or C_IDLE_SYNC). If disabled, a Sensor will power-up with its SlotCounter set to 0, and will go directly Online. This allows the Sensors to initialize without any Host interaction. However, if a Sensor gets power-on-reset after the bus is in operation, its counter may be out of synch with other Sensors, and this could result in bus contention.
- C_IDLE_SYNC (cfg_slot_sync,0x14). When enabled, a Sensor will monitor the bus for a long high (BusIdle) period greater than 510 ticks and reset its SlotCounter to 0. This option could be used if Sensor polling is expected to always be periodic and continuous, such that the only extended BusIdle time would be after power-up.

SSENT FUNCTION PULSES

SSENT has a set of function pulses where the host controller must hold the output low. The duration of the low pulse provided by the host controller defines the function, as described in Table 17 and Table 18. Following the low pulse, if the part is addressed to respond and the slot number matches the device slot counter, the device delays the output SENT frame with a minimum of 7 ticks high period to differentiate between the host trigger, and the device response. For the fast tick times, the 7 tick high period may be extended, to preserve a minimum time of 70.4 µs from the rising edge of the function pulse to the end of the sync pulse required for internal processing. Whether the device responds to a function pulse is defined by the purpose of each pulse.

- F_OUTPUT: Addressed sensor will return a SENT frame with sampled magnetic data. If there is data from a sample-and-hold operation available (F_SAMPLE or via C_ZERO_SAMPLE=1 [cfg_zero_sample,0x14]), then that data is returned, otherwise current data is sampled and returned. A Sensor configured with C_ZERO_SAMPLE=1 will sample-and-hold on the rising edge of the F_OUTPUT pulse for Slot 0. A Sensor configured with C_NO_SAMPLE=1 (cfg_no_sample,0x14) and C_ZERO_SAMPLE=0 will never sample-and-hold, so will always return current data in response to F_OUTPUT.
- F_SAMPLE: All sensors except those configured for C_NO_SAMPLE=1 will sample and hold their data at the rising edge of the pulse. If C_SAMPLE_ADR=0 (cfg_fsample_adr,0x14), this is a BroadcastPulse to a Sensor, and that Sensor will not respond. If C_SAMPLE_ADR=1, this is also an AddressingPulse to a Sensor, and the addressed sensor will return a SENT frame with either the sampled or current data. It is recommended, but not required, that all Sensors on the bus be configured the same.
- F_DIAG: Sensor(s) will enter self-test Diagnostics based on C_DIAG_ENABLE (lbist_dis, 0x9) and C_DIAG_ADR (cfg_diag_adr,0x14) options. If configured with C_DIAG_ADR=0, the Sensor treats F_DIAG as a BroadcastPulse, does not respond, and immediately enters Diagnostics unless C_DIAG_ENABLE=0. If configured with C_DIAG_ADR=1, the Sensor treats F_DIAG as an AddressingPulse. The addressed Sensor does not respond, but enters diagnostics if C_DIAG_ENABLE=1.
- F_SYNC: All Sensors will synchronize their SlotNumbers by setting their SlotCounters such that the next AddressingPulse is for Slot 0.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

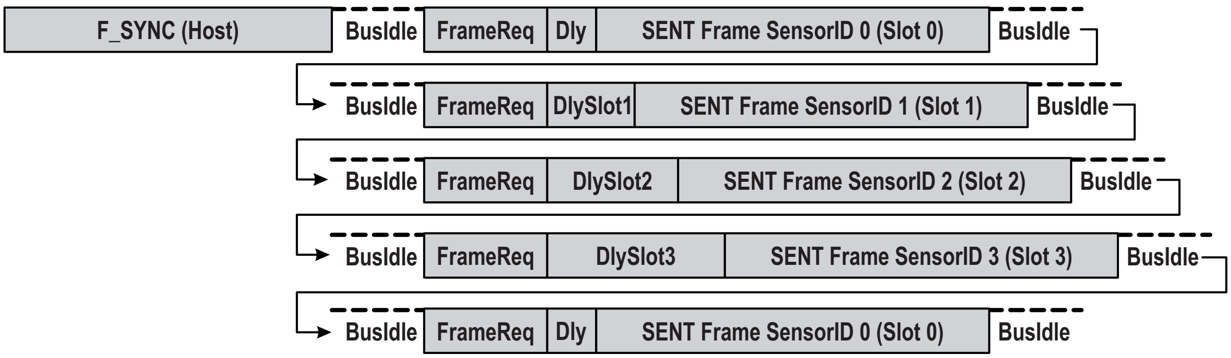


Figure 20: SSENT Sensor Addressing - with Slot Marking (4 Sensors on Bus)

Table 16: SSENT Function Pulses in short_trigger Mode, outmsg_mode = 4

Function	Type	Min. Tick	Nom. Tick	Max. Tick
F_OUTPUT	Addressing/Broadcast	15	17	19
F_SAMPLE	Addressing/Broadcast	31	35	39
F_DIAG	Addressing/Broadcast	56	63	70
F_SYNC	Broadcast	93	104	115

Table 17: SSENT Function Pulses in long_trigger Mode, out-msg_mode = 3

Function	Type	Min. Tick	Nom. Tick	Max. Tick
F_OUTPUT	Addressing/Broadcast	9	–	81
F_SYNC	Broadcast	105	140	171
F_DIAG	Addressing/Broadcast	216	240	264

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ASENT ADDRESSING PROTOCOL

The ASENT protocol allows Sensors to be polled in an arbitrary order. The SensorID is transmitted by the Host following any AddressingPulse as a series of 0, 1, 2, or 3 IncAdrPulses. After this sequence, the SENT line is left in a high state, and each sensor will recognize after a time period of about 18 nominal ticks that there are no more IncAdrPulses coming. This 18 tick high period may be delayed to allow enough time for signal processing of the latched data. This is done to preserve a minimum time of 70.4 µs from the rising edge of the function and addressing pulse to end of the sync pulse, required for internal signal processing. The sensor whose ID matches the number of IncAdrPulses received will respond.

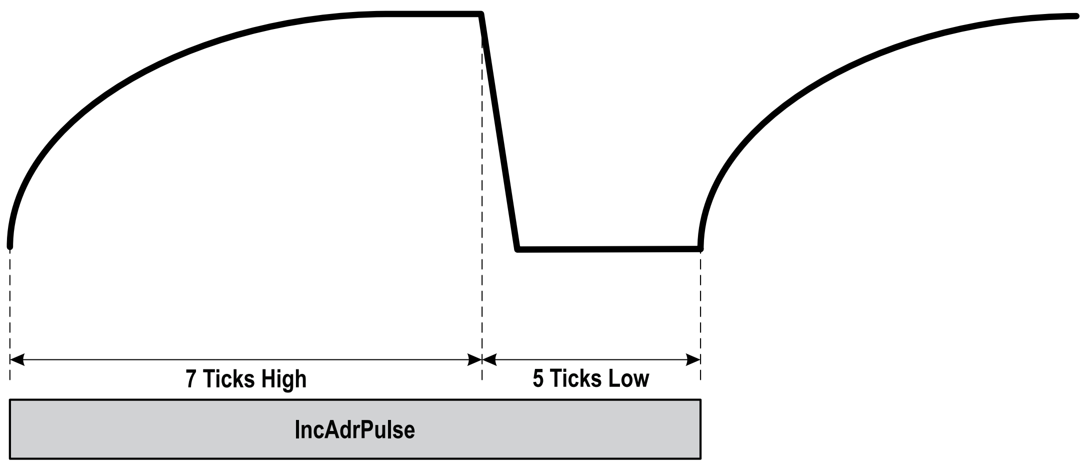


Figure 21: ASENT IncAdrPulse (output by Host)

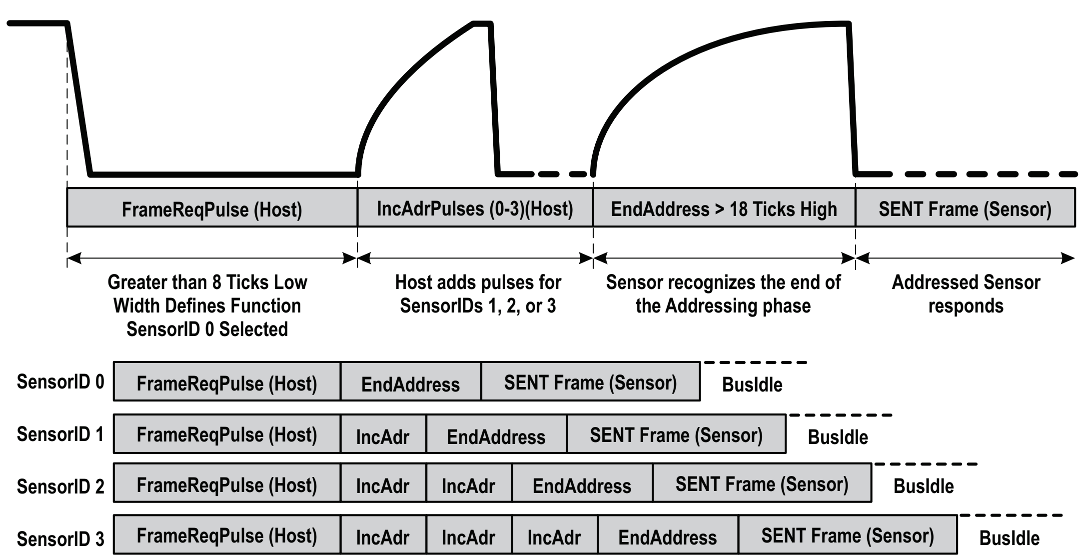


Figure 22: ASENT Sensor Addressing

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ASENT FUNCTION PULSES

- F_OUTPUT: Addressed sensor will return a SENT frame with sampled magnetic data. If there is data available from a sample-and-hold operation (F_SAMPLE), then that data is returned, otherwise current data is sampled and returned. A Sensor configured with C_NO_SAMPLE=1 will not sample-and-hold, so will always return current data in response to F_OUTPUT.
- F_SAMPLE: All sensors except those configured for C_NO_SAMPLE=1 will sample and hold their data at the rising edge of the pulse. If C_SAMPLE_ADR=0, this is a BroadcastPulse to a Sensor, and that Sensor will not respond. If C_SAMPLE_ADR=1, this is also an AddressingPulse to a Sensor, and the addressed sensor will return a SENT frame with either the sampled or current data. It is recommended, but not required, that all Sensors on the bus be configured the same.
- F_DIAG: Sensor(s) will enter self-test Diagnostics based on C_DIAG_ENABLE and C_DIAG_ADR options. If configured with C_DIAG_ADR=0, the Sensor treats F_DIAG as a BroadcastPulse, does not respond, and immediately enters Diagnostics unless C_DIAG_ENABLE=0. If configured with C_DIAG_ADR=1, the Sensor treats F_DIAG as an AddressingPulse. The addressed Sensor does not respond, but enters diagnostics if C_DIAG_ENABLE=1.

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, in the A1342 using a point-to-point command/acknowledge protocol. The A1342 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledging from the A1342. If the command is a read, the A1342 responds by transmitting the requested data.

NOTE:
It is the external controller's responsibility to avoid sending a Command Frame which overlaps a Read Acknowledge frame.

The serial interface uses a Manchester encoding based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the A1342: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the A1342 in response to a Read command.

Table 18: ASENT Function Pulses

Function	Type	Min. Tick	Nom. Tick	Max. Tick
F_OUTPUT	Addressing/Broadcast	15	17	19
F_SAMPLE	Addressing/Broadcast	31	35	39
F_DIAG	Addressing/Broadcast	56	63	70

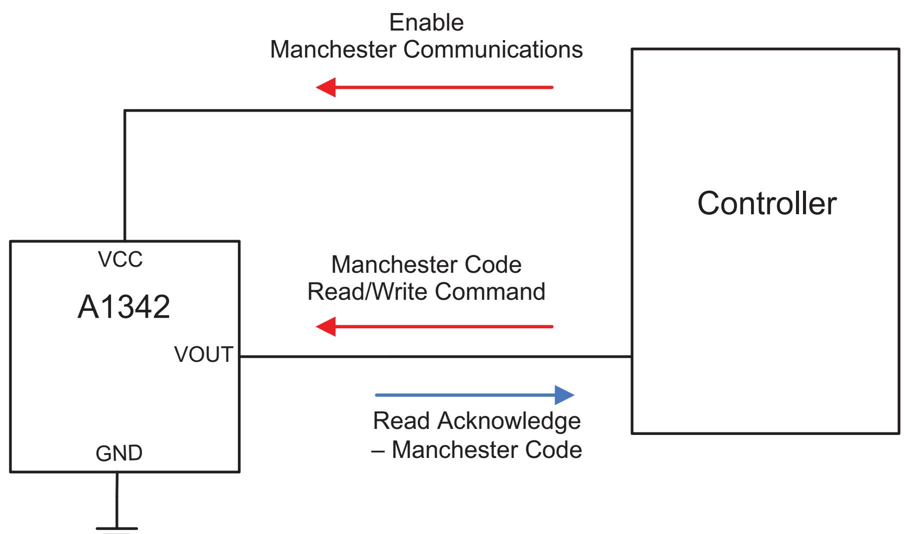


Figure 23: Top-Level Programming Interface

PROGRAMMING INFORMATION

The A1342 device uses a three-wire programming interface, where the input signal on VCC controls the program enable signal, data is transmitted on VOUT, and all signals are referenced to ground. This three-wire interface make it possible to use multiple devices with shared VCC and ground lines.

Four transactions, write access, write to EEPROM, write to volatile memory, and read, are shown in the Figure 24 to Figure 28. To initialize any communication, V_{CC} increases to a level above V_{PRGH}(min). At this time, VOUT is disabled and acts as input. After program enable is asserted, the external controller must drive the output low for a minimum of two Manchester bit periods before sending the message frame. Once the command is complete, V_{CC} is reduced below V_{PRGL}(max) back to its normal operating level, the output is enabled and responds to magnetic input.

When performing a write to EEPROM transaction, the A1342 requires a delay of t_w to store the data into the EEPROM. The device will respond with a high-to-low transition on VOUT to indicate the write to EEPROM sequence is complete.

Table 19: Programming Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Program Enable Voltage (High)	V_{PRGH}	dev_lock = 0, 1, 2, 4, 7	$V_{CC(OV)HIGH}$(max)	–	19	V
		dev_lock = 3	$V_{CC(HV)HIGH}$(max)	–	19	V
Program Enable Voltage (Low)	V_{PRGL}	dev_lock = 0, 1, 2, 4, 7	–	–	$V_{CC(OV)LOW}$(min)	V
		dev_lock = 3	–	–	$V_{CC(HV)LOW}$(min)	V
Manchester Start Delay	t_m	Minimum delay before first edge of the Manchester signal.	200	–	–	µs
Output Enable Delay	t_e		–	25	–	µs
Program Time Delay	t_d		–	–	50	µs
Program Write Delay	t_w		–	20	–	ms
Bit Time Delay	t_b		–	2	–	t_{bit} [1]
BIST Output Enable	t_l	Time for V_{CC} to reduce below V_{PRGL} for BIST acknowledgmen	–	–	2	ms
Access Code Timeout	t_{acc}		500	–	–	ms
Bit Rate		Communication Rate	4	–	100	kBPS
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT	2.8	–	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT	0	–	1.2	V

[1] The unit t_{bit}, is the period for single bit defined by the Manchester encoding bit boundaries and is determined by the communication rate.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

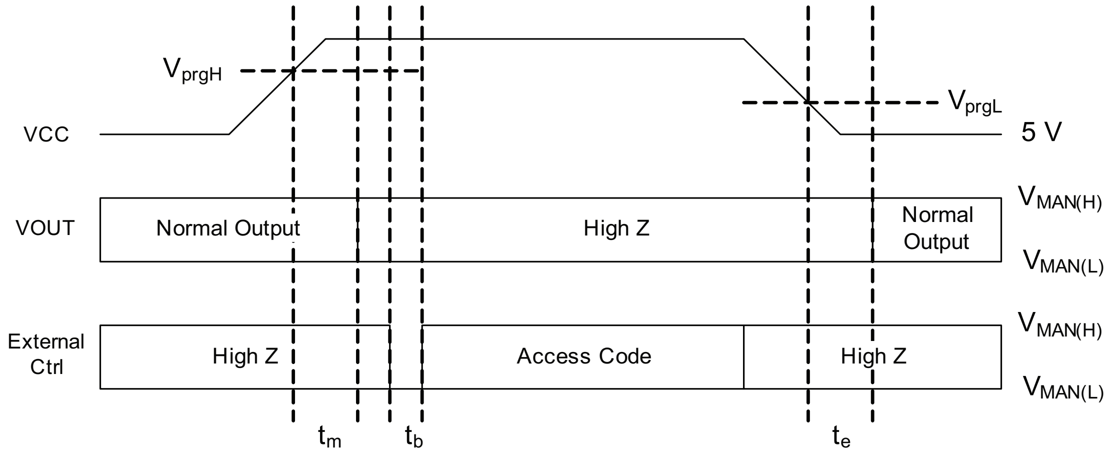


Figure 24: Write Access Code

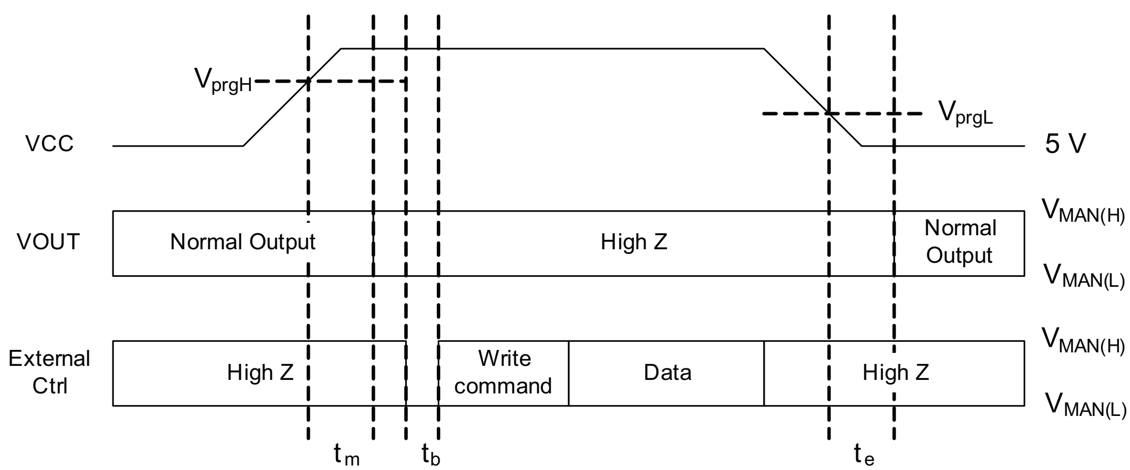


Figure 25: Write to Volatile Memory

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

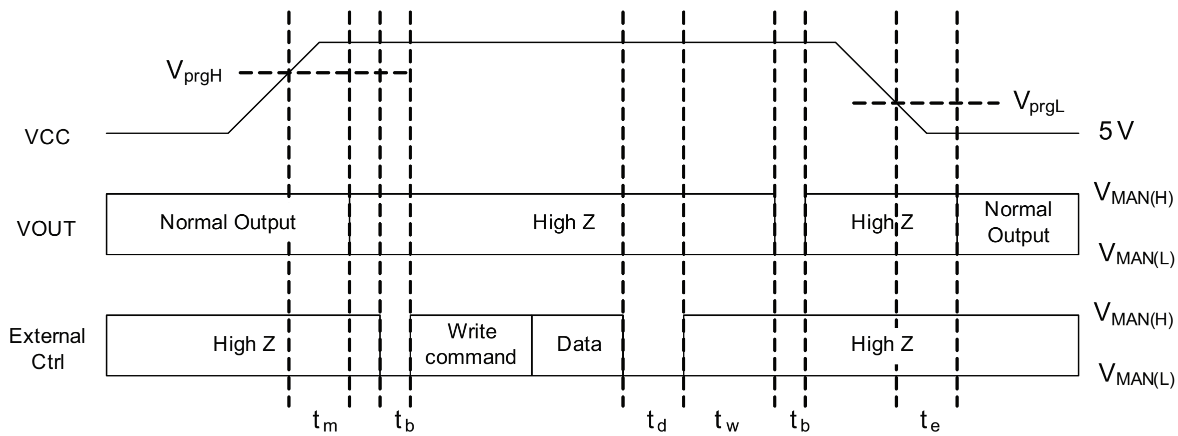


Figure 26: Write to Non-Volatile Memory (EEPROM)

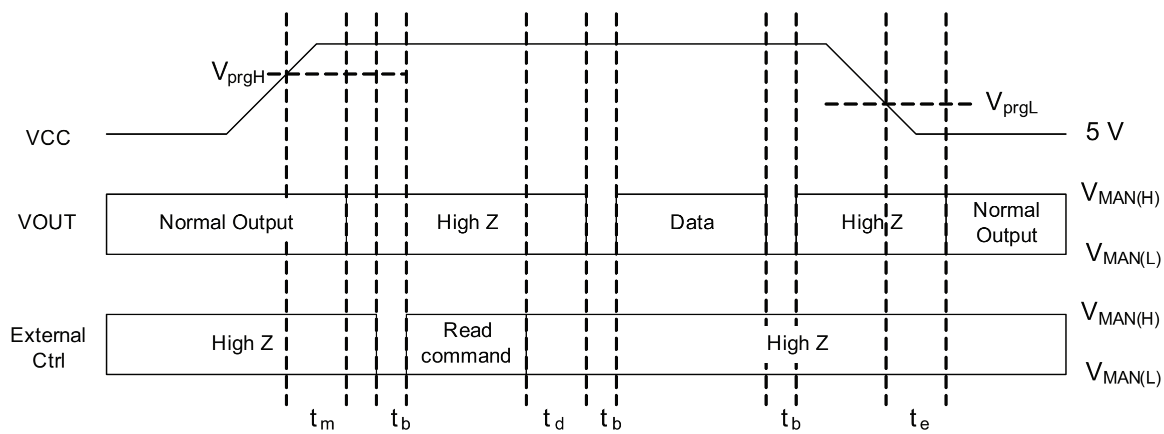


Figure 27: Read Request

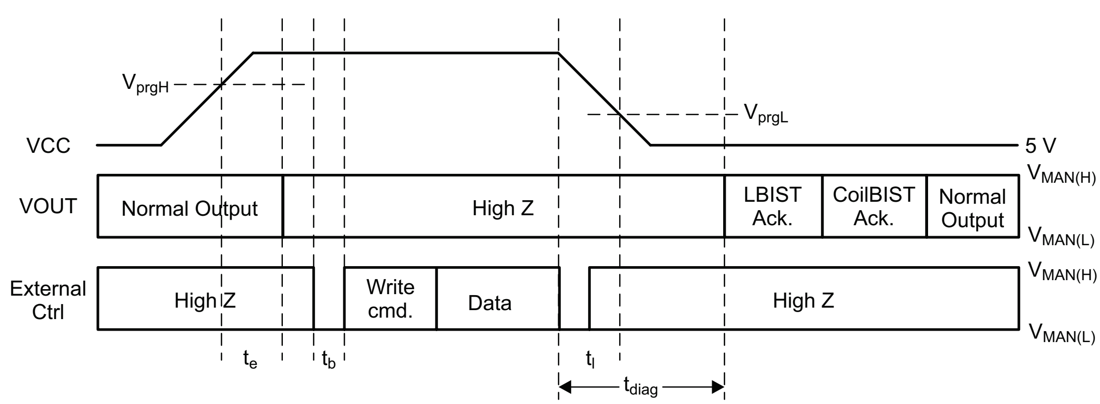


Figure 28: BIST Request

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Serial Interface Message Structure

The general format of a command message frame is shown in Figure 29. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary. The time period for the bit boundary is determined by the baud rate initiated by the external controller. The A1342 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 29.

For a Write Access command frame, the data consists of 32 bits. For a Read Request frame, the data bits are omitted. For a Read Acknowledge or Write frame the data bits are defined as shown in Figure 30, where bit 0 is the LSB.

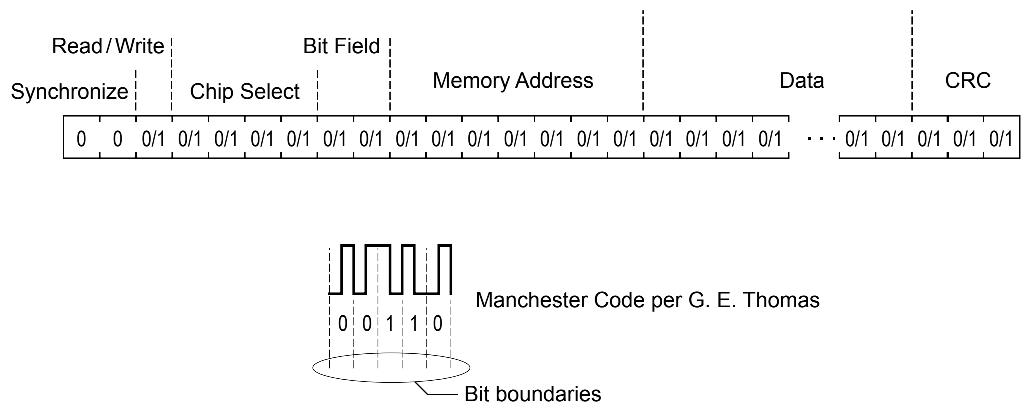


Figure 29: General Format for Serial Interface Commands

Table 20: Serial Interface Command General Format

Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command and communication bit time
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
4	Chip Select	0-15	Chip select for up to 4 die connected in parallel: XXX1 binary = device communication address 0 XX1X binary = device communication address 1 X1XX binary = device communication address 2 1XXX binary = device communication address 3 0000, 1111 binary = Broadcast
2	Field Select	0-2	Selects field for partial register access (R/W) 0: Access entire 32 bits of data from address 1: Access bits 11-0 of data from address 2: Access bits 25-12 of data from address 3: Not used
7	Address		[Read/Write] Register address EEPROM: 0x00-0x1F Shadow Memory: 0x20-0x3F Volatile Memory: 0x40-0x7F
32	Data		[Write] 26 data bits and 6 ECC bits
3	CRC		Bits to check the validity of the frame

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Read and Write Transmission

The A1342 has an advanced read and write message format that permits reading and writing a partial bits of a selected address. The addresses are split into two bit fields; field 1 contains bits [11:0], field 2 contains bits [25:12]. The field select bits in the message frame determine how an address is accessed. For a description, see Figure 30.

CRC

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check). The CRC algorithm is based on the following polynomial, and the calculation is represented graphically in Figure 31.

$$g(x) = x^3 + x + 1 \ ,$$

The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111 (see Figure 31).

Field	31	---	26	25	---	14	13	12	11	---	0	Data Bit
F=0	Write = DC Read = ECC			Field 2 data [25:12]					Field 1 data [11:0]			Entire Register
F=1	Write = don't care (DC), Read = 0								Field 1 data [11:0]			Field 1 only
F=2	Write = don't care (DC), Read = 0						Field 2 data [25:12]					Field 2 only

Figure 30: Read Acknowledge or Write Frame General Structure

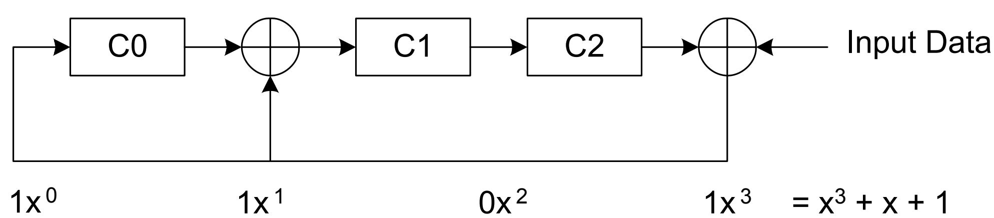


Figure 31: CRC Calculation

Customer/Factory Access Modes

The internal memory is accessible via the serial interface. The memory address space is divided into two areas: Factory and Customer.

Access is controlled by a specific code, which must be loaded within 500 milliseconds of power-on. The access codes are constants. The customer access code is given in Table 21.

For software convenience, the table gives an 8 bit "address" and 32 bit "data" field, similar to a normal Write command format (the address and data fields concatenated yield the full access code). The Customer area can be written only if the serial interface receives a Customer Unlock code within 500 milliseconds after power-on reset. When the customer access code is received, factory registers are addressable but are read only.

Table 21: Customer Access Code

Name	Serial Interface Format	
	Address (Hex)	Data (Hex)
Customer	0x79	0xC41D3432

Customer Memory Lock

The A1342 contains lock features to prevent access to the device memory. The EEPROM parameter, dev_lock bits [2:0] in register cfg_c, configure the lock mode. When dev_lock is set to 0, 1, 2, 4, or 7, full read and write access to the EEPROM is enabled. When dev_lock is set to 3, write access to the EEPROM is disabled, write access to the volatile memory is enabled, and read access to the entire memory is enabled. When dev_lock is set to 6, write access to the device is disabled and read access to the entire memory is enabled. When dev_lock is set to 5, all write and read access to the device is disabled.

Note:
Setting dev_lock to 5 may limit some factory debug support.

EEPROM Margin Checking

The A1342 contains a test mode, called EEPROM Margining, to check the logic levels of the EEPROM bits. EEPROM margining is accessible with customer EEPROM access. EEPROM margining is selectable to check all logic 1 bits, logic 0 bits, or both. To run EEPROM Margining—checking both logic 1 and logic 0 bits for the entire EEPROM—write the parameter margin_start in address marg_tst_c, 0x43, to logic 1. The results of the test are reported back in EEPROM registers ee_data_c, 0x41, and ee_status_c, 0x42. For more EEPROM Margining information and options, refer to the table Memory Address Map.

Note:
A fail of the margin test does not force the output to a diagnostic state.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

MEMORY ADDRESS MAP

Table 22: Memory Address Map

Type [1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
eeprom (continued on the next page)	id_cfg	wlot_f	0x00	factory_lot	Factory Lot Number	ro	16	15	0
				factory_wafer	Factory Wafer Number	ro	6	21	16
				unused		ro	4	25	22
		id_f	0x01	x_die_loc	8-bit X die location	ro	8	7	0
				y_die_loc	8-bit Y die location	ro	8	15	8
				unused		ro	10	25	16
		id_c	0x02	cust_id	Bits reserved for customer ID	rw	22	21	0
				die_addr_0	Die address for Manchester communication and Shared SENT	rw	1		22
				die_addr_1	Die address for Manchester communication and Shared SENT	rw	1		23
				unused		rw	2	25	24
	sens_c	sens_trim_c	0x03	sens_c	Customer Sensitivity trim (fine)	rw	11	10	0
				unused		rw	1		11
				sensm_c	Customer Sensitivity trim (coarse) multiplier: 0: 1× 1: 2× 2: 4× 3: 8× 4: 16× 5: 32× 6: 32× 7: 32×	rw	3	14	12
				pol_c	Magnetic sensitivity polarity (0 = + south pole, 1 = – south pole)	rw	1		15
				bw_sel_c	Bandwidth selection for signal path IIR filter: 0: 40 Hz 1: 160 Hz 2: 680 Hz 3: 3000 Hz 4-7: 7400 Hz	rw	3	18	16
				bw_sel_comp_c	Reference coil path bandwidth selection for IIR Filter: 0: 0.08 Hz 1: 0.3 Hz 2: 1.25 Hz 3: 4 Hz 4-7: 16 Hz	rw	3	21	19
				ee_spare_c	Spare control in customer space. Brought to top level outputs.	rw	4	25	22
		senstc1_c	0x04	senstc1_hot_c	1st order customer sensitivity temperature compensation, room to hot	rw	11	10	0
				unused		rw	1		11
				senstc1_cld_c	1st order customer sensitivity temperature compensation, room to cold	rw	11	22	12
				unused1		rw	3	25	23
		senstc2_c	0x05	senstc2_hot_c	2nd order customer sensitivity temperature compensation, room to hot	rw	10	9	0
				unused		rw	2	11	10
				senstc2_cld_c	2nd order customer sensitivity temperature compensation, room to cold	rw	10	21	12
				unused1		rw	4	25	22
	qout_c	qo_trim_c	0x06	qo_c	Customer Quiescent Output (QO) adjustment (fine)	rw	16	15	0
				unused		rw	10	25	16
		qotc_c	0x07	qotc_hot_c	1st order QO temperature compensation, room to hot	rw	12	11	0
				qotc_cld_c	1st order QO temperature compensation, room to cold	rw	12	23	12
				unused		rw	2	25	24
		clamp_c	0x08	clamph	High Clamp: 0x000 = upper rail, 0xFFF = clamph(min)	rw	12	11	0
				clampl	Low Clamp: 0x000 = lower rail, 0xFFF = clampl(max)	rw	12	23	12
				unused		rw	2	25	24

Continued on the next page…

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 22: Memory Address Map (continued)

Type [1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
eeprom (continued)		cfg_c	0x09	dev_lock	0 - Write and read access permitted. 1 - Write and read access permitted. 2 - Write and read access permitted. 3 - EEPROM Lock: Prevents writes to EEPROM but all registers including shadow can be written. All registers and EEPROM can be read. 4 - Write and read access permitted. 5 - Full Lock: Prevents all access to the device. 6 - Write Lock: Prevents writing anything to either EEPROM or registers. All registers and EEPROM can still be read. 7 - Write and read access permitted.	rw	3	2	0
				unused1		rw	7	9	3
				cfg_spcmin_adj	Determines minimum low time for detecting an SSENT, Long Trigger Mode, F_OUTPUT command. 0: 7 ticks 1: 8 ticks 2: 9 ticks 3: 10 ticks	rw	2	11	10
				out_msg_imm	0: Waits after a power-on reset for some time to allow signal path to settle before sending first PWM or SENT message 1: Do not wait for signal path to settle before sending first PWM or SENT message	rw	1		12
				coil_freq	Fraction of time coil is turned on. When coil is off, triggered CoilBIST can be invoked with a BIST request. 0: Coil always on 1: 1/2 time 2: 1/256 time 3: Coil always off, CoilBIST acknowledge is available following BIST.	rw	2	14	13
				report_dig_err	Has no function.	rw	1		15
				coilcomp_dis	0: Coil compensation remains enabled 1: Disables coil compensation	rw	1		16
				diag_mode	0: Default outputs a diag message in PWM / SENT 1: Outputs is high Z for all diagnostic errors. Only supported when V_{OUT} is configured for PWM, outmsg_mode = 0.	rw	1		17
				lbist_dis	0: BIST check enabled following a BIST request. 1: Prevent BIST check from responding to a BIST request	rw	1		18
				coilbist_dis	0: Coil measurement monitor will report errors 1: Prevent coil measurement monitor from reporting errors at the output	rw	1		19
				uvd_dis	0: Undervoltage errors will be reported 1: Prevent undervoltage detection from reporting errors at the output	rw	1		20
				ovd_dis	0: Overvoltage errors will be reported 1: Prevent overvoltage detection from reporting errors at the output	rw	1		21
				otmp_dis	0: Overtemperature errors will be reported 1: Prevent overtemperature monitor from reporting errors at the output	rw	1		22
				oor_dis	0: Magnetic signal out-of-range errors will be reported 1: Prevent out-of-range monitor from reporting errors at the output	rw	1		23
				lbist_ack	Determines if a Logic BIST acknowledge message (SENT or PWM) should be transmitted following BIST 0: Do not send a message 1: Send a message	rw	1		24
				coilbist_ack	Determines if a CoilBIST acknowledge message (SENT or PWM) should be transmitted following BIST 0: Do not send a message 1: Send a message	rw	1		25
	lin_c (continued on next page)	lin0_c	0x0A	lint00	Linearization Table entry 0	rw	12	11	0
				lint01	Linearization Table entry 1	rw	12	23	12
				unused		rw	2	25	24
		lin1_c	0x0B	lint02	Linearization Table entry 2	rw	12	11	0
				lint03	Linearization Table entry 3	rw	12	23	12
				unused		rw	2	25	24
		lin2_c	0x0C	lint04	Linearization Table entry 4	rw	12	11	0
				lint05	Linearization Table entry 5	rw	12	23	12
				unused		rw	2	25	24

Continued on the next page…

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 22: Memory Address Map (continued)

Type [1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
eeprom (continued)	lin_c	lin3_c	0x0D	lint06	Linearization Table entry 6	rw	12	11	0
				lint07	Linearization Table entry 7	rw	12	23	12
				unused		rw	2	25	24
		lin4_c	0x0E	lint08	Linearization Table entry 8	rw	12	11	0
				lint09	Linearization Table entry 9	rw	12	23	12
				unused		rw	2	25	24
		lin5_c	0x0F	lint10	Linearization Table entry 10	rw	12	11	0
				lint11	Linearization Table entry 11	rw	12	23	12
				unused		rw	2	25	24
		lin6_c	0x10	lint12	Linearization Table entry 12	rw	12	11	0
				lint13	Linearization Table entry 13	rw	12	23	12
				unused		rw	2	25	24
		lin7_c	0x11	lint14	Linearization Table entry 14	rw	12	11	0
				lint15	Linearization Table entry 15	rw	12	23	12
				unused		rw	2	25	24
		lin8_c	0x12	lint16	Linearization Table entry 15	rw	12	11	0
				lint_e	0: Bypass linearization table 1: Enable valid linearization table	rw	1		12
				lint_bin_e	0: Linearization mode functions normally if enabled by lint_e 1: Enable bin mode for linearization table	rw	1		13
				lint_out_inv	0: Normal output of linearization table 1: Invert output of linearization table	rw	1		14
				lint_in_inv	0: Normal input to linearization table 1: Invert input of linearization table	rw	1		15
				unused		rw	10	25	16
		post_lin_c	0x13	plin_sens	Post Linearization sensitivity adjustment	rw	12	11	0
				plin_qvo	Post Linearization offset adjustment	rw	12	23	12
				unused		rw	2	25	24
		out_cfg_c (continued on next page)	0x14 (cont. next page)	outmsg_mode	0: PWM 1: SENT 2: TSENT 3: SSENT, Long Trigger Mode 4: SSENT, Short Trigger Mode 5-7: ASENT	rw	3	2	0
				sent_pwm_rate	Specifies the frequency of the SENT or PWM message. This is shown in Table 14.	rw	5	7	3
				sent_data_cfg	Only valid for SENT modes. Number and format of data nibbles in SENT frame. 0: 3 Data Nibbles 1: 6 Nibbles- 3 Magnetic Data Nibbles, 2 Diagnostic Flag Nibbles, 1 Counter Nibble 2: 6 Nibbles- 3 Magnetic Data Nibbles, 3 Counter Nibbles 3: 6 Nibbles- 3 Magnetic Data Nibbles, 3 Temperature Sensor Output Nibbles	rw	2	9	8
				sent_slow_ser_dis	Selects bits for SCN[3:2], Only valid for SENT mode. 0: Enables the slow serial message stream. 1: Disables the slow serial message stream. SCN bits are determined by sen_no_smsg	rw	1		10
				outdrv_sel	Adjust fall time of digital output. This is shown in Table 12.	rw	3	13	11
				sen_crc_has_scn	Determines if SCN is included in CRC 0: SCN not included in CRC 1: SCN included in CRC	rw	1		14
				sen_no_smsg	Selects bits for SCN[3:2], Only valid for SENT mode. Only valid if sent_slow_ser_dis = 1 0: SCN[3:2] = All Zeros 1: SCN[3:2] = Device ID.	rw	1		15

Continued on the next page…

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 22: Memory Address Map (continued)

Type [1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
eeprom (continued)		out_cfg_c (continued)	0x14 (cont.)	cfg_max_sensor	Highest sensor number on the bus for SSENT	rw	2	17	16
				cfg_diag_adr	Sets whether the diagnostic trigger is for a specific addressed sensor, or broadcast to all sensors 0: Diagnostic Trigger is broadcast mode (all sensors) 1: Diagnostic trigger is addressing mode (only addressed sensor)	rw	1		18
				cfg_no_sample	0: F_SAMPLE will cause the sensor to sample and hold magnetic data 1: F_SAMPLE will not create a sample and hold of the magnetic data	rw	1		19
				cfg_fsample_adr	0: F_SAMPLE will not address the sensor 1: F_SAMPLE will be an addressing (frame request) as well as a sample and hold request	rw	1		20
				cfg_idle_sync	0: A bus idle will not resynchronize the sensors 1: For SSENT Short or Long, a bus idle time of > 510 ticks will act as an F_SYNC pulse	rw	1		21
				cfg_por_offline	0: The sensor will come online after a power-on reset 1: the sensor will be in OFFLINE mode following a power-on reset (but not a reset that is not also power-on) and will require an F_SYNC pulse to come online	rw	1		22
				cfg_slot_marking	0: SSENT will not include slot marking times 1: for SSENT, the slot marking times will be applied prior to the start of a frame NOTE: This option is not reccommended for tick times below 1.22 µs	rw	1		23
				cfg_slot_sync	0: Slot marking will not resynchronize the slot counter 1: for SSENT and cfg_slot_marking=1, then the sequencer will use the slot marking to synchronize the slot counter	rw	1		24
				cfg_zero_sample	0: A sample and hold will only be requested using an F_SAMPLE pulse 1: For SSENT, a sample_and_hold will be requested when the slot counter is 0	rw	1		25
		Reserved	0x15-0x1F		Address 0x15 through 0x1F reserved for factory use	ro			
shadow			0x22-0x3F		Addresses 0x22 through 0x3F are reserved for shadow memory, a volitile representation of EEPROM. 0x22 is shadow from 0x02.				
volatile (continued on the next page)		test_c	0x40	out_dis	0: No effect 1: test mode to disable output	rw	1		0
				ee_test_addr	If ee_use_test_addr is set, then margining or check testing will start at this address. If the test fails, this will contain the failing address	rw	5	19	15
				ee_use_test_addr	0: No effect 1: Uses ee_test_addr as the start address for margining. If ee_loop is set, this bit is ignored and the starting address is always 0x0	rw	1		20
				ee_loop	0: Test completes at final address or fail 1: Test loops until MARGIN_START is written low or fail	rw	1		21
				comm_en	Allows for serial communication without raising VCC 0: Default mode. VCC must be raised to allow serial communication 1: Serial communication can occur with VCC at nominal operating level	rw	1		22
		ee_data_c	0x41	ee_data	If margin or self test fails this is the failed data read from EEPROM.	rw	26	25	0
		ee_status_c	0x42	ee_dbe_flag	Latched and held high when a dbe has occurred.	rw	1		0
				ee_sbe_flag	Latched and held high when a sbe has occurred.	rw	1		1
				ee_err	Indicates an EEPROM write error occurred. This bit is latch and hold with clear on read.	rc	1		2
				ee_err_status	When ee_err is asserted this parameter contains a factory error code for the aborted EEPROM write transaction	ro	5	7	3
				ee_addr	Reflects the read/write address to the EEPROM. This allows for a manual write to the EEPROM or will contain data read from the EEPROM if magining or self check fails.	rw	5	12	8
				ee_ecc	Reflects bits [29:24] to be written to the eeprom or read from the eeprom. This allows for a manual write to the EEPROM or will contain data read from the EEPROM if magining or self check fails.	rw	6	18	13
				cp_err	High to indicate an error occurred during charge pump ramp. ee_err_status stores information about the error.	rc	1		19

Continued on the next page…

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 22: Memory Address Map (continued)

Type [1]	Group	Register Name	Addr	Field Name	Description	Access	Size	MSB	LSB
volatile (continued)		marg_tst_c	0x43	margin_min_ max_fail	If margining fails, this bit indicates if the min or max reference failed. 0: Min margining failed. 1: Max margining failed.	ro	1		5
				margin_status	Bits are cleared after a read or reset. 0: Reset condition (no result from margin testing) 1: Pass, no failure detected during margin testing 2: Fail, failure detected during margin testing 3: Running, margin test is still running	ro	2	4	3
				margin_no_min	Does not perform minimum margin testing 0: Margining done a min voltage. 1: No margining at min voltage	rw	1		2
				margin_no_max	Does not perform maximum margin testing 0: Margining done a max voltage. 1: No margining at max voltage.	rw	1		1
				margin_start	Write to 1 to start margin testing. If EE_LOOP is low, this bit will self clear when address 0x1F is reached. If EE_LOOP is high, this bit must be written to 0 to stop test. This bit always clears on a fail.	rw	1		0
		status_c	0x44	cust_access	Indicates customer access enabled	ro	1		25
		err_status_c	0x45	diag_reg_c	Status bits to report diagnostic errors. 0 = no errors Bit [0] = 1: EEPROM Dual Bit Error Bit [1] = 1: Logic BIST Error Bit [2] = 1: CoilBIST error Bit [3] = 1: Undervoltage Error Bit [4] = 1: Overvoltage Error Bit [5] = 1: Overtemperature Error Bit [6] = 1: Signal Out of Range Low Error Bit [7] = 1: Signal Out of Range High Error	rw	8	23	16
		lbist_ctrl_c	0x46	run_lbist	Runs BIST and may send result via SENT/PWM depending on customer configuration settings.	wo	1		0
				lbist_sig	LBIST Ack: 0x8A0 (Bit [7] = lbist pass [6:0] = lbist crc)	ro	8	11	4
				abist_sig	ABIST Ack: [9:0] = CoilBIST acknowledge value. Passing values between 0x333 to 0xCD (2's complement).	ro	10	21	12
	sigpath_c	sigpath_byp_c	0x47	byp_trim_c	0: No effect 1: Bypass Customer Sensitivity and Offset trim	rw	1		0
				byp_tc_c	0: No effect 1: Bypass Customer sensitivity and offset temp. compensation	rw	1		1
				byp_lint	0: No effect 1: Bypass Linearization block	rw	1		2
				byp_plin	0: No effect 1: Bypass Post-Linearization Trim block	rw	1		3
				byp_clamp	0: No effect 1: Bypass Clamp block	rw	1		4
		temp_out_c	0x48	temp_out	Output of Temp Sensor Trim block	ro	12	11	0
		mag_out_c	0x49	mag_out	Output of the magnetic signal path	ro	12	11	0
		Reserved	0x4A-0X59		Addreses 0x4A through 0x59 reserved for factory use				

[1] All EEPROM addresses contain 32 bits. Bits 26 through 31 are used for EEPROM diagnostics. For more information, see Application Information: EEPROM Diagnostics.

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PROGRAMMABLE PARAMETER REFERENCE

Table 23: die_addr_0: Address 0x02, field 2, bit 22
die_addr_1: Address 0x02, field 2, bit 23

<table>
<tr><td>Function</td><td>Sets address of the die for SENT and Addressable Manchester</td></tr>
<tr><td>Syntax</td><td>Quantity of bits 2 (1 for each parameter)</td></tr>
<tr><td>Related Commands</td><td>outmsg_mode</td></tr>
<tr><td>Values</td><td><table>
<tr><th>die_addr_1</th><th>die_addr_0</th><th>Device Address</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>3</td></tr>
</table></td></tr>
<tr><td>Options</td><td></td></tr>
</table>

Table 24: : bw_sel_comp_c: Address 0x03, field 2, bits 21:19

Function	Sets the 3 dB frequency of the calibration path filter for noise reduction. This setting has no effect on CoilBIST response time.
Syntax	Quantity of bits 3
Related Commands	
Values	Code: 3 dB (Hz) 0: 0.08 Hz, 1: 0.3 Hz, 2: 1.25 Hz, 3: 4 Hz, 4-7: 16 Hz
Options	

Table 25: bw_sel_c: Address 0x03, field 2, bits 18:16

Function	Sets the 3 dB frequency for input magnetic signal path noise reduction
Syntax	Quantity of bits: 3
Related Commands	
Values	Code: 3 dB (Hz) 0: 40 Hz, 1: 160 Hz, 2: 680 Hz, 3: 3000 Hz, 4-7: 7400 Hz Note: Decreasing the calibration path filter bandwidth may decrease the noise, while increasing the signal path compensation settling.
Options	

Table 26: clamph: Address 0x08, field 1, bits 11:0

Function	Sets level for the upper output clamp
Syntax	Quantity of bits: 12 Inverted, unsigned
Related Commands	clampl
Values	0x0: Default, Upper output clamp is at $OUT_{CLP(HIGH)}$(max) 0xFFF: Upper output clamp is at $OUT_{CLP(HIGH)}$(min)
Options	

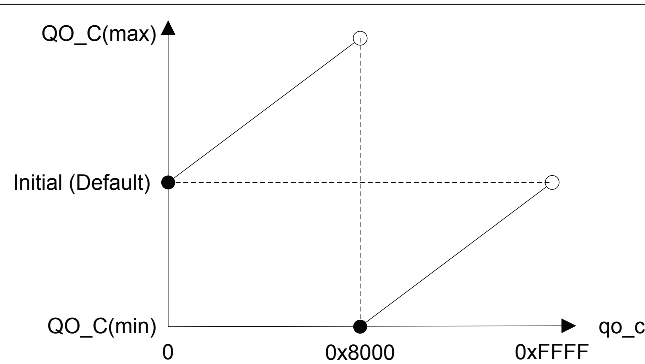
Table 27: clampl: Address 0x08, field 2, bits 23:12

Function	Sets level for the lower output clamp
Syntax	Quantity of bits: 12
	unsigned
Related Commands	clamph
Values	0x0: Default, lower output clamp is at $OUT_{CLP(LOW)}$(min) 0xFFF: Upper output clamp is at $OUT_{CLP(LOW)}$(max)
Options	
Examples	

Table 28: sent_pwm_rate: Address 0x14, field 1, bits 7:3

Function	Sets the PWM Frequency or SENT Tick Time
Syntax	Quantity of bits: 5
Related Commands	outmsg_mode
Values	Refer to Table 14: PWM Frequency / SENT Tick Times for values.
Options	
Examples	

Table 29: qo_c: Address 0x06 bits 15:0

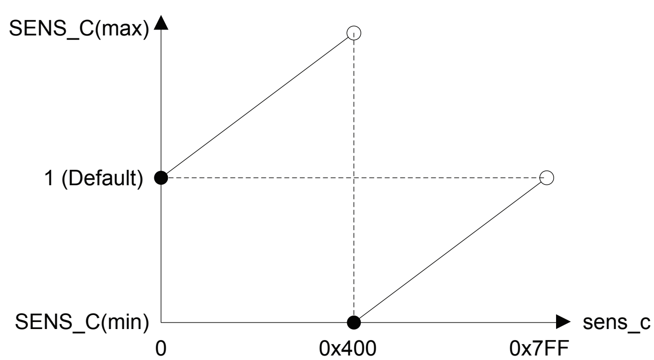
Function	Fine quiescent output adjustment
Syntax	Quantity of bits: 16 signed
Related Commands	
Values	
Options	
Examples	See Operating Characteristics

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 30: sensm_c: Address 0x03, field 2, bits 14:12

Function	Coarse Sensitivity adjustment, SENS_COARSE. Multiplier applied to the nominal factory Sensitivity, $SENS_{INIT}$.	
Syntax	Quantity of bits: 3	
Related Commands	sens_c	
Values	0 = 1× (default)	4 = 16×
	1 = 2×	5 = 32×
	2 = 4×	6 = Not used
	3 = 8×	7 = Not used
Options		
Examples	See Operating Characteristics	

Table 31: sens_c: Address 0x03, field 1, bits 10:0

Function	Fine Sensitivity adjustment, SENS_C. Multiplier applied after the Coarse Sensitivity adjustment.
Syntax	Quantity of bits: 11 signed
Related Commands	sensm_c
Values	
Options	
Examples	See Operating Characteristics

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 32: senstc1_hot_c: Address 0x04, field 1, bits 10:0
senstc1_cld_c: Address 0x04, field 2, bits 22:12

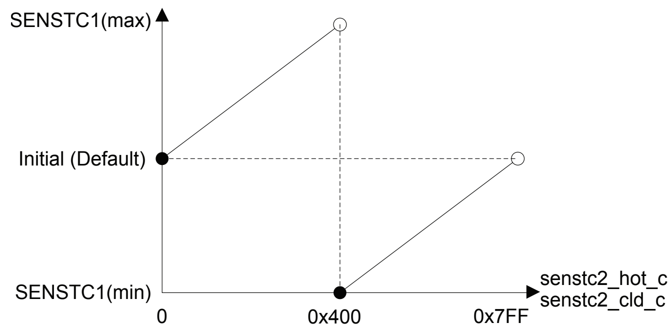
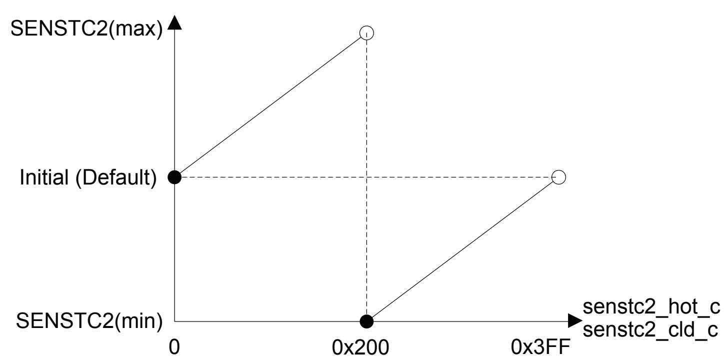
Function	First order Sensitivity Temperature Compensation, segmented for hot (25°C < T_A ≤ 150°C) and cold (–40°C ≤ T_A < 25°C)
Syntax	Quantity of bits: 11 signed
Related Commands	
Values	
Options	
Examples	

Table 33: senstc2_hot_c: Address 0x04, field 1, bits 9:0
senstc2_cld_c: Address 0x04, field 2, bits 21:12

Function	Second order Sensitivity Temperature Compensation, segmented for hot (25°C < T_A ≤ 150°C) and cold (–40°C ≤ T_A < 25°C)
Syntax	Quantity of bits: 10 signed
Related Commands	
Values	
Options	
Examples	

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000409, Rev. 1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

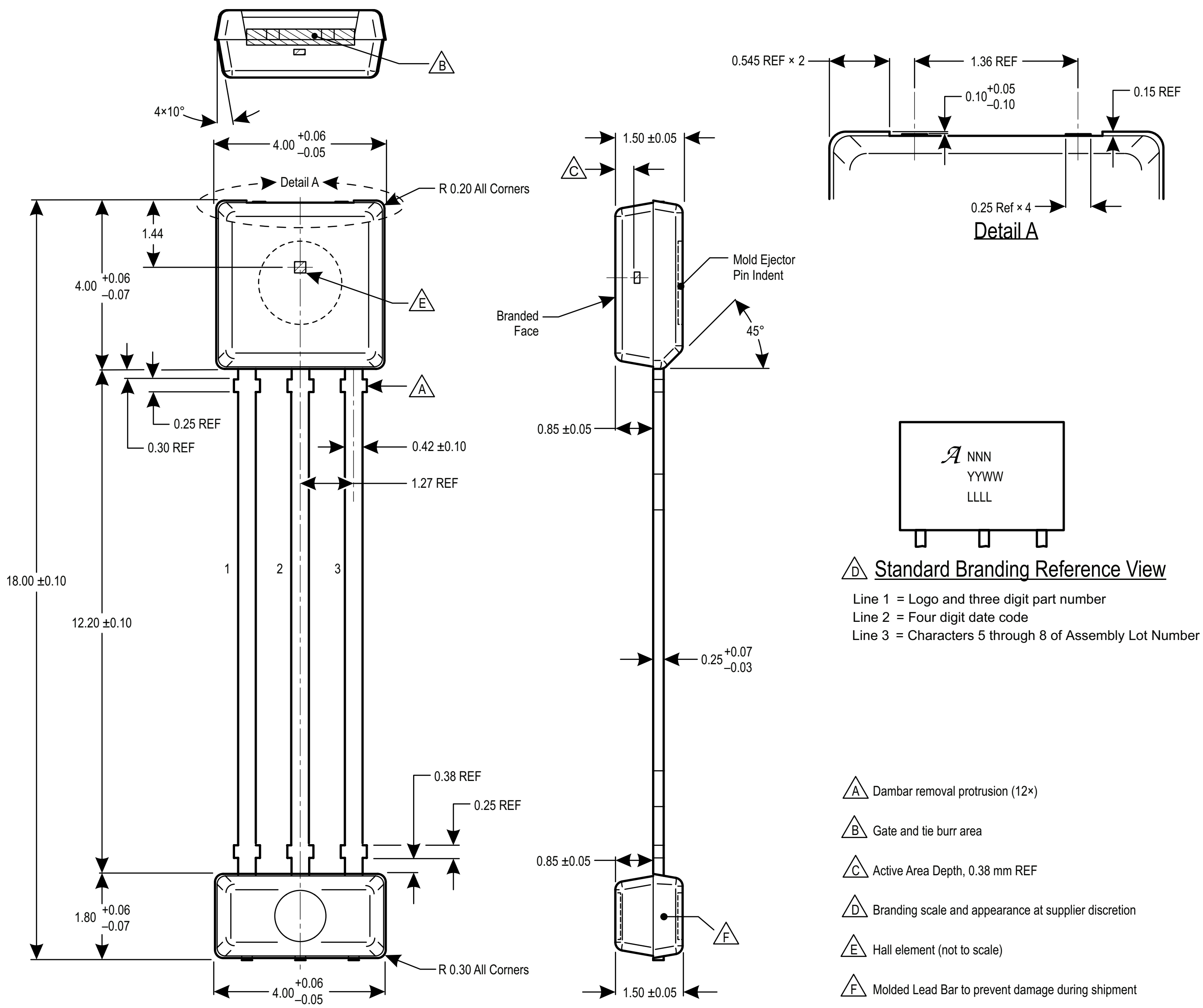


Figure 32: Package UC, 3-Pin SIP

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	August 24, 2016	Initial release
1	December 2, 2016	Updated Functional Block Diagram (page 1), Features and Benefits (page 2), Electrical Characteristics (Bandwidth, page 5), Magnetic Characteristics (Input Field Range, Initial Sensitivity, page 7), Programmable Characteristics (Output Sensitivity Trim Range, page 9), Figure 8 (page 15), EEPROM Diagnostics (page 17), Diagnostic Summary table (page 18), Table 8 (SENT Output Trigger Signal, page 19), Memory Address Map (pages 38-42), and Package Outline Drawing (page 47)
2	January 25, 2019	Updated Table 7 (p. 18),Table 8 (p. 19), and Table 19 (p. 32), and minor editorial updates

Copyright ©2019, Allegro MicroSystems, LLC

Allegro MicroSystems, LLC reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, LLC assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:

www.allegromicro.com

Allegro MicroSystems, LLC
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com