Micropower, 10-Bit Current Output DAC with SMBus Serial Interface

FEATURES

- **Precision 50µA, ±1.5% Initial Full-Scale Output Current, ±2.5% Over Temperature**
- Wide Output Voltage DC Compliance: –15V to (V_{CC} – 1.3V)
- Wide Supply Range: 2.7V ≤ V_{CC} ≤ 5.5V
- Supply Current in Shutdown: 10µA Typ
- Low Supply Current: 115µA Typ
- Available in 8-Pin SO
- **SMBus Serial Interface**
- **Four Selectable SMBus Addresses**
- DAC Powers Up at Zero or Midscale
- DAC Contents Are Retained in Shutdown

APPLICATIONS

- LCD Contrast and Backlight Brightness Control
- Power Supply Voltage Adjustment
- Battery Charger Voltage/Current Adjustment
- GaAs FET Bias Adjustment
- Trimmer Pot Elimination

DESCRIPTION

The LTC®1427-50 is a micropower, 10-Bit current output DAC with an output range of 0µA to 50µA. The DAC output is guaranteed monotonic and DNL is less than 0.9LSB under all operating conditions. Full-scale accuracy is ±2.5% over the commercial temperature range. The LTC1427-50 operates with power supply voltages from 2.7V to 5.5V and the DAC current source output can be biased from (V_{CC} – 1.3V) to –15V.

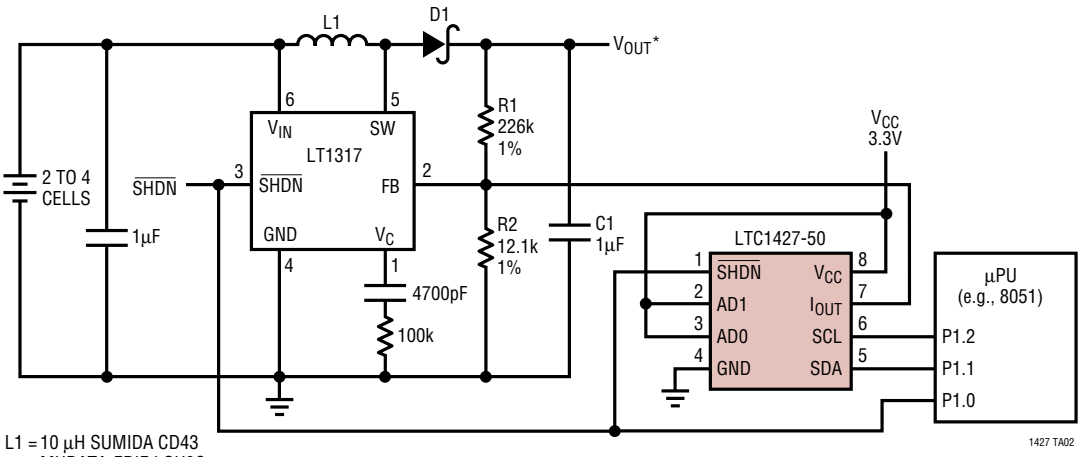
The LTC1427-50 communicates with external circuitry by using the SMBus serial interface. It acts as an SMBus slave device using one of four selectable SMBus addresses set by the two address pins AD0 and AD1 .

On power-up, the DAC output assumes midrange or zero scale, depending on the logic state of the two address pins. The LTC1427-50 can be shut down through the $\overline{SHDN}$ pin or by setting the SHDN bit = 1 in the SMBus command byte. Digital data for the DAC output is retained internally and the supply current drops to 10µA typically when in shutdown.

The LTC1427-50 is available in an 8-pin SO package.

TYPICAL APPLICATION

Digitally Controlled LCD Bias Generator



L1 = 10 µH SUMIDA CD43
MURATA-ERIE LQH3C
OR COILCRAFT DO1608
D1 = MBR0530

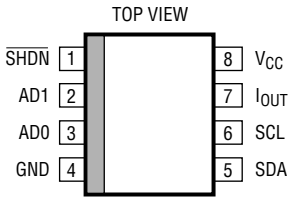
*V_{OUT} = 12.7V TO 24V IN 11mV STEPS
15mA (2 CELLS)
35mA (3 CELLS)

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC}) 7V
Input Voltage (All Inputs)..... –0.3V to (V_{CC} + 0.3V)
DAC Output Voltage ..... –15V to (V_{CC} + 0.3V)
DAC Output Short-Circuit Duration ..... Indefinite
Operating Ambient Temperature Range ..... 0°C to 70°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LTC1427CS8-50
S8 PART MARKING
14275

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	$V_{\overline{SHDN}} = V_{SCL} = V_{SDA} = V_{CC} = 3.3V$ $V_{\overline{SHDN}} = 0V$	● ●		115 10	225 25	µA µA
	DAC Resolution		●		10		Bits
I_{FS}	DAC Full-Scale Current	$V_{CC} = 3.3V$, $V(I_{OUT}) = 0V$	 ●	49.25 48.75	50 50	50.75 51.25	µA µA
I_{ZS}	DAC Zero-Scale Current	$V_{CC} = 3.3V$, $V(I_{OUT}) = 0V$	●		±0.1	±200	nA
DNL	DAC Differential Nonlinearity	$V_{CC} = 3.3V$, Monotonicity Guaranteed, $V(I_{OUT}) = 0V$	●		±0.15	±0.9	LSB
	Supply Voltage Rejection	$V_{CC} = 2.7V$ to $5.5V$, $V(I_{OUT}) = 0V$	●			±8	LSB
	Output Voltage Rejection	$V_{CC} = 3.3V$, Full-Scale Current, $-15V \le V(I_{OUT}) \le 2V$	●			±5	LSB
I_{IN}	Logic Input Current	$0V \le V_{IN} \le V_{CC}$	●			±1	µA
V_{IH}	High Level Input Voltage	AD0, AD1 $\overline{SHDN}$ SCL, SDA	● ● ●	$V_{CC} - 0.3$ 2.4 1.4			V V V
V_{IL}	Low Level Input Voltage	$\overline{SHDN}$, AD0, AD1 SCL, SDA	● ●			0.8 0.6	V V
V_{OL}	Low Level Output Voltage	$I_{OUT} = 3mA$, SDA Only	●			0.4	V

RECOMMENDED OPERATING CONDITIONS

V_{CC} = 3.3V, T_A = operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SMBus Timing (Notes 2, 3)							
f_{SMB}	SMB Operating Frequency		●	10		100	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		●	4.7			µs
$t_{HD:STA}$	Hold Time After (Repeated) Start Condition		●	4.0			µs
$t_{SU:STA}$	Repeated Start Condition Setup Time		●	4.7			µs
$t_{SU:STO}$	Stop Condition Setup Time		●	4.0			µs
$t_{HD:DAT}$	Data Hold Time		●	300			ns
$t_{SU:DAT}$	Data Setup Time		●	250			ns
t_{LOW}	Clock Low Period		●	4.7			µs
t_{HIGH}	Clock High Period		●	4.0		50	µs
t_f	Clock/Data Fall Time		●			300	ns
t_r	Clock/Data Rise Time		●			1000	ns

The ● denotes specifications that apply over the full operating temperature range.

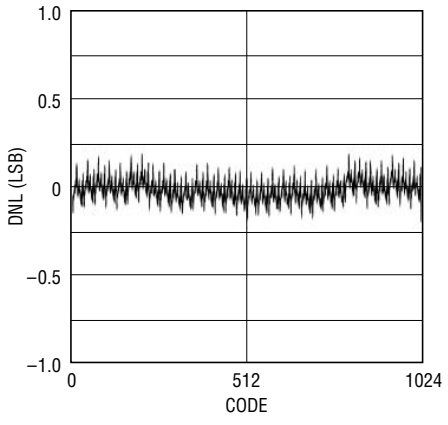
Note 1: Absolute Maximum Ratings are those beyond which the life of the device may be impaired.

Note 2: All values are referenced to V_{IH} and V_{IL} levels.

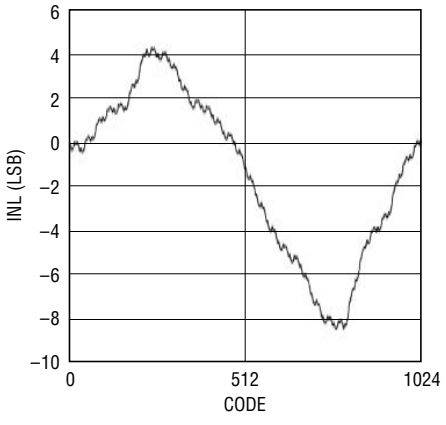
Note 3: These parameters are guaranteed by design and are not tested. Refer to the Timing Diagrams for additional information.

TYPICAL PERFORMANCE CHARACTERISTICS

DNL vs Code

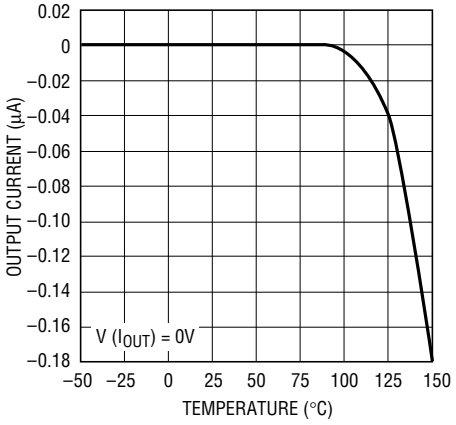


INL vs Code

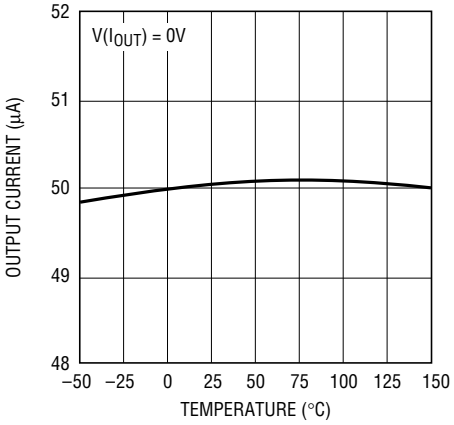


TYPICAL PERFORMANCE CHARACTERISTICS

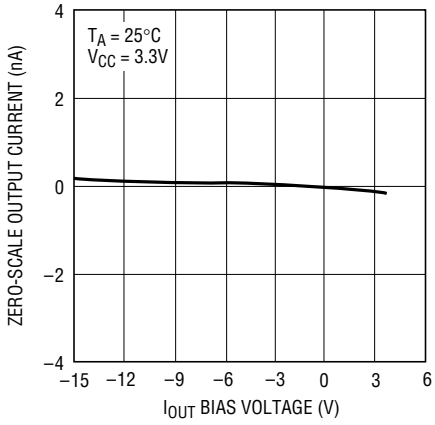
Zero-Scale Current vs Temperature



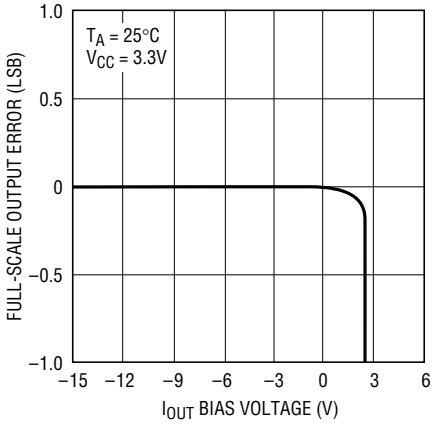
Full-Scale Current vs Temperature



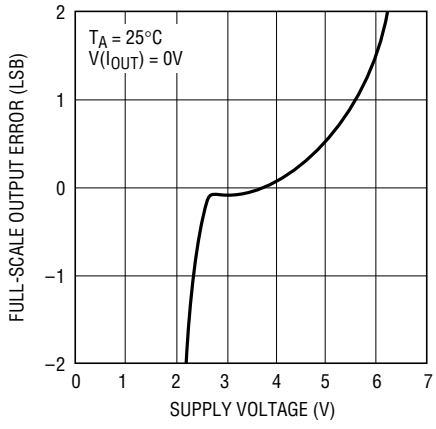
Bias Voltage Rejection (Zero-Scale Current)



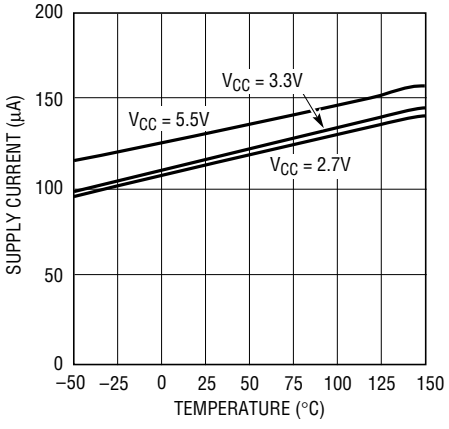
Bias Voltage Rejection (Full-Scale Current)



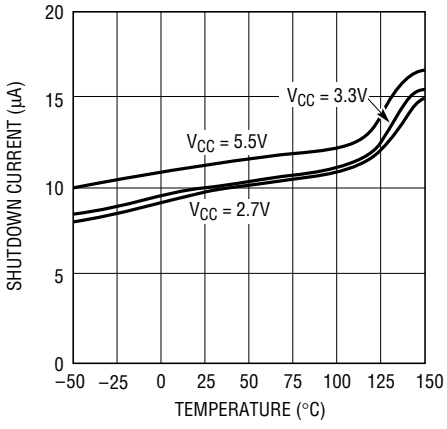
Supply Voltage Rejection



Supply Current vs Temperature



Shutdown Current vs Temperature



PIN FUNCTIONS

$\overline{SHDN}$ (Pin 1): Shutdown. A logic low puts the chip into shutdown mode. In shutdown, the digital settings for the DAC are retained. On release from shutdown, the previously programmed value for I_{OUT} is reinstated.

AD1, AD0 (Pins 2, 3): Address Selection Pins. Tie these two pins to either V_{CC} or GND to select one of four SMBus addresses to which the LTC1427-50 will respond.

GND (Pin 4): Ground. Ground should be tied directly to a ground plane.

SDA (Pin 5): SMBus Bidirectional Data Input/Digital Output. This pin is an open-drain output and requires a pull-up resistor or current source to V_{CC}. Data is shifted into the SDA pin and acknowledged by the SDA pin.

SCL (Pin 6): SMBus Clock Input. Data is shifted into the SDA pin at the rising edges of the SCL clock during data transfer.

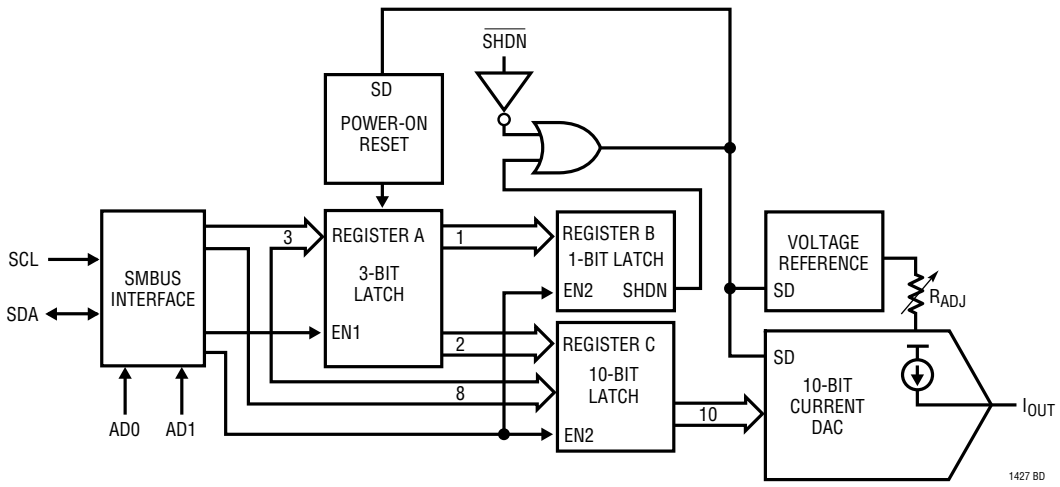
I_{OUT} (Pin 7): DAC Current Output.

V_{CC} (Pin 8): Voltage Supply. This supply must be kept free from noise and ripple by bypassing directly to the ground plane.

FUNCTION TABLE

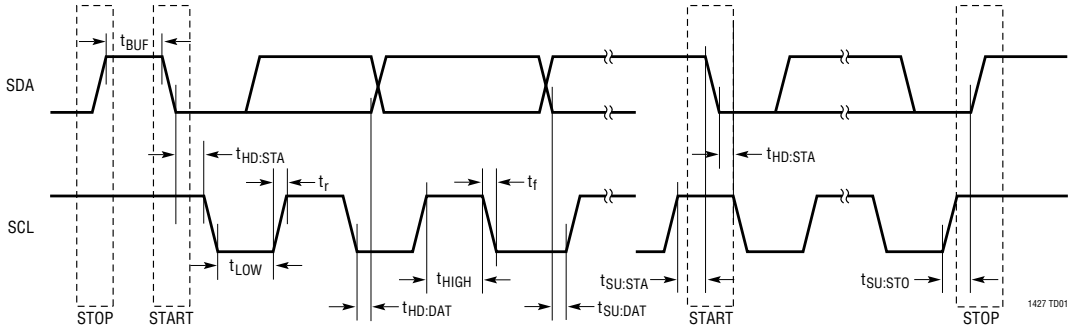
AD1	AD0	SMBus Address Location	DAC Power-Up Value	Application
L	L	0101101	Zero-Scale	CCFL Backlight Control
L	H	0101111	Zero-Scale	General Purpose
H	L	0101110	Zero-Scale	General Purpose
H	H	0101100	Midscale	LCD Contrast Control

BLOCK DIAGRAM

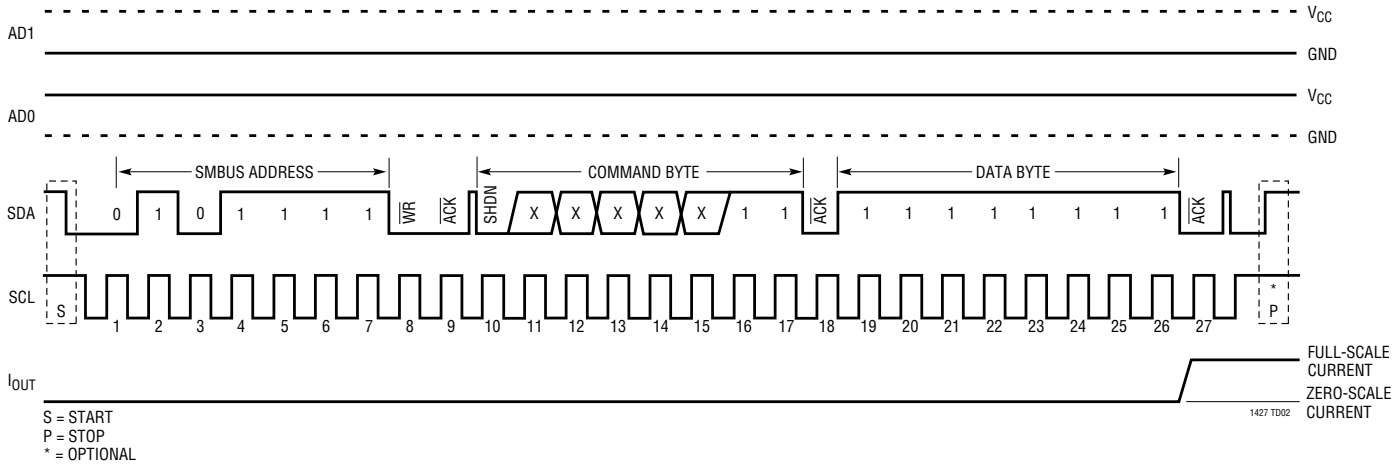


TIMING DIAGRAMS

Timing for SMBus Interface



Operating Sequence
SMBus Write Byte Protocol, with SMBus Address = 0101111B,
Command Byte = 0XXXXX11B and Data Byte = 11111111B



APPLICATIONS INFORMATION

Digital Interface

The LTC1427-50 communicates with an SMBus host using the standard 2-wire SMBus interface. The Timing Diagram shows the signals on the SMBus. The SCL and SDA bus lines must be high when the bus is not in use. External pull-up resistors or current sources are required at these lines.

The LTC1427-50 is a receive-only (slave) device. The master must apply the following Write Byte protocol to communicate with the LTC1427-50:

1	7	1	1	8	1	8	1	1
S	Slave Address	WR	A	Command Byte	A	Data Byte	A	P

S = Start Condition, WR = Write Bit, A = Acknowledge Bit, P = Stop Condition

The master initiates communication with the LTC1427-50 with a START condition (see SMBus Operating Sequence) and a 7-bit address followed by the write bit = 0. The LTC1427-50 acknowledges and the master delivers the command byte. The LTC1427-50 acknowledges and latches the active bits of the command byte into register A (see Block Diagram) at the falling edge of the acknowledge pulse. The master sends the data byte and the LTC1427-50 acknowledges the data byte. The data byte and last two output bits from register A are latched into register C at the falling edge of the final acknowledge pulse and the DAC current output assumes the new 10-bit data value (see Block Diagram). A STOP condition is optional. The com-

APPLICATIONS INFORMATION

mand code and data byte are defined with the following format:

Command Byte								Data Byte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
SHDN	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

SHDN: 0 for Normal Operation, 1 for Shutdown
D9 to D0: DAC Data Bits, D9 is the Most Significant Bit

START and STOP Conditions

At the beginning of any SMBus communication, the master must transmit a START condition by switching the SDA from high to low while SCL is high. When a master has finished communicating with a slave device, a STOP condition is issued by switching the SDA from low to high while SCL is high. The SMBus is then free for communication with another SMBus slave device.

Early STOP Conditions

The LTC1427-50 recognizes a STOP condition at any point in the SMBus communication sequence. If the STOP occurs prematurely before the data byte is acknowledged in the Write Byte protocol, the DAC output current value is not updated; otherwise internal register C is updated with the new data and the DAC output current changes correspondingly.

The Slave Address

The LTC1427-50 can respond to one of four 7-bit addresses. The first five bits have been factory programmed to 01011. The two address bits, AD1 and AD0, are programmed by the user (see Function Table).

10-Bit Current Output DAC

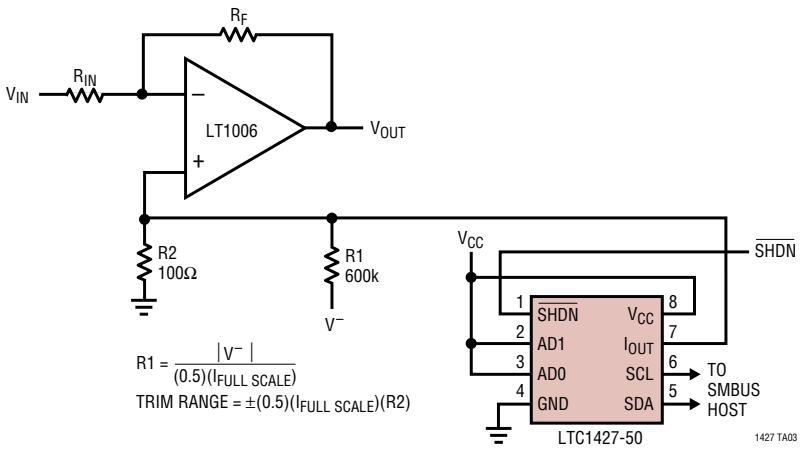
The 10-Bit current output DAC is guaranteed monotonic and is digitally adjustable in 1023 equal steps. On power-up, if AD1 and AD0 are both connected to V_{CC}, the 10-bit internal register C (see Block Diagram) resets to 1000000000B and the DAC output is set to midrange. If either AD1 or AD0 is connected to ground, register C resets to 0000000000B on power-up and the DAC output is set to zero. For the LTC1427-50, the source current output (I_{OUT}) can be biased from –15V to (V_{CC} – 1.3V). Full-scale current is trimmed to ±1.5% at room temperature and ±2.5% over the commercial temperature range.

Shutdown

There are two ways to shut down the LTC1427-50 (see Block Diagram). The LTC1427-50 will enter shutdown mode whenever it sees a logic low at the $\overline{SHDN}$ pin or whenever it receives a logic high at bit 7 of the command byte through the SMBus interface. In shutdown mode, the digital data is retained internally and the supply current drops to only 10µA typically.

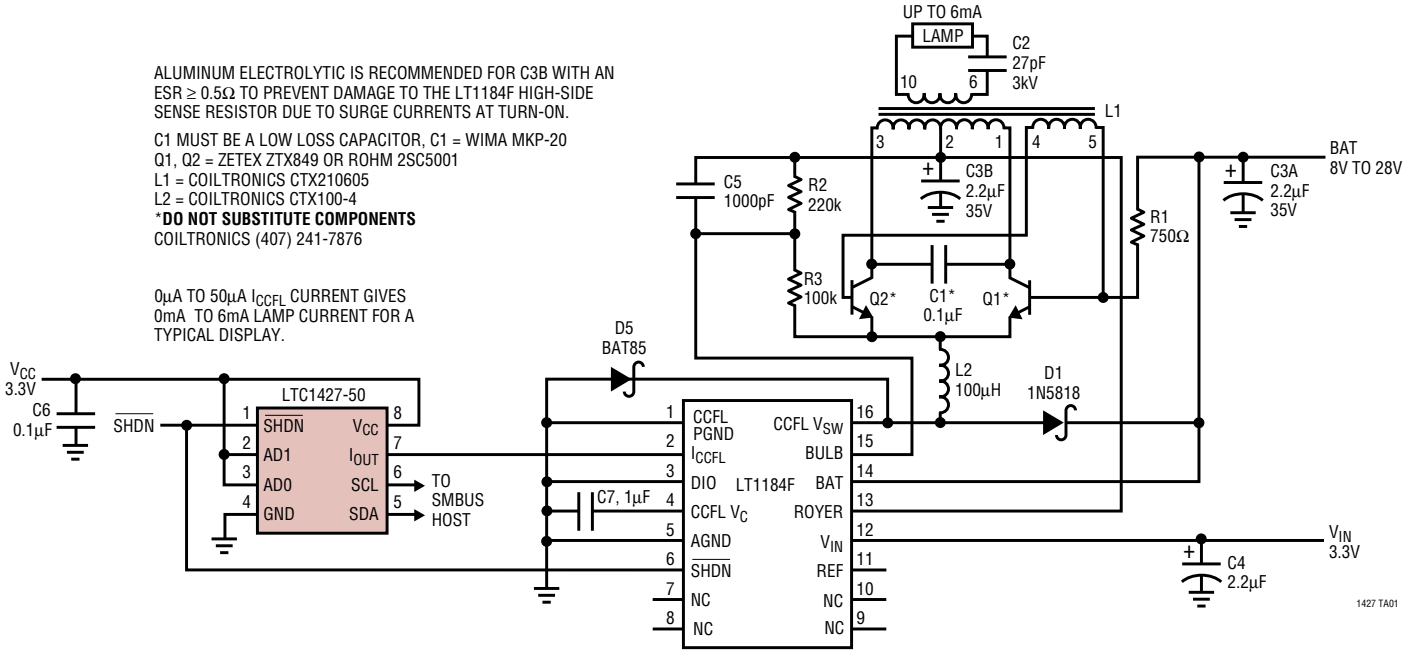
TYPICAL APPLICATIONS

LTC1427-50 Used to Null Op Amp's Offset Voltage



TYPICAL APPLICATIONS

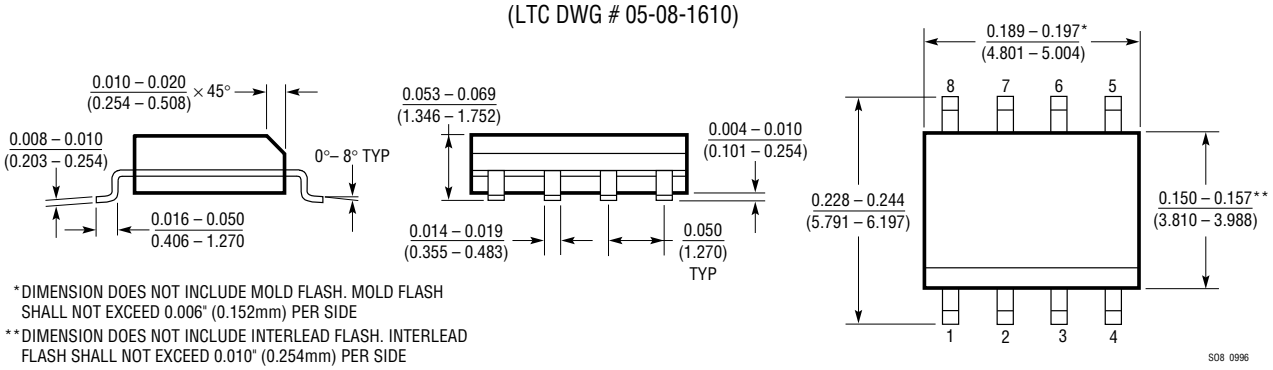
SMBus-Controlled Floating CCFL Power Supply



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1329-10/LTC1329-50	Micropower 8-Bit Current Source DAC	1-Wire, 2-Wire or Standard 3-Wire SPI Control
LTC1380/LTC1393	SMBus Single-Ended 8-Channel/Differential 4-Channel Multiplexers	Single 2.7V to ±5V Supply, Low Power
LTC1426	Micropower Dual 6-Bit PWM DAC	Pulse Mode and Push-Button Mode Interface
LTC1428	Micropower 8-Bit Current Sink DAC	1-Wire, 2-Wire or Standard 3-Wire SPI Control
LTC1623	SMBus Dual High Side Switch Controller	Regulated Onboard Charge Pump Drives External N-Channel MOSFETs

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417• (408)432-1900
FAX: (408) 434-0507•TELEX: 499-3977 • www.linear-tech.com

142750f LT/TP 0398 4K • PRINTED IN USA