



MSFB1G, MSFB3G, MSFB5G, MSFB6G Bandwidth/Gain Selectable Bandpass Filter Data Sheet

Description

The MSFBxG series of selectable filter ICs can be configured as 6 pole full, third or sixth octave response bandpass filter. The devices utilize low power and high precision Switched-Capacitor Filter (SCF) techniques that require only an external clock to set the corner frequencies for the low-pass filters. No external components (except for decoupling capacitors) are required.

The MSFB1G and MSFB3G are 50:1 clock to corner ratio bandpass filters for corner frequencies of up to 20 kHz and 3 kHz, respectively.

The MSFB5G and MSFB6G are 100:1 clock to corner ratio bandpass filters for corner frequencies of up to 20 kHz and 3 kHz, respectively.

Externally selectable gain setting pin and filter response select pin are included. The devices are packaged in a small 8-lead 4x4x0.9 mm VDFN package, making them very suitable for space constrained designs.

Absolute Maximum Ratings

Power Supply Voltage	+6V
Storage Temperature Range	-60° to +150° C
Operating Temperature Range	-40° to +85° C

Features

- Low Voltage Operation down to 2.7V
- Three Distinct Filter Types in One Package
- Adjustable Gain Settings: 0, 10 or 20 dB
- No External Components
- High Precision Switched-Capacitor Filters
- Low Power Ideal for Battery Operated Applications
- Small Package Size

Applications

- Spectrum Analyzers
- General Purpose Telecom or Telephony
- Portable Systems
- Anti-Alias Filters
- Reconstruction Filters
- Tracking Filters
- Harmonic Analysis
- Noise Analysis
- Sensors and MEMS
- Distortion Analysis

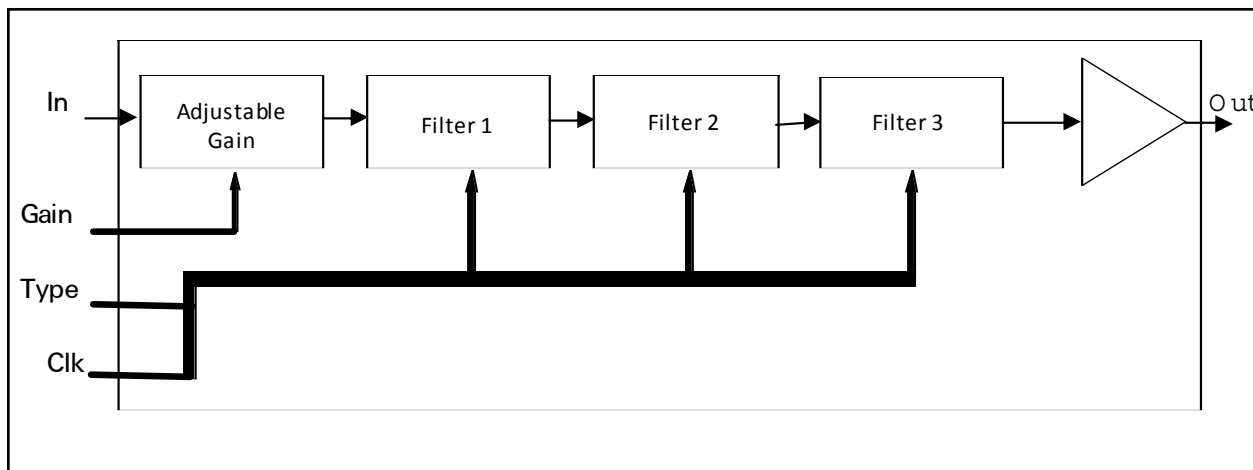


Figure 1 - Block Diagram

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MSFB1G, MSFB3BG, MSFB5G, MSFB6G

Bandwidth/Gain Selectable Bandpass Filter

Data Sheet

Electrical Characteristics

VDD=+3.0V, T=25°C, unless otherwise noted						
Parameter	Symbol	Min	Typ	Max	Units	Notes
DC Specifications						
Operating Voltage	VDD	2.7	3.0	5.5	V	
Supply Current	IDD		200	300	μA	MSFB3G/6G
			1	1.5	mA	MSFB1G/5G
Reference Voltage Output	VREF		1.5		V	
AC Specifications						
Gain Accuracy	GA	-0.5	0	0.5	dB	From selected value
Noise	e _n		200		μVrms	To ½ sample
Distortion	THD		-72		dB	A weighted
Input Voltage	V _{IN0}			4	V _{pp}	Gain=0dB; VDD=5V
	V _{IN10}			1.25	V _{pp}	Gain=10dB;VDD=5V
	V _{IN20}			0.4	V _{pp}	Gain=20dB;VDD=5V
Input Impedance	Z _{IN}		1		MΩ	f _O =350 kHz
Output Voltage Range	V _{OUT}	0.5		4.5	V	
Output Drive	I _O		300		μA	
Output Impedance	Z _O		500		Ω	
Output Capacitive Load	C _{MAX}			20	pF	
Clock to Center Ratio	CCR		50			MSFB1G/3G
			100			MSFB5G/6G
Center Frequency Range	CFR	0.0001		3	kHz	MSFB3G/6G
		0.0001		20	kHz	MSFB1G/5G
Ripple						
Full Octave	R _{FO}		0.2		dB	
Third Octave	R _{TO}		0.2		dB	
Sixth Octave	R _{SO}		0.2		dB	
40 dB Bandwidth						
Full Octave	BW _{FO}	0.3		3	Hz	Normalized Fo
Third Octave	BW _{TO}	0.6		1.67	Hz	Normalized Fo
Sixth Octave	BW _{SO}	0.76		1.32	Hz	Normalized Fo
Bandpass Q						
Full Octave	Q		1.5			
Third Octave	Q		4.5			
Sixth Octave	Q		9			





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Filter Selection _____

Gain Selection _____

The filter type is selected using the filter select pin, TYPE. TYPE is a tertiary control pin that selects the filter response. State 0 is GND, state 1 is VREF and state 2 is VDD.

The Gain control pin G is a tertiary control pin where state 0 is GND, state 1 is VREF level and state 2 is VDD.

TYPE	Bandpass
0	Full Octave
1	Third Octave
2	Sixth Octave

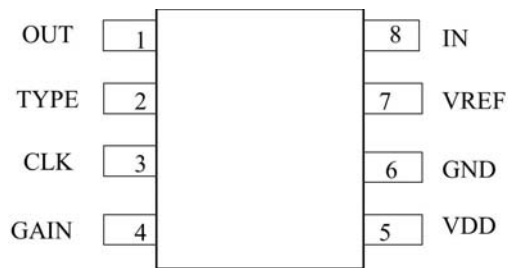
G	Gain
0	0dB
1	10dB
2	20dB

The sample rate ratio is twice the clock to corner ratio (double sampling).

Pin Description _____

Pin Configuration _____

1. OUT Filter Output
2. TYPE Filter Response Select Pin.
3. CLK CMOS Level Clock Input
4. G Gain Select Pin
5. VDD Positive Power Supply, Typically +1.5 Volts for Split Supply, +3.0 Volts for Single Supply
6. GND Negative Power Supply, Typically -1.5 Volts for Split Supply, 0 Volts for Single Supply
7. VREF Reference output, 0V for Split Supplies +1.5 Volts Typical for Single Supply. For other VDD: $VREF = (VDD - VGND) / 2$
8. IN Filter Input



Note that the large pads on the solder side of the VDFN package is tied internally to VDD. Do not ground this pad.

Ordering Information			
Part Number	Package	Clock to Corner Ratio	Max F
MSFB1GD	8 Pin VDFN	50	20 kHz
MSFB3GD	8 Pin VDFN	50	3 kHz
MSFB5GD	8 Pin VDFN	100	20 kHz
MSFB6GD	8 Pin VDFN	100	3 kHz





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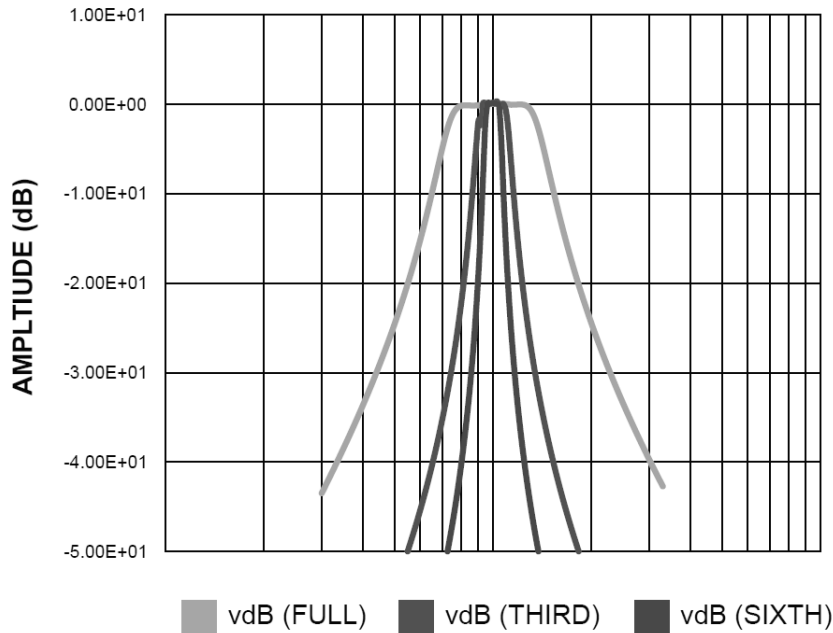


Figure 2 - Normalized Filter Responses

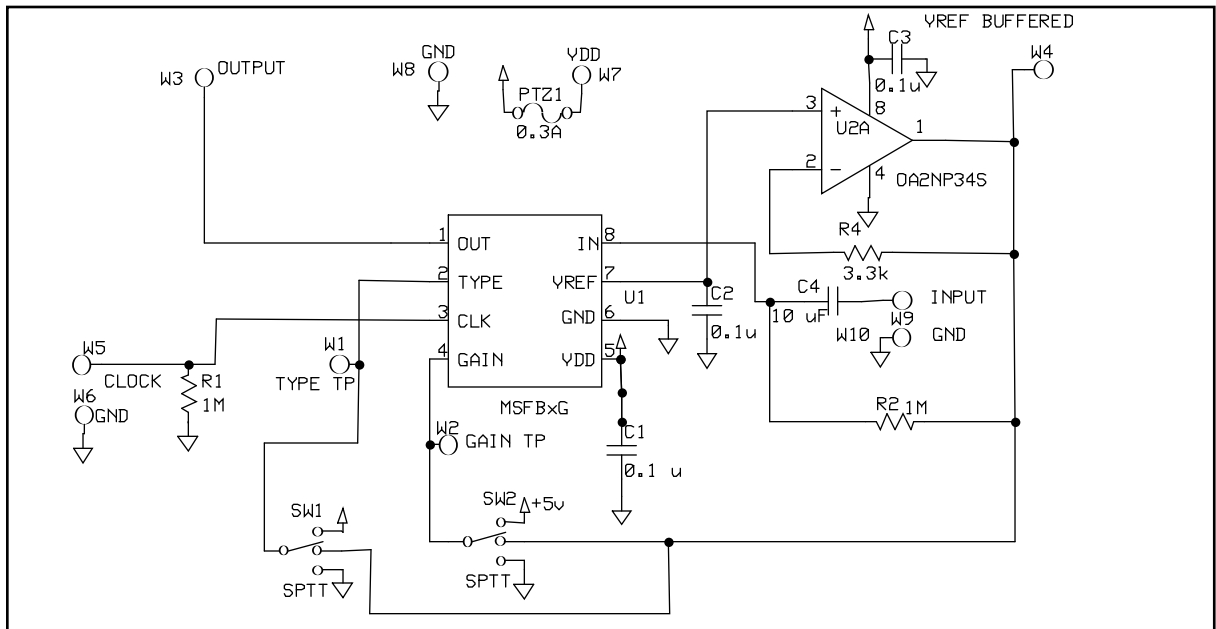


Figure 3 - Application Schematic

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