# 4-channel temperature sensor IC for PCs with I²C BUS interface

## BU9817FV

The BU9817FV is a 4-channel, 8-bit, A / D converter / overvoltage detector that is perfect for temperature sensors with built-in I²C BUS interfaces. The host can access the BU9817FV anytime for the voltage data.

### ●Applications

Notebook computers, desktop computers, household electric appliances

### ●Features

1) By attaching a thermistor, a maximum four-channel temperature sensor is possible.
2) Can set comparison voltages independently.
3) Built-in I²C BUS interface.
4) Detection level and operating mode settings are programmable.
5) Extremely low operating current perfect for portable equipment.
6) Operating voltage of $V_{DD}$ = 3V to 5.5V.

### ●Absolute maximum ratings (Ta = 25°C)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD}$ | 7.0 | V |
| Power dissipation | Pd | 350 | mW |
| Operating temperature | Topr | – 15 ~ + 75 | ˚C |
| Storage temperature | Tstg | – 55 ~ +125 | ˚C |
| Voltage applied to pins | $V_{IN}$ | GND – 0.5 ~ $V_{DD}$ + 0.5 | V |

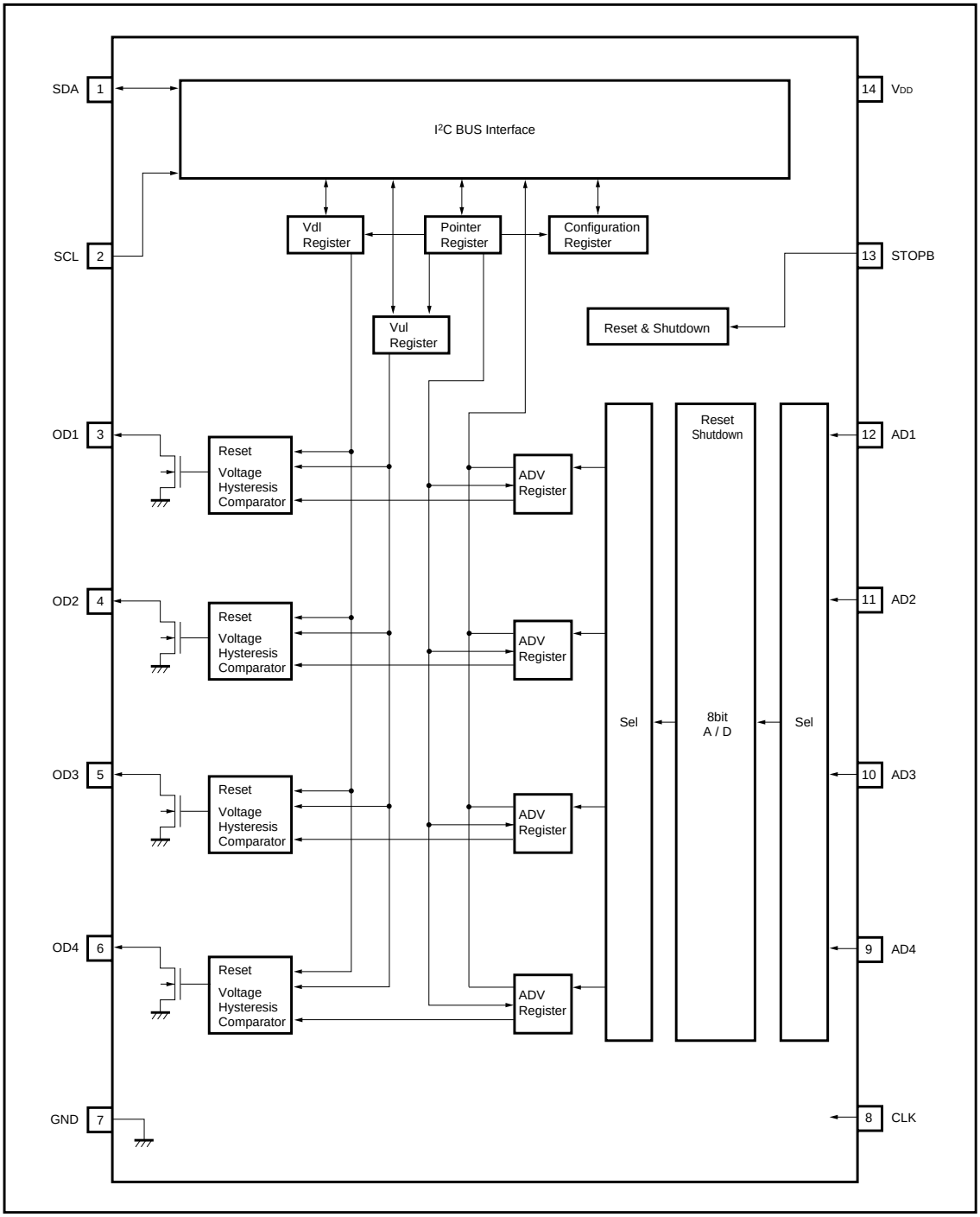
* Reduced by 3.5mW for each increase in Ta of 1˚C over 25˚C.

### ●Recommended operating conditions (Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Operating power supply voltage | $V_{DD}$ | 3.0 | — | 5.5 | V |

Note) I²C BUS is a registered trademark philips.

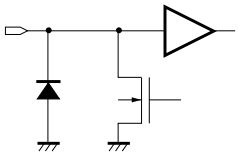
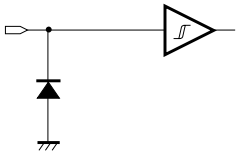
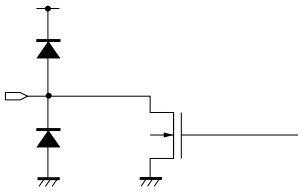
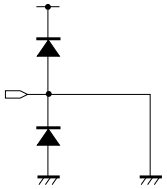
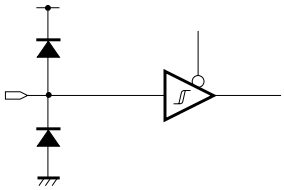
●**Block diagram**



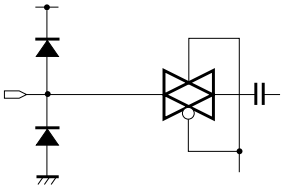
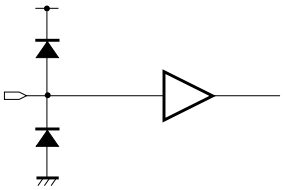
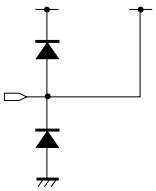
**●Pin descriptions**

| Pin No. | Pin name | Function |
|---|---|---|
| 1 | SDA | $I^2C$ BUS Serial Data Line |
| 2 | SCL | $I^2C$ BUS Serial Clock Input |
| 3 | OD1 | Open Drain Output 1 |
| 4 | OD2 | Open Drain Output 2 |
| 5 | OD3 | Open Drain Output 3 |
| 6 | OD4 | Open Drain Output 4 |
| 7 | GND | Ground |
| 8 | CLK | Clock for Logic Input |
| 9 | AD4 | Analog-to-Digtal Converter Input 4 |
| 10 | AD3 | Analog-to-Digtal Converter Input 3 |
| 11 | AD2 | Analog-to-Digtal Converter Input 2 |
| 12 | AD1 | Analog-to-Digtal Converter Input 1 |
| 13 | STOPB | Reset & Power save mode set |
| 14 | $V_{DD}$ | Supply Voltage 3.0V to 5.5V |

**●Input / output equivalent circuits**

| Pin. No | Pin name | Input / output circuits | Function |
|---|---|---|---|
| 1 | SDA |  | I²C BUS serial data input / output.<br>When only input address accords slave address (BU9817FV's), register data is inputted or outputted. |
| 2 | SCL |  | I²C BUS serial clock input. |
| 3<br>4<br>5<br>6 | OD1<br>OD2<br>OD3<br>OD4 |  | Open-drain output corresponds to AD1 to AD4 input.<br>Connect this pin a pull-up resister.<br>The pull-up resister should be above $V_{DD}$ / 4mA (Ω). |
| 7 | GND |  | Ground terminal. |
| 8 | CLK |  | Clock input for ADC block.<br>Input clock is 32.768kHz.<br>AD converter and voltage hysteresis comparator use this clock to operate. |

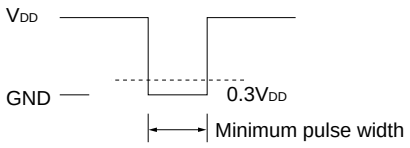
**●Input / output equivalent circuits**

| Pin. No | Pin name | Input / output circuits | Function |
|---|---|---|---|
| 9<br>10<br>11<br>12 | AD1<br>AD2<br>AD3<br>AD4 |  | AD input.<br>Each channel is converted in order.<br>(AD1, AD2, AD3, AD4, AD1,AD2...) |
| 13 | STOPB |  | Reset and power save mode setting.<br>High: Operation mode<br>Operation follows the setting of configuration register.<br>Low : Reset & Power save mode<br>Reset the all internal circuit and stop the ADC operation.<br>Go into power save mode.<br>* Be sure to set STOPB pin low for initial reset of the internal circuit, when the BU9816FV is power up. |
| 14 | $V_{DD}$ |  | Power supply.<br>Supply voltage 3.0V to 5.5V. |

● **Electrical characteristics** (unless otherwise noted, $V_{DD}$ = 5.0V, Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Circuit current (normal) | $I_{CC}$ | 0.2 | 0.75 | 2.0 | mA | SDA, SCL = "H"<br>CLK = 32.768kHz |
| Circuit current<br>(shutdown / reset / STOPB) | $I_{CC}$.sd | — | 1.0 | 2.0 | µA | SDA, SCL = "H"<br>CLK = 32.768kHz<br>Mode setting or<br>STOPB = Low |
| Input high level voltage | $V_{iH}$ | $V_{DD} \times 0.7$ | $V_{DD}$ | $V_{DD}$ + 0.5 | V | — |
| Input low level voltage | $V_{iL}$ | – 0.5 | 0.0 | $V_{DD} \times 0.3$ | V | — |
| Input high level current | $I_{iH}$ | — | 0.0 | 1.0 | µA | — |
| Input low level current | $I_{iL}$ | – 1.0 | 0.0 | — | µA | — |
| Input capacity | Ci | — | — | 10 | pF | — |
| Open drain output<br>low level voltage | VoLod | 0.0 | 0.2 | 0.6 | V | IoL = 4.0mA |
| SDA<br>output low level voltage | VoLsda | 0.0 | 0.2 | 0.6 | V | IoL = 6.0mA |
| SDA<br>output fall time | tfsda | — | — | 250 | ns | CL = 400pF<br>IoL = 6.0mA |
| STOPB<br>minimum pulse width | pwstopb | 10 | — | — | µs | — |

〈STOPB minimum pulse width〉




〈A / D〉

| | | | | | | |
|---|---|---|---|---|---|---|
| AD resolution | RES | — | 8 | — | bits | — |
| Non-linearity error | Nle | – 2 | — | 2 | LSB | — |
| Differential non-linearity error | Ndle | – 1 | — | 1 | LSB | 2 points connected |
| 1-channel conversion time | Tc | — | 305 | — | µs | fCLK = 32.768kHz |
| Input range | Ai | GND | — | $V_{DD}$ | V | — |

●**Measurement circuit**

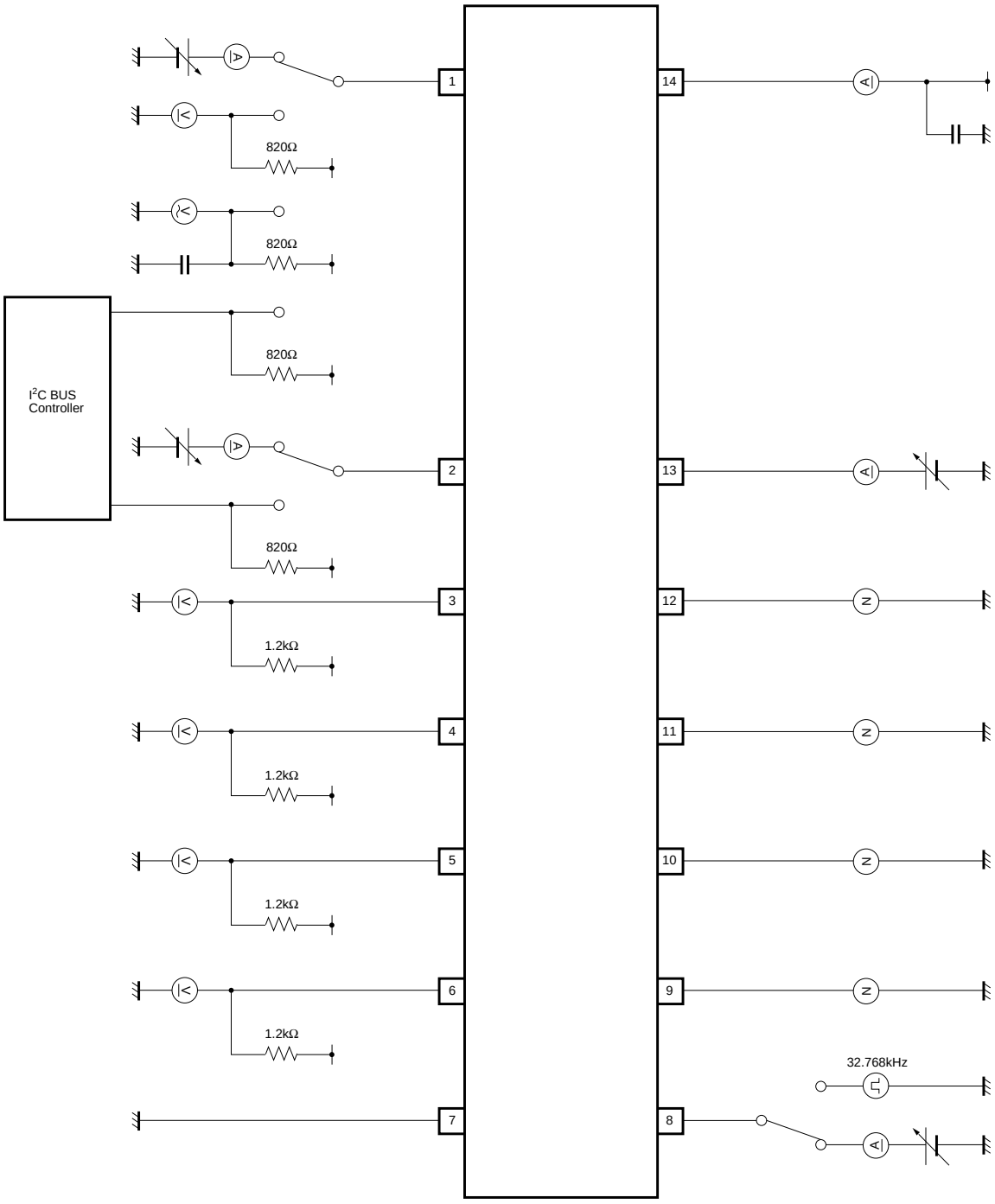



Fig.1

## ●Circuit operation

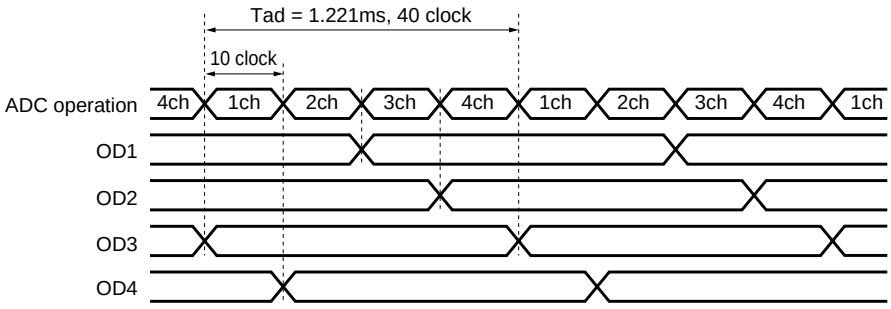
### Explanation of operating mode

| Operating mode | Configuration register settings | ADC operation conversion interval | Open drain operation timing | Register status | Current consumption (typ.) |
|---|---|---|---|---|---|
| Normal mode | 00000∗∗0b | 1.221ms | 10th clock after A / D conversion | Normal operation | 0.75mA |
| Interval High mode | 00110∗∗0b | 1 second intervals | 10th clock after A / D conversion | Normal operation | Note: average less than 3μA |
| Interval Low mode | 00100∗∗0b | 4 second intervals | 10th clock after A / D conversion | Normal operation | Note: average less than 2μA |
| Shutdown mode | 00000∗∗1b | Stopped | Hold status | Hold data | Less than 1μA |
| Reset mode | 00∗∗1∗∗∗b | Stopped | Reset fixed at high | Data reset | Less than 1μA |

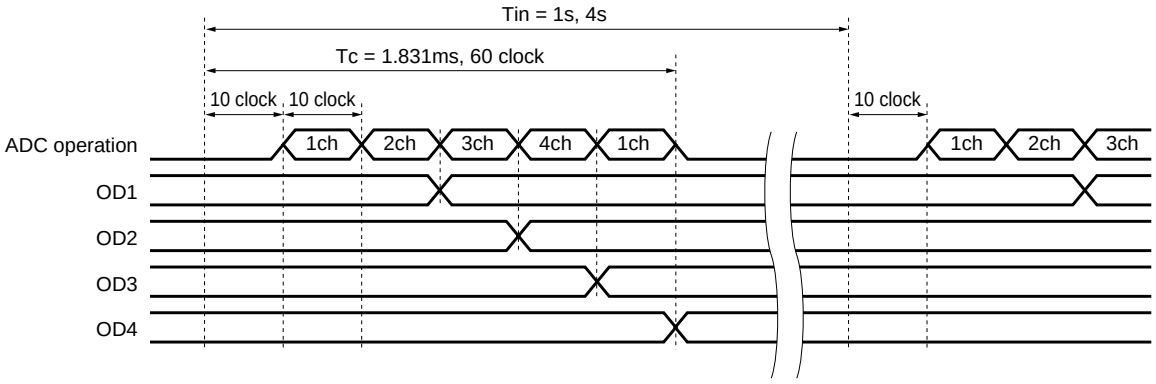
The asterisk can be either 0 or 1.
∗ Conversion time is for fCLK = 32.768kHz.
∗ These mode setting bits (bit 0 and bits 3 to 5) are common for each channel, the last setting of bits (bit0 and bits3 to 5) is effective for all channels. Furthermore, bits 1 and 2 are independent and can be set for each channel.
∗ Note: These parameters are reference values derived through calculations and are not guaranteed characteristic values.

### Explanation of ADC / open drain operation

(Normal mode)




(Interval mode)



## ●Circuit operation

Explanation of I²C BUS interface

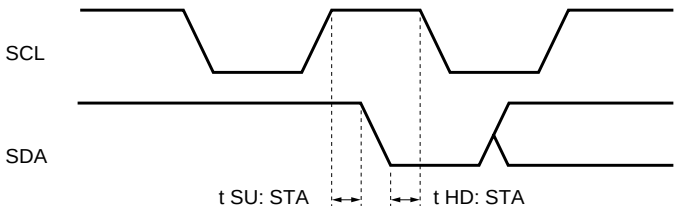
• Slave address

| 1 | 0 | 0 | 1 | 1 | 1 | 1 | R / W |
|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB |

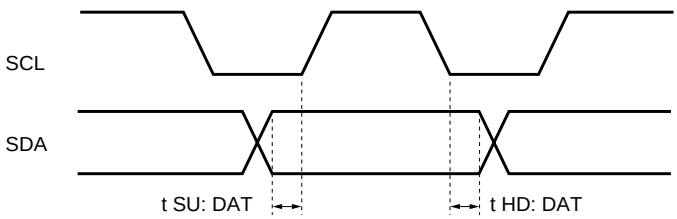
• Conforms to I²C BUS standards

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| SCL clock frequency | f SCL | 0 | 400 | kHz |
| Start condition hold time | t HD: STA | 0.6 | — | µs |
| Start condition setup time | t SU: STA | 0.6 | — | µs |
| Data setup time | t SU: DAT | 100 | — | ns |
| Data hold time | t HD: DAT | 0 | 0.9 | µs |
| Stop condition setup time | t SU: STO | 0.6 | — | µs |

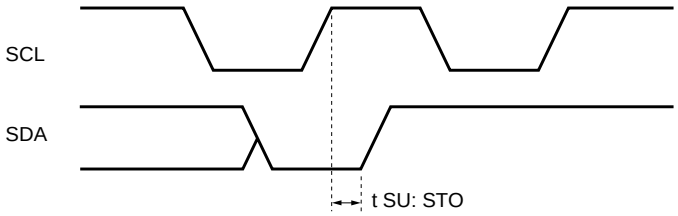
(Start conditions)




(Data conditions)



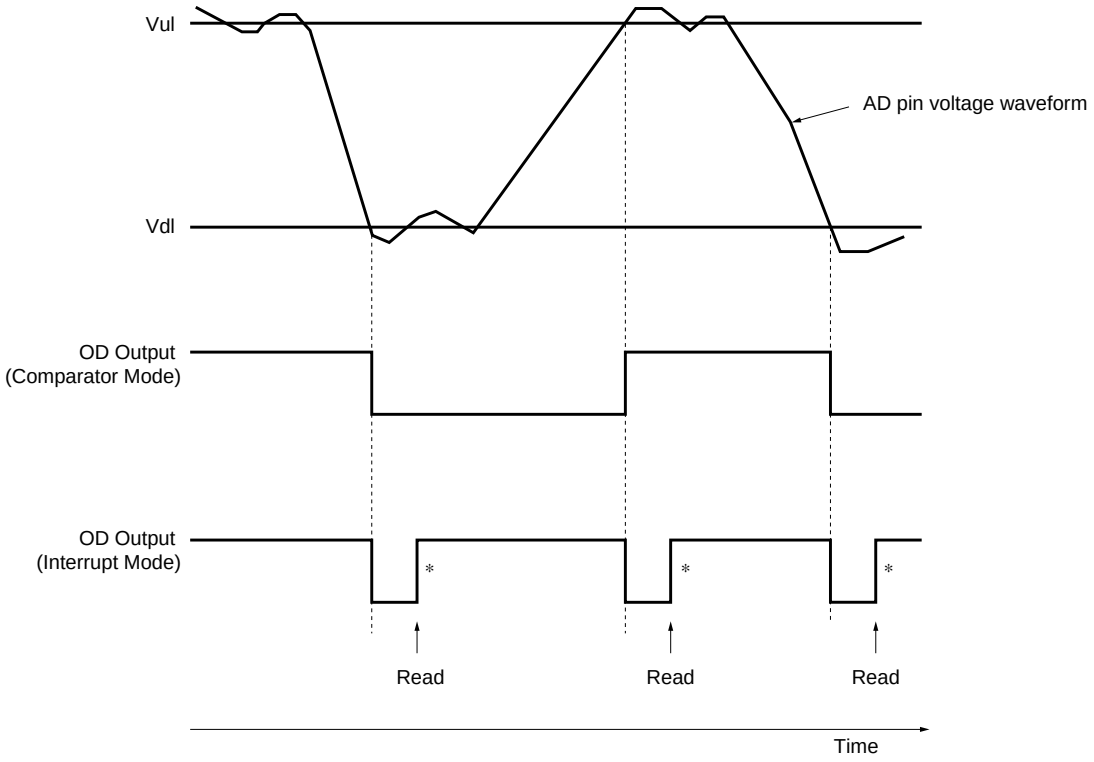

(Stop conditions)



**●Circuit operation**

OD output voltage response diagram

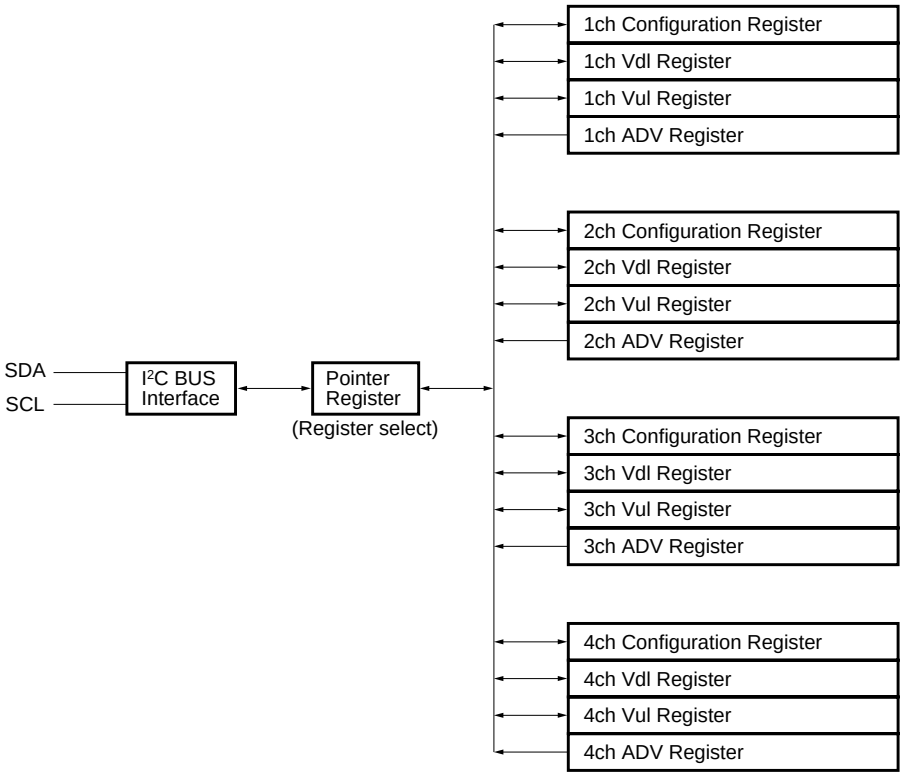
(Example: open-drain output is set active low)




* Note: Resetting OD output under interrupt mode occurs at only shutdown mode or reset mode or STOPB or when data read generated from host. Except for these cases, OD output is kept setting.

● **Circuit operation**

Register structure




I²C Bus data structure

(1) Write Mode

| S | Address | $\overline{W}$ | A | Pointer reg. Byte | A | Write Data Byte | A | P |
|---|---|---|---|---|---|---|---|---|

(2) Read Mode

1) Pointer register set

| S | Address | $\overline{W}$ | A | Pointer reg. Byte | A |
|---|---|---|---|---|---|

| Sr | Address | R | A | Read Data Byte | $\overline{A}$ | P |
|---|---|---|---|---|---|---|

2) Preset pointer register

| S | Address | R | A | Read Data Byte | $\overline{A}$ | P |
|---|---|---|---|---|---|---|

S: Start condition
P: Stop condition
Sr: Restart condition
A: acknowledge
$\overline{A}$: acknowledge bar

Mode settings table 1 / 2

(1) Pointer register (selects which registers will be read from or written to)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Channel Select | | Register Select | |

D4 to D7: These bits are used for test mode and must be kept zero for normal operation.

Channel Select

| D3 | D2 | Channel |
|---|---|---|
| 0 | 0 | Channel 1 |
| 0 | 1 | Channel 2 |
| 1 | 0 | Channel 3 |
| 1 | 1 | Channel 4 |

Register Select

| D1 | D0 | Register |
|---|---|---|
| 0 | 0 | ADV Register (Read only) (Power on Reset default) |
| 0 | 1 | Configuration Register (Read / Write) |
| 1 | 0 | Vdl Register (Read / Write) |
| 1 | 1 | Vul Register (Read / Write) |

(2) ADV Register (Read only)

| Channel | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 1 ch | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB |
| 2 ch | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB |
| 3 ch | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB |
| 4 ch | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB |

D0 to D7: Voltage data
The defaults for the power-on-reset and reset modes are 1 for all bits.

(3) Configuration Register (Read / Write)

| Channel | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 1 ch | 0 | 0 | Interval Mode | Interval Speed | Reset | Opendrain Polarity | Comp. / Int. | Shutdown |
| 2 ch | 0 | 0 | | | | Opendrain Polarity | Comp. / Int. | |
| 3 ch | 0 | 0 | | | | Opendrain Polarity | Comp. / Int. | |
| 4 ch | 0 | 0 | | | | Opendrain Polarity | Comp. / Int. | |

The defaults for the power-on-reset and reset modes are 0 for all bits.

Mode settings table 2 / 2

D0 : Shutdown
"0" - Operation mode.
"1" - The BU9817FV stops A / D operation and goes into low power shutdown mode.
D0 bit of each channel is common bit.

D1 : Comparator / Interrupt mode
"0" - Comparator mode.
"1" - Interrupt mode.

D2 : Open Drain Polarity
"0" - active low.
"1" - active high.

D3 : Reset
"0" - Operation mode.
"1" - Reset any bits except D3 bit of the configuration register, any registers, the A / D converter, and the voltage hysteresis comparator.
D3 bit of each channel is common bit.

D4 : Interval Speed
Set the conversion cycle time of the 8bit A / D and the voltage hysteresis comparator when D5 bit (Interval Mode) is "1".
"0" - conversion cycle time is 4s.
"1" - conversion cycle time is 1s.
D4 bit of each channel is common bit.

D5 : Interval Mode
"0" - normal mode.
"1" - Interval mode.
D5 bit of each channel is common bit.

(4) Vul and Vdl Register (Read / Write)

| Channel | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 1 ch | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB |
| 2 ch | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB |
| 3 ch | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB |
| 4 ch | MSB | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB |

D0 to D7: Voltage limit data of Vul and Vdl.
Default after power on reset and reset mode is Vul = 80h, Vdl = 66h.

●**Application example**

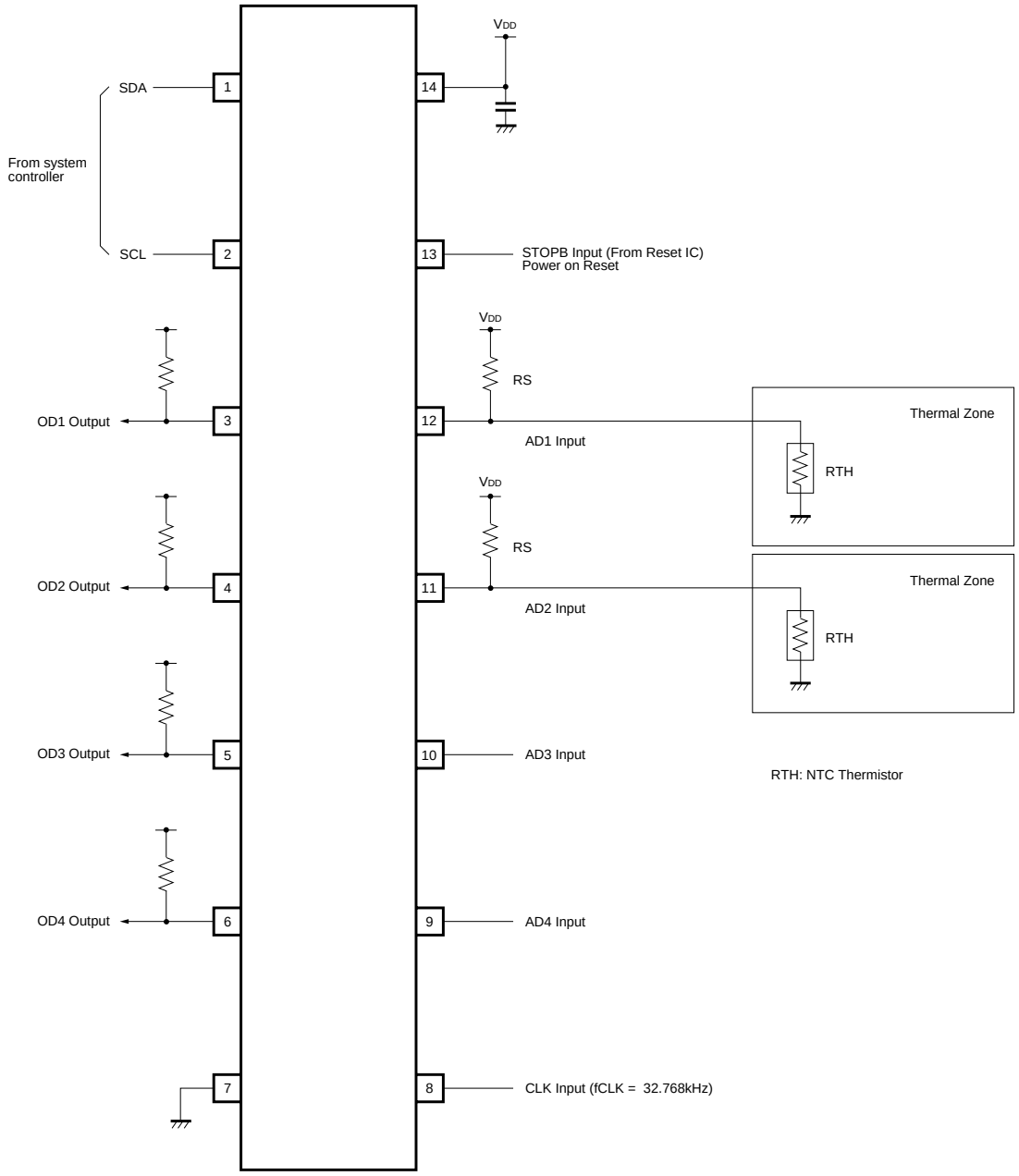
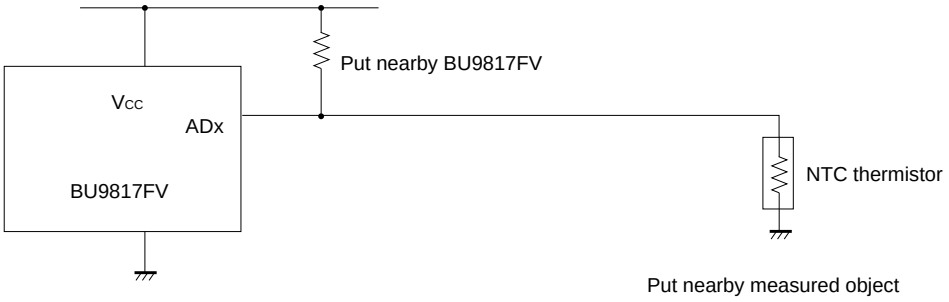



Fig.2

●**Explanation for external components**

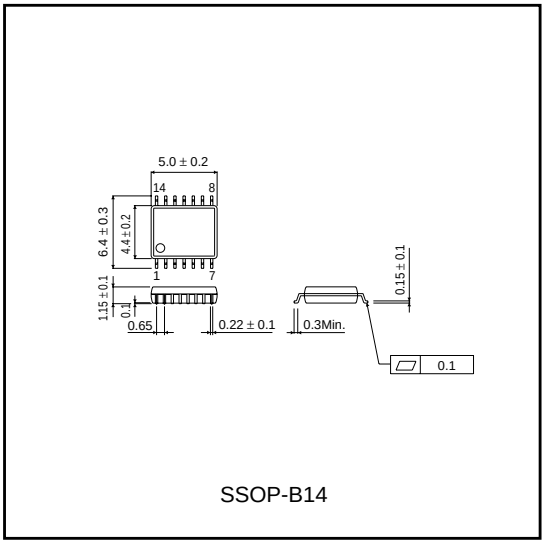
(1) AD input pin (example when used as a temperature sensor)

To the AD input pin, input a voltage with divided resistance from a resistor and NTC thermistor. For the sensor to measure the temperature, the NTC thermistor is used. The thermistor is a p-type semiconductor and as the temperature increases, the resistance value becomes lower. In other words, the resistance temperature coefficient is negative, and so the AD input pin voltage temperature characteristics are also negative.




GND is required common and stability.

●**External dimensions** (Units : mm)




SSOP-B14