2.5 MSPS, 20-Bit ΣΔ ADC

Preliminary Technical Data

AD7760

FEATURES

High performance 20-bit Sigma-Delta ADC
118dB SNR at 78kHz output data rate
100dB SNR at 2.5MHz output data rate
2.5 MHz maximum fully filtered output word rate
Programmable over-sampling rate (8x to 256x)
Flexible parallel interface
Fully differential modulator input
On-chip differential amplifier for signal buffering
Low pass FIR filter with default or user programmable coefficients
Over-range alert bit
Digital offset and gain correction registers
Filter bypass modes
Low power and power down modes
Synchronization of multiple devices via $\overline{\text{SYNC}}$ pin

APPLICATIONS

Data acquisition systems
Vibration analysis
Instrumentation

FUNCTIONAL BLOCK DIAGRAM

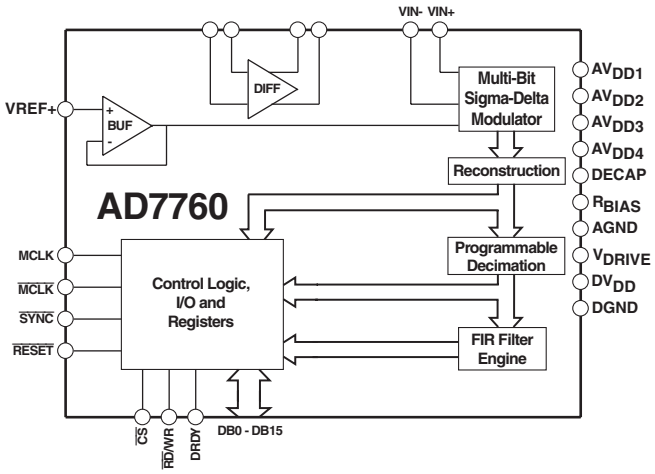


Figure 1.

PRODUCT OVERVIEW

The AD7760 high performance 20-bit sigma delta analog to digital converter combines wide input bandwidth and high speed with the benefits of sigma delta conversion with performance of 100dB SNR at 2.5MSPS making it ideal for high speed data acquisition. Wide dynamic range combined with significantly reduced anti-aliasing requirements simplify the design process. An integrated buffer to drive the reference, a differential amplifier for signal buffering and level shifting, an over-range flag, internal gain & offset registers and a low-pass digital FIR filter make the AD7760 a compact highly integrated data acquisition device requiring minimal peripheral component selection. In addition the device offers programmable decimation rates and the digital FIR filter can be adjusted if the default characteristics are not appropriate to the application. The AD7760 is ideal for applications demanding high SNR without necessitating design of complex front end signal processing.

The differential input is sampled at up to 40MS/s by an analog modulator. The modulator output is processed by a series of low-pass filters, the final one having default or user programmable coefficients. The sample rate, filter corner frequencies and output word rate are set by a combination of the external clock frequency and the configuration registers of the AD7760.

The reference voltage supplied to the AD7760 determines the analog input range. With a 4V reference, the analog input range is ±3.2V differential biased around a common mode of 2V. This common mode biasing can be achieved using the on-chip differential amplifiers, further reducing the external signal conditioning requirements.

The AD7760 is available in an exposed paddle 64-lead TQFP and 48-lead CSP packages and is specified over the industrial temperature range from -40°C to +85°C.

Rev. PrN
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REVISION HISTORY

AD7760—SPECIFICATIONS

Table 1. V_{DD1} = 2.5 V, V_{DD2} = 5 V, V_{REF} = 4.096 V, T_A = +25°C, Full Power Mode, unless otherwise noted

Parameter	Test Conditions/Comments	Specifcation	Unit
DYNAMIC PERFORMANCE			
Decimate by 256	MCLK = 24.576MHz, ODR = 48kHz, FIN = 1kHz Sine Wave		
Signal to Noise Ratio (SNR) [1]		118	dB typ
Spurious Free Dynamic Range (SFDR) [1]	Non-harmonic	118	dBFS typ
Total Harmonic Distortion (THD) [1]	Input Amplitude = -6dB	-100	dB typ
Intermodulation Distortion (IMD) [1]		-100	dB typ
Decimate by 16	MCLK = 40MHz, ODR = 1.25MHz, FIN =100kHz Sine Wave		
Signal to Noise Ratio (SNR) [1]		103	dB typ
Spurious Free Dynamic Range (SFDR) [1]	Non-harmonic	103	dBFS typ
Total Harmonic Distortion (THD) [1]	Input Amplitude = -6dB	-100	dB typ
Intermodulation Distortion (IMD) [1]		-100	dB typ
Decimate by 8	MCLK = 40MHz, ODR = 2.5MHz, FIN = 100kHz Sine Wave		
Signal to Noise Ratio (SNR) [1]		100	dB typ
Spurious Free Dynamic Range (SFDR) [1]	Non-harmonic	100	dBFS typ
Total Harmonic Distortion (THD) [1]	Input Amplitude = -6dB	-100	dB typ
Intermodulation Distortion (IMD) [1]	FIN = 100kHz Sine Wave	-100	dB typ
Intermodulation Distortion (IMD) [1]	FIN = 1MHz Sine Wave	-100	dB typ
DC ACCURACY			
Resolution		20	Bits
Integral Nonlinearity[1]	At 18 bits	1	LSB typ
Differential Nonlinearity[1]	Guaranteed monotonic to 20 bits	1	LSB typ
Offset Error[1]		0.03	% typ
Gain Error[1]		5	LSB typ
Offset Error Drift		0.0006	% /°C
Gain Error Drift		0.1	LSB /°C
DIGITAL FILTER RESPONSE			
Decimate by 8			
Group Delay	MCLK = 40MHz	12	µS typ
Decimate by 16			
Group Delay	MCLK = 40MHz	24	µS typ
Decimate by 128			
Group Delay	MCLK = 24.576MHz	480	µS typ
ANALOG INPUT			
Differential Input Voltage	Vin(+) – Vin(-), V_{REF} = 2.5V	±2	V pk-pk
	Vin(+) – Vin(-), V_{REF} = 4.096V	±3.25	V pk-pk
DC Leakage Current		±2	µA max
Input Capacitance	With internal buffer	5	pF typ
	With external buffer	55	pF typ
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage	V_{DD3} = 3.3V	+2.5	Volts
	V_{DD3} = 5V	+4.096	Volts
V_{REF} Input DC Leakage Current		±1	µA max
V_{REF} Input Capacitance		5	pF max
POWER REQUIREMENTS			
AV_{DD1} (Modulator Supply)	±5%	+2.5	Volts
AV_{DD2} (General Supply)	±5%	+5	Volts
AV_{DD3} (Diff-Amp Supply)		+3.0/+5.5	V min/max
AV_{DD4} (Ref Buffer Supply)		+3.15/+5.25	V min/max
DV_{DD}	±5%	+2.5	Volts
V_{DRIVE}		+1.65/+2.7	V min/max

Parameter	Test Conditions/Comments	Specifcation	Unit
Full Power Mode			
AI_{DD1} (Modulator)		50	mA typ
AI_{DD2} (General)		35	mA typ
AI_{DD4} (Reference Buffer)	AV_{DD4} = +5V	35	mA typ
Low Power Mode			
AI_{DD1} (Modulator)		26	mA typ
AI_{DD2} (General)		20	mA typ
AI_{DD4} (Reference Buffer)	AV_{DD4} = +5V	10	mA typ
AI_{DD3} (Diff Amp)	AV_{DD3} = +5V, Both Modes	42	mA typ
D_{IDD}	Both Modes	45	mA typ
Standby Mode			
AI_{DD1} (Modulator)		210	µA typ
AI_{DD2} (General)		30	nA typ
AI_{DD3} (Diff Amp)	AV_{DD3} = +5V	30	nA typ
AI_{DD4} (Reference Buffer)	AV_{DD4} = +5V	30	nA typ
D_{IDD}	Clock Stopped	250	µA typ
	Clock Running	690	µA typ
POWER DISSIPATION			
Full Power Mode			
Modulator (P_1)		125	mW typ
General (P_2)		175	mW typ
Reference Buffer (P_4)	AV_{DD4} = +3.3V	101	mW typ
	AV_{DD4} = +5V	175	mW typ
Low Power Mode			
Modulator (P_1)		65	mW typ
General (P_2)		100	mW typ
Reference Buffer (P_4)	AV_{DD4} = +3.3V	27	mW typ
	AV_{DD4} = +5V	50	mW typ
Differential Amplifier (P_3)	AV_{DD3} = +3.3V	116	mW typ
	AV_{DD3} = +5V	210	mW typ
Digital Power		112.5	mW typ
Standby Mode	Clock Stopped	1.2	mW typ
	Clock Running	2.3	mW typ

[1] See Terminology

TIMING SPECIFICATIONS

Table 2. V_{DD1} = 2.5 V, V_{DD2} = 5 V, V_{REF} = 4.096 V, V_{DRIVE} = TBD V, T_A = +25°C, C_{LOAD} = 25pF, Full Power Mode, unless otherwise noted

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{MCLK}	12.288	MHz min	Applied Master Clock Frequency
	80	MHz max	
f_{ICLK}	12.288	MHz min	Internal Modulator Clock Derived from MCLK.
	20	MHz max	
t_1[1]	$0.5 \times t_{ICLK}$	typ	$\overline{DRDY}$ Pulse Width
t_2	10	nS min	$\overline{DRDY}$ Falling Edge to $\overline{CS}$ falling Edge
t_3	2	nS min	$\overline{RD}$/WR Setup Time to $\overline{CS}$ Falling Edge
t_4	10	nS typ	Data Access Time
t_5	t_{ICLK}	min	$\overline{CS}$ Low Pulse Width
t_6	t_{ICLK}	min	$\overline{CS}$ High Pulse Width Between Reads
t_7	2	nS min	$\overline{RD}$/WR Hold Time to $\overline{CS}$ Rising Edge
t_8	10	nS max	Bus Relinquish Time
t_9	$0.5 \times t_{ICLK}$	typ	$\overline{DRDY}$ High Period
t_{10}	$0.5 \times t_{ICLK}$	typ	$\overline{DRDY}$ Low Period
t_{11}	15	nS typ	Data Access Time
t_{12}	TBD	xS min	Data Valid Prior to $\overline{DRDY}$ Rising Edge
t_{13}	TBD	xS min	Data Valid After $\overline{DRDY}$ Rising Edge
t_{14}	10	nS max	Bus Relinquish Time
t_{15}	t_{ICLK}	xS min	$\overline{CS}$ Low Pulse Width
t_{16}	t_{ICLK}	xS min	$\overline{CS}$ High Period Between Address and Data
t_{17}	10	nS min	Data Setup Time
t_{18}	10	nS min	Data Hold Time

[1] $t_{ICLK} = 1/f_{ICLK}$

TIMING DIAGRAMS

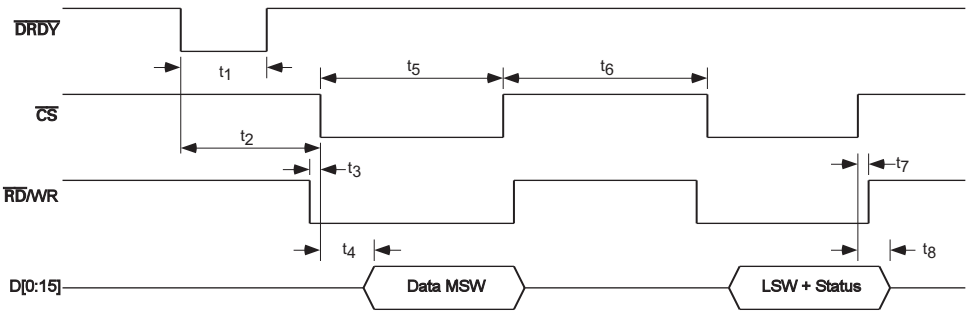


Figure 2. Parallel Interface Timing Diagram

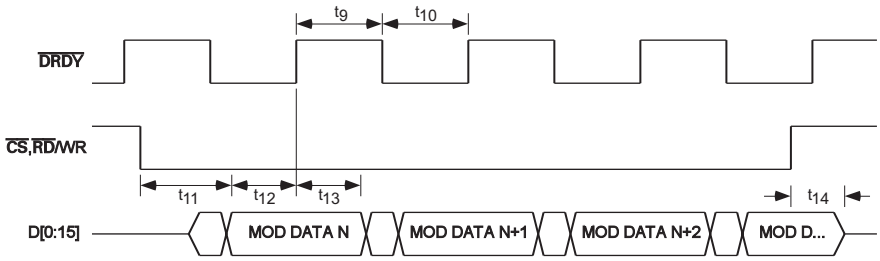


Figure 3. 20MHz Modulator Data Output Mode

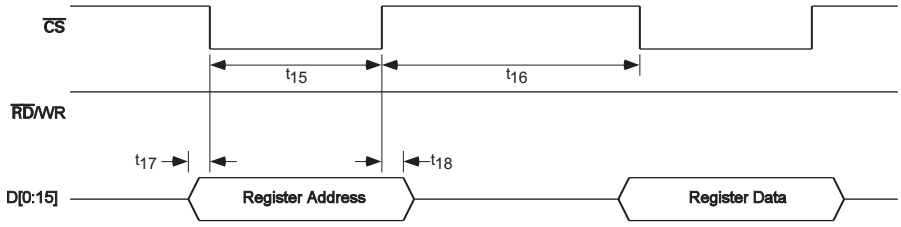


Figure 4. AD7760 Register Write

ABSOLUTE MAXIMUM RATINGS

Table 3. T_A = 25°C, unless otherwise noted.

Parameters	Rating
V_{DD} to GND	TBD
V_{IN+} to GND	TBD
V_{IN-} to GND	TBD
Digital input voltage to GND	TBD
Digital output voltage to GND	TBD
V_{REF} to GND	TBD
Input current to any pin except supplies[1]	TBD
Operating temperature range	
Commercial (A, B version)	−40°C to +85°C
Storage temperature range	−65°C to +150°C
Junction temperature	150°C
TQFP Exposed Paddle Package	
θ_{JA} thermal impedance	92.7 °C/W
θ_{JC} thermal impedance	5.1 °C/W
CSP Package	
θ_{JA} thermal impedance	26.7 °C/W
θ_{JC} thermal impedance	30 °C/W
Lead temperature, soldering	
Vapor phase (60 secs)	215°C
Infrared (15 secs)	220°C
ESD	TBD kV

[1]Transient currents of up to TBD mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

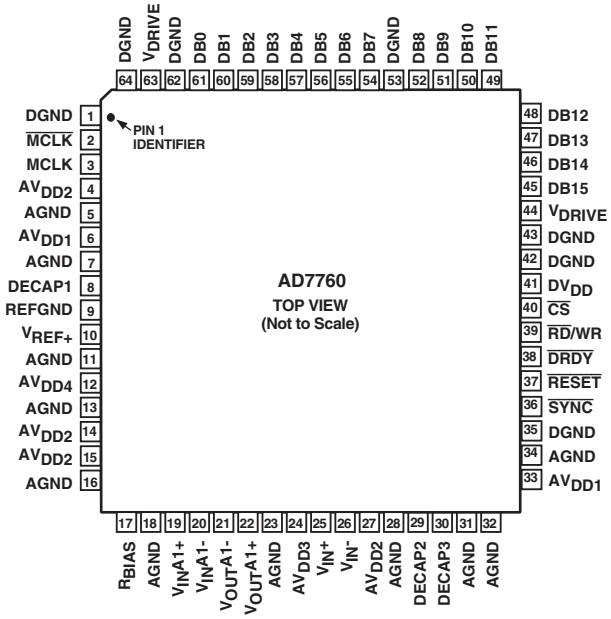


Figure 5. 64-Lead TQFP Pin Configuration

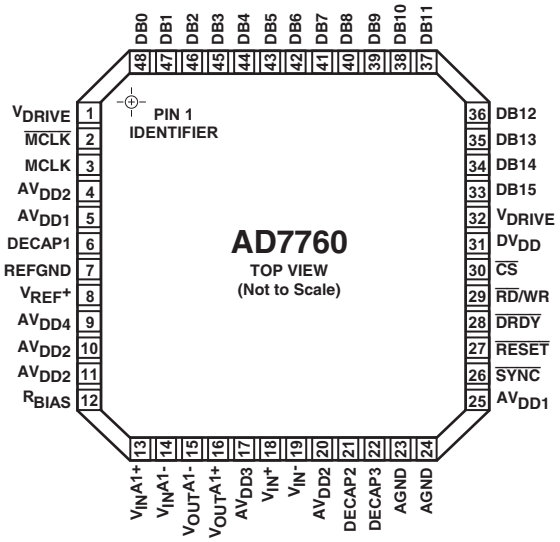


Figure 6. 48-PIN LFCSP Pin Configuration

Table 4. Pin Function Descriptions

TQFP Pin Number	CSP Pin Number	Pin Mnemonic	Description
6, 33	5, 25	AV_{DD1}	+2.5V power supply for modulator. These pins should be decoupled to AGND with 100nF and 10µF capacitors on each pin.
4, 14, 15, 27	4, 10, 11, 20	AV_{DD2}	+5V power supply. These pins should be decoupled to AGND with TBD nF and TBD µF capacitors on each pin.
24	17	AV_{DD3}	+3.3V to +5V power supply for differential amplifier. These pins should be decoupled to AGND with a 100nF capacitor.
12	9	AV_{DD4}	+3.3V to +5V power supply for reference buffer. This pin should be decoupled to AGND with a 10nF capacitor in series with a 22Ω resistor.
5, 7, 11, 13, 16, 18, 23, 28, 31, 32, 34	23, 24, Paddle	AGND	Power supply ground for analog circuitry. In the Chip Scale package, most of the internal AGND pads are down-bonded to the exposed paddle. This paddle then become the main analog ground connection for the AD7760.
9	7	REFGND	Reference Ground. Ground connection for the reference voltage.
41	31	DV_{DD}	+2.5V power supply for digital circuitry and FIR filter. This pin should be decoupled to DGND with a 470nF capacitor.
44, 63	1, 32	V_{DRIVE}	Logic power supply input, +1.8V to +2.5V. The voltage supplied at these pins will determine the operating voltage of the logic interface. Both these pins must be connected together and tied to the same supply. Each pin should also be decoupled to DGND with a 470nF capacitor.
1, 35, 42, 43, 53, 62, 64	Paddle	DGND	Ground Reference for digital circuitry. In the Chip Scale package, all the internal DGND pads are down-bonded to the exposed paddle. This paddle then becomes the single ground connection for the AD7760.

TQFP Pin Number	CSP Pin Number	Pin Mnemonic	Description
19	13	V_{IN}A1+	Positive Input to Full-Power Differential Amplifier 1.
20	14	V_{IN}A1-	Negative Input to Full-Power Differential Amplifier 1.
21	15	V_{OUT}A1-	Negative Output from Full-Power Differential Amplifier 1.
22	16	V_{OUT}A1+	Positive Output from Full-Power Differential Amplifier 1.
25	18	V_{IN}+	Positive Input to the Modulator.
26	19	V_{IN}-	Negative Input to the Modulator.
10	8	V_{REF+}	Reference Input. The input range of this pin is determined by the reference buffer supply voltage (AV_{DD4}). See Reference Section for more details.
8	6	DECAP1	Decoupling Pin. A 100nF capacitor must be inserted between this pin and AGND.
29	21	DECAP2	Decoupling Pin. A TBD µF capacitor must be inserted between this pin and AGND.
30	22	DECAP3	Decoupling Pin. A TBD µF capacitor must be inserted between this pin and AGND.
17	12	R_{BIAS}	Bias Current setting pin. A resistor must be inserted between this pin and AGND. For more details on this, see the Bias Resistor Section.
45-52, 54-61	33-48	DB15 – DB0	16-bit bi-directional data bus. These are three-state pins that are controlled by the $\overline{CS}$ and $\overline{RD}$ /WR pins. The operating voltage for these pins is determined by the V_{DRIVE} voltage. See Interfacing Section for more details.
37	27	$\overline{RESET}$	A falling edge on this pin resets all internal digital circuitry. Holding this pin lows keeps the AD7760 in a reset state.
3	3	MCLK	Master Clock Input. A low jitter digital clock must be applied to this pin. The output data rate will depend on the frequency of this clock. See Clocking Section for more details.
2	2	$\overline{MCLK}$	Master Clock ground sensing pin.
36	26	$\overline{SYNC}$	Synchronization Input. A falling edge on this pin resets the internal filter. This can be used to synchronize multiple devices in a system.
39	29	$\overline{RD}$/WR	Read/Write Input. This pin, in conjunction with the Chip Select pin, is used to read and write data to and from the AD7760. If this pin is low when $\overline{CS}$ is low, a read will take place. If this pin is high and $\overline{CS}$ is low, a write will occur. See AD7760 Interface Section for more details.
38	28	$\overline{DRDY}$	Data Ready Output. Each time that new conversion data is available, an active low pulse, ½ ICLK period wide, is produced on this pin. See AD7760 Interface Section for further details.
40	30	$\overline{CS}$	Chip Select Input. Used in conjunction with the $\overline{RD}$/WR pin to read and write data to and from the AD7760. See AD7760 Interface Section for further details.

TERMINOLOGY

Signal to (Noise + Distortion) Ratio
The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\left(Noise + Distortion\right) = \left(6.02\ N + 1.76\right)\ dB$$

Thus, for an 18-bit converter, this is 110.12dBs and for a 20-bit converter, 122.16 dB.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7760, it is defined as

$$THD(dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.

V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but, for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Non-Harmonic Spurious Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component excluding harmonics.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7760 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB.

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (000...000 to 000...001) from the ideal (that is, AGND + 1 LSB).

Gain Error
The deviation of the last code transition (111...110 to 111...111) from the ideal (that is, V_{REF} − 1 LSB), after the offset error has been adjusted out.

Power Supply Rejection Ratio (PSRR)
The ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC V_{DD} supply of frequency fs. The frequency of this input varies from 1 kHz to 1 MHz.

$$PSRR(dB) = 10 \log\left(Pf / Pfs\right)$$

P*f* is the power at frequency f in the ADC output; P*f*s is the power at frequency fs in the ADC output.

TYPICAL PERFORMANCE CHARACTERISTICS

Default Conditions: T_A = 25°C, TBD, unless otherwise noted.

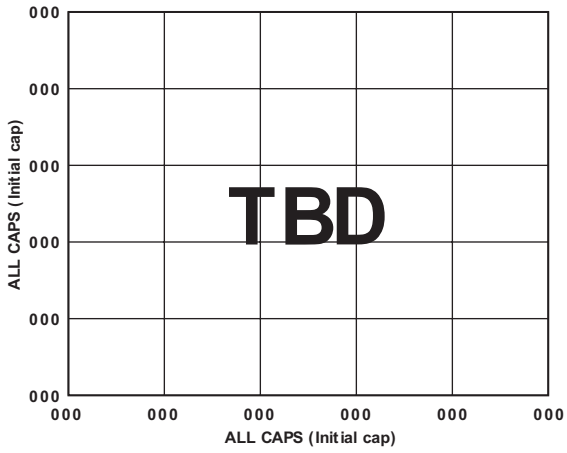


Figure 7. TBD

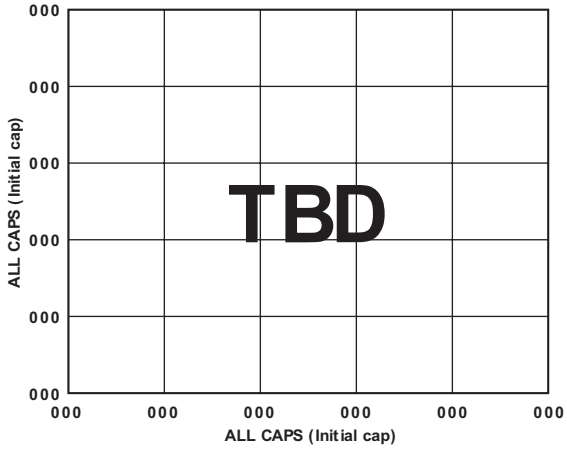


Figure 8. TBD

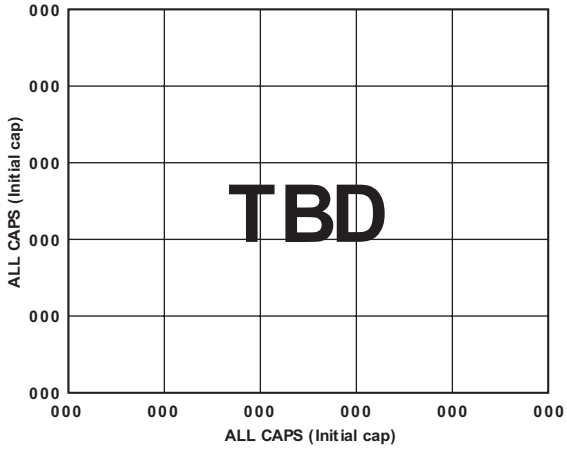


Figure 9. TBD

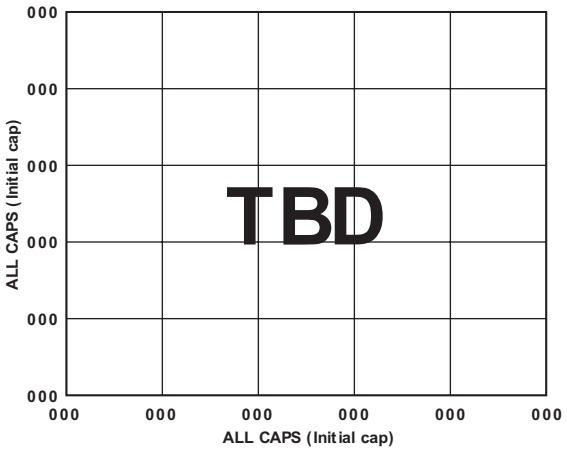


Figure 10. TBD

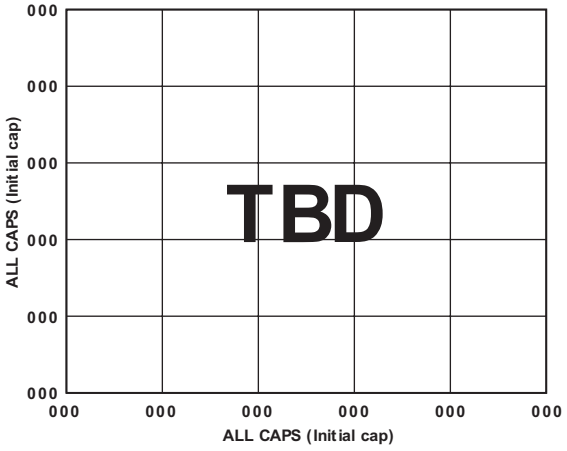


Figure 11. TBD

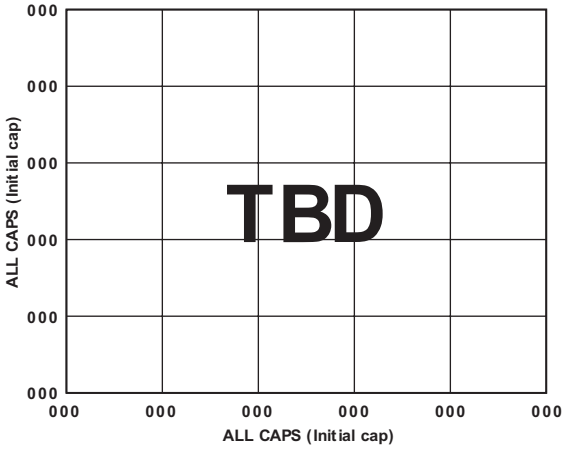


Figure 12. TBD

THEORY OF OPERATION

The AD7760 employs a sigma-delta conversion technique to convert the analog input into an equivalent digital word. The modulator samples the input waveform and outputs an equivalent digital word to the digital filter at a rate equal to I_{CLK}.

Due to the high over-sampling rate, which spreads the quantization noise from 0 to f_{ICLK}, the noise energy contained in the band of interest is reduced (Figure 13a). To further reduce the quantization noise, a high order modulator is employed to shape the noise spectrum; so that most of the noise energy is shifted out of the band of interest (Figure 13b).

The digital filtering which follows the modulator removes the large out-of-band quantization noise (Figure 13c) while also reducing the data rate from f_{ICLK} at the input of the filter to $f_{ICLK}/8$ or less at the output of the filter, depending on the decimation rate used.

Digital filtering has certain advantages over analog filtering. It does not introduce significant noise or distortion and can be made perfectly linear phase.

The AD7760 employs three Finite Impulse Response (FIR) filters in series. By using different combinations of decimation ratios and filter selection and bypassing, data can be obtained from the AD7760 at a large range of data rates. Multi-bit data from the modulator can be obtained at a rate of 20MHz. The first filter receives data from the modulator at 20MHz where it is decimated by four to output data at 5MHz. This partially filtered data can also be output at this stage. The second filter allows the decimation rate to be chosen from 2x to 32x or to be completely bypassed. The third filter has a fixed decimation rate of 2x and is user programmable as well as having a default configuration. It is described in detail in the Programmable FIR Filter Section. This filter can also be bypassed. Table X below shows some characteristics of the default filter. The group delay of the filter is defined to be the delay to the centre of the impulse response and is equal to the computation + filter delays. The delay until valid data is available (the DVALID status bit is set) is equal to 2x the filter delay + the computation delay.

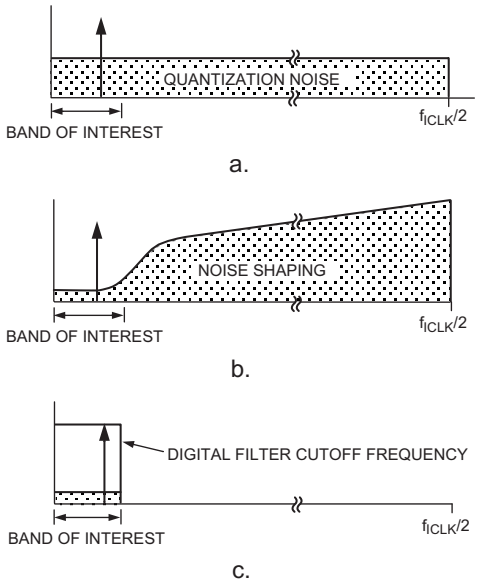


Figure 13. Sigma-Delta ADC

Table 5. Configuration With Default Filter

ICLK Frequency	Filter 1	Filter 2	Filter 3	Data State	Computation Delay	Filter Delay	Passband Bandwidth	Output Data Rate (ODR)
20 MHz	Bypassed	Bypassed	Bypassed	Unfiltered	0	0	(10 MHz)	20 MHz
20 MHz	4x	Bypassed	Bypassed	Partially Filtered	0.325	1.2µS	1.35 MHz	5 MHz
20 MHz	4x	Bypassed	2x	Fully Filtered	1.075	10.8µS	1 MHz	2.5 MHz
20 MHz	4x	2x	Bypassed	Partially Filtered	1.35	3.6µS	562.5 kHz	2.5 MHz
20 MHz	4x	2x	2x	Fully Filtered	1.625	22.8µS	500 kHz	1.25 MHz
20 MHz	4x	4x	Bypassed	Partially Filtered	1.725	6µS	281.25 kHz	1.25 MHz
20 MHz	4x	4x	2x	Fully Filtered	1.775	44.4µS	250 kHz	625 kHz
20 MHz	4x	8x	Bypassed	Partially Filtered	2.6	10.8µS	140.625 kHz	625 kHz
20 MHz	4x	8x	2x	Fully Filtered	2.25	87.6µS	125 kHz	312.5 kHz
20 MHz	4x	16x	Bypassed	Partially Filtered	4.175	20.4µS	70.3125 kHz	312.5 kHz
20 MHz	4x	16x	2x	Fully Filtered	3.1	174µS	62.5 kHz	156.25 kHz
20 MHz	4x	32x	Bypassed	Partially Filtered	7.325	39.6µS	35.156 kHz	156.25 kHz
20 MHz	4x	32x	2x	Fully Filtered	4.65	346.8µS	31.25 kHz	78.125 kHz
12.288MHz	4x	8x	2x	Fully Filtered	3.66	142.6µS	76.8 kHz	192 kHz
12.288MHz	4x	16x	2x	Fully Filtered	5.05	283.2µS	38.4 kHz	96 kHz
12.288MHz	4x	32x	Bypassed	Partially Filtered	11.92	64.45µS	21.6 kHz	96 kHz
12.288MHz	4x	32x	2x	Fully Filtered	7.57	564.5µS	19.2 kHz	48 kHz

AD7760 INTERFACE

Reading Data

The AD7760 uses a 16-bit bi-directional parallel interface. This interface is controlled by the $\overline{RD}$/WR and $\overline{CS}$ pins. There are two read operating modes depending on the output data rate.

When the AD7760 is outputting data at 5MSPS or less, the interface operates in a conventional mode as shown in Figure 2. When a new conversion result is available, an active low pulse is output on the $\overline{DRDY}$ pin. To read a conversion result from the AD7760, two 16-bit read operations are performed. The $\overline{DRDY}$ pulse indicates that a new conversion result is available. Both $\overline{RD}$/WR and $\overline{CS}$ go low to perform the first read operation. Shortly after both these lines go low, the databus becomes active and the 16 Most Significant Bits (MSBs) of the conversion result are output. The $\overline{RD}$/WR and $\overline{CS}$ lines must return high for a period of TBD ns before the second read is performed. This second read will contain the 8 Least Significant Bits (LSBs) of the conversion result along with 7 status bits. These status bits are shown in Table 6. The Cal bit is set to a 1 if a calibration has been performed. Table 14 contains descriptions of the other status bits.

Table 6. Status Bits During Data Read

D7							D0
DValid	Ovr	UFilt	LPwr	FiltOk	DLOk	Cal	0

Shortly after $\overline{RD}$/WR and $\overline{CS}$ return high, the databus will return to a high impedance state. Both read operations must be completed before a new conversion result is available as the new result will overwrite the contents on the output register. If a $\overline{DRDY}$ pulse occurs during a read operation, the data read will be invalid.

When the AD7760 is operating in modulator data output mode, i.e. Output Data Rate at 20MHz, a different interfacing scheme is necessary. To obtain data from the AD7760 in this mode, both $\overline{RD}$/WR and $\overline{CS}$ lines must be held low. This will bring the databus out of its high impedance state. Figure 3 shows the 20MHz Output Data Rate operation. A $\overline{DRDY}$ pulse is generated for each word and the data is valid on the rising edge of the $\overline{DRDY}$ pulse. This $\overline{DRDY}$ pulse could be used to latch the modulator data into a FIFO or as a DMA control signal. Shortly after the $\overline{RD}$/WR and $\overline{CS}$ lines return high, the AD7760 will stop outputting data and the databus will return to high impedance.

Sharing The Parallel Bus

By its nature, the high accuracy of the AD7760 make it sensitive to external noise sources. These include digital activity on the parallel bus. For this reason it is recommended that the AD7760 data lines are isolated from the system databus by means of a latch or buffer to ensure that there is no digital activity on the D0-D15 pins that is not controlled by the AD7760. If multiple, synchronized, AD7760 parts that share a properly distributed common MCLK signal exist in a system, these parts can share a common bus without being isolated from each other. This bus can then be isolated from the system bus by a single latch or buffer.

Writing To The AD7760

After a reset, only a single write operation to power up the AD7760 is necessary to start the part converting on default settings. While the AD7760 is configured to convert analog signals with the default settings on reset, there are many features and parameters on this part that the user can change by writing to the device. As some of the programmable registers are 16 bits wide, to program a register requires two write operations. The first write contains the register address while the second write contains the register data. There is an exception to this when a user filter is being downloaded to the AD7760. This is dealt with in detail in the following section. The AD7760 Registers section contains the register addresses and further details.

Figure 4 shows a write operation to the AD7760. The $\overline{RD}$/WR line is held high while the $\overline{CS}$ line is brought low for a minimum of TBD ns. The register address is latched during this period. The $\overline{CS}$ line is brought high again for a minimum of TBD ns before the register data is put onto the databus. If a read operation occurs between the writing of the register address and the register data, the register address is cleared and the next write must be the register address again. This also provides a method to get back to a known situation if the user somehow loses track whether the next write is an address or data.

It is envisaged that the AD7760 will be written to and configured on power-up and very infrequently, if at all, after that. Following any write operation, the full group delay of the filter must pass before valid data will be output from the AD7760.

Reading Status and Other Registers

The AD7760 features a number of programmable registers. To read back the contents of these registers or the status register, the user must first write to the control register of the device setting a bit corresponding to the register they wish to read. The next read operation will then output the contents of the selected register instead of a conversion result. More information on the relevant bits in the control register is given in the AD7760 Registers section.

CLOCKING THE AD7760

The AD7760 requires an external low jitter clock source. This signal is applied to the MCLK and $\overline{\text{MCLK}}$ pins. An internal clock signal (ICLK) is derived from the MCLK input signal. This ICLK controls all the internal operation of the AD7760. The maximum ICLK frequency is 20MHz but due to an internal clock divider, a range of MCLK frequencies can be used. There are three possibilities available to generate the ICLK:

1. ICLK = MCLK (CDIV[1:0] = 10)
2. ICLK = MCLK / 2 (CDIV[1:0] = 00)
3. ICLK = MCLK / 4 (CDIV[1:0] = 01)

These options are selected from the control register (See Register Section for further details). On power-up, the default is ICLK = MCLK / 4 to ensure that the part can handle the maximum MCLK frequency of 80MHz. If the user wishes to get output data rates equal to those used in audio systems, a 12.288 MHz ICLK frequency can be used. As shown in Table 5, output data rates of 192, 96 and 48kHz are achievable with this ICLK frequency. As mentioned previously, this ICLK frequency can be derived from different MCLK frequencies.

The MCLK jitter requirements depend on a number of factors and are given by the following equation:

$$t_{j(RMS)} = \frac{\sqrt{OSR}}{2 \times \pi \times f_{IN} \times 10^{\frac{SNR(dB)}{20}}}$$

OSR = Over-sampling ratio = $\frac{f_{ICLK}}{ODR}$

f_{IN} = Maximum Input Frequency

SNR(dB) = Target SNR.

Taking an example from Table 5:

ODR = 2.5MHz, f_{ICLK} = 20MHz, f_{IN} (max) = 1MHz, SNR = 108dB

$$t_{j(RMS)} = \frac{\sqrt{8}}{2 \times \pi \times 10^6 \times 10^{5.4}} = 1.79\,ps$$

This is the maximum allowable clock jitter for a full-scale 1MHz input tone with the given ICLK and Output Data Rate.

Taking a second example from Table 5:

ODR = 48kHz, f_{ICLK} = 12.288MHz, f_{IN} (max) = 19.2kHz, SNR = 120dB

$$t_{j(RMS)} = \frac{\sqrt{256}}{2 \times \pi \times 19.2 \times 10^3 \times 10^6} = 133\,ps$$

The input amplitude also has an effect on these jitter figures. If, for example, the input level was 3dB down from full-scale, the allowable jitter would be increased by a factor of √2 increasing the first example to 2.53ps RMS. This is due to the fact that the maximum slew rate is reduced by a reduction in amplitude. Figure 14 and Figure 15 illustrate this point showing the maximum slew rate of a sine wave of the same frequency but with different amplitudes.

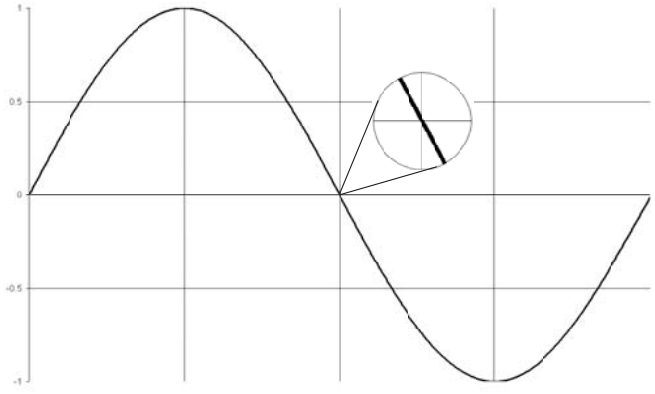


Figure 14. Maximum Slew Rate of Sine Wave with Amplitude of 2V Pk-Pk

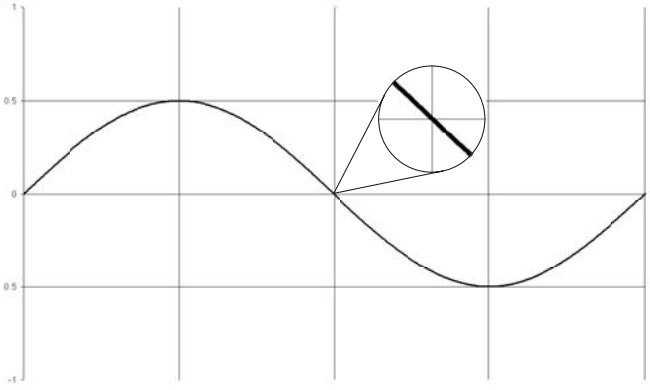


Figure 15. Maximum Slew Rate of Same Frequency Sine Wave with Amplitude of 1V Pk-Pk

DRIVING THE AD7760

The AD7760 has an on-chip differential amplifier. This amplifier will operate with a supply voltage (AV_{DD3}) from 3V to 5.5V. For a 4.096V reference, the supply voltage must be 5V.

To achieve the specified performance in full power mode, the differential amplifier should be configured as a first order anti-alias filter as shown in Figure 16. Any additional filtering should be carried out in previous stages using low noise, high-performance op-amps such as the AD8021.

Suitable component values for the first order filter are listed in Table 7. Using the first row as an example would yield a 10dB attenuation at the first alias point of 19MHz.

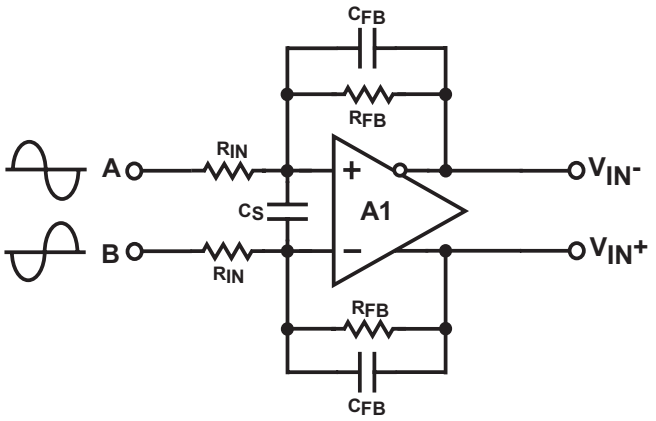


Figure 16. Differential Amplifier Configuration

Table 7. Full Power Component Values

ODR	V_{REF}	R_{IN}	R_{FB}	C_S	C_{FB}
2.5MHz	4.096v	1kΩ	655 Ω	5.6pF	33pF
2.5MHz	2.5v	TBD Ω	TBD Ω	TBD	TBD pF
48kHz	4.096v	TBD Ω	TBD Ω	TBD	TBD pF
48kHz	2.5v	TBD Ω	TBD Ω	TBD	TBD pF

Figure 17 shows the signal conditioning that occurs using the circuit in Figure 16 with a ±2.5v input signal biased around ground using the component values and conditions in the first row of Table 7. The differential amplifier will always bias the output signal to sit on the optimum common mode of $V_{REF}/2$, in this case 2.048V. The signal is also scaled to give the maximum allowable voltage swing with this reference value. This is calculated as 80% of V_{REF}, i.e. $0.8 \times 4.096V \approx 3.275V$ peak to peak on each input.

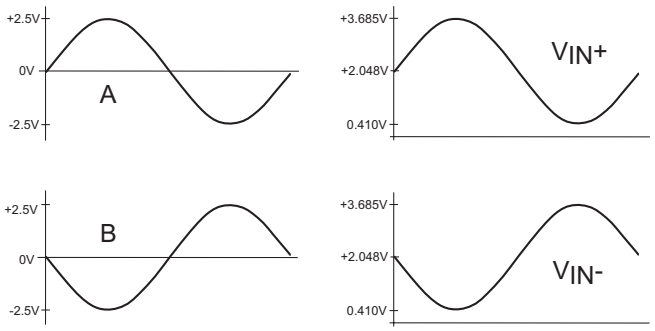


Figure 17. Differential Amplifier Signal Conditioning

To obtain maximum performance from the AD7760, it is advisable to drive the ADC with differential signals. However, it is possible to drive the AD7760 with a single ended signal once the common mode of the signal is within the range of +0.7V to +2.1V with V_{DD3} = 5V or +0.7 to +1.25V with V_{DD3} = 3.3V. In this case the on-chip differential amplifier can be used to convert the signal from single-ended to differential before being fed into the modulator inputs. Figure 18 shows how a bipolar single-ended signal biased around ground can be used to drive the AD7760 with the use of an external op-amp such as the AD8021.

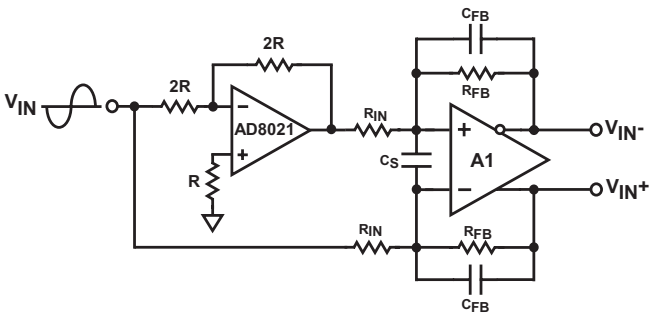


Figure 18. Single Ended to Differential Conversion

USING THE AD7760

The following is the recommended sequence for powering up and using the AD7760.

1. Apply Power
2. Start clock oscillator, applying MCLK
3. Take $\overline{\text{RESET}}$ low for a minimum of 1 MCLK cycle
4. Wait a minimum of 2 MCLK cycles after $\overline{\text{RESET}}$ has been released.
5. Write to Control Register 2 to power up the ADC and the differential amplifiers as required. The correct Clock Divider (CDIV[1:0]) ratio should be programmed here also.
6. Write to Control Register 1 to set up the Output Data Rate.
7. Take $\overline{\text{SYNC}}$ low for a minimum of 2 MCLK cycles.

Data can now be read from the part using the default filter, offset, gain and over range threshold values. The conversion data read will not be valid however until the group delay of the filter has passed. When this has occurred, the DVALID bit read with the data LSW will be set indicating that the data is indeed valid.

The user can now download their own filter if required (see Downloading a User-Defined Filter). Values for gain, offset and over range threshold registers can be written or read at this stage. An internal calibration sequence can also be initiated at this point.

BIAS RESISTOR SELECTION

The AD7760 requires a resistor to be connected between the R_{BIAS} pin and AGND. The value for this resistor is dependant on the reference voltage being applied to the device. The resistor value should be selected to give a current of 25µA through the resistor to ground. For a 2.5V reference voltage, the correct resistor value is 100kΩ and for a 4.096V reference, 160kΩ.

PROGRAMMABLE FIR FILTER

As previously mentioned, the third FIR filter on the AD7760 is user programmable. The default coefficients that are loaded on reset are given in Table 8. This gives a frequency response shown in Figure 19. The frequencies quoted in Figure 19 scale directly with the Output Data Rate.

Table 8. Default Filter Coefficients

#	Dec. Value	Hex Value	#	Dec. Value	Hex Value
0	53656736	332BCA0	24	700847	AB1AF
1	25142688	17FA5A0	25	-70922	401150A
2	-4497814	444A196	26	-583959	408E917
3	-11935847	4B62067	27	-175934	402AF3E
4	-1313841	4140C31	28	388667	5EE3B
5	6976334	6A734E	29	294000	47C70
6	3268059	31DDDB	30	-183250	402CBD2
7	-3794610	439E6B2	31	-302597	4049E05
8	-3747402	4392E4A	32	16034	3EA2
9	1509849	1709D9	33	238315	3A2EB
10	3428088	344EF8	34	88266	158CA
11	80255	1397F	35	-143205	4022F65
12	-2672124	428C5FC	36	-128919	401F797
13	-1056628	4101F74	37	51794	CA52
14	1741563	1A92FB	38	121875	1DC13
15	1502200	16EBF8	39	16426	402A
16	-835960	40CC178	40	-90524	401619C
17	-1528400	4175250	41	-63899	400F99B
18	93626	16DBA	42	45234	B0B2
19	1269502	135EFE	43	114720	1C020
20	411245	6466D	44	102357	18FD5
21	-864038	40D2F26	45	52669	CDBD
22	-664622	40A242E	46	15559	3CC7
23	434489	6A139	47	1963	7AB

The default filter should be sufficient for almost all applications. It is a standard brick wall filter with a symmetrical impulse response. The default filter has a length of 96, in non-aliasing with 120dB of attenuation at Nyquist. This filter not only performs signal anti-aliasing but also suppresses out-of-band quantization noise produced by the A-D conversion process. Any significant relaxation in the stop-band attenuation or transition band width relative to the default filter may result in a failure to meet the SNR specifications.

If a user does wish to create their own filter then the following should be noted:

- The filter must be even, symmetrical FIR.
- The coefficients are in sign-and-magnitude format with 26 magnitude bits and sign coded as positive=0.
- The filter length must be between 12 and 96 in steps of 12.
- As the filter is symmetrical, the number of coefficients that must be downloaded will be half the filter length. The default filter coefficients are an example of this with only 48 coefficients listed for a 96-tap filter.
- Coefficients are written from the center of impulse response (adjacent to the point of symmetry) outwards.
- The coefficients are scaled so that the in-band gain of the filter is equal to 134217726 with the coefficients rounded to the nearest integer. For a low pass filter this is the equivalent of having the coefficients sum arithmetically (including sign) to +67108863 (0x3FF FFFF) positive value over the half-impulse-response coefficient set (max 48 coefficients). Any deviation from this will result in a gain error being introduced.

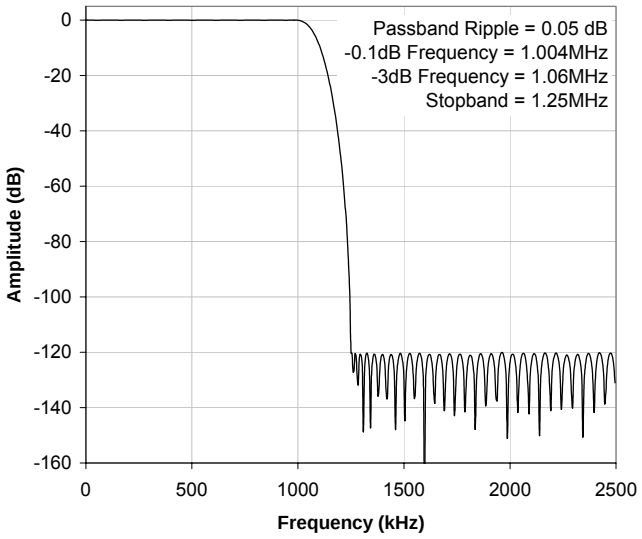


Figure 19. Default Filter Frequency Response (2.5MHz ODR)

The procedure for downloading a user-defined filter is detailed in the Downloading a User-Defined Filter section.

DOWNLOADING A USER-DEFINED FILTER

As previously mentioned, the filter coefficients are 27 bits in length; one sign and 26 magnitude bits. Since the AD7760 has a 16-bit parallel bus, the coefficients are padded with 5 MSB zeros to generate a 32-bit word and split into two 16-bit words for downloading. The first 16-bit word for each coefficient becomes (00000, Sign bit, Magnitude[25:16]), while the second word becomes (Magnitude [15:0]). To ensure that a filter is downloaded correctly, a checksum must also be generated and downloaded following the final coefficient. The checksum is a 16-bit word generated by splitting each 32-bit word mentioned above into 4 bytes and summing all bytes from all coefficients up to a maximum of 192 bytes (48 coefficients × 4 bytes). The same checksum is generated internally in the AD7760 and compared with the checksum downloaded. The DL_OK bit in the Status Register is set if these two checksums agree. The following is the procedure for downloading a user filter:

1. Write to Control Register 1 setting the DL_Filt bit and also the correct filter length bits corresponding to the length of the filter about to be downloaded (See Table 9).
2. Write the first half of the current coefficient data (00000, Sign bit, Magnitude[25:16]). The first coefficient to be written must be the one adjacent to the point of filter symmetry.
3. Write the second half of the current coefficient data (Magnitude [15:0]).
4. Repeat Steps 2 and 3 for each coefficient.
5. Write the 16-bit checksum.
6. There are two methods to verify that the filter coefficients have been downloaded correctly:
    a. Read the Status Register checking the DL_OK bit.
    b. Start reading data and observe the status of the DL_OK bit.

Table 9. Filter Length Values

FLEN[3:0]	Num Coeffs	Filter Length
0000	Default	Default
0001	6	12
0011	12	24
0101	18	36
0111	24	48
1001	30	60
1011	36	72
1101	42	84
1111	48	96

It should be borne in mind that since the user coefficients are stored in RAM, they will be cleared after a $\overline{\text{RESET}}$ operation or a loss of power..

EXAMPLE FILTER DOWNLOAD

The following is an example of downloading a short user defined filter with 24-taps. The frequency response is shown in Figure 20.

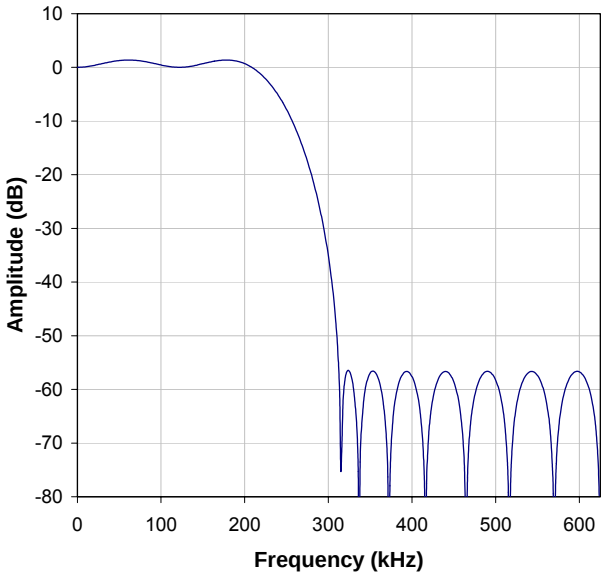


Figure 20. 24-Tap FIR Frequency Response

The coefficients for the filter are listed in Table 10. The coefficients are in shown from the center of symmetry outwards. The raw coefficients were generated using a commercially available filter design tool and scaled appropriately so their sum equals +67108863 (0x3FF FFFF).

Table 10. 24-Tap FIR Coefficients

Coeff	Raw	Scaled
1	0.365481974	53188232
2	0.201339905	29300796
3	0.009636604	1402406
4	-0.075708848	-11017834
5	-0.042856209	-6236822
6	0.019944246	2902466
7	0.036437914	5302774
8	0.007592007	1104856
9	-0.021556583	-3137108
10	-0.024888355	-3621978
11	-0.012379538	-1801582
12	-0.001905756	-277343

Table 11 shows the Hex values (in sign and magnitude format) that are downloaded to the AD7760 to realize this filter. The table is also split into the bytes which are all summed to produce the checksum. The checksum generated from these coefficients is 0x0E6B.

Table 11. Filter Hex Values

Coeff	Word 1		Word 2	
	Byte 1	Byte 2	Byte 3	Byte 4
1	03	2B	96	88
2	01	BF	18	3C
3	00	15	66	26
4	04	A8	1E	6A
5	04	5F	2A	96
6	00	2C	49	C2
7	00	50	E9	F6
8	00	10	DB	D8
9	04	2F	DE	54
10	04	37	44	5A
11	04	1B	7D	6E
12	04	04	3B	5F

What follows is a list of 16-bit words that the user would write to the AD7760 to set up the ADC and download this filter assuming an output data rate of 1.25MHz has already been selected.

0x0001 Address of Control Register 1

0x8079 Control Reg Data; DL Filter, Set Filter Length = 24, Set Output Data Rate = 1.25MHz

0x032B First Coefficient, Word 1

0x9688 First Coefficient, Word 2

0x01BF Second Coefficient, Word 1

0x183C Second Coefficient, Word 2

… …

0x0404 Twelfth (Final) Coefficient, Word 1

0x3B5F Final Coefficient, Word 2

0x0E6B Checksum

Wait TBD xS for AD7760 to fill remaining unused coefficients with zeros.

0x0001 Address of Control Register

0x0879 Control Reg Data; Set Read Status and maintain filter length and decimation settings.

Read contents of Status Register. Check Bit 7 (DL_OK) to determine that the filter was downloaded correctly.

AD7760 REGISTERS

The AD7760 has a number of user-programmable registers. The control registers are used to set the decimation rate, the filter configuration, the clock divider etc. There are also digital gain, offset and over-range threshold registers. Writing to these registers involves writing the register address first, then a 16-bit data word. Register Addresses, details of individual bits and default values are given here.

Table 12. Control Register 1 (Address 0x0001, Default Value 0x001A)

MSB **LSB**

DL Filt	RD Ovr	RD Gain	RD Off	RD Stat	CAL	SYNC	FLEN3	FLEN2	FLEN1	FLEN0	$\overline{\text{BYP F3}}$	$\overline{\text{BYP F1}}$	DEC2	DEC1	DEC0

Bit	Mnemonic	Comment
15	DL Filt[1]	Download Filter. Before downloading a user defined filter, this bit must be set. The Filter Length bits must also be set at this time. The write operations that follow will be interpreted as the user coefficients for the FIR filter until all the coefficients and the checksum have been written.
14	RD Ovr[1,2]	Read Overrange. If this bit has been set, the next read operation will output the contents of the Overrange Threshold Register instead of a conversion result.
13	RD Gain[1,2]	Read Gain. If this bit has been set, the next read operation will output the contents of the digital Gain Register.
12	RD Off[1,2]	Read Offset. If this bit has been set, the next read operation will output the contents of the digital Offset Register.
11	RD Stat[1,2]	Read Status. If this bit has been set, the next read operation will output the contents of the Status Register.
10	CAL[1]	Calibration. Setting this bit will initiate an internal calibration routine. This routine will take 14mS with a 20MHz ICLK.
9	SYNC[1]	Synchronize. Setting this bit will initiate in internal synchronisation routine. Setting this bit simultaneously on multiple devices will synchronize all filters.
8-5	FLEN3:0	Filter Length Bits. These bits must be set when the DL Filt bit is set and before a user defined filter is downloaded.
4	$\overline{\text{BYP F3}}$	Bypass Filter 3. If this bit is a 0, Filter 3 (Programmable FIR) will be bypassed.
3	$\overline{\text{BYP F1}}$	Bypass Filter 1. If this bit is a 0, Filter 1 will be bypassed. This should only occur when the user requires unfiltered modulator data to be output.
2-0	DEC2:0	Decimation Rate. These bits set the decimation rate of Filter 2. All zeros implies that the filter is bypassed. A value of 1 corresponds to 2x decimation, a value of 2 corresponds to 4x and so on up to the maximum value of 5, corresponding to 32x decimation.

[1] Bits 15-9 are all self clearing bits.
[2] Only one of the bits 14-11 may be set in any write operation as they all determine the contents of the next read operation

Table 13. Control Register 2 (Address 0x0002, Default Value 0x009B)

MSB **LSB**

0	0	0	0	0	0	0	0	0	0	CDIV1	CDIV0	PD	LPWR	1	D1PD

Bit	Mnemonic	Comment
5-4	CDIV1:0	Clock Divider Bits. These set the divide ratio of the MCLK signal to produce the internal ICLK. Setting CDIV[1:0] = 00 divides the MCLK by 2, setting CDIV[1:0] = 01 divides MCLK by 4. If CDIV[1:0] = 10 then the MCLK frequency is equal to the ICLK. CDIV[1:0] = 11 is not allowed.
3	PD	Power Down. Setting this bit powers down the AD7760 reducing the power consumption to TBD µW.
2	LPWR	Low Power. If this bit is set, the AD7760 is operating in a low power mode. The power consumption is reduced for a 6dB reduction in noise performance.
1		Write a '1' to this bit.
0	D1PD	Differential Amplifier Power Down. Setting this bit powers down the on-chip differential amplifier.

Table 14. Status Register (Read Only)

MSB															LSB
PART 1	PART 0	DIE 2	DIE 1	DIE 0	DVALID	LPWR	OVR	DL OK	Filter OK	U Filter	$\overline{\text{BYP F3}}$	$\overline{\text{BYP F1}}$	DEC2	DEC1	DEC0

Bit	Mnemonic	Comment
15,14	PART1:0	Part Number. These bits will be constant for the AD7760.
13-11	DIE2:0	Die Number. These bits will reflect the current AD7760 die number for identification purposes within a system.
10	DVALID	Data Valid. This bit corresponds to the DVALID bit in the status word output in the second 16-bit read operation.
9	LPWR	Low Power. If the AD7760 is operating in Low Power Mode, this bit is set to a 1.
8	OVR	If the current analog input exceeds the current overrange threshold, this bit will be set.
7	DL OK	When downloading a user filter to the AD7760, a checksum is generated. This checksum is compared to the one downloaded following the coefficients. If these checksums agree, this bit is set.
6	Filter OK	When a user-defined filter is in use, a checksum is generated when the filter coefficients pass through the filter. This generated checksum is compared to the one downloaded. If they match, this bit is set.
5	U Filter	If a user-defined filter is in use, this bit is set.
4	$\overline{\text{BYP F3}}$	Bypass Filter 3. If Filter 3 is bypassed by setting the relevant bit in Control Register 1, this bit is also set.
3	$\overline{\text{BYP F1}}$	Bypass Filter 1. If Filter 1 is bypassed by setting the relevant bit in Control Register 1, this bit is also set.
2-0	DEC2:0	Decimation Rate. These correspond to the bits set in Control Register 1.

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NON BIT-MAPPED REGISTERS

Offset Register (Address 0x0003, Default Value 0x0000)

The Offset Register uses 2's Complement notation and is scaled such that 0x7FFF (maximum positive value) and 0x8000 (maximum negative value) correspond to an offset of +0.78125% and -0.78125% respectively. Offset correction is applied after any gain correction. Using the default gain value of 1.25 and assuming a reference voltage of 4.096V, the offset correction range is approximately ±25mV.

Gain Register (Address 0x0004, Default Value 0xA000)

The Gain Register is scaled such that 0x8000 corresponds to a gain of 1.0. The default value of this register is 1.25 (0xA000). This gives a full scale digital output when the input is at 80% of V_{REF}. This ties in with the maximum analog input range of ±80% of V_{REF} Pk-Pk.

Over Range Register (Address 0x0005, Default Value 0xCCCC)

The Over Range register value is compared with the output of the first decimation filter to obtain an overload indication with minimum propagation delay. This is prior to any gain scaling or offset adjustment. The default value is 0xCCCC which corresponds to 80% of V_{REF} (the maximum permitted analog input voltage) Assuming V_{REF} = 4.096V, the bit will then be set when the input voltage exceeds approximately 6.55v pk-pk differential. Note that the over-range bit is also set immediately if the analog input voltage exceeds 100% of V_{REF} for more than 4 consecutive samples at the modulator rate.

OUTLINE DIMENSIONS

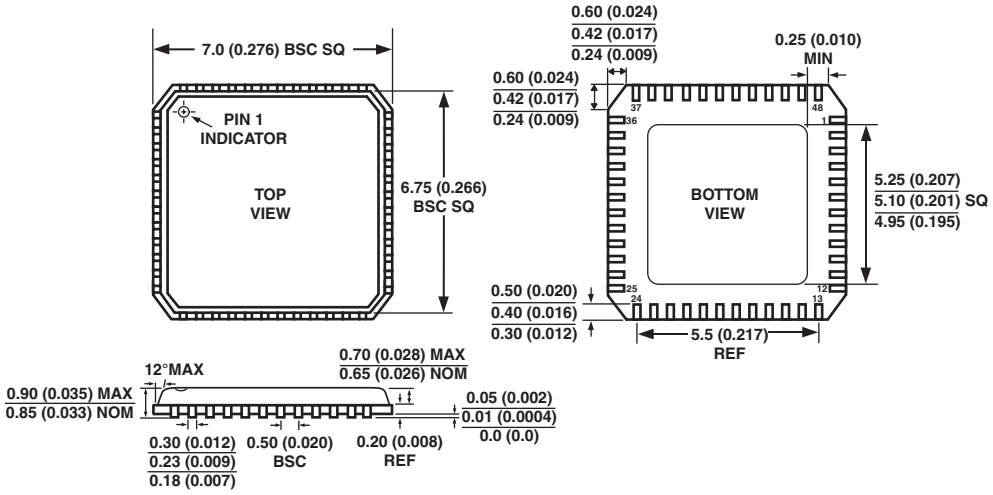


Figure 21. 48-Lead Frame Chip Scale Package [LFCSP] (CP-48)—Dimensions shown in millimeters

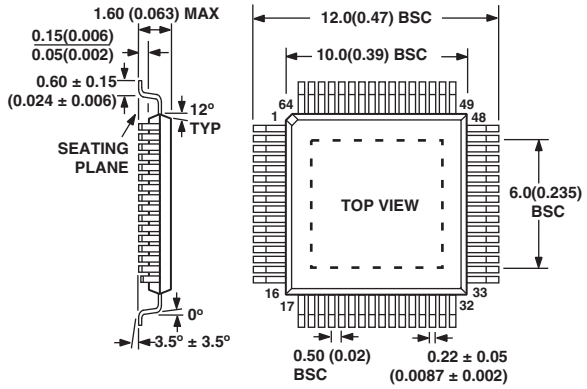


Figure 22. 64-Lead Thin Quad Flat Pack (Exposed Paddle) [TQFP] (SV-64)—Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7760BCP	–40°C to +85°C	Lead Frame Chip Scale Package	CP-48
AD7760BSV	–40°C to +85°C	Thin Quad Flat Pack, Exposed Paddle	SV-64

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