PI3HDMI511

HDMI™1.4 Redriver Source-side Application

Features

- HDMI™ 1.4 compliant re-driver
- Operation upto 3.4 Gbps per lane (340MHz pixel clock)
  - 4K x 2K 24Hz(297MHz)
  - 3D Video formats(1080p, 1080i, 720p)
- Support up to 48-bit per pixel Deep Color™
- Convert low-swing DC or AC coupled differential input
  - Open-drain current steering Rx terminated differential output
  - Support Dual Mode DisplayPort source devices
- Provide Output Squelch function to turn off TMDS common mode output buffer when TMDS clock is not present
- Built-in Rx sense detection function
- Programmable equalizer, emphasis and amplitude settings to achieve optimized HDMI signal integrity
- Integrated Passive DDC level shifter
  - 3.3V source to 5V sink
- Idle clock detection function for output squelch and auto standby
- Programmable input TMDS termination control (on or off)
- 3.3V Power supply required
- Integrated ESD protection on I/O pins
  - 8kV contact per IEC61000-4-2, level 4
  - 8kV HBM
- Packaging
  - Pb-free & Green
  - 32-contact TQFN (ZL)Description

Application

- Notebook computers and docking station
- Set-Top Box(STB)
- A/V Home entertainment systems
- Dongle and switch boxes

Description

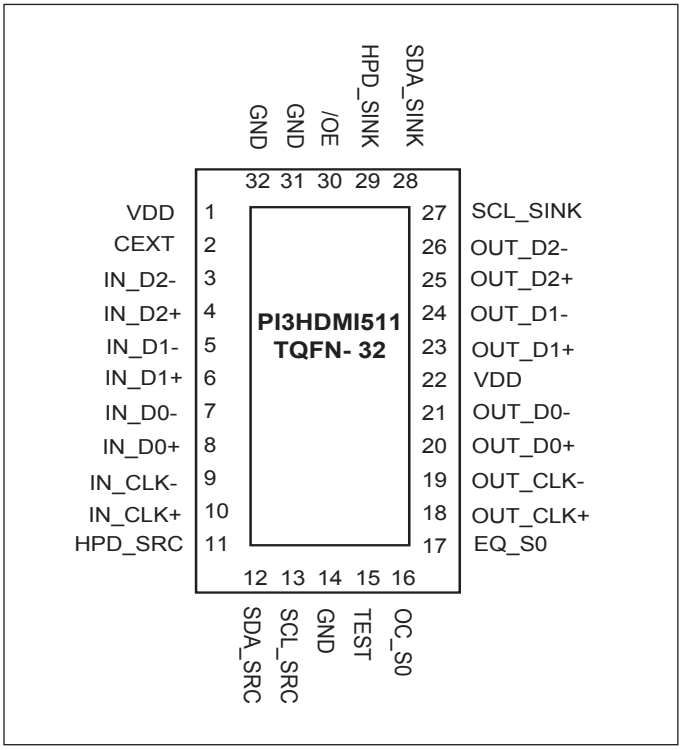
PI3HDMI511 is TMDS Redriver supporting HDMI 1.4 and DVI specifications up to a data rate of 3.4Gbps with 48-bit per pixel Deep Color™. It also support enhanced robust ESD/EOS protection of 8kV, which is required by many consumer video networks today.

It converts the DC and AC coupled source devices into the HDMI compliant signal with proper signal swing, espically in the Notebook HDMI and Dual mode DP PC systems.

Programmable termination settings at TMDS input help to avoid the compatibility issue caused by non standard HDMI source to determine the connection status of TMDS channel with proper termination voltage setting.

With Pericom's intelligent power management techniques, the PI3HDMI511 can automatically enter low power states when no valid signal presents on the TMDS link.

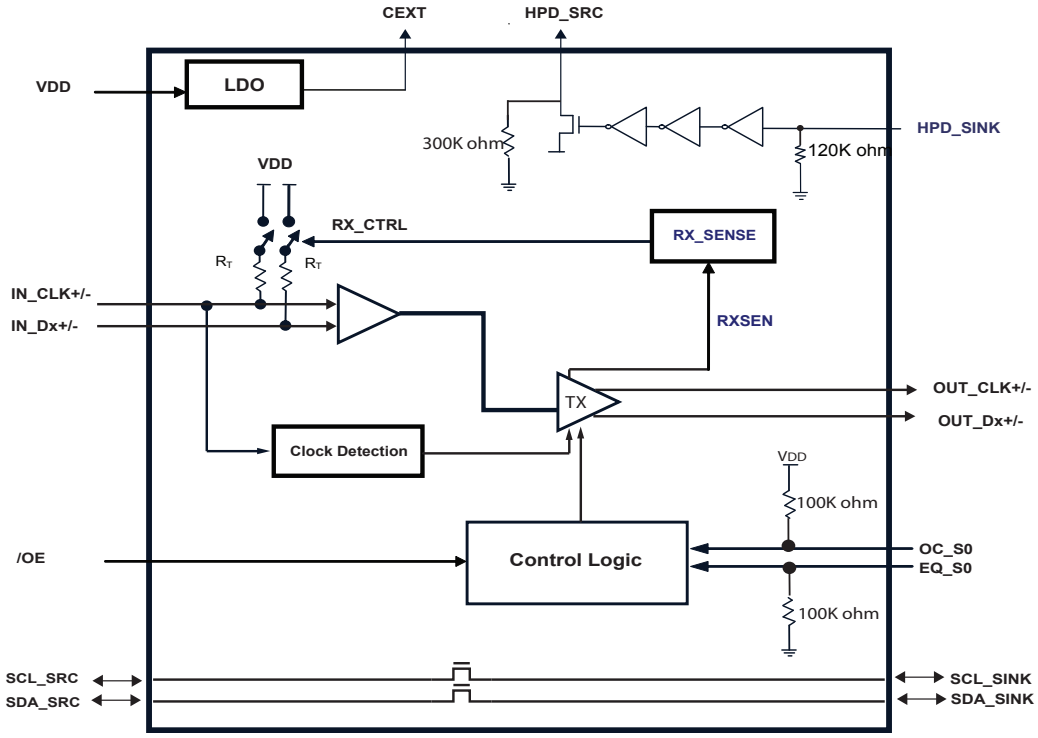
Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
2	CEXT	PWR	LDO output for internal core supplier. External capacitor 2.2 to 4.7µF should be added to GND.
3	IN_D2-	I	TMDS inputs. R_T=50 ohm
4	IN_D2+	I	
5	IN_D1-	I	
6	IN_D1+	I	
7	IN_D0-	I	
8	IN_D0+	I	
9	IN_CLK-	I	
10	IN_CLK+	I	
11	HPD_SRC	O	HPD output; internal pull-down at 300K ohm
12	SDA_SRC	IO	DDC Data on source side
13	SCL_SRC	IO	DDC Clock on source side
15	Test	I	Must be tied LOW for normal operation
16	OC_S0	I	TMDS output pre-emphasis selection. See OC_S0 truth table for functionality. This pin has internal 100K ohm pull-up
17	EQ_S0	I	TMDS input equalization selection. If LOW or floating , EQ is set at 9dB for all TMDS data inputs If HIGH, EQ is set at 15dB for all TMDS data inputs (please note, TMDS clock inputs are always set to 3dB EQ) This pin has an internal 100K ohm pull-down
18	OUT_CLK+	O	TMDS outputs.
19	OUT_CLK-	O	
20	OUT_D0+	O	
21	OUT_D0-	O	
23	OUT_D1+	O	
24	OUT_D1-	O	
25	OUT_D2+	O	
26	OUT_D2-	O	
27	SCL_SINK	IO	Sink side DDC Clock
28	SDA_SINK	IO	Sink side DDC Data
29	HPD_SINK	I	Sink side hot plug detector input; internal pull-down at 120K ohm.
30	/OE	I	Output Enable control. Active low. Internal 100K ohm pull-down. See truth table for functionality.
1, 22	VDD	PWR	3.3V power supply
14, 31, 32	GND	Ground	Power Ground

Block diagram:



Description of Operation

Squelch function:

Squelch control is using low frequency signal detection. When TMDS input clock frequency is less than 10MHz, it will show no input signal. When input signal is not present, IC will enter power-down mode.

Rx-sense detector:

The PI3HDMI511 will check 50 ohm termination resistor(R_T) within HDMI Rx chipset. If the R_T=50 ohm is not present, we assume no valid HDMI Rx is connected.

Therefore, IC will turn off our 50 ohm input termination resistor for all TMDS data and clock channels.When no valid R_T = 50 ohm is detected in the HDMI Receiver, the IC will enter to the power-down mode.

OC_S0 Truth Table

TMDS Output Pre-emphasis Setting

OC_S0 (internal pull-up)	Single-end Vswing (mV)	Pre-emphasis (dB)
0	500	0 (open drain)
1	500	2.5 (open drain)

Note

For clock channel, pre-emphesis value is fixed to 0 dB.

TMDS Input Equalization Setting

EQ_S0	Equalization (dB)
0	9dB
1	15dB

Note

For CLK channel, the EQ value is fixed to 3dB.

/OE Truth Table

/OE	Operation
0	Normal Operation Mode
1	Power Down Mode

Absolute Maximum Ratings

Item	Rating
Supply Voltage to Ground Potential	5.5V
All Inputs and Outputs	-0.5V to V_{DD}+0.5V
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	3.0	3.3	3.6	V

DC Specification

Parameter	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage			3.3		V
I_{DD}	V_{DD} Supply Current	Output Enable (open drain 500mV single-ended 0dB pre-emphasis)		120	150	mA
Idd_Squelch	Supply Current in squelch mode	Input TMDS signal not valid, /OE = Low		11	13	mA
Idd_Rx Sense	supply current when no 50ohm detected in Rx	Input TMDS is valid, but 50ohm Rx Sense(RXSEN) is not detected /OE = Low		4	5	mA
I_{stb}	Standby mode	V_{DD}=3.6V, HPD_SINK=0, /OE = High		4	5	mA
V_{OL_HPD}	Open Drain Output Low Voltage	I_{OL} = 4 mA	0		0.4	V
I_{OFF_HPD}	Off leakage current	V_{DD}=0, V_{IN}=3.6V			20	µA
		V_{DD}=0, V_{IN}=5.5V			40	
I_{OZ_HPD}	Open drain Output leakage current	V_{DD}=3.6, V_{IN}=3.6V			20	
		V_{DD}=3.6, V_{IN}=5.5V			40	

HPD_SINK

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	High level digital input current	V_{IH} =VDD	25		40	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage	V_{DD}=3.3V	2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V

Control Pin (/OE)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	High level digital input current	V_{IH} =VDD	30		45	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage		2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V

DDC Channel Block

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IO}	Input/Output capacitance	V_I peak-peak = 1V, 100 KHz		10		pF
R_{ON}	On resistance	I_O = 3mA, V_O = 0.4V		25	50	Ω
V_{pass}	Switch Output voltage	V_I=3.3V, I_I=100uA V_{DD}=3.3V, External pull-up to VDD(15K ohm ~ 5K ohm)	1.5	2.0	2.5	V

Control Pins(OC_S0 with 100K ohm pull-up)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	High level logic input current	V_{IH}=VDD			10	µA
I_{IL}	Low level logic input current	V_{IL}=GND		35	50	µA

Control Pins(EQ_S0 with 100K ohm pull-down)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	High level logic input current	V_{IH}=VDD		35	50	µA
I_{IL}	Low level logic input current	V_{IL}=GND			10	µA

TMDS Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units

V_{OH}	Single-ended high level output voltage	V_{DD} = 3.3V, Rout=50 ohm	V_{DD}-10		V_{DD}+10	mV
V_{OL}	Single-ended low level output voltage		V_{DD}-600		V_{DD}-400	mV
V_{swing}	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage (1)				180	mV
$V_{OD(U)}$	Undershoot of output differential voltage (2)				200	mV
$V_{OD(U)}$	Change in steady-state common-mode output voltage between logic				5	mV
I_{OS}	Short Circuit output current		-12		12	mA
	Short Circuit output current	at double termination mode	-24		24	
$V_{I(open)}$	Single-ended input voltage under high impedance input or open	I_I = 10uA	V_{DD}-10		V_{DD}+10	mV
R_T	Input termination resistance	V_{IN} = 2.9V	45	50	55	Ω
I_{OZ}	Leakage current with Hi-Z I/O	V_{DD} = 3.6V, /OE=High			10	μA

Note:
1. Overshoot of output differential voltage $V_{OD(O)} = (V_{SWING(MAX)} * 2) * 15\%$,
2. Undershoot of output differential voltage $V_{OD(U)} = (V_{SWING(MIN)} * 2) * 25\%$

AC Characteristics (Over recommended operating conditions unless otherwise noted)

TMDS Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation delay	V_{DD} = 3.3V, Rout = 50-ohm			2000	ps
t_r	Differential output signal rise time (20% - 80%)				190	
t_f	Differential output signal fall time (20% - 80%)				190	
$t_{sk(p)}$	Pulse skew			10	50	ps
$t_{sk(D)}$	Intra-pair differential skew			23	50	
$t_{sk(o)}$	Inter-pair differential skew				100	
$t_{jit(pp)}$	Peak-to-peak output jitter CLK residual jitter	Data Input = 1.65 Gbps HDMI data pattern CLK Input = 165 MHz clock		15	30	
$t_{jit(pp)}$	Peak-to-peak output jitter DATA Residual Jitter			18	50	
t_{en}	Enable time				1000	ns
t_{dis}	Disable time				10	

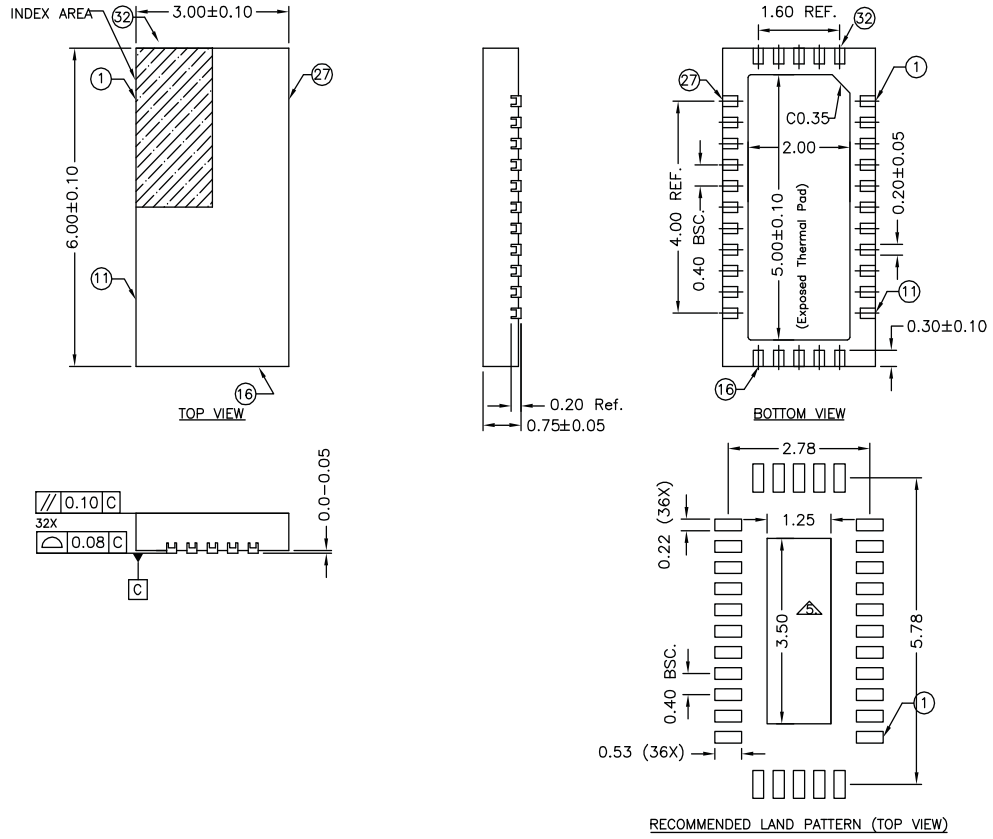
DDC I/O Pins (SCL_SRC, SCL_SINK, SDA_SRC, SDA_SINK)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{pd(DDC)}$	Propagation Delay	C_L = 10pF		0.4	2.5	ns

Control and Status Pins (HPD_SINK, HPD)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{pd(HPD)}$	Propagation Delay	C_L = 10pF, pull-up resistor=1K ohm, Open drain output		10		ns

Packaging Mechanical: 32-Contact TQFN (ZL)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

PERICOM Enabling Serial Connectivity	DATE: 10/09/09
DESCRIPTION: 32-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZL (ZL32)	
DOCUMENT CONTROL #: PD-2044	REVISION: A

09-0125

Please check for the latest package information on the Pericom web site at www.pericom.com/packaging/.

Related DisplayPort/Dual Mode DisplayPort Products

Part Number	Product Description	Availability
PI3HDMI1201	DisplayPort 1.2 Re-driver with built-in AUX listener	Now
PI3VDP1430	Dual Mode DisplayPort to HDMI Level Shifter and Re-driver	Now
PI3HDMI611	3.4G HDMI1.4 Re-driver for Sink application, supporting Dual Mode DisplayPort	Now
PI3VDP3212	2-Lane DisplayPort1.2 Compliant Switch	Now
PI3VDP12412	4-Lane DisplayPort1.2 Compliant Switch	Now
PI3HDMI412AD	1:2 Active 3.4Gbps HDMI1.4 compliant Splitter/Re-driver	Now
PI3HDMI521	2:1 3.4Gbps HDMI1.4 Switch/Re-driver with built-in ARC and Fast Switching support for Source Application	Now
PI3HDMI621	2:1 3.4Gbps HDMI1.4 Switch/Re-driver with built-in ARC and Fast Switching support for Sink Application	Now
PI3HDMI336	3:1 Active 3.4Gbps HDMI Switch/Re-driver with I^2C control and ARC Transmitter	Now

Reference Information

Document	Description
AN	PI3HDMI511 HDMI1.4 Application Note
VESA	VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010 VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012 VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009
HDMI	High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC, June 5, 2009

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDMI511ZLE	ZLE	Pb-free & Green 32-Contact TQFN

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

• E = Pb-free and Green

• X suffix = Tape/Reel

Revision Histroy

Date	Changes
07/19/12	Add Tr in the block diagram, IDD,Istb with Passive DDC level shifter.

Appendix A: Generic Application Information

Eye Diagram Performance:

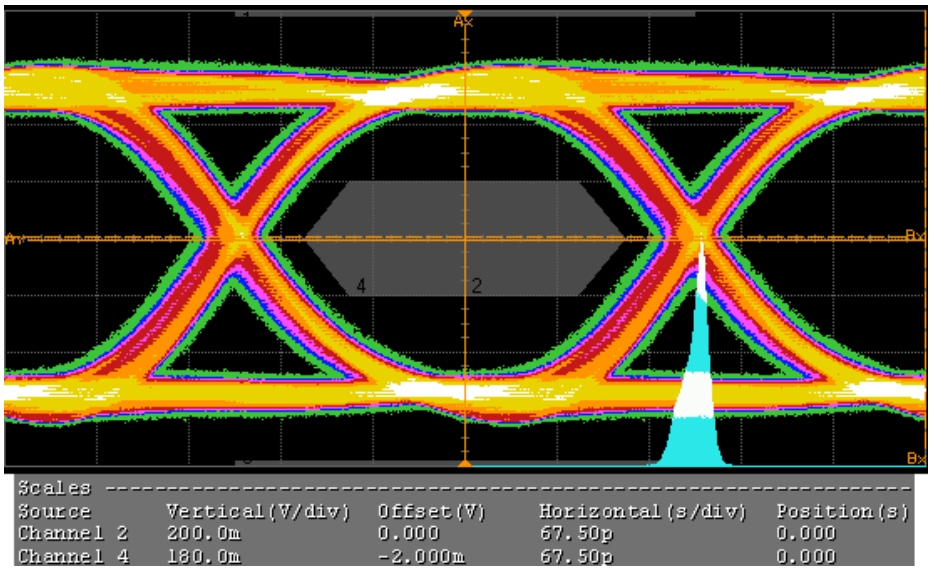


Figure 1: Eye Diagram at 1920x1080p 48bit Deep Color with 48" Input Trace, 9dB Equalization, 500mV Swing, 2.5dB Pre-emphasis.

Measurement setup:

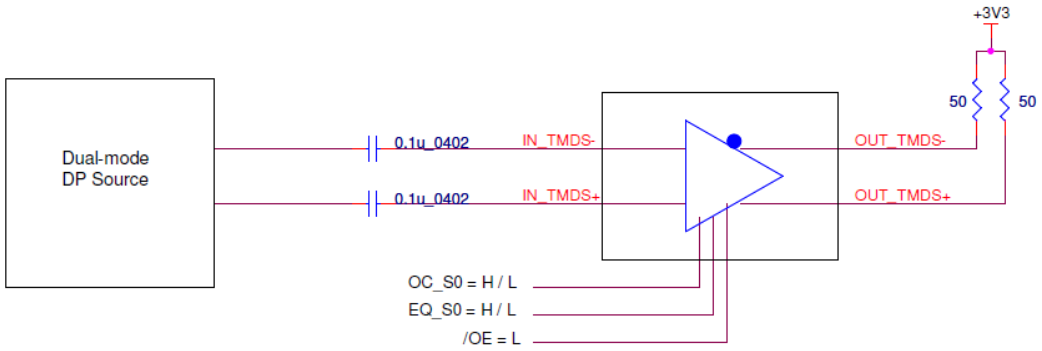


Figure 2: Test Setup of AC-coupled TMDS Input

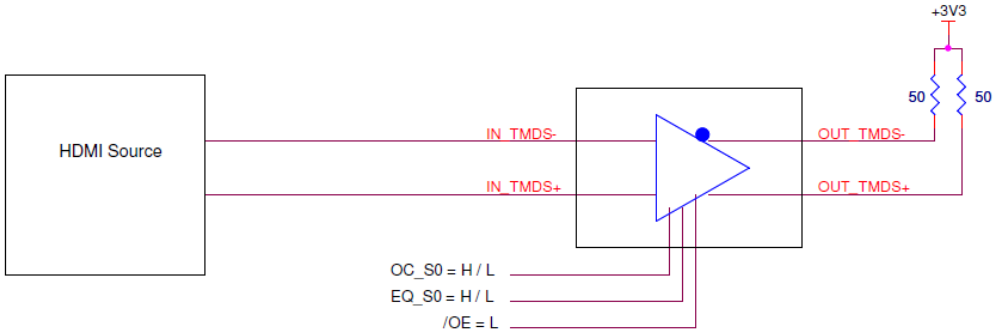


Figure 3: Test Setup of DC-coupled TMDS Input

Application Information:

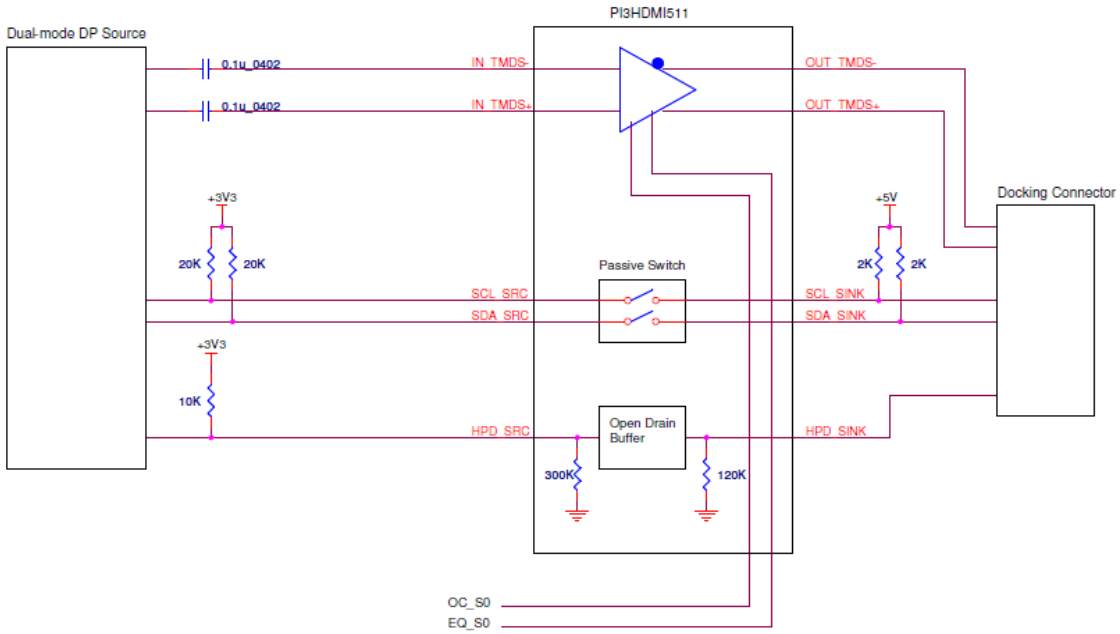


Figure 4: Application Diagram

For more detailed application information, please refer to "PI3HDMI511_HDMI_ApplicationInformation.doc".

Recommended Power Supply Decoupling Circuit

Figure 5 is the recommended power supply decoupling circuit configuration. It is recommended to put a 0.1µF decoupling capacitors on each VDD pin of our part. Four 0.1µF decoupling capacitors are put in Figure 5 with an assumption of only four VDD pins on our part.

On top of 0.1µF decoupling capacitor on each VDD pin, it is recommended to put a 10µF decoupling capacitor near our part's VDD for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

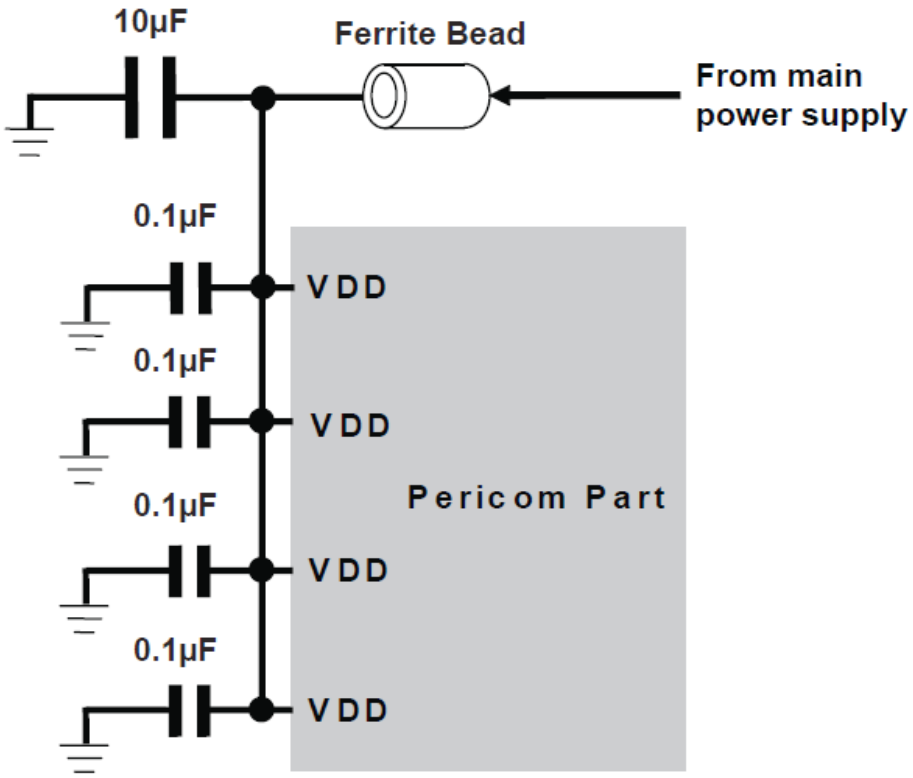


Figure 5 Recommended Power Supply Decoupling Circuit Diagram

Requirements on the Decoupling Capacitors

i: There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.
ii: 0.1uF decoupling capacitor in 0402 package is recommended.

Layout and Decoupling Capacitor Placement Consideration

i. Each 0.1µF decoupling capacitor should be placed as close as possible to each VDD pin.
ii. VDD and GND planes should be used to provide a low impedance path for power and ground.
iii. Via holes should be placed to connect to VDD and GND planes directly.
iv. The width between the traces should be as wide as possible.
v. Trace length should be as short as possible.
vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
vii. 10µF capacitor should also be placed close to our part and should be placed in the middle location of 0.1µF capacitors.
viii. Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes, since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.

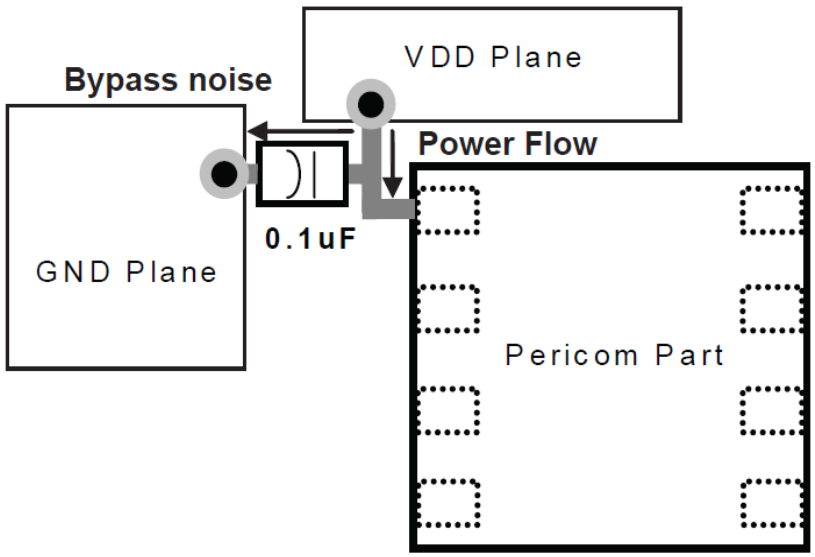
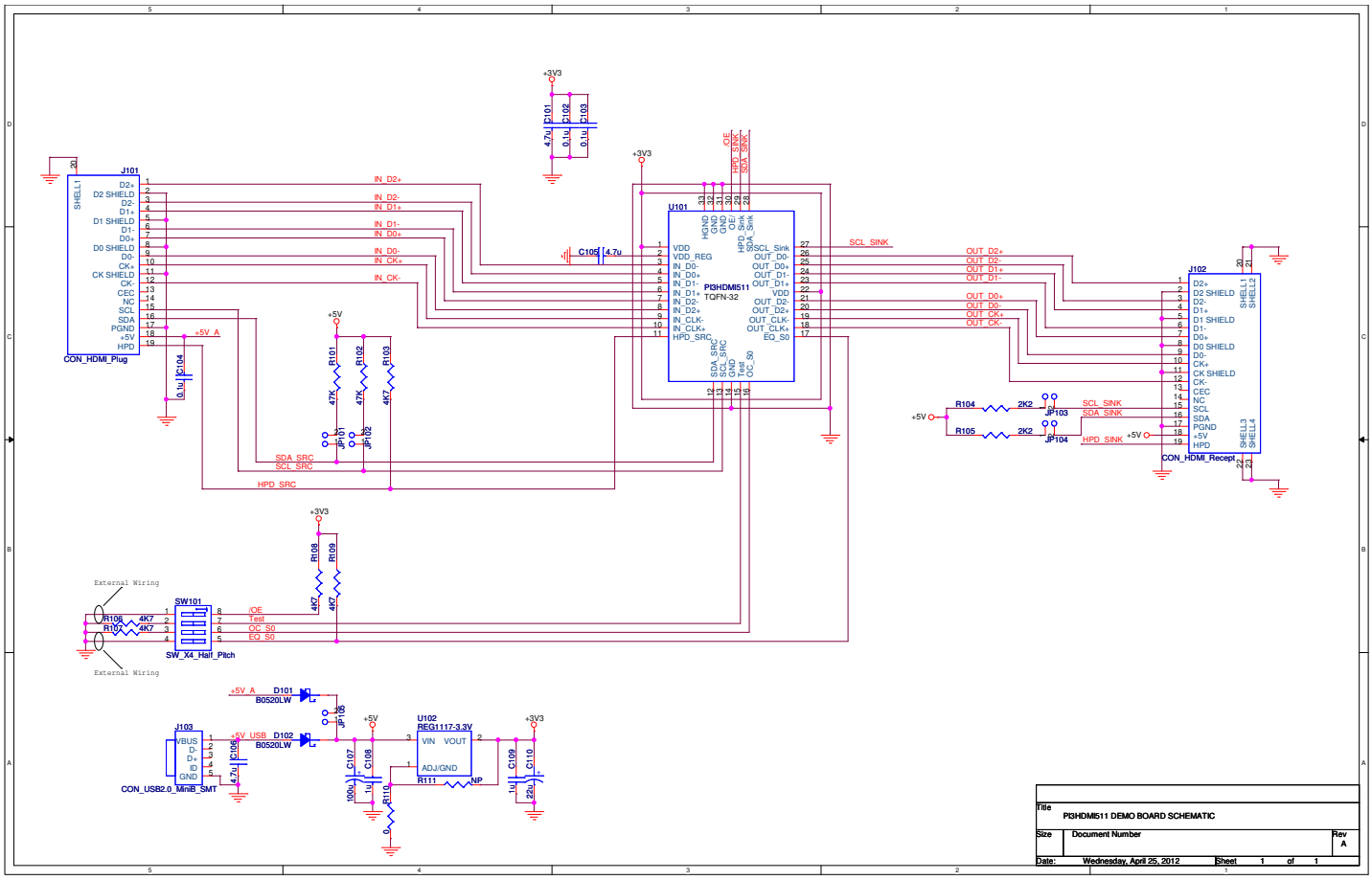
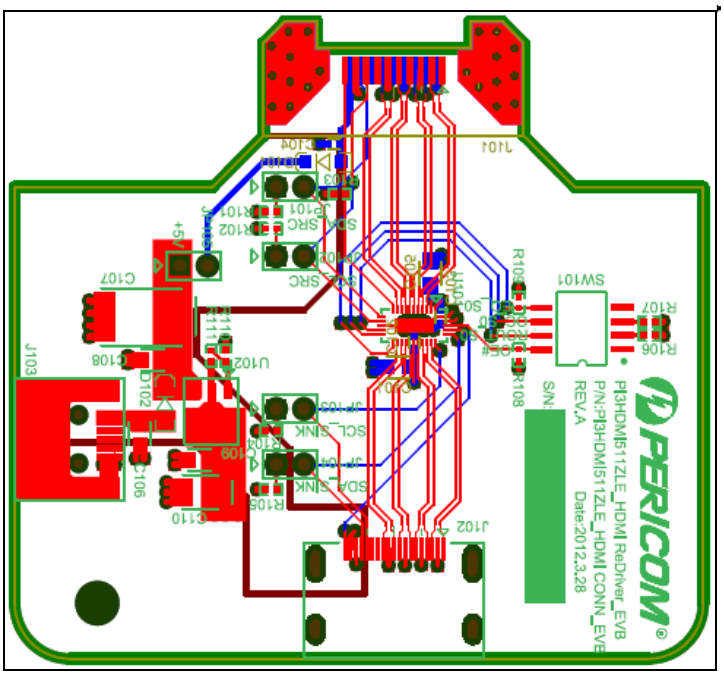


Figure 6 Layout and Decoupling Capacitor Placement Diagram

Appendix B: Evaluation Board Schematic and Layout





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