

# M5003 Series

## 9x16 mm FR-4, 3.3 Volt, CMOS/TTL/PECL/LVDS, HPVCXO



- Ideal for applications requiring long term (20 year) all-inclusive stability

**Ordering Information**

**00.0000**  
**MHz**

**M5003 2 0 R 1 P K -R**

**Product Series** \_\_\_\_\_

**Temperature Range** \_\_\_\_\_

1: 0°C to +70°C      2: -40°C to +85°C  
6: -20°C to +70°C    7: 0°C to +85°C

**Stability** \_\_\_\_\_

0: Nominal per APR selection

**Output Type** \_\_\_\_\_

R: Complementary tri-state (PECL/LVDS)  
T: Tri-state (CMOS)

**Absolute Pull Range (APR)** \_\_\_\_\_

1: ±25 ppm  
2: ±15 ppm

**Symmetry/Logic Compatibility** \_\_\_\_\_

D: 45/55% CMOS/TTL      L: 45/55% LVDS  
P: 45/55% PECL

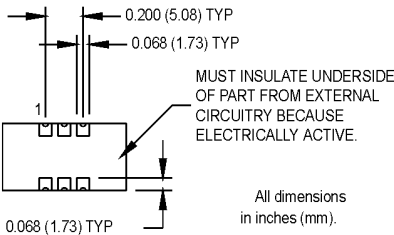
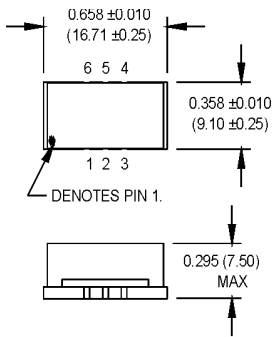
**Package/Lead Configurations** \_\_\_\_\_

K: FR-4, 6-Pad

**RoHS Compliance** \_\_\_\_\_

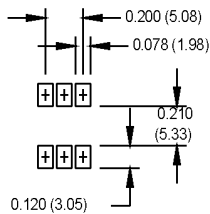
Blank: non-RoHS compliant part  
-R: RoHS compliant part

**Frequency (customer specified)** \_\_\_\_\_



All dimensions in inches (mm).

**SUGGESTED SOLDER PAD LAYOUT**



**Pin Connections**

PIN	FUNCTION
1	Control Voltage
2	Tristate
3	Ground
4	Output 1
5	N/C or Output 2
6	+Vdd

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	1 19.44		160 800	MHz MHz	CMOS/TTL PECL/LVDS
Operating Temperature	T <sub>A</sub>	(See Ordering Information)				
Storage Temperature	T <sub>s</sub>	-55		+105	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				
Aging						
1st Year				1.5	ppm	
Thereafter (per year)				0.5	ppm	
Pullability/APR		(See Ordering Information)				
Control Voltage	V <sub>c</sub>	0.3	1.65	3.0	V	Over Control Voltage
Tuning Range				25	ppm/V	
Modulation Bandwidth	f <sub>m</sub>	10			kHz	
Input Impedance	Z <sub>in</sub>	50K			Ohms	
Input Voltage	V <sub>cc</sub> /V <sub>dd</sub>	3.15	3.3	3.45	V	
Input Current	I <sub>cc</sub> /I <sub>dd</sub>	5 50 5		50 120 75	mA mA mA	CMOS/TTL PECL LVDS
Output Type						
Load		2 TTL or 15 pF Max. 50 Ohms to V <sub>cc</sub> -2 Volts 100 Ohm differential load				
Symmetry (Duty Cycle)		(See Ordering Information)				
Output Skew				50	ps	PECL
Differential Voltage		250	375	500	mV	LVDS
Logic "1" Level	V <sub>oh</sub>	2.5 2.2 1.375		2.4	V V V	CMOS/TTL PECL LVDS
Logic "0" Level	V <sub>ol</sub>	1.4		0.5 1.7 1.125	V V V	CMOS/TTL PECL LVDS
Rise/Fall Time	T <sub>r</sub> /T <sub>f</sub>	2.0 0.25		10 3.0	ns ns	CMOS/TTL PECL/LVDS
Tristate Function		Input Logic "1": output active Input Logic "0": output disables				
		Opposite tristate logic Available upon request				
Start up Time		10 ms				
Phase Noise (Typical)						
@ 19.44 MHz	-60	-90	-120	-135	-148	Offset from carrier dBc/Hz
@ 155.52 MHz	-60	-90	-110	-120	-120	dBc/Hz
@ 622.08 MHz	-60	-90	-100	-105	-105	dBc/Hz

1. Stability includes initial tolerance, deviation over temperature, supply and load variation, and aging for 20 years @ 25°C.

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# MtronPTI Lead Free Solder Profile

