DATA SHEET



SAA5264; SAA5265
10 and 1 page intelligent teletext decoders

Preliminary specification
Supersedes data of 1999 Oct 05
File under Integrated Circuits, IC02

2000 Jan 27

Philips
Semiconductors

PHILIPS

FEATURES

The following features apply to both SAA5264 and SAA5265:

- Complete 625 line teletext decoder in one chip reduces printed circuit board area and cost
- Automatic detection of transmitted fastext links or service information (packet 8/30)
- On-Screen Display (OSD) for user interface menus using teletext and dedicated menu icons
- Video Programming System (VPS) decoding
- Wide Screen Signalling (WSS) decoding
- Pan-European, Cyrillic, Greek/Turkish and French/Arabic character sets in each chip
- High-level command interface via I^2C-bus gives easy control with a low software overhead
- High-level command interface is backward compatible to Stand-Alone Fastext And Remote Interface (SAFARI)
- 625 and 525 line display
- RGB interface to standard colour decoder ICs, current source
- Versatile 8-bit open-drain Input/Output (I/O) expander, 5 V tolerant
- Single 12 MHz crystal oscillator
- 3.3 V supply voltage.

SAA5264 features

- Automatic detection of transmitted pages to be selected by page up and page down
- 8 Page fastext decoder
- Table Of Pages (TOP) decoder with Basic Top Table (BTT) and Additional Information Tables (AITs)
- 4 Page user-defined list mode.

GENERAL DESCRIPTION

The SAA5264 is a single-chip ten page 625-line World System Teletext decoder with a high-level command interface, and is SAFARI compatible.

The SAA5265 is a single-chip one page version of the SAA5264.

Both devices are designed to minimize the overall system cost, due to the high-level command interface offering the benefit of a low software overhead in the TV microcontroller.

The SAA5264 has the following functionality:

- 10 page teletext decoder with OSD, Fastext, TOP, default and list acquisition modes
- Automatic channel installation support
- Closed caption acquisition and display
- Violence Chip (VChip) support.

The SAA5265 has the following functionality:

- 1 Page teletext decoder with OSD, fastext and default acquisition modes
- Automatic channel installation support
- Closed caption acquisition and display
- VChip support
- No EEPROM fitted (there is no list mode feature).

ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5264PS/M3/nnnn	SDIP52	plastic shrink dual-in-line package; 52 leads (600 mil)	SOT247-1
SAA5265PS/M4/nnnn	SDIP52	plastic shrink dual-in-line package; 52 leads (600 mil)	SOT247-1

Note

1. ‘nnnn’ is a unique four digit number denoting the software version.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDX}	all supply voltages	referenced to V_{SS}	3.0	3.3	3.6	V
I_{DDP}	periphery supply current	note 1	1	–	–	mA
I_{DDC}	core supply current	normal mode	–	15	18	mA
		idle mode	–	4.6	6	mA
I_{DDA}	analog supply current	normal mode	–	45	48	mA
		idle mode	–	0.87	1	mA
$f_{xtal(nom)}$	nominal crystal frequency	fundamental mode	–	12	–	MHz
T_{amb}	ambient temperature		–20	–	+70	°C
T_{stg}	storage temperature		–55	–	+125	°C

Note

1. Periphery supply current is dependent on external components and I/O voltage levels.

BLOCK DIAGRAM

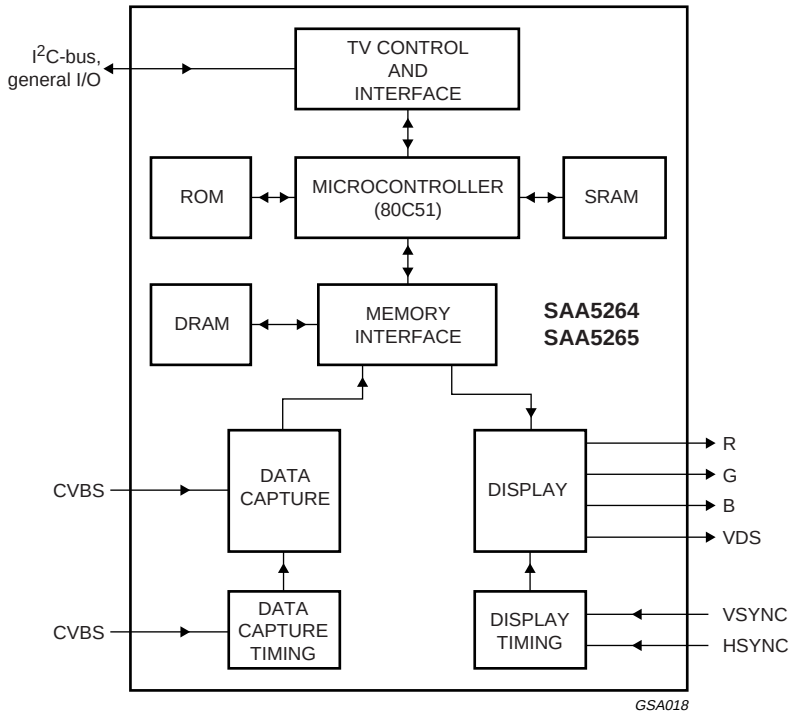


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
Port 2: 8-bit programmable bidirectional port with alternative functions			
P2.0/PWM	1	I/O	output for 14-bit high precision Pulse Width Modulator (PWM)
P2.1/PWM0	2	I/O	outputs for 6-bit PWMs 0 to 6
P2.2/PWM1	3	I/O	
P2.3/PWM2	4	I/O	
P2.4/PWM3	5	I/O	
P2.5/PWM4	6	I/O	
P2.6/PWM5	7	I/O	
P2.7/PWM6	8	I/O	
Port 3: 8-bit programmable bidirectional port with alternative functions			
P3.0/ADC0	9	I/O	inputs for the software Analog-to-Digital-Converter (ADC) facility
P3.1/ADC1	10	I/O	
P3.2/ADC2	11	I/O	
P3.3/ADC3	12	I/O	
P3.4/PWM7	30	I/O	output for 6-bit PWM7
V_{SSC}	13	–	core ground
Port 0: 8-bit programmable bidirectional port			
SCL(NVRAM)	14	I	I^2C-bus Serial Clock input to Non-Volatile RAM
SDA(NVRAM)	15	I/O	I^2C-bus Serial Data input/output (Non-Volatile RAM)
P0.2	16	I/O	input/output for general use
P0.3	17	I/O	input/output for general use
P0.4	18	I/O	input/output for general use
P0.5	19	I/O	8 mA current sinking capability for direct drive of Light Emitting Diodes (LEDs)
P0.6	20	I/O	
P0.7	21	I/O	input/output for general use
V_{SSA}	22	–	analog ground
CVBS0	23	I	Composite Video Baseband Signal (CVBS) input; a positive-going 1 V (peak-to-peak) input is required; connected via a 100 nF capacitor
CVBS1	24	I	
SYNC_FILTER	25	I	sync-pulse-filter input for CVBS; this pin should be connected to V_{SSA} via a 100 nF capacitor
IREF	26	I	reference current input for analog circuits; for correct operation a 24 kΩ resistor should be connected to V_{SSA}
FRAME	27	O	Frame de-interlace output synchronized with the VSYNC pulse to produce a non-interlaced display by adjustment of the vertical deflection circuits
TEST	28	I	not available; connect this pin to V_{SSA}
$\overline{COR}$	29	O	contrast reduction: open-drain, active LOW output which allows selective contrast reduction of the TV picture to enhance a mixed mode display
	30	I/O	P3.4/PWM7 (described above)
V_{DDA}	31	–	analog supply voltage (3.3 V)
B	32	O	Blue colour information pixel rate output

SYMBOL	PIN	TYPE	DESCRIPTION
G	33	O	Green colour information pixel rate output
R	34	O	Red colour information pixel rate output
VDS	35	O	video/data switch push-pull output for pixel rate fast blanking
HSYNC	36	I	horizontal sync pulse input: Schmitt triggered for a Transistor Transistor Level (TTL) version; the polarity of this pulse is programmable by register bit TXT1.H POLARITY
VSYNC	37	I	vertical sync pulse input; Schmitt triggered for a TTL version; the polarity of this pulse is programmable by register bit TXT1.V POLARITY
V_{SSP}	38	–	periphery ground
V_{DDC}	39	–	core supply voltage (+3.3 V)
OSCGND	40	–	crystal oscillator ground
XTALIN	41	I	12 MHz crystal oscillator input
XTALOUT	42	O	12 MHz crystal oscillator output
RESET	43	I	reset input; if this pin is HIGH for at least 2 machine cycles (24 oscillator periods) while the oscillator is running, the device resets; this pin should be connected to V_{DDP} via a capacitor
V_{DDP}	44	–	periphery supply voltage (+3.3 V)
Port 1: 8-bit programmable bidirectional port			
P1.0	45	I/O	input/output for general use
P1.1	46	I/O	input/output for general use
P1.2	47	I/O	input/output for general use
P1.3	48	I/O	input/output for general use
SCL	49	I	I^2C-bus Serial Clock input from application
SDA	50	I/O	I^2C-bus Serial Data input/output (application)
P1.4	51	I/O	input/output for general use
P1.5	52	I/O	input/output for general use

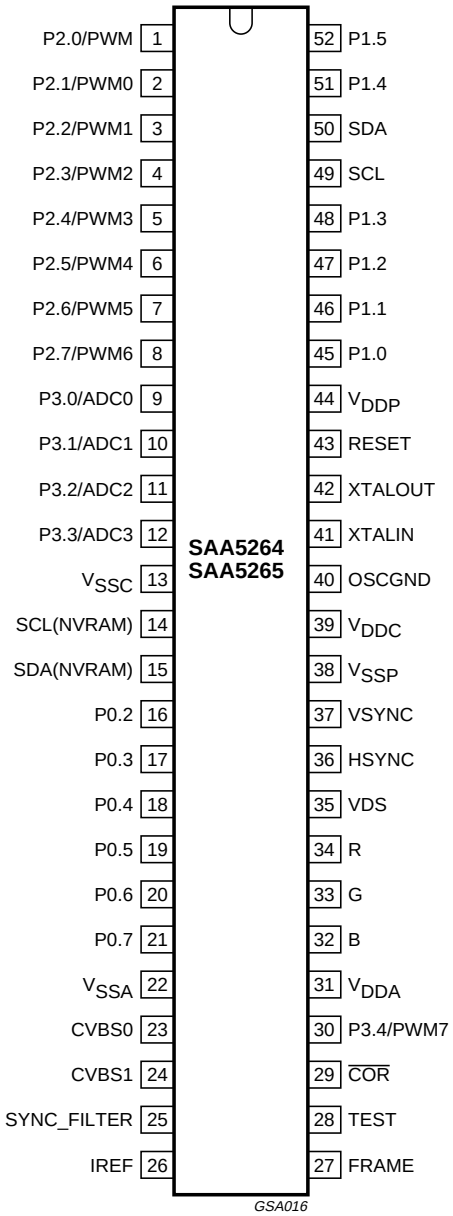


Fig.2 Pin configuration.

HIGH LEVEL COMMAND INTERFACE

The I²C-bus interface is used to pass control commands and data between the SAA5264/SAA5265 and the television microcontroller. The interface uses high-level commands, which are backward compatible with the SAFARI.

The I²C-bus transmission formats are:

Table 1 User command

START	I²C-BUS ADDRESS	WRITE	ACK	COMMAND	ACK	STOP

Table 2 System command

START	I²C-BUS ADDRESS	WRITE	ACK	COMMAND	ACK	PARAMETER	ACK	STOP

Table 3 User read

START	I²C-BUS ADDRESS	READ	ACK	DATA	ACK	STOP

CHARACTER SETS

The following standard character sets are included in the SAA5264 and in the SAA5265:

Set 0 = Pan-European

Set 1 = Cyrillic

Set 2 = Greek/Turkish

Set 3 = French/Arabic

If you require any other character sets, please discuss them with your local Regional Sales Office first.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDX}	all supply voltages		–0.5	+4.0	V
V_I	input voltage (any input)	note 1	–0.5	V_{DD} + 0.5 or +4.1	V
V_O	output voltage (any output)	note 1	–0.5	V_{DD} + 0.5	V
I_O	output current (each output)		–	10	mA
$I_{IO(d)}$	diode DC input or output current		–	20	mA
T_{amb}	ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. This maximum value refers to 5 V tolerant I/Os and may be 6 V maximum but only when V_{DD} is present.

CHARACTERISTICS

V_{DD} = 3.3 V ±10%; V_{SS} = 0 V; T_{amb} = −20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDX}	all supply voltages	referenced to V_{SS}	3.0	3.3	3.6	V
I_{DDP}	periphery supply current	note 1	1	–	–	mA
I_{DDC}	core supply current	normal mode	–	15	18	mA
$I_{DDC(idle)}$	idle mode core supply current		–	4.6	6	mA
I_{DDA}	analog supply current		–	45	48	mA
$I_{DDA(idle)}$	idle mode analog supply current	normal mode	–	0.87	1	mA
Digital inputs						
RESET (PIN 43)						
V_{IL}	LOW-level input voltage		–	–	1.00	V
V_{IH}	HIGH-level input voltage		1.85	–	–	V
V_{hys}	Schmitt trigger input hysteresis voltage		0.44	–	0.58	V
I_{LI}	input leakage current	V_I = 0	–	–	0.17	µA
$R_{pd(eq)}$	equivalent pull-down resistance	$V_I = V_{DD}$	55.73	70.71	92.45	kΩ
HSYNC, VSYNC (PINS 36 AND 37)						
V_{IL}	LOW-level input voltage		–	–	0.96	V
V_{IH}	HIGH-level input voltage		1.80	–	–	V
V_{hys}	Schmitt trigger input hysteresis voltage		0.40	–	0.56	V
I_{LI}	Input leakage current	V_I = 0 to V_{DD}	–	–	0.00	µA
Digital outputs						
FRAME, VDS (PINS 27 AND 35)						
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.13	V
V_{OH}	HIGH-level output voltage	I_{OH} = 3 mA	2.84	–	–	V
$t_{o(r)}$	output rise time	between 10% and 90%; C_L = 70 pF	7.50	8.85	10.90	ns
$t_{o(f)}$	output fall time	between 10% and 90%; C_L = 70 pF	6.70	7.97	10.00	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{COR}$ (OPEN-DRAIN OUTPUT, PIN 29)						
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.14	V
$V_{OH(pu)}$	HIGH-level pull-up output voltage	I_{OL} = –3 mA; push-pull	2.84	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.00	V
V_{IH}	HIGH-level input voltage		0.00	–	5.50	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.12	µA
$t_{o(r)}$	output rise time	between 10% and 90%; C_L = 70 pF	7.20	8.64	11.10	ns
$t_{o(f)}$	output fall time	between 10% and 90%; C_L = 70 pF	4.90	7.34	9.40	ns
Digital input/outputs						
SCL(NVRAM), SDA(NVRAM), P0.4, P0.7, P1.0, P1.1, P2.1 TO P2.7, P3.0 TO P3.4 (PINS 14, 15, 18, 21, 45, 46, 2 TO 12, 30)						
V_{IL}	LOW-level input voltage		–	–	0.98	V
V_{IH}	HIGH-level input voltage		1.78	–	–	V
V_{hys}	Schmitt trigger input hysteresis voltage		0.41	–	0.55	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.01	µA
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.18	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA push-pull	2.81	–	–	V
$t_{o(r)}$	output rise time	between 10% and 90%; C_L = 70 pF push-pull	6.50	8.47	10.70	ns
$t_{o(f)}$	output fall time	between 10% and 90%; C_L = 70 pF	5.70	7.56	10.00	ns
P1.2, P1.3, P2.0 (PINS 47, 48, 1)						
V_{IL}	LOW-level input voltage		–	–	0.99	V
V_{IH}	HIGH-level input voltage		1.80	–	–	V
V_{hys}	Schmitt trigger input hysteresis voltage		0.42	–	0.56	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.02	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	0.17	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA push-pull	2.81	–	–	V
$t_{o(r)}$	output rise time	between 10% and 90%; C_L = 70 pF push-pull	7.00	8.47	10.50	ns
$t_{o(f)}$	output fall time	between 10% and 90%; C_L = 70 pF	5.40	7.36	9.30	ns
P0.5, P0.6 (PINS 19, 20)						
V_{IL}	LOW-level input voltage		–	–	0.98	V
V_{IH}	HIGH-level input voltage		1.82	–	–	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.11	µA
V_{hys}	Schmitt trigger input hysteresis voltage		0.42	–	0.58	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA	–	–	0.20	V
V_{OH}	HIGH-level output voltage	I_{OH} = –8 mA push-pull	2.76	–	–	V
$t_{o(r)}$	output rise time	between 10% and 90%; C_L = 70 pF push-pull	7.40	8.22	8.80	ns
$t_{o(f)}$	output fall time	between 10% and 90%; C_L = 70 pF	4.20	4.57	5.20	ns
P1.4, P1.5 (OPEN-DRAIN) (PINS 51, 52)						
V_{IL}	LOW-level input voltage		–	–	1.08	V
V_{IH}	HIGH-level input voltage		1.99	–	–	V
V_{hys}	Schmitt trigger input hysteresis voltage		0.49	–	0.60	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–	–	0.13	µA
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA	–	–	0.35	V
$t_{o(f)}$	output fall time	between 10% and 90%; C_L = 70 pF	69.70	83.67	103.30	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs						
CVBS0 AND CVBS1(PINS 23 AND 24)						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{i(v)(p-p)}$	video input voltage (peak-to-peak value)		0.7	1.0	1.4	V
Z_{source}	source impedance		0	–	250	Ω
V_{IH}	HIGH-level input voltage		3.0	–	V_{DDA} +0.3	V
C_i	input capacitance		–	–	10	pF
IREF (PIN 26)						
R_{IREF}	resistance from IREF to V_{SSA}	resistor tolerance = 2%	–	24	–	kΩ
ADC0 TO ADC3 (PINS 9 TO 12)						
V_{IH}	HIGH-level input voltage		–	–	V_{DDA}	V
C_i	input capacitance		–	–	10	pF
Analog outputs						
B, G AND R (PINS 32 TO 34)						
$I_{o(bl)}$	output current (black level)	V_{DDA} = 3.3 V	–10	–	+10	μA
$I_{o(max)}$	output current (maximum intensity)	V_{DDA} = 3.3 V intensity level code = 15 (Dec)	6.0	6.67	7.3	mA
$I_{o(70\%max)}$	output current (70% of maximum intensity)	V_{DDA} = 3.3 V intensity level code = 0 (Dec)	4.2	4.7	5.1	mA
R_L	load resistance (to V_{SSA})	resistor tolerance = 5%	–	150	–	Ω
C_L	load capacitance		–	–	15	pF
Analog input/output						
SYNC_FILTER (PIN 25)						
C_{stg}	storage capacitor (to V_{SSA})		–	100	–	nF
$V_{sync(nom)}$	sync filter level voltage with nominal sync amplitude		0.35	0.55	0.75	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
XTALIN (PIN 41)						
V_{IL}	LOW-level input voltage		V_{SSA}	–	–	V
V_{IH}	HIGH-level input voltage		–	–	V_{DDA}	V
C_i	input capacitance		–	–	10	pF
XTALOUT (PIN 42)						
C_o	output capacitance		–	–	10	pF
Crystal specification; notes 2 and 3						
$f_{xtal(nom)}$	nominal frequency	fundamental mode	–	12	–	MHz
C_L	load capacitance		–	–	30	pF
C_{mot}	motional capacitance	T_{amb} = 25 °C	–	–	20	fF
R_{xtal}	crystal resonance resistance	T_{amb} = 25 °C	–	–	60	Ω
C_{osc}	capacitance at XTALIN, XTALOUT	T_{amb} = 25 °C	–	$2C_L - C_{chip} - C_{stray}$	–	pF
$C_{xtal(hold)}$	crystal holder capacitance	T_{amb} = 25 °C	–	–	$35 - \frac{C_{osc}}{2} - \frac{C_{chip}}{2} - \frac{C_{stray}}{2}$	pF
T_{xtal}	crystal temperature range		–20	+25	+85	°C
X_j	adjustment tolerance	T_{amb} = 25 °C	–	–	$\pm 50 \times 10^{-6}$	
X_d	drift		–	–	$\pm 100 \times 10^{-6}$	

Notes

1. Periphery supply current is dependent on I/O external components and voltage levels.
2. Crystal order number 4322 143 05561. If crystal 4322 143 05561 is not used, then the formulae in the crystal specification should be used.
3. C_{osc} may need to be reduced from the initially selected value. C_{chip} = 7 pF, the mean of the capacitances due to the chip at XTALIN and at XTALOUT. C_{stray} is a value for the mean of the stray capacitances due to the external circuit at XTALIN and XTALOUT. The maximum value for $C_{xtal(hold)}$ is to ensure start-up.

I²C-BUS CHARACTERISTICS

SYMBOL	PARAMETER	FAST-MODE I²C-bus		UNIT
		MIN.	MAX.	
f_{SCL}	SCL clock frequency	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition	1.3	–	µs
$t_{HD;STA}$	hold time START condition; after this period, the first clock pulse is generated	0.6	–	µs
t_{LOW}	SCL LOW time	1.3	–	µs
t_{HIGH}	SCL HIGH time	0.6	–	µs
$t_{SU;STA}$	set-up time repeated START	0.6	–	µs
$t_{HD;DAT}$	data hold time; notes 1 and 2	0	0.9	µs
$t_{SU;DAT}$	data set-up time; note 3	100	–	ns
t_r	rise time SDA and SCL; note 4	20	300	ns
t_f	fall time SDA and SCL; note 4	20	300	ns
$t_{SU;STO}$	set-up time STOP condition	0.6	–	µs
C_b	capacitive load of each bus line	–	400	pF

Notes

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referenced to the V_{IHmin} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
2. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period of the SCL signal ($t_{LOW(SCL)}$).
3. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch $t_{LOW(SCL)}$. If such a device does stretch $t_{LOW(SCL)}$, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the SCL line is released.
4. C_b = total capacitance of one bus line in pF.

EMC GUIDELINES

Optimization of circuit return paths and minimization of common mode emission will be assisted by using a double sided Printed Circuit Board (PCB) with low inductance ground plane.

On a single-sided PCB a local ground plane under the whole IC should be present as shown in Fig.3. This should have the widest possible connection between the PCB ground and bulk electrolytic decoupling capacitor. Preferably, the PCB local ground plane connection should not be connected to other grounds on route to the PCB ground. Do not use wire links. Wire links cause ground inductance which increases ground bounce.

The supply pins can be decoupled at the ground pin plane below the IC. This is easily achieved by using surface mount capacitors, which, at high frequency, are more effective than components with leads.

Using a device socket would increase the area and therefore increase the inductance of the external bypass loop.

To provide a high-impedance to any high frequency signals on the V_{DD} supplies to the IC, a ferrite bead or inductor can be connected in series with the supply line close to the decoupling capacitor. To prevent signal radiation, pull-up resistors of signal outputs should not be connected to the V_{DD} supply on the IC side of the ferrite bead or inductor.

OSCGND should only be connected to the crystal load capacitors and not to any other ground connection.

Distances to physical connections of associated active devices should be as short as possible.

PCB output tracks should have close proximity, mutually coupled, ground return paths.

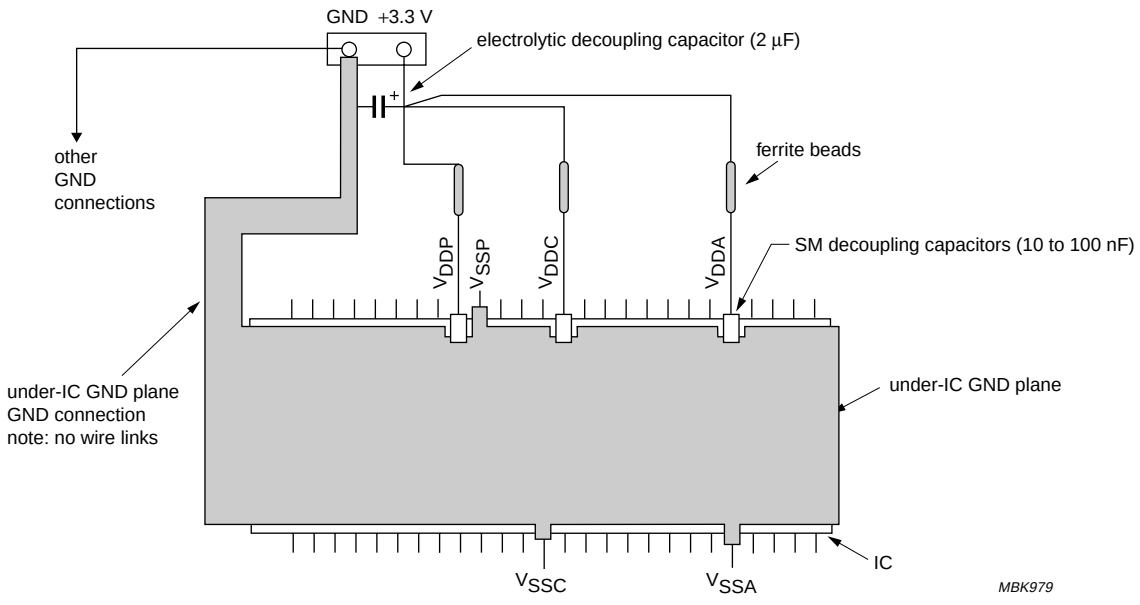


Fig.3 Power supply connections for EMC.

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors general quality specification for business group *"Consumer Integrated Circuits SNW-FQ-611-Part E"*. The principal requirements are shown in Tables 4 to 7.

Group A

Table 4 Acceptance tests per lot; note 1

TEST	REQUIREMENTS
Mechanical	cumulative target: <80 ppm
Electrical	cumulative target: <100 ppm

Note

1. ppm = fraction of defective devices, in parts per million.

Group B

Table 5 Processability tests (by package family)

TEST	REQUIREMENTS
Solderability	0/16 on all lots
Mechanical	0/15 on all lots
Solder heat resistance	0/15 on all lots

Group C

Table 6 Reliability tests (by package family); note 1

TEST	CONDITIONS	REQUIREMENTS
Operational life	168 hours at T_j = 150 °C	<1000 FPM at T_j = 150 °C
Humidity life	temperature, humidity, bias 1000 hours; T_{amb} = 85 °C, 85% RH (or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Note

1. FPM = fraction of devices failing at test condition, in Failures Per Million.

Table 7 Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS
ESD and latch-up	ESD Human body model 100 pF, 1.5 kΩ	2000 V
	ESD Machine model 200 pF, 0 Ω	200 V
	latch-up	100 mA, 1.5 × V_{DD} (absolute maximum)

APPLICATION INFORMATION

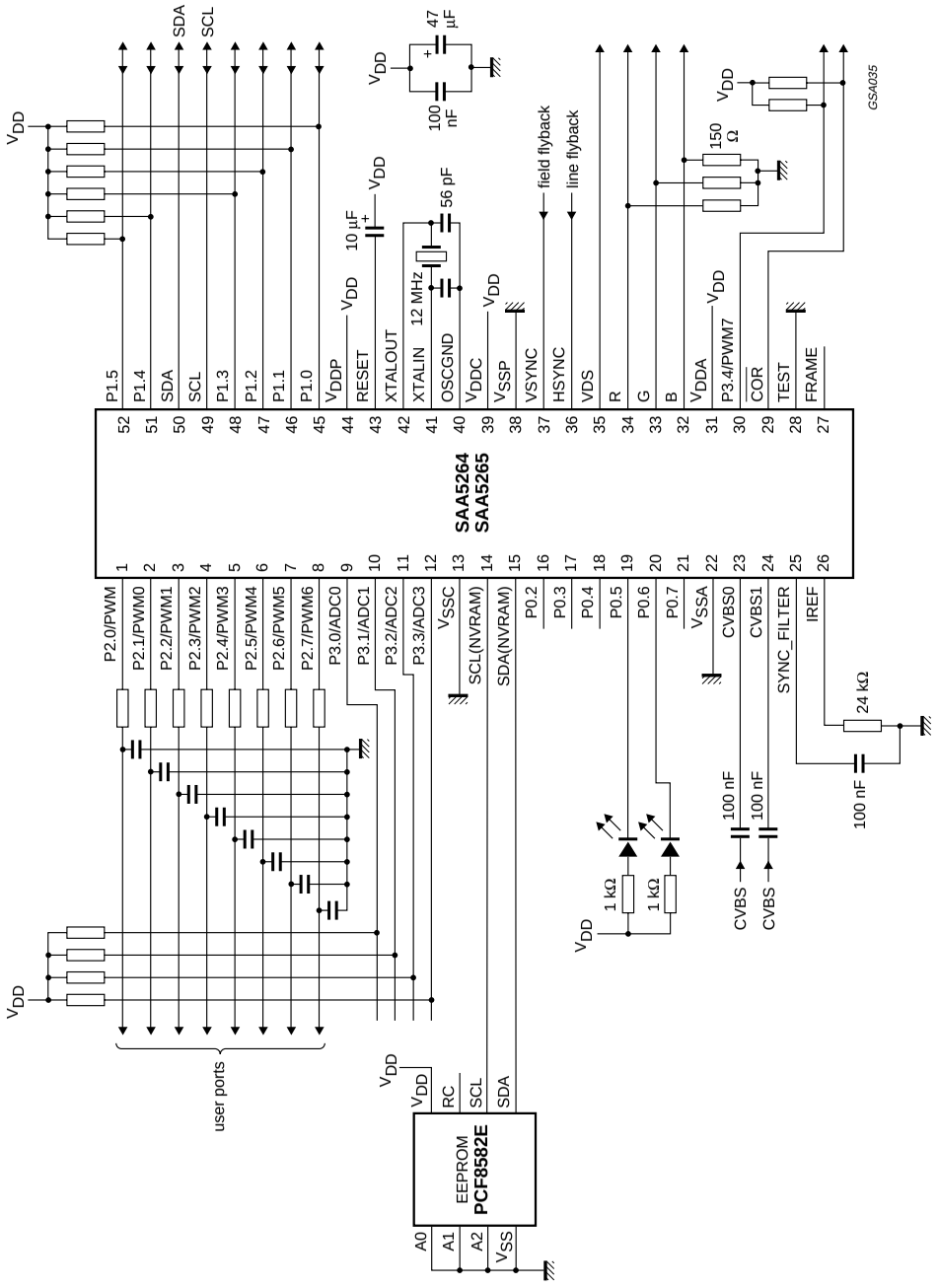
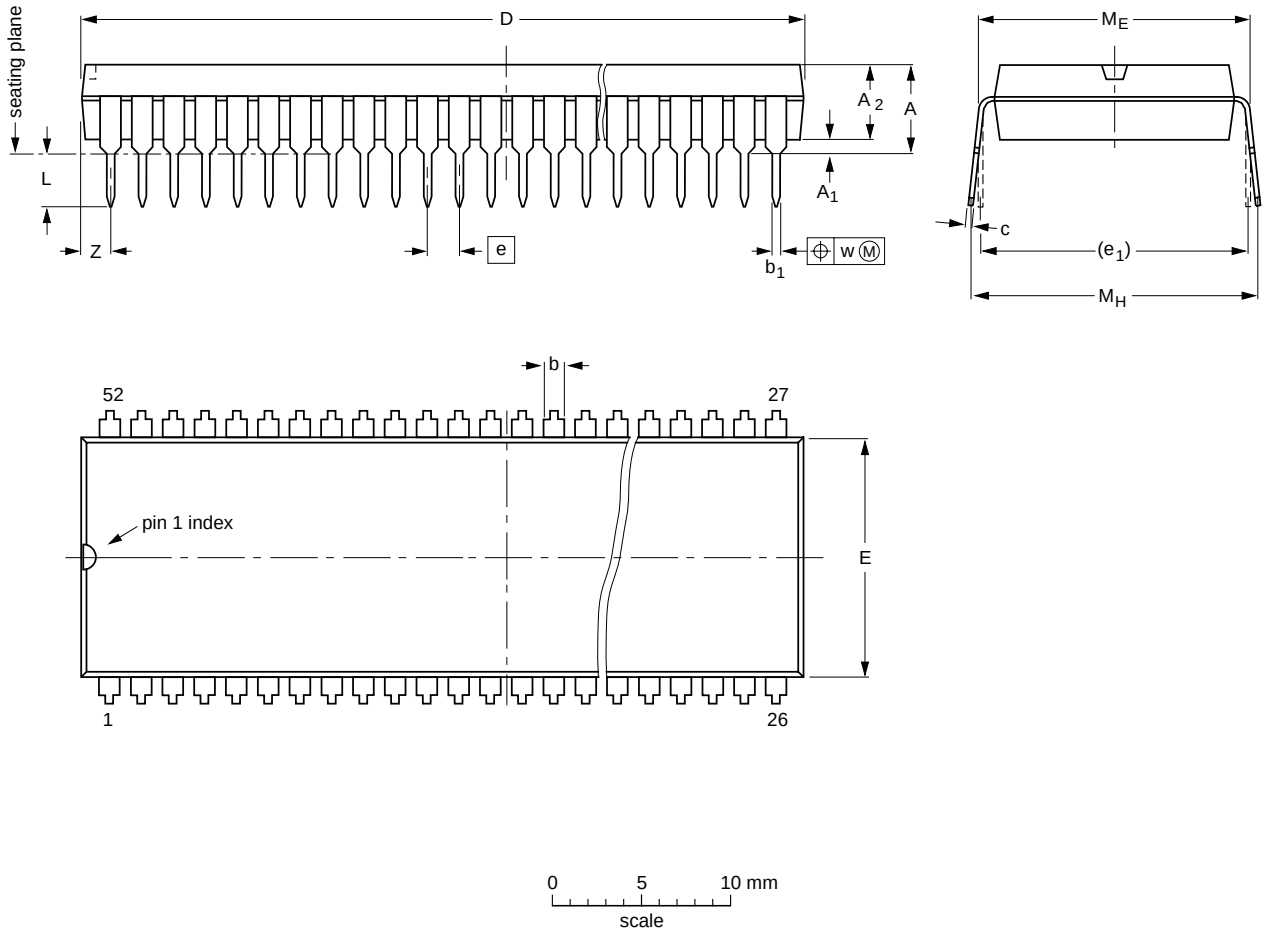


Fig.4 Application diagram.

Bi-directional ports have been configured as open-drain. Output ports have been configured as push-pull.

PACKAGE OUTLINE

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1		MS-020				~~95-03-11~~ 99-12-27

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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