



**SOT-89K Plastic-Encapsulate Thyristors**

**CT401J** 4Q TRIACs

**MAIN CHARACTERISTICS**

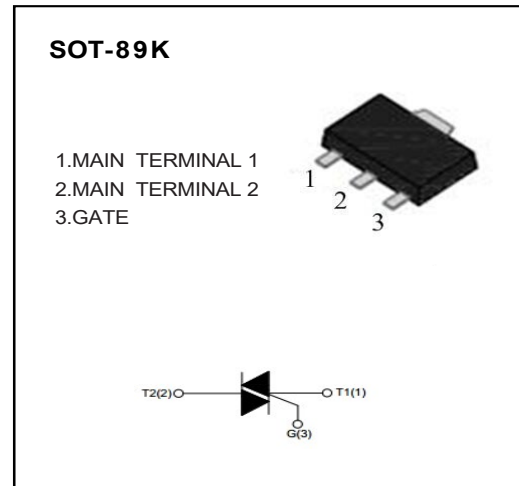
$I_{T(RMS)}$		<b>1A</b>
$V_{DRM}/V_{RRM}$	CT401J-600T/S	<b>600V</b>
	CT401J-800T/S	<b>800V</b>
$V_{TM}$		<b>1.55V</b>

**FEATURES**

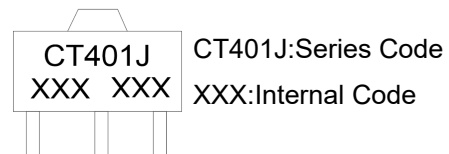
- NPNPN 5-layer Structure TRIACs
- Mesa Glass Passivated Technology
- Multi Layers Metal Electrodes
- High Junction Temperature
- Good Commutation Performance

**APPLICATIONS**

- Heater Control
- Motor Speed Controller
- Mixer



**MARKING**



**ABSOLUTE RATINGS (  $T_a=25^{\circ}C$  unless otherwise noted )**

Symbol	Parameter	Test condition	Value	Unit	
$V_{DRM}/V_{RRM}$	Repetitive peak off-state voltage	$T_j=25^{\circ}C$	CT401J-600T/S	600	V
			CT401J-800T/S	800	V
$I_{T(RMS)}$	RMS on-state current	SOT- 89K( $T_c \leq 70^{\circ}C$ ), Fig. 1,2	1	A	
$I_{TSM}$	Non repetitive surge peak on-state current	Full sine wave , $T_j(\text{init})=25^{\circ}C$ , $t_p=20\text{ms}$ ; Fig. 3,5	10	A	
$I^2t$	$I^2t$ value	$t_p=10\text{ms}$	1.28	A <sup>2</sup> s	
$di_T/dt$	Critical rate of rise of on-state current	$I_G=2 \cdot I_{GT}$ , $t_r \leq 10\text{ns}$ , $F=120\text{Hz}$ , $T_j=125^{\circ}C$	I - II -III	50	A/ $\mu$ s
			IV	10	
$I_{GM}$	Peak gate current	$t_p=20\mu\text{s}$ , $T_j=125^{\circ}C$	2	A	
$P_{G(AV)}$	Average gate power	$T_j=125^{\circ}C$	0.5	W	
$T_{STG}$	Storage temperature		-40~+150	$^{\circ}C$	
$T_j$	Operating junction temperature		-40~+125		

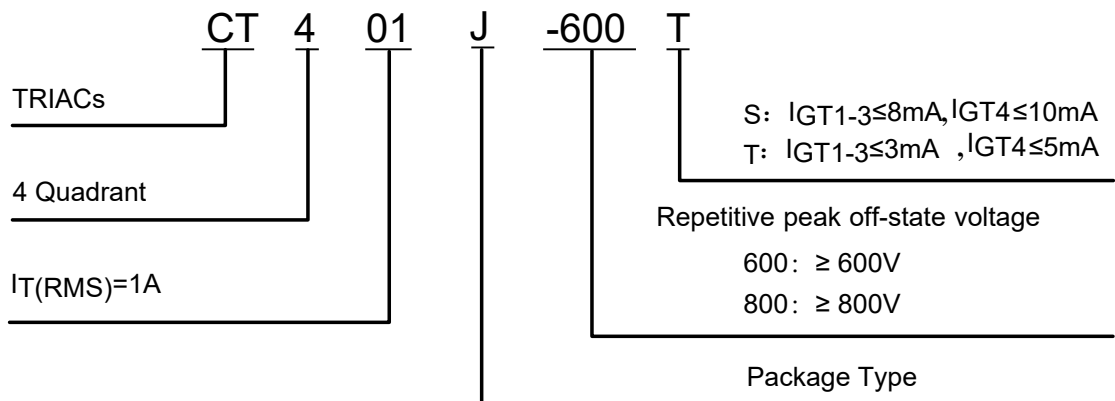
## ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test condition	Value		Unit	
			T	S		
I <sub>GT</sub>	Gate trigger current	V <sub>D</sub> =12V, I <sub>T</sub> =0.1A,	I - II - III	≤3	≤8	mA
			IV	≤5	≤10	
V <sub>GT</sub>	Gate trigger voltage	T <sub>j</sub> =25°C, Fig. 6	I - II - III - IV	≤1.3		V
V <sub>GD</sub>	Non-triggering gate voltage	V <sub>D</sub> =V <sub>DRM</sub> , T <sub>j</sub> =125°C		≥0.2		V
I <sub>H</sub>	Holding current	V <sub>D</sub> =12V, I <sub>GT</sub> =0.1A, T <sub>j</sub> =25°C, Fig. 6	I - II - III - IV	≤5	≤5	mA
I <sub>L</sub>	Latching current		I - III - IV	≤6	≤10	mA
			II	≤10	≤15	mA
dV <sub>D</sub> /dt	Critical rate of rise of off-state	V <sub>D</sub> =67%V <sub>DRM</sub> , Gate Open T <sub>j</sub> =125°C		≥20	≥50	V/μs
V <sub>TM</sub>	On-state Voltage	I <sub>TM</sub> =1.5A, t <sub>p</sub> =380μs, Fig. 4		≤1.55		V
I <sub>DRM</sub> / I <sub>RRM</sub>	Repetitive peak off-state current	V <sub>D</sub> =V <sub>DRM</sub> /V <sub>RRM</sub> , T <sub>j</sub> =25°C		≤5	≤5	μA
		V <sub>D</sub> =V <sub>DRM</sub> /V <sub>RRM</sub> , T <sub>j</sub> =125°C		≤0.1	≤0.1	mA

## THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R <sub>th</sub> (j-c)	Junction to case (AC)		SOT-89K	23 °C/W
R <sub>th</sub> (j-a)	Junction to ambient	S=5cm <sup>2</sup>	SOT-89K	100 °C/W

## PART NUMBER



# CHARACTERISTICS CURVES

FIG.1: Maximum power dissipation versus RMS on-state current (full cycle)

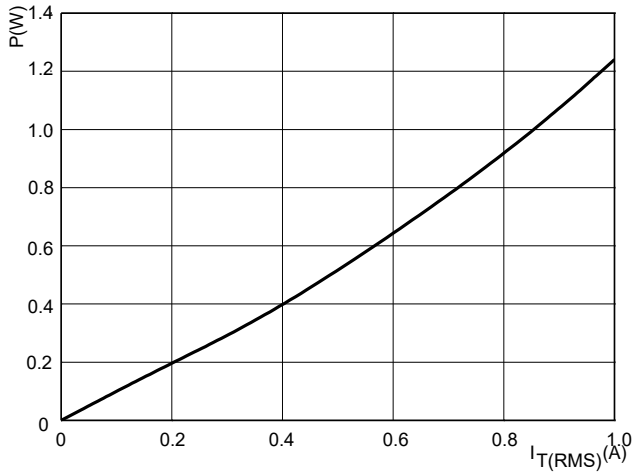


FIG.2: RMS on-state current versus case temperature (full cycle)

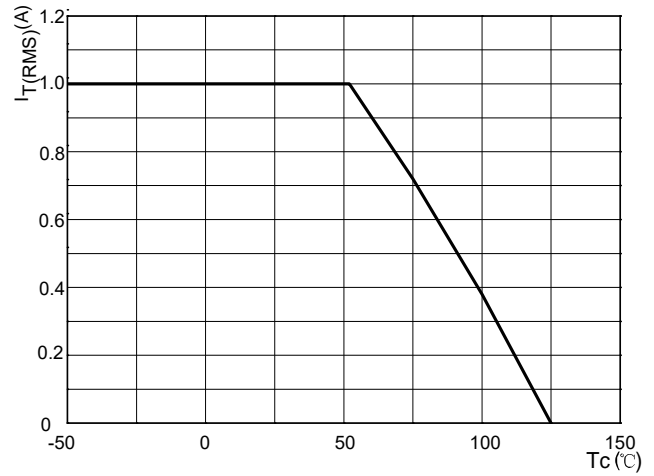


FIG.3: Surge peak on-state current versus number of cycles

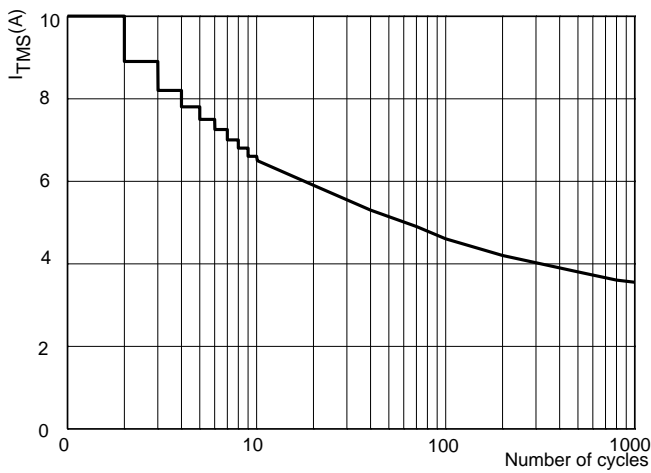


FIG.4: On-state characteristics (maximum values)

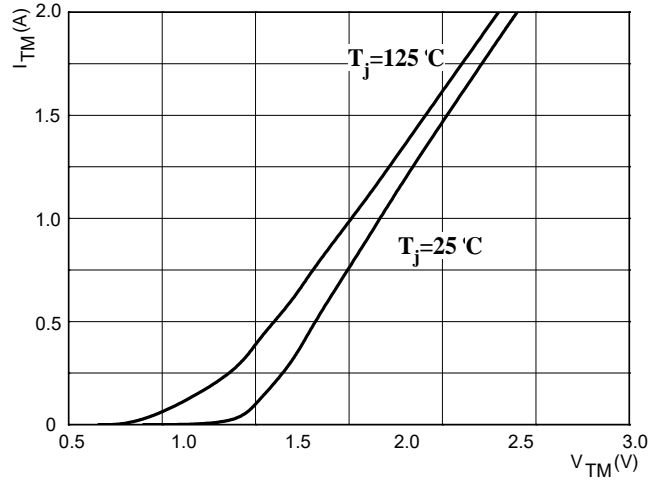


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10\text{ms}$

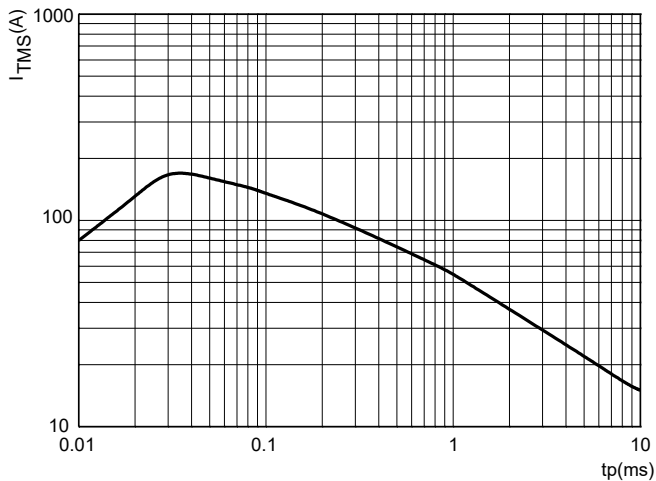
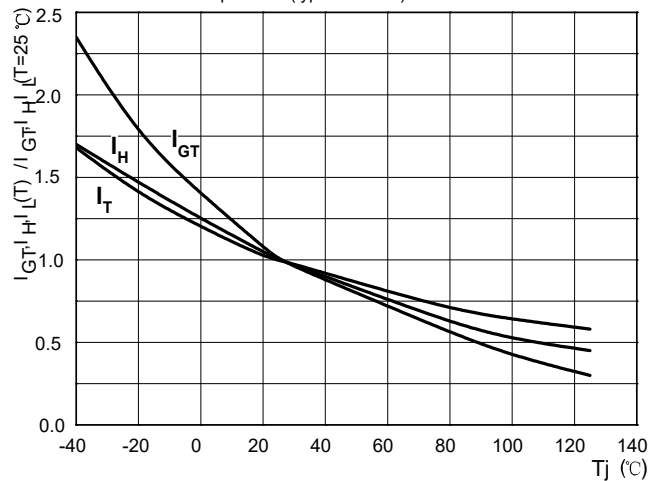
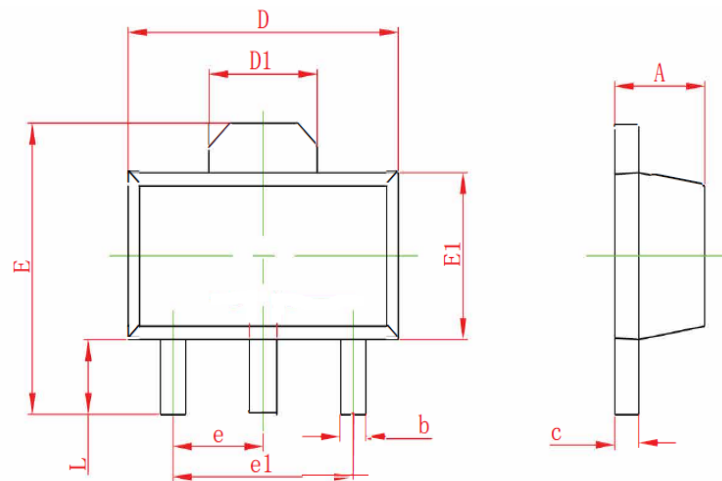


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature (typical values)



## SOT-89K PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
c	0.350	0.460	0.014	0.017
D	4.300	4.700	0.169	0.185
D1	1.550 REF.		0.061 REF.	
E	3.940	4.250	0.155	0.167
E1	2.300	2.700	0.091	0.106
e	1.500 TYP.		0.060 TYP.	
e 1	3.000 TYP.		0.118 TYP.	
L	0.800	1.200	0.031	0.047