TPS3890
延迟可编程的低静态电流、1% 精密监控器

1 特性

- 上电复位 (POR) 发生器，可调节延迟时间：40μs 至 30s
- 超低静态电流：2.1μA（典型值）
- 高阈值精度：1%（最大值）
- 高精度迟滞
- 固定和可调节阈值电压：
  - 固定阈值适用于标准电压轨：1.2V 到 3.3V
  - 可调节阈值电压低至 1.15V
- 手动复位 ($\overline{\text{MR}}$) 输入
- 开漏 $\overline{\text{RESET}}$ 输出
- 温度范围：-40°C 至 +125°C
- 封装：1.5mm × 1.5mm 晶圆级小外形无引线 (WSON) 封装

2 应用

- 数字信号处理器 (DSP) 或微控制器
- 现场可编程门阵列 (FPGA)、专用集成电路 (ASIC)
- 笔记本电脑、台式计算机
- 智能手机，手持产品
- 便携式电池供电产品
- 固态硬盘
- 机顶盒
- 工业控制系统

3 说明

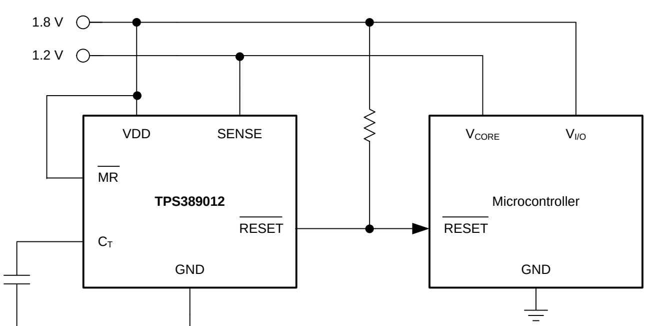
TPS3890 是一款静态电流较低的精密电压监控器，可监视低至 1.15V 的系统电压，开漏 $\overline{\text{RESET}}$ 信号在 SENSE 电压降至低于预设阈值或手动复位 ($\overline{\text{MR}}$) 引脚降为逻辑低电平时置为有效。$\overline{\text{RESET}}$ 输出在用户可调节延迟时间内保持低电平，条件是 SENSE 电压和手动复位 ($\overline{\text{MR}}$) 返回至超出相应阈值。TPS3890 系列使用精密电压实现 1% 的阈值精度。通过将 CT 引脚与外部电容相连，可在 40μs 到 30s 范围内调节复位延迟时间。TPS3890 具有 2.1μA 的超低静态电流，采用 1.5mm × 1.5mm 小型封装，使得器件非常适用于电池供电和空间受限 应用。该器件的额定工作温度范围为 -40℃ 至 +125℃ (T_J)。

器件信息[(1)]

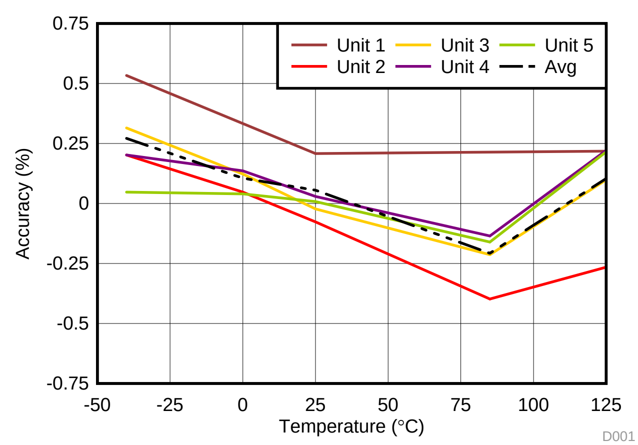
器件型号	封装	封装尺寸（标称值）
TPS3890	WSON (6)	1.50mm x 1.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路



V_{ITN} 精度与温度间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

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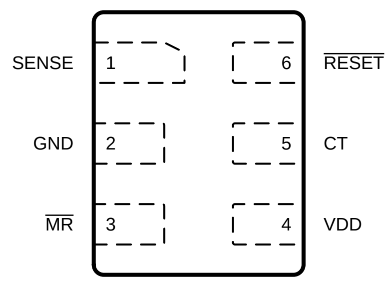
5 Device Comparison Table

PART NUMBER	NOMINAL SUPPLY VOLTAGE	NEGATIVE THRESHOLD (V_{ITN})	POSITIVE THRESHOLD (V_{ITP})
TPS389001	Adjustable	1.15 V	1.157 V
TPS389012	1.2 V	1.15 V	1.157 V
TPS389015	1.5 V	1.44 V	1.449 V
TPS389018	1.8 V	1.73 V	1.740 V
TPS389020	2.0 V	1.90 V	1.911 V
TPS389025	2.5 V	2.40 V	2.414 V
TPS389030	3.0 V	2.89 V	2.907 V
TPS389033	3.3 V	3.17 V	3.189 V

6 Pin Configuration and Functions

DSE Package
6-Pin WSON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
5	CT	—	The CT pin offers a user-adjustable delay time. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$ delay time to deassert. $t_{PD(r)}$ (sec) = C_{CT} (µF) × 1.07 + 25 µs (nom).
2	GND	—	Ground
3	$\overline{\text{MR}}$	I	Driving the manual reset pin ($\overline{\text{MR}}$) low causes $\overline{\text{RESET}}$ to go low (assert).
6	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ is an open-drain output that is driven to a low-impedance state when either the $\overline{\text{MR}}$ pin is driven to a logic low or the monitored voltage on the SENSE pin is lower than the negative threshold voltage (V_{ITN}). $\overline{\text{RESET}}$ remains low (asserted) for the delay time period after both $\overline{\text{MR}}$ is set to a logic high and the SENSE input is above V_{ITP}. A pullup resistor from 10 kΩ to 1 MΩ can be used on this pin.
1	SENSE	I	This pin is connected to the voltage to be monitored. When the voltage on SENSE falls below the negative threshold voltage V_{ITN}, $\overline{\text{RESET}}$ goes low (asserts). When the voltage on SENSE rises above the positive threshold voltage V_{ITP}, $\overline{\text{RESET}}$ goes high (deasserts).
4	VDD	I	Supply voltage pin. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	VDD	–0.3	7	V
	SENSE	–0.3	7	
	$\overline{\text{RESET}}$	–0.3	7	
	$\overline{\text{MR}}$	–0.3	7	
	V_{CT}	–0.3	7	
Current	$\overline{\text{RESET}}$	–20	20	mA
Temperature	Operating junction temperature, T_J	–40	125	°C
	Storage temperature, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Power-supply voltage	1.5		5.5	V
V_{SENSE}	SENSE voltage	0		5.5	V
V_{RESET}	$\overline{\text{RESET}}$ pin voltage	0		5.5	V
I_{RESET}	$\overline{\text{RESET}}$ pin current	–5		5	mA
C_{IN}	Input capacitor, VDD pin	0	0.1		µF
C_{CT}	Reset timeout capacitor, CT pin	0		22	µF
R_{PU}	Pullup resistor, $\overline{\text{RESET}}$ pin	1		1000	kΩ
T_J	Junction temperature (free-air temperature)	–40	25	125	℃

7.4 Thermal Information

THERMAL METRIC[1]		TPS3890	UNIT
		DSE (WSON)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	321.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	207.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	281.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	42.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	284.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	142.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR}$ = V_{DD} (unless otherwise noted); typical values are at V_{DD} = 5.5 V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply voltage		1.5		5.5	V
V_{POR}	Power-on reset voltage	$V_{OL(max)}$ = 0.2 V, I_{RESET} = 15 µA			0.8	V
I_{DD}	Supply current (into VDD pin)	V_{DD} = 3.3 V, I_{RESET} = 0 mA, –40°C < T_J < 85°C		2.09	3.72	µA
		V_{DD} = 3.3 V, I_{RESET} = 0 mA, –40°C < T_J < 105°C			4.5	
		V_{DD}= 3.3 V, I_{RESET} = 0 mA			5.8	
		V_{DD} = 5.5 V, I_{RESET} = 0 mA, –40°C < T_J < 85°C		2.29	4	
		V_{DD} = 5.5 V, I_{RESET} = 0 mA, –40°C < T_J < 105°C			5.2	
		V_{DD} = 5.5 V, I_{RESET} = 0 mA			6.5	
V_{ITN}, V_{ITP}	SENSE input threshold voltage accuracy		–1%	±0.5%	1%	
V_{HYST}	Hysteresis (1)		0.325%	0.575%	0.825%	
I_{SENSE}	Input current	V_{SENSE} = 5 V			8	µA
		V_{SENSE} = 5 V, TPS389001, TPS389012		10	100	nA
I_{CT}	CT pin charge current		0.90	1.15	1.35	µA
V_{CT}	CT pin comparator threshold voltage		1.17	1.23	1.29	V
R_{CT}	CT pin pulldown resistance	When $\overline{RESET}$ is deasserted		200		Ω
V_{IL}	Low-level input voltage ($\overline{MR}$ pin)				0.25 × V_{DD}	V
V_{IH}	High-level output voltage		0.7 x V_{DD}			V
V_{OL}	Low-level output voltage	V_{DD} ≥ 1.5 V, I_{RESET} = 0.4 mA			0.25	V
		V_{DD} ≥ 2.7 V, I_{RESET} = 2 mA			0.25	
		V_{DD} ≥ 4.5 V, I_{RESET} = 3 mA			0.3	
$I_{LKG(OD)}$	Open-drain output leakage	High impedance, V_{SENSE} = V_{RESET} = 5.5 V			250	nA

(1) $V_{HYST} = [(V_{ITP} – V_{ITN}) / V_{ITN}] \times 100\%$.

7.6 Timing Requirements

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, $\overline{MR}$ = V_{DD}, and 5% input overdrive(1) (unless otherwise noted); typical values are at V_{DD} = 5.5 V and T_J = 25°C

			MIN	NOM	MAX	UNIT
$t_{PD(f)}$	SENSE (falling) to $\overline{RESET}$ propagation delay	C_T = open, V_{DD} = 3.3 V		18		µs
		C_T = open, V_{DD} = 5.5 V		8		
$t_{PD(r)}$	SENSE (rising) to $\overline{RESET}$ propagation delay	C_T = open, V_{DD} = 3.3 V		25		µs
$t_{GI(SENSE)}$	SENSE pin glitch immunity	V_{DD} = 5.5 V		9		µs
$t_{GI(MR)}$	$\overline{MR}$ pin glitch immunity	V_{DD} = 5.5 V		100		ns
t_{MRW}	$\overline{MR}$ pin pulse duration to assert $\overline{RESET}$		1			µs
$t_{d(MR)}$	$\overline{MR}$ pin low to out delay			250		ns
t_{STRT}	Startup delay			325		µs

(1) Overdrive = | (V_{IN} / V_{THRESH} – 1) × 100% |.

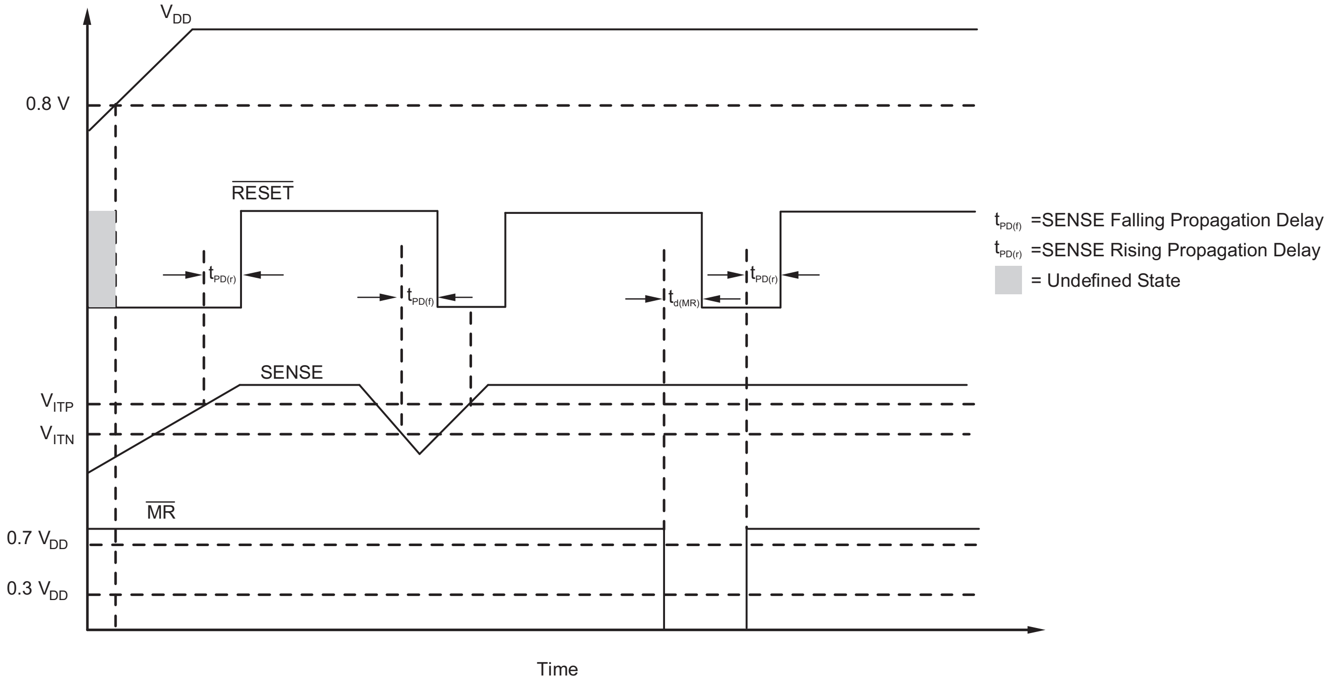


图 1. Timing Diagram

7.7 Typical Characteristics

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR}$ = V_{DD} (unless otherwise noted)

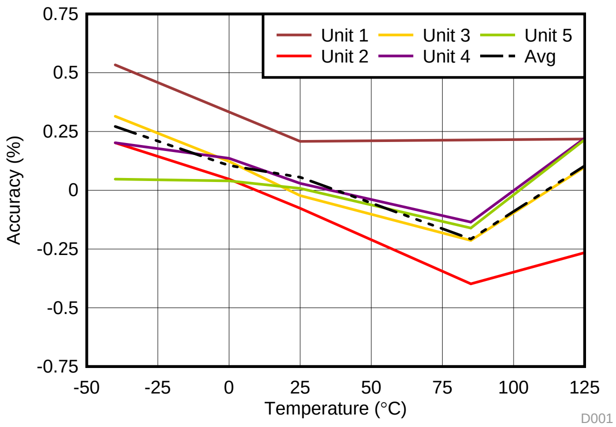


图 2. V_{ITN} Accuracy vs Temperature

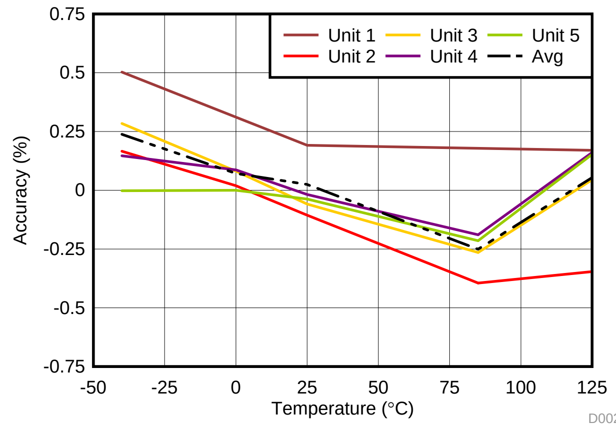
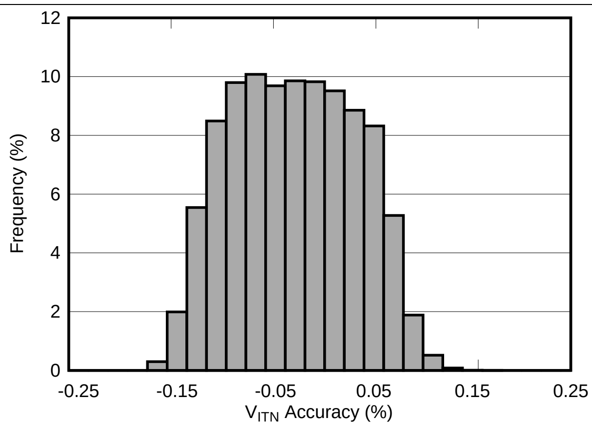
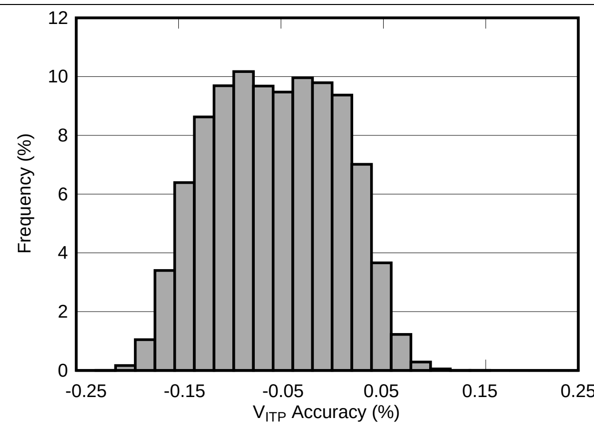


图 3. V_{ITP} Accuracy vs Temperature



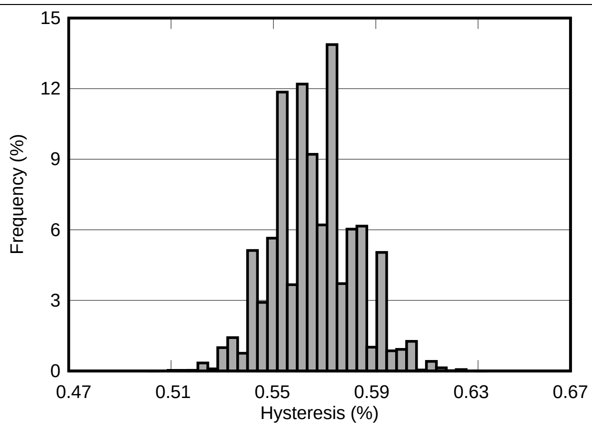
Tested at V_{DD} = 1.5 V and V_{DD} = 5.5 V, total tests = 136,348

图 4. V_{ITN} Accuracy Histogram



Tested at V_{DD} = 1.5 V and V_{DD} = 5.5 V, total tests = 136,348

图 5. V_{ITP} Accuracy Histogram



Tested at V_{DD} = 1.5 V and V_{DD} = 5.5 V, total tests = 136,348

图 6. Hysteresis Histogram

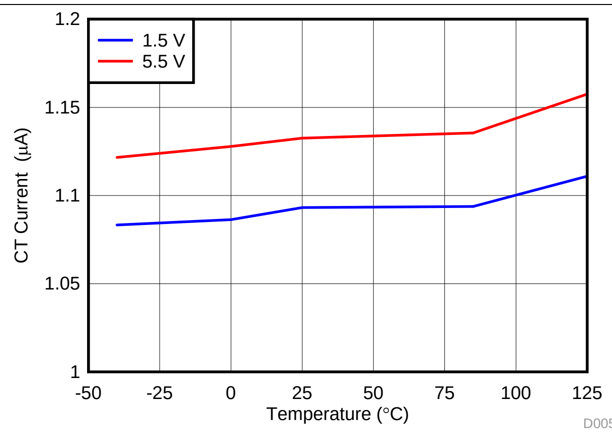
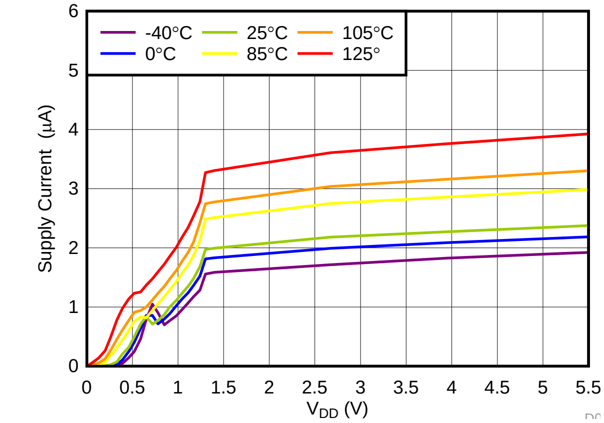


图 7. CT Current vs Temperature

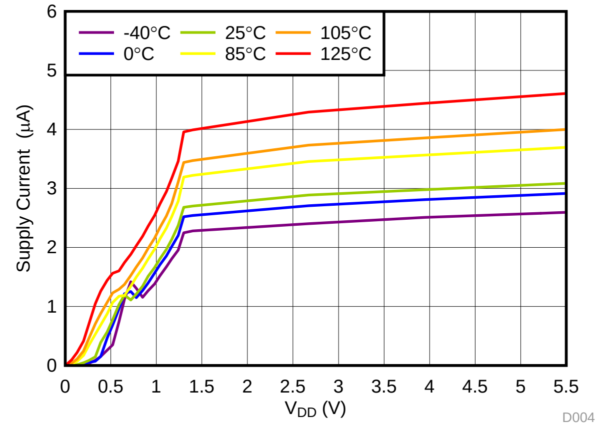
Typical Characteristics (接下页)

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR}$ = V_{DD} (unless otherwise noted)



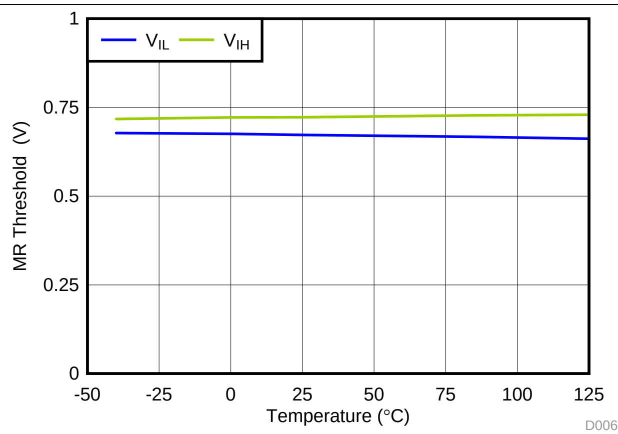
$\overline{MR}$ = V_{DD}

图 8. Supply Current vs Power-Supply Voltage



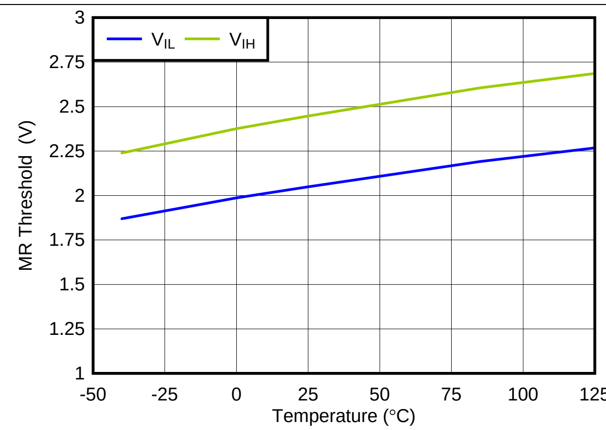
$\overline{MR}$ = 0 V

图 9. Supply Current vs Power-Supply Voltage



V_{DD} = 1.5 V

图 10. $\overline{MR}$ Threshold vs Temperature



V_{DD} = 5.5 V

图 11. $\overline{MR}$ Threshold vs Temperature

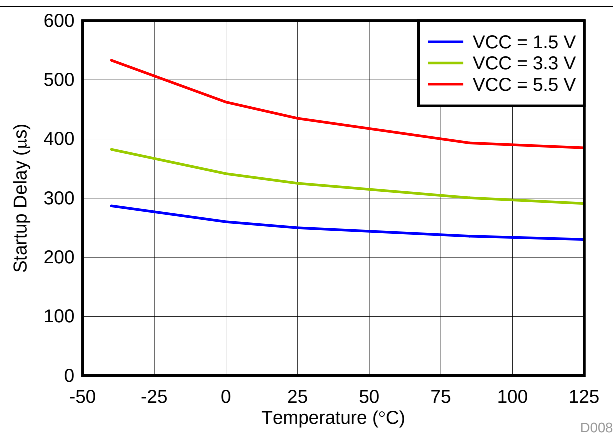
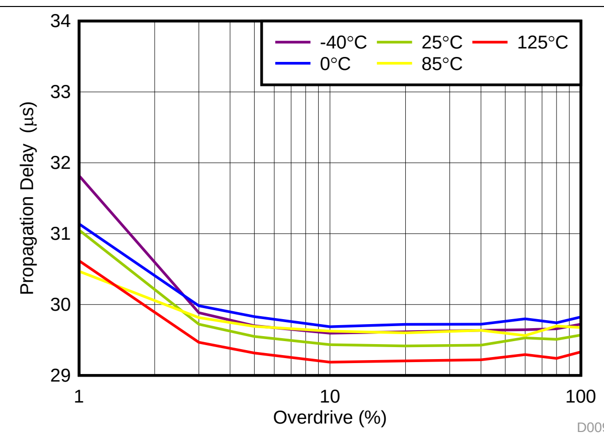


图 12. Startup Delay vs Temperature



V_{DD} = 5.5 V

图 13. Propagation Delay ($t_{PD(r)}$) vs Overdrive

Typical Characteristics (接下页)

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR}$ = V_{DD} (unless otherwise noted)

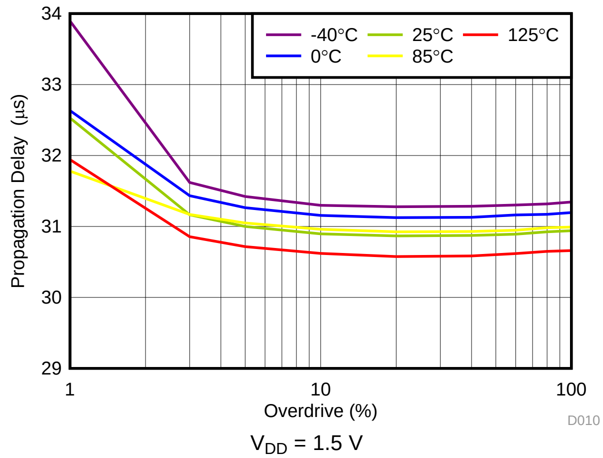


图 14. Propagation Delay ($t_{PD(r)}$) vs Overdrive

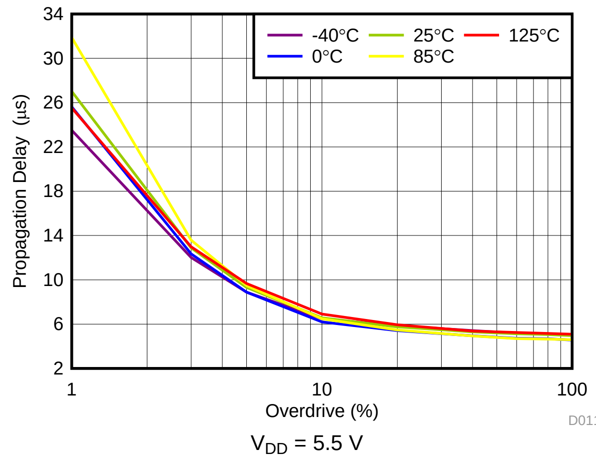


图 15. Propagation Delay ($t_{PD(f)}$) vs Overdrive

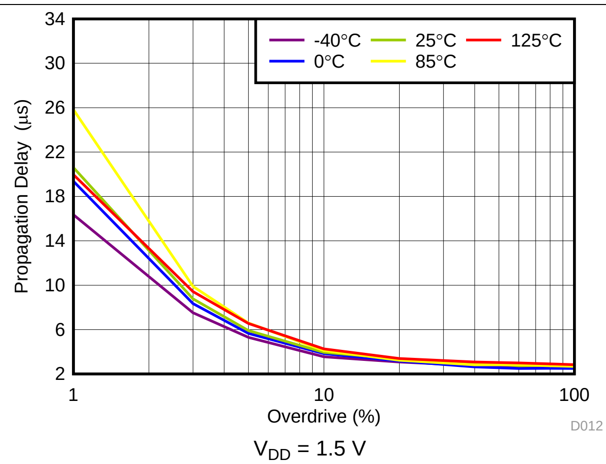


图 16. Propagation Delay ($t_{PD(f)}$) vs Overdrive

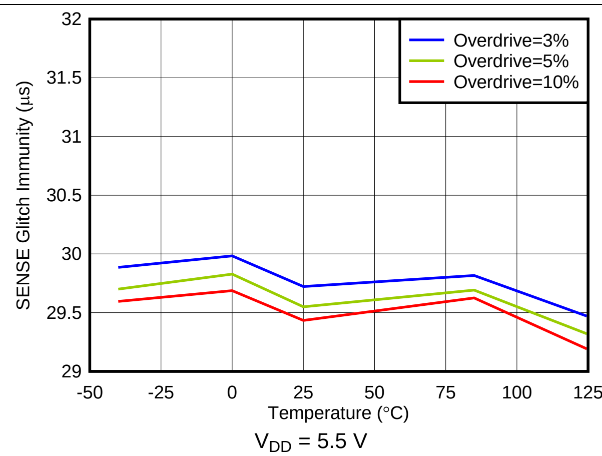


图 17. Low-to-High Glitch Immunity vs Temperature

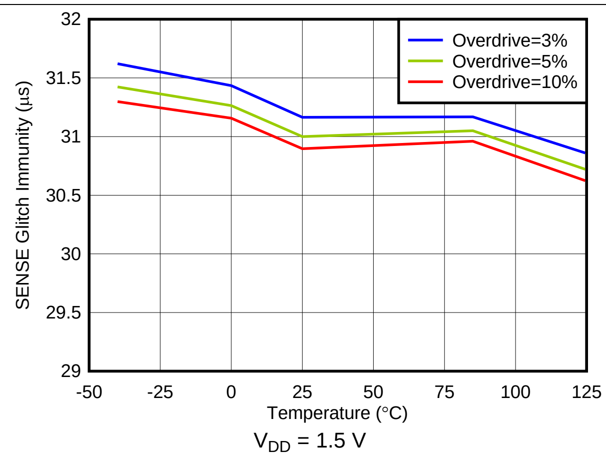


图 18. Low-to-High Glitch Immunity vs Temperature

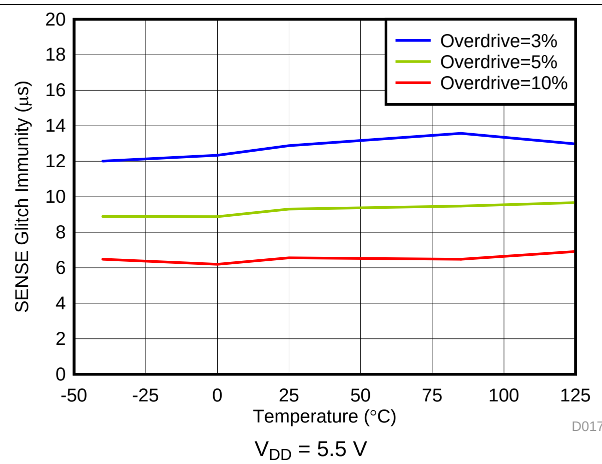
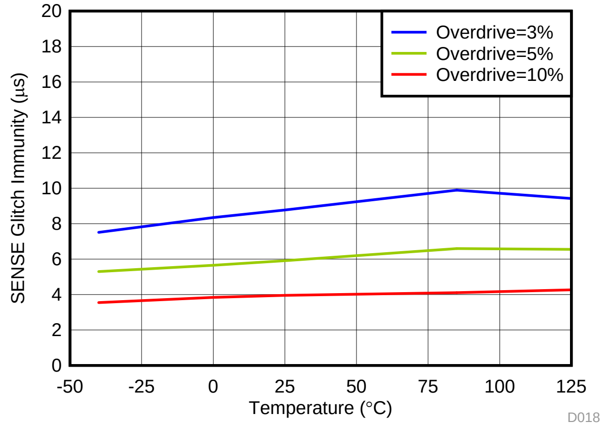


图 19. High-to-Low Glitch Immunity vs Temperature

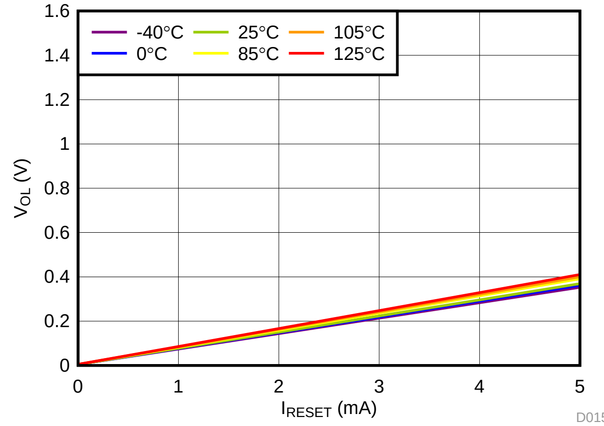
Typical Characteristics (接下页)

over the operating junction temperature range of –40°C to +125°C, 1.5 V ≤ V_{DD} ≤ 5.5 V, and $\overline{MR}$ = V_{DD} (unless otherwise noted)



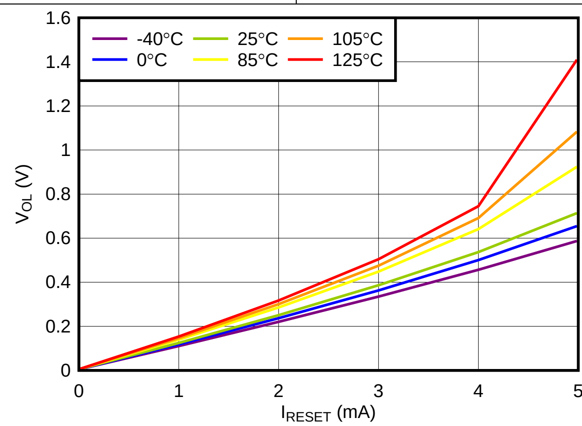
V_{DD} = 1.5 V

图 20. High-to-Low Glitch Immunity vs Temperature



V_{DD} = 5.5 V

图 21. Low-Level Output Voltage vs RESET Current



V_{DD} = 1.5 V

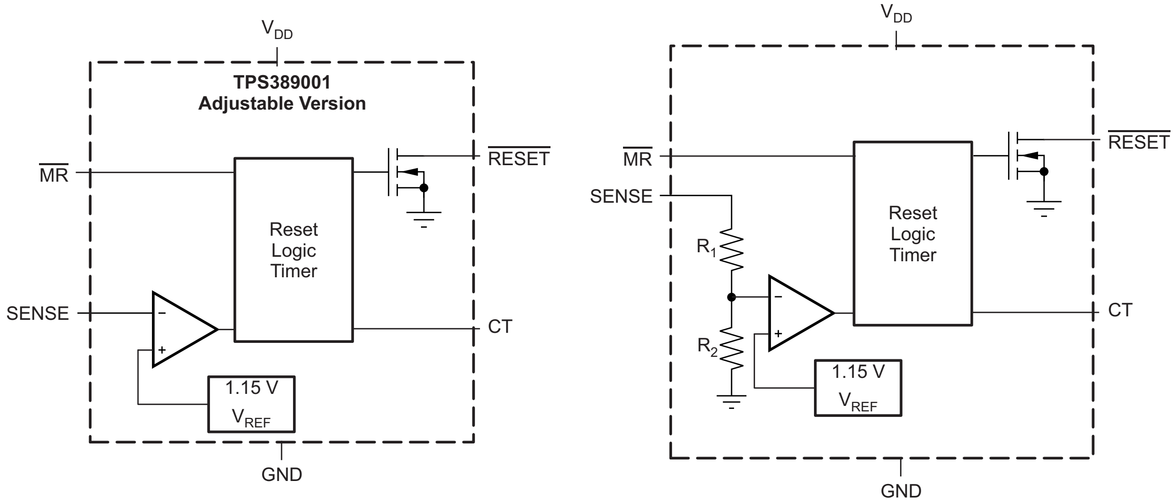
图 22. Low-Level Output Voltage vs RESET Current

8 Detailed Description

8.1 Overview

The TPS3890 supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{ITN} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above their respective thresholds.

8.2 Functional Block Diagram



Adjustable Voltage Version

Fixed Voltage Version

8.3 Feature Description

The combination of user-adjustable reset delay time with a broad range of threshold voltages allow these devices to be used in a wide array of applications. Fixed negative threshold voltages (V_{ITN}) can be factory set from 1.15 V to 3.17 V (see the *Device Comparison Table* for available options), and the adjustable device can be used to customize the threshold voltage for other application needs by using an external resistor divider. The CT pin allows the reset delay to be set between 25 µs and 30 s with the use of an external capacitor.

8.3.1 User-Configurable $\overline{\text{RESET}}$ Delay Time

The rising $\overline{\text{RESET}}$ delay time ($t_{PD(r)}$) can be configured by installing a capacitor connected to the CT pin. The TPS3890 uses a CT pin charging current (I_{CT}) of 1.15 µA to help counter the effect of capacitor and board-level leakage currents that can be substantial in certain applications. The rising $\overline{\text{RESET}}$ delay time can be set to any value between 25 µs (no C_{CT} installed) and 30 s (C_{CT} = 26 µF).

The capacitor value needed for a given delay time can be calculated using 公式 1:

$$t_{PD(r)}\ (\text{sec}) = C_{CT} \times V_{CT} \div I_{CT} + t_{PD(r)(nom)} \qquad (1)$$

The slope of 公式 1 is determined by the time that the CT charging current (I_{CT}) takes to charge the external capacitor up to the CT comparator threshold voltage (V_{CT}). When $\overline{\text{RESET}}$ is asserted, the capacitor is discharged through the internal CT pulldown resistor (R_{CT}). When the $\overline{\text{RESET}}$ conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor and when the voltage on this capacitor reaches 1.22 V, $\overline{\text{RESET}}$ is deasserted. Note that in order to minimize the difference between the calculated $\overline{\text{RESET}}$ delay time and the actual $\overline{\text{RESET}}$ delay time, use a low-leakage type capacitor (such as a ceramic capacitor) and minimize parasitic board capacitance around this pin.

Feature Description (接下页)

8.3.2 Manual Reset ($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above V_{ITP}, $\overline{\text{RESET}}$ is deasserted after the user-defined reset delay. If $\overline{\text{MR}}$ is not controlled externally, then $\overline{\text{MR}}$ must be connected to VDD. Note that if the logic signal driving $\overline{\text{MR}}$ is not greater than or equal to V_{DD}, then some additional current flows into VDD and out of $\overline{\text{MR}}$ and the difference is apparent when comparing 图 8 and 图 9.

图 23 shows how $\overline{\text{MR}}$ can be used to monitor multiple system voltages when only a single CT capacitor is needed to set the $\overline{\text{RESET}}$ delay time.

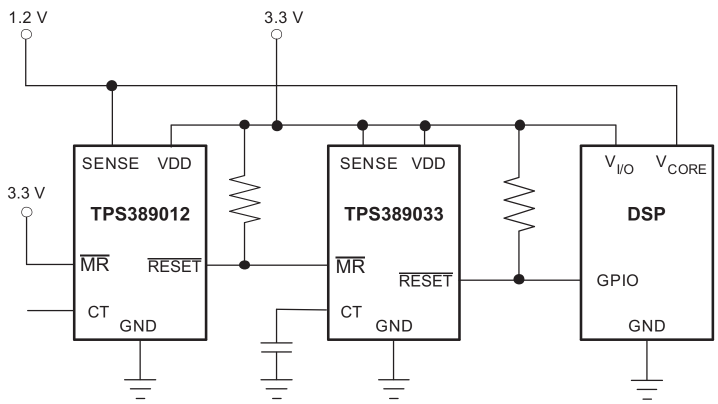


图 23. Using $\overline{\text{MR}}$ to Monitor Multiple System Voltages

8.3.3 $\overline{\text{RESET}}$ Output

$\overline{\text{RESET}}$ remains high (deasserted) as long as SENSE is above the positive threshold (V_{ITP}) and the manual reset signal ($\overline{\text{MR}}$) is logic high. If SENSE falls below the negative threshold (V_{ITN}) or if $\overline{\text{MR}}$ is driven low, then $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to a low impedance.

When $\overline{\text{MR}}$ is again logic high and SENSE is above V_{ITP}, a delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period ($t_{PD(r)}$). When the reset delay has elapsed, the $\overline{\text{RESET}}$ pin goes to a high-impedance state and uses a pullup resistor to hold $\overline{\text{RESET}}$ high. Connect the pullup resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level. $\overline{\text{RESET}}$ can be pulled up to any voltage up to 5.5 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by V_{OL}, the output capacitive loading, and the output leakage current ($I_{LKG(OD)}$).

8.3.4 SENSE Input

The SENSE input can vary from ground to 5.5 V (7.0 V, absolute maximum), regardless of the device supply voltage used. The SENSE pin is used to monitor the critical voltage rail. If the voltage on this pin drops below V_{ITN}, then $\overline{\text{RESET}}$ is asserted. When the voltage on the SENSE pin exceeds the positive threshold voltage, $\overline{\text{RESET}}$ deasserts after the user-defined $\overline{\text{RESET}}$ delay time.

The internal comparator has built-in hysteresis to ensure well-defined $\overline{\text{RESET}}$ assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3890 device is relatively immune to short transients on the SENSE pin. Glitch immunity is dependent on threshold overdrive, as illustrated in 图 19 for V_{ITN} and 图 18 for V_{ITP}. Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

Feature Description (接下页)

The adjustable version (TPS389001) can be used to monitor any voltage rail down to 1.15 V using the circuit shown in 图 24.

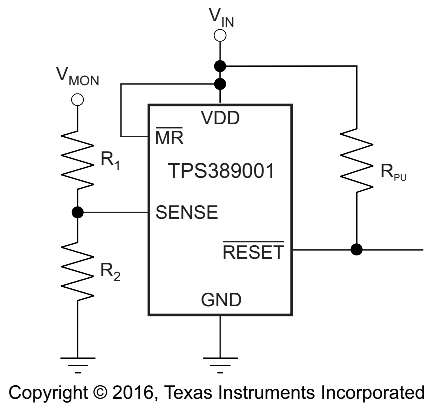


图 24. Using the TPS389001 to Monitor a User-Defined Threshold Voltage

The target threshold voltage for the monitored supply ($V_{ITx(MON)}$) and the resistor divider values can be calculated by using 公式 2 and 公式 3, respectively:

$$V_{ITx(MON)} = V_{ITx} \times (1 + R_1 \div R_2) \tag{2}$$

公式 3 can be used to calculate either the negative threshold or the positive threshold by replacing V_{ITx} with either V_{ITN} or V_{ITP}, respectively.

$$R_{TOTAL} = R_1 + R_2 \tag{3}$$

Resistors with high values minimize current consumption; however, the input bias current of the device degrades accuracy if the current through the resistors is too low. Therefore, choosing an R_{TOTAL} value so that the current through the resistor divider is at least 100 times larger than the SENSE input current is simplest. See application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for more details on sizing input resistors.

8.3.4.1 Immunity to SENSE Pin Voltage Transients

The TPS3702 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient. Overdrive is defined by how much VSENSE exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs (that is, undervoltage and overvoltage). Threshold overdrive is calculated as a percent of the threshold in question, as shown in 公式 4.

$$\text{Overdrive} = |\,(V_{SENSE} / V_{ITx} - 1) \times 100\%\,| \tag{4}$$

图 17 to 图 20 illustrate the glitch immunity that the TPS3890 has versus temperature with three different overdrive voltages. The propagation delay versus overdrive curves (图 13 to 图 16) can be used to determine how sensitive the TPS3890 family of devices are across an even wider range of overdrive voltages.

8.4 Device Functional Modes

表 1 summarizes the various functional modes of the device.

表 1. Truth Table

V_{DD}	$\overline{MR}$	SENSE	$\overline{RESET}$
$V_{DD} < V_{POR}$	—	—	Undefined
$V_{POR} < V_{DD} < V_{DD(MIN)}$ (1)	—	—	L
$V_{DD} \geq V_{DD(MIN)}$	L	—	L
$V_{DD} \geq V_{DD(MIN)}$	H	$V_{SENSE} < V_{ITN}$	L
$V_{DD} \geq V_{DD(MIN)}$	H	$V_{SENSE} > V_{ITP}$	H

(1) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and $\overline{RESET}$ is held low until V_{DD} falls below V_{POR}.

8.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$ signal is determined by the voltage on the SENSE pin and the logic state of $\overline{MR}$.

- $\overline{MR}$ high: when the voltage on VDD is greater than 1.5 V, the $\overline{RESET}$ signal corresponds to the voltage on the SENSE pin relative to the threshold voltage.
- $\overline{MR}$ low: in this mode, $\overline{RESET}$ is held low regardless of the voltage on the SENSE pin.

8.4.2 Above Power-On-Reset But Less Than $V_{DD(min)}$ ($V_{POR} < V_{DD} < V_{DD(min)}$)

When the voltage on VDD is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage (V_{POR}), the $\overline{RESET}$ signal is asserted regardless of the voltage on the SENSE pin.

8.4.3 Below Power-On-Reset ($V_{DD} < V_{POR}$)

When the voltage on VDD is lower thanV_{POR}, the device does not have enough voltage to internally pull the asserted output low and $\overline{RESET}$ is undefined and must not be relied upon for proper device function.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

A typical application for the TPS389018 is shown in 图 25. The TPS389018 can be used to monitor the 1.8-V VDD rail required by the TI Delfino™ microprocessor family. The open-drain $\overline{\text{RESET}}$ output of the TPS389018 is connected to the $\overline{\text{XRS}}$ input of the microprocessor. A reset event is initiated when the VDD voltage is less than V_{ITN} or when $\overline{\text{MR}}$ is driven low by an external source.

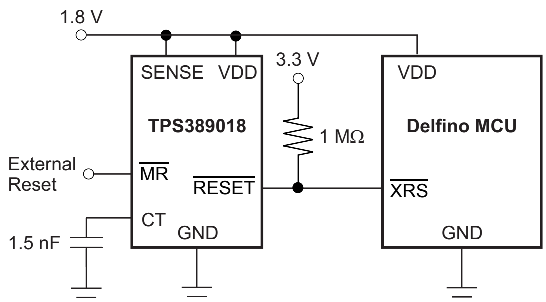


图 25. TPS3890 Monitoring the Supply Voltage for a Delfino Microprocessor

9.2.1 Design Requirements

The TPS3890 $\overline{\text{RESET}}$ output can be used to drive the reset ($\overline{\text{XRS}}$) input of a microprocessor. The $\overline{\text{RESET}}$ pin of the TPS3890 is pulled high with a 1-MΩ resistor; the reset delay time is controlled by the CT capacitor and is set depending on the reset requirement times of the microprocessor. During power-up, $\overline{\text{XRS}}$ must remain low for at least 1 ms after VDD reaches 1.5 V for the C2000™ Delfino family of microprocessors. For 100-MHz operation, the Delfino TMS320F2833x microcontroller uses a supply voltage of 1.8 V that must be monitored by the TPS3890.

9.2.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS389018 has a negative threshold of 1.73 V and a positive threshold of 1.74 V, making the device suitable for monitoring a 1.8-V rail. The secondary constraint for this application is the reset delay time that must be at least 1 ms to allow the Delfino microprocessor enough time to startup up correctly. Because a minimum time is required, the worst-case scenario is a supervisor with a high CT charging current (I_{CT}) and a low CT comparator threshold (V_{CT}). For applications with ambient temperatures ranging from –40°C to +125°C, C_{CT} can be calculated using $I_{CT(Max)}$, $V_{CT(MIN)}$, and solving for C_{CT} in 公式 1 such that the minimum capacitance required at the CT pin is 1.149 nF. If standard capacitors with ±20% tolerances are used, then the CT capacitor must be 1.5 nF or larger to ensure that the 1-ms delay time is met.

A 0.1-µF decoupling capacitor is connected to the VDD pin as a good analog design practice and a 1-MΩ resistor is used as the $\overline{\text{RESET}}$ pullup resistor to minimize the current consumption when $\overline{\text{RESET}}$ is asserted. The $\overline{\text{MR}}$ pin can be connected to an external signal if desired or connected to VDD if not used.

Typical Application (接下页)

9.2.3 Application Curve

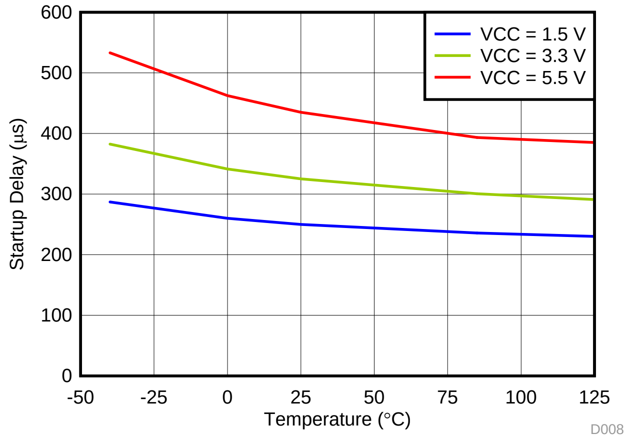


图 26. Startup Delay vs Temperature

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.5 V and 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor near the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the $\overline{\text{RESET}}$ delay time is not adversely affected.

11.2 Layout Example

The layout example in shows how the TPS3890 is laid out on a printed circuit board (PCB) with a user-defined delay.

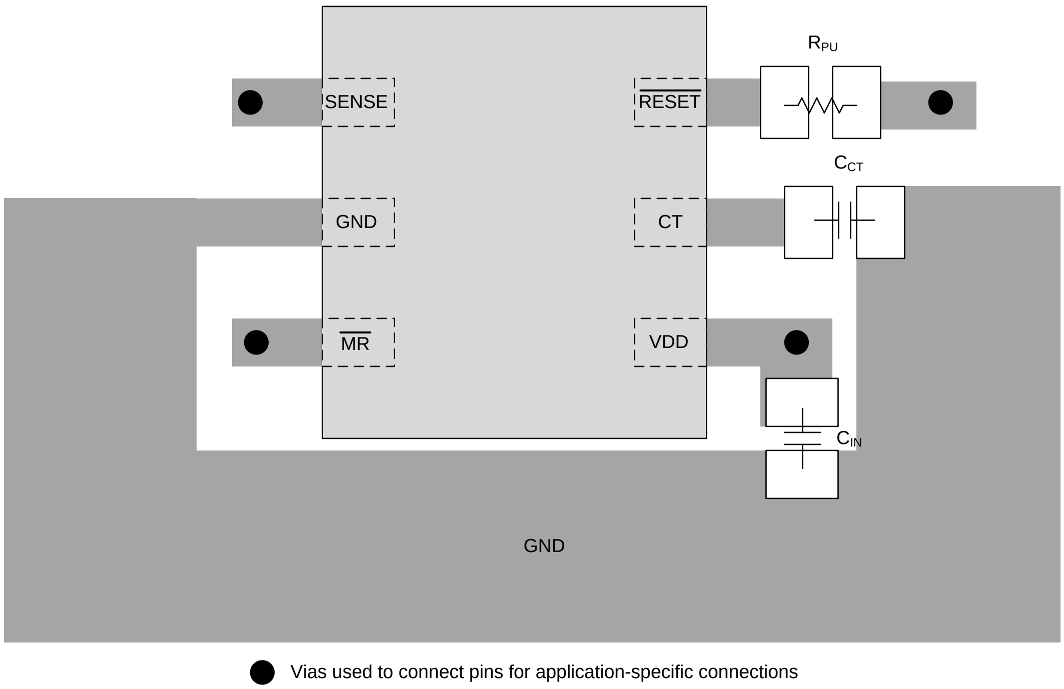


图 27. Recommended Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

以下相关文档可从 www.ti.com 下载：

- *优化比较器输入上的电阻分压器*，SLVA450
- *《电源设计灵敏度分析》*，SLVA481
- *《TMS320C28x 数字信号控制器入门》*，SPRAAM0
- 《TPS3890EVM-775 评估模块用户指南》，SBVU030
- C2000 Delfino 系列微处理器
- 《TMS320F2833x 微控制器》，SPRS439

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

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12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS389001DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2V	Samples
TPS389001DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2V	Samples
TPS389012DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2W	Samples
TPS389012DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2W	Samples
TPS389015DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2X	Samples
TPS389015DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2X	Samples
TPS389018DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y	Samples
TPS389018DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y	Samples
TPS389020DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y	Samples
TPS389020DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Y	Samples
TPS389025DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Z	Samples
TPS389025DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Z	Samples
TPS389030DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3A	Samples
TPS389030DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3A	Samples
TPS389033DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3B	Samples
TPS389033DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	3B	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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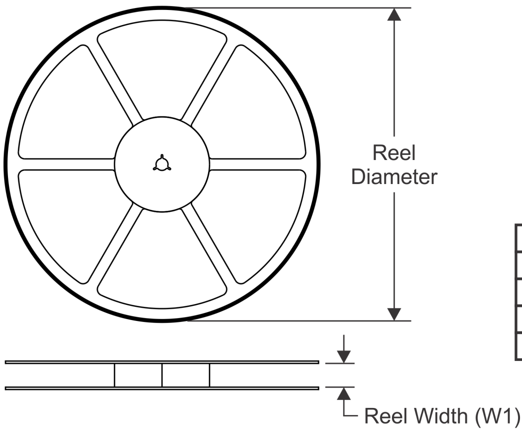
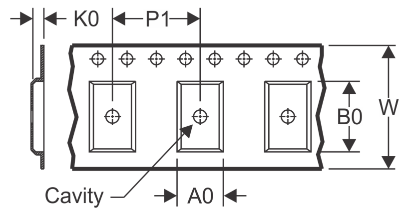
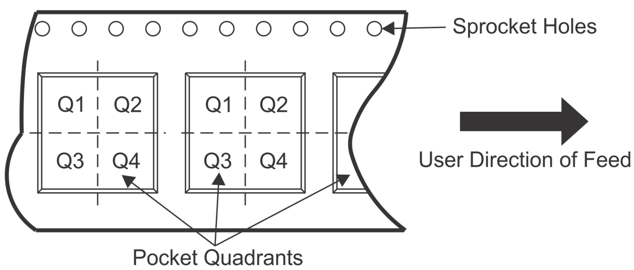
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

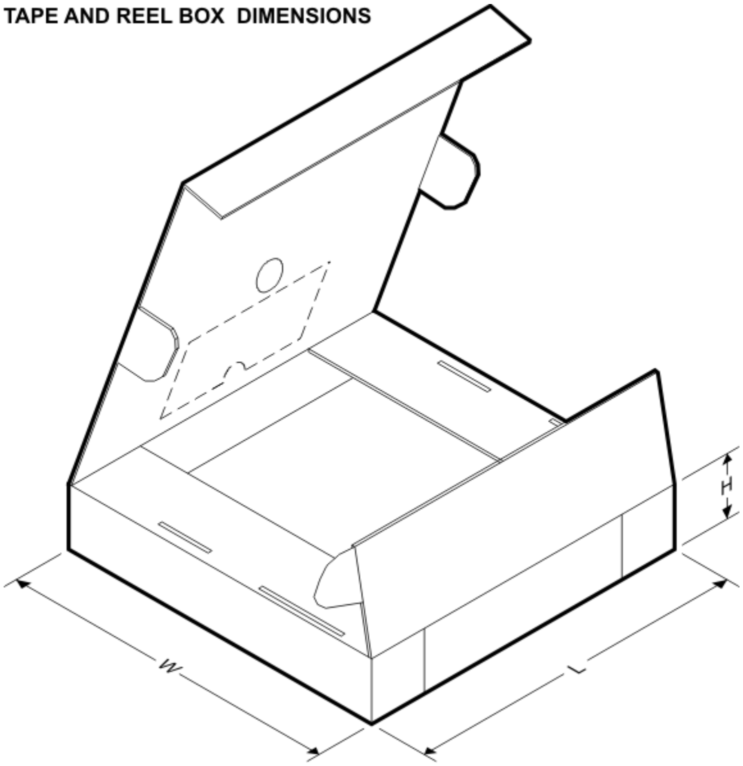
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS389001DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389001DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389012DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389012DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389015DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389015DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389018DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389018DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389020DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389020DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389025DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389025DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389030DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389030DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2

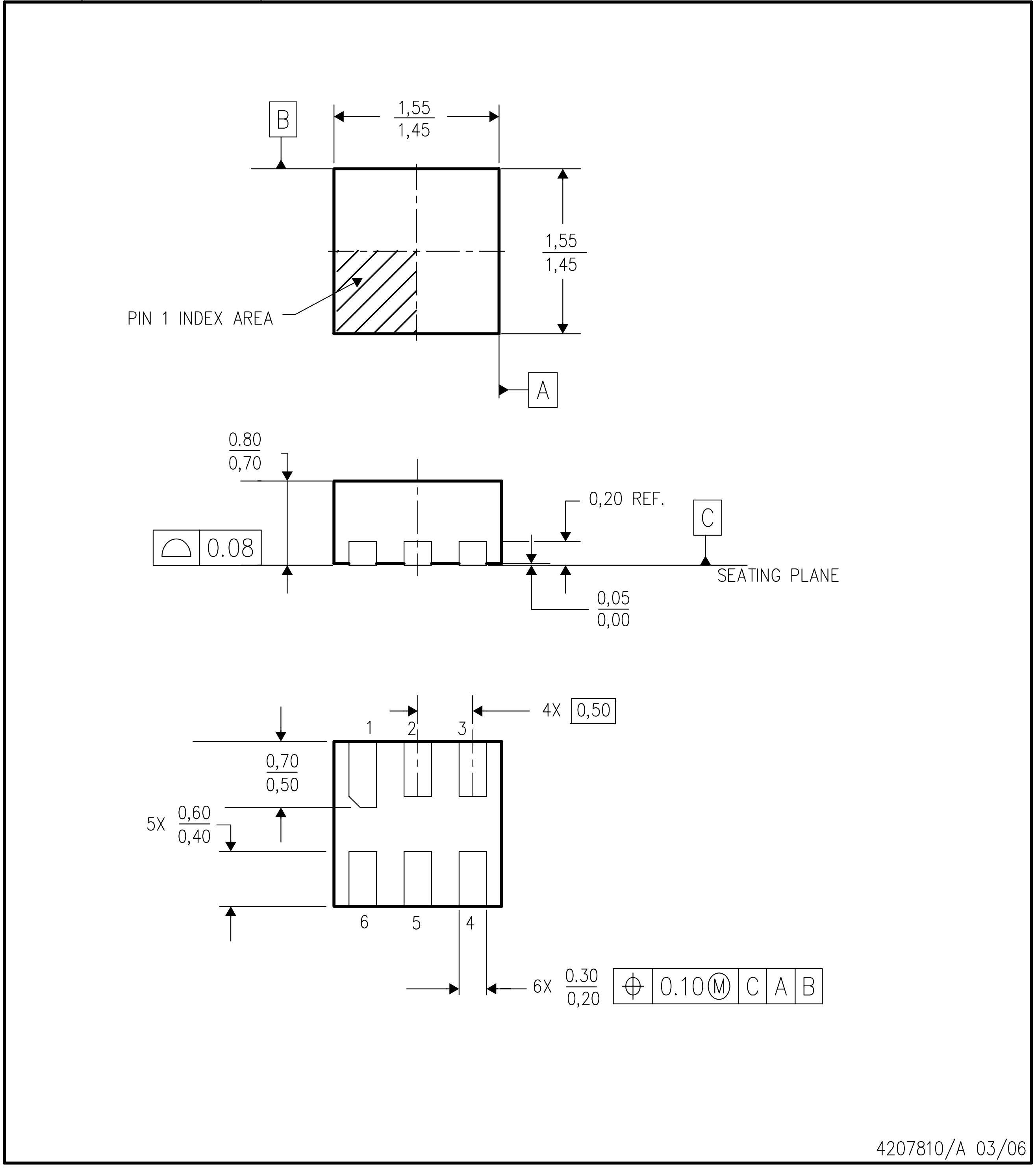
TAPE AND REEL BOX DIMENSIONS



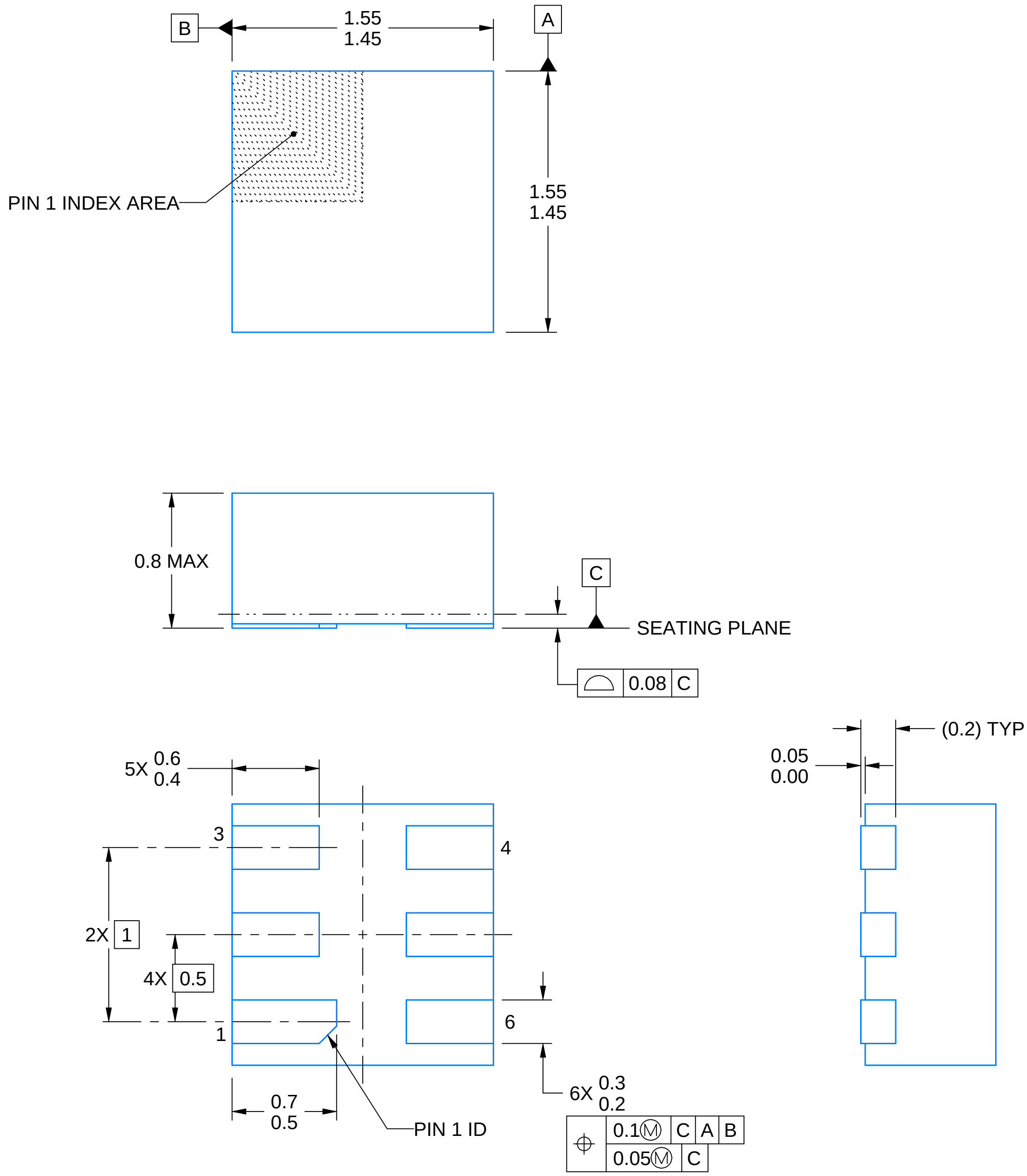
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS389001DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389001DSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS389012DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389012DSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS389015DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389015DSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS389018DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389018DSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS389020DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389020DSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS389025DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389025DSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS389030DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389030DSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS389033DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389033DSET	WSON	DSE	6	250	183.0	183.0	20.0

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



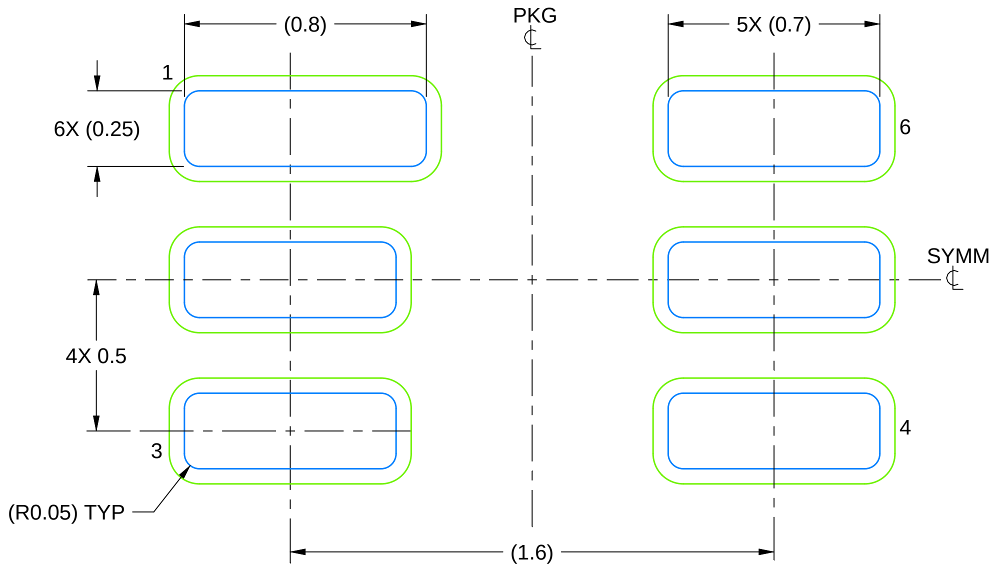
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. This package is lead–free.



4220552/A 04/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

PADS 4-6
NON SOLDER MASK
DEFINED

PADS 1-3
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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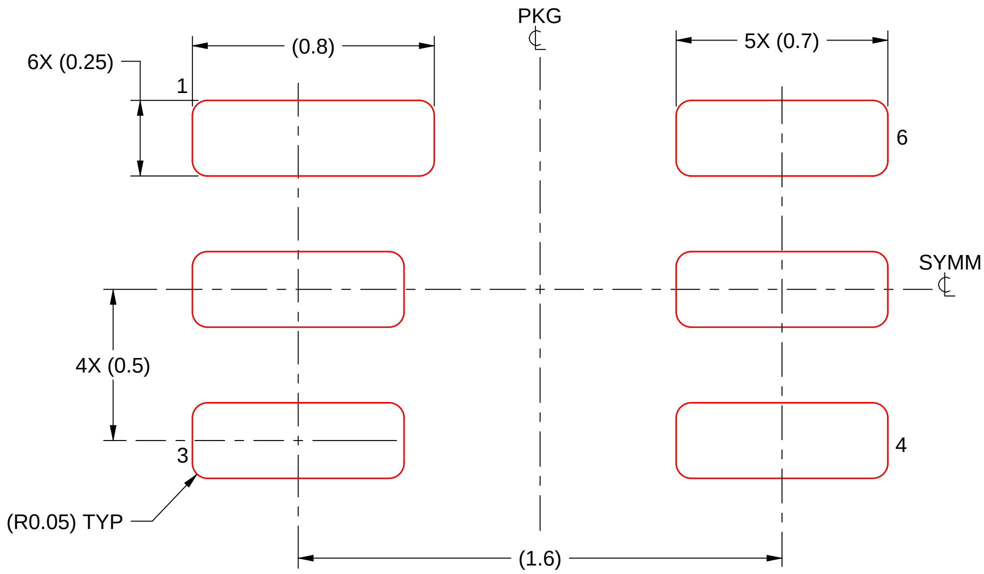
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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