

Crystal to LVPECL Clock Generator

Features

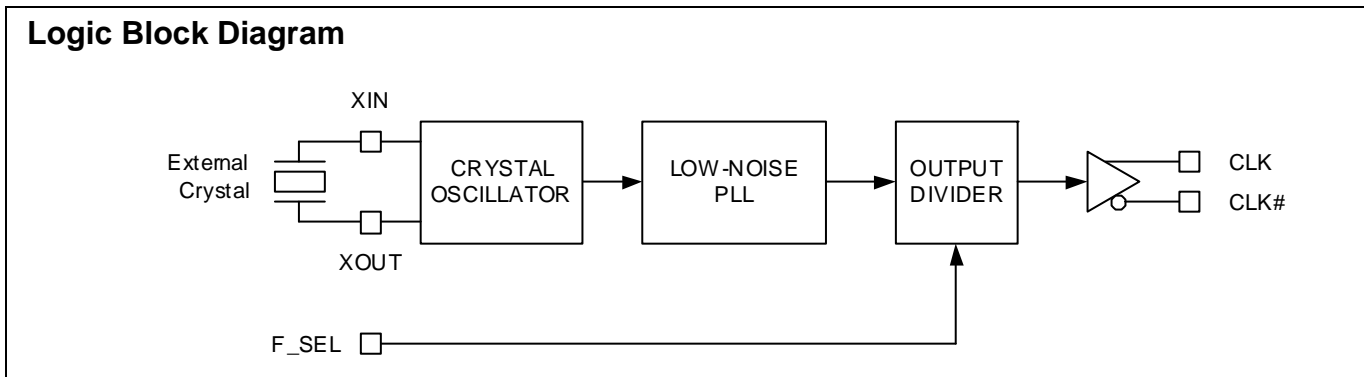
- One LVPECL Output Pair
- Selectable Frequency Multiplication: x2.5 or x5
- External Crystal Frequency: 25.0 MHz
- Output Frequency: 62.5 MHz or 125 MHz
- Low RMS Phase Jitter at 125 MHz, using 25 MHz Crystal (1.875 MHz to 20 MHz): 0.4 ps (Typical)
- Phase Noise at 125 MHz:

Offset	Noise Power
1 kHz	-117 dBc/Hz
10 kHz	-126 dBc/Hz
100 kHz	-131 dBc/Hz
1 MHz	-131 dBc/Hz

- Pb-free 8-Pin TSSOP Package
- Supply Voltage: 3.3V or 2.5V
- Commercial and Industrial Temperature Ranges

Functional Description

The CY2XP22 is a PLL (Phase Locked Loop) based high performance clock generator that uses an external reference crystal. It is specifically targeted at FibreChannel and Gigabit Ethernet applications. It produces a selectable output frequency that is 2.5 or 5 times the crystal frequency. With a 25 MHz crystal, the user can select either a 62.5 MHz or 125 MHz output. It uses Cypress's low noise VCO technology to achieve less than 1 ps typical RMS phase jitter. The CY2XP22 has a crystal oscillator interface input and one LVPECL output pair.



Pinouts

Figure 1. Pin Diagram - 8-Pin TSSOP

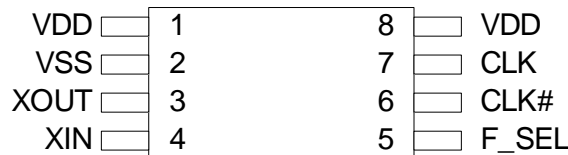


Table 1. Pin Definition - 8-Pin TSSOP

Pin Number	Pin Name	I/O Type	Description
1, 8	VDD	Power	3.3V or 2.5V power supply
2	VSS	Power	Ground
3, 4	XOUT, XIN	XTAL output and input	Parallel resonant crystal interface
5	F_SEL	CMOS input	Frequency Select: see Frequency Table
6,7	CLK#, CLK	LVPECL output	Differential Clock Output

Frequency Table

Inputs		PLL Multiplier Value	Output Frequency (MHz)
Crystal Frequency (MHz)	F_SEL		
25	0	5	125
	1	2.5	62.5

Absolute Maximum Conditions

Parameter	Description	Conditions	Min	Max	Unit
V _{DD}	Supply Voltage		-0.5	4.4	V
V _{IN} ^[1]	Input Voltage, DC	Relative to V _{SS}	-0.5	V _{DD} + 0.5	V
T _S	Temperature, Storage	Non operating	-65	150	°C
T _J	Temperature, Junction			135	°C
ESD _{HBM}	ESD Protection, Human Body Model	JEDEC STD 22-A114-B	2000		V
UL-94	Flammability Rating	At 1/8 in.	V-0		
Θ _{JA} ^[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	100		°C/W
		1 m/s airflow	91		
		2.5 m/s airflow	87		

Operating Conditions

Parameter	Description	Min	Max	Unit
V _{DD}	3.3V Supply Voltage	3.135	3.465	V
	2.5V Supply Voltage	2.375	2.625	V
T _A	Ambient Temperature, Commercial	0	70	°C
	Ambient Temperature, Industrial	-40	85	°C
T _{PU}	Power up time for all V _{DD} to reach minimum specified voltage (ensure power ramps is monotonic)	0.05	500	ms

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I _{DD} ^[3]	Operating Supply Current with output terminated	V _{DD} = 3.465V, F _{OUT} = 125 MHz, output terminated	-	-	150	mA
		V _{DD} = 2.625V, F _{OUT} = 125 MHz, output terminated	-	-	145	mA
V _{OH}	LVPECL Output High Voltage	V _{DD} = 3.3V or 2.5V, R _{TERM} = 50Ω to V _{DD} - 2.0V	V _{DD} - 1.15	-	V _{DD} - 0.75	V
V _{OL}	LVPECL Output Low Voltage	V _{DD} = 3.3V or 2.5V, R _{TERM} = 50Ω to V _{DD} - 2.0V	V _{DD} - 2.0	-	V _{DD} - 1.625	V
V _{OD1}	LVPECL Peak-to-Peak Output Voltage Swing	V _{DD} = 3.3V or 2.5V, R _{TERM} = 50Ω to V _{DD} - 2.0V	600	-	1000	mV
V _{OD2}	LVPECL Output Voltage Swing (V _{OH} - V _{OL})	V _{DD} = 2.5V, R _{TERM} = 50Ω to V _{DD} - 1.5V	500	-	1000	mV

Notes

1. The voltage on any input or IO pin cannot exceed the power pin during power up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
3. I_{DD} includes approximately 24 mA of current that is dissipated externally in the output termination resistors.

DC Electrical Characteristics (continued)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V _{OCM}	LVPECL Output Common Mode Voltage (V _{OH} + V _{OL})/2	V _{DD} = 2.5V, R _{TERM} = 50Ω to V _{DD} - 1.5V	1.2	–	–	V
V _{IH}	Input High Voltage, F_SEL		0.7*V _{DD}	–	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage, F_SEL		-0.3	–	0.3*V _{DD}	V
I _{IH}	Input High Current, F_SEL	F_SEL = V _{DD}	–	–	115	μA
I _{IL}	Input Low Current, F_SEL	F_SEL = V _{SS}	-50	–	–	μA
C _{IN}	Input Capacitance, F_SEL			15		pF
C _{INX}	Pin Capacitance, XIN & XOUT			4.5		pF

AC Electrical Characteristics^[4]

Parameter	Description	Conditions	Min	Typ	Max	Unit
F _{OUT}	Output Frequency		62.5	–	125	MHz
T _R , T _F	Output Rise or Fall Time	20% to 80% of full output swing	–	500	–	ps
T _{Jitter(φ)}	RMS Phase Jitter (Random)	125 MHz, (1.875–20 MHz)	–	0.4	–	ps
T _{DC}	Output Duty Cycle	Measured at zero crossing point	48	50	52	%
T _{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time V _{DD} = V _{DD(min.)} or from F_SEL changing	–	–	10	ms

Recommended Crystal Specifications^[5]

Parameter	Description	Min	Max	Unit
Mode	Mode of Oscillation	Fundamental		
F	Frequency	25	25	MHz
ESR	Equivalent Series Resistance	–	50	Ω
C ₀	Shunt Capacitance	–	7	pF

Notes

- 4. Not 100% tested, guaranteed by design and characterization.
- 5. Characterized using an 18 pF parallel resonant crystal.

Parameter Measurements

Figure 2. 3.3V Output Load AC Test Circuit

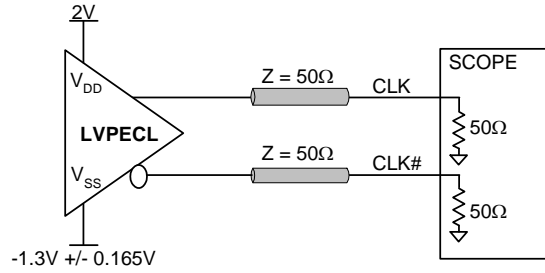


Figure 3. 2.5V Output Load AC Test Circuit

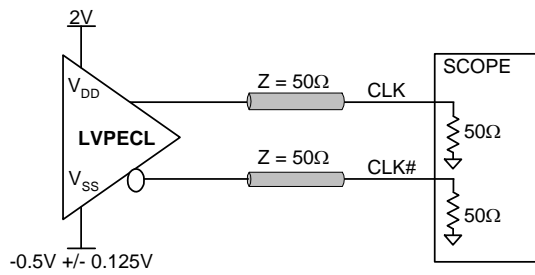


Figure 4. Output DC Parameters

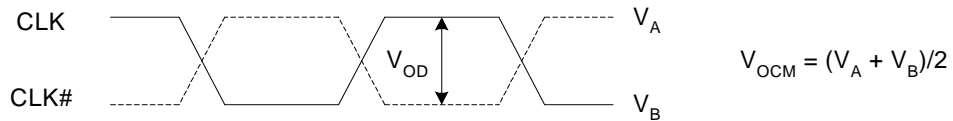


Figure 5. Output Rise and Fall Time

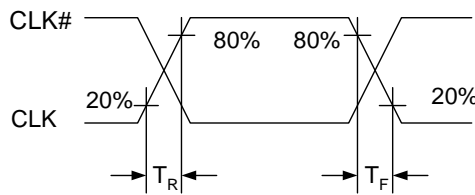


Figure 6. RMS Phase Jitter

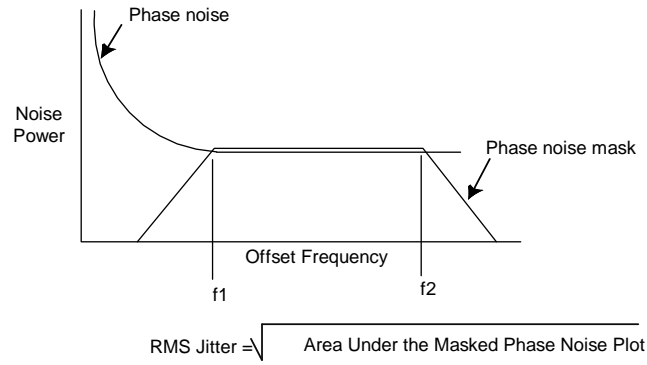
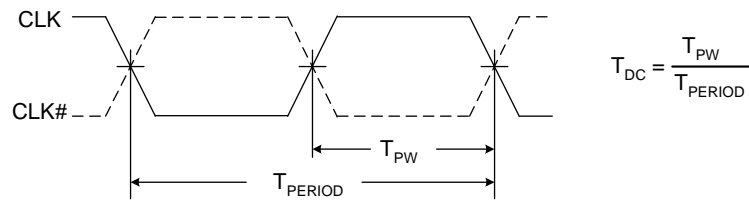


Figure 7. Output Duty Cycle

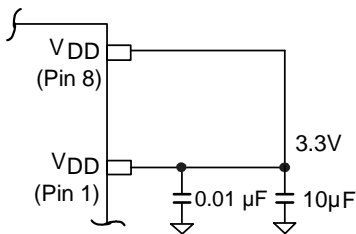


Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, noise at the power supply pins can degrade performance. To achieve optimum jitter performance, use good power supply isolation practices. Figure 8 illustrates a typical filtering scheme. Since all the current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 μF ceramic chip capacitor is also located close to this pin to provide a short and low impedance AC path to ground. A 1 to 10 μF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

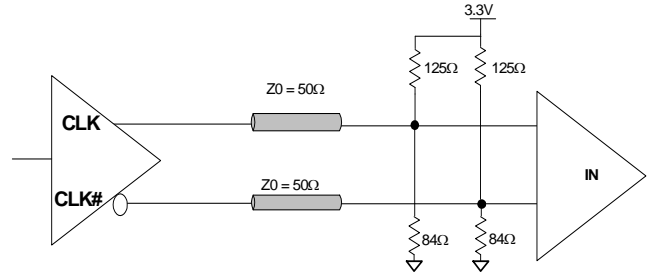
Figure 8. Power Supply Filtering



Termination for LVPECL Output

The CY2XP22 implements its LVPECL driver with a current steering design. For proper operation, it requires a 50 ohm dc termination on each of the two output signals. For 3.3V operation, this data sheet specifies output levels for termination to $V_{DD}-2.0\text{V}$. This same termination voltage can also be used for $V_{DD} = 2.5\text{V}$ operation, or it can be terminated to $V_{DD}-1.5\text{V}$. Note that it is also possible to terminate with 50 ohms to ground (V_{SS}), but the high and low signal levels differ from the data sheet values. Termination resistors are best located close to the destination device. To avoid reflections, trace characteristic impedance (Z_0) should match the termination impedance. Figure 9 shows a standard termination scheme.

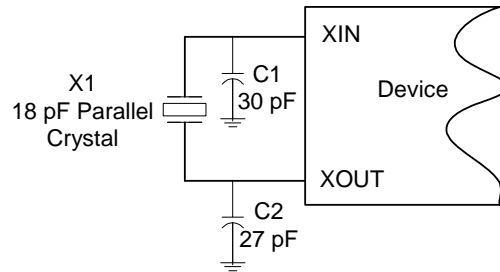
Figure 9. LVPECL Output Termination



Crystal Interface

The CY2XP22 is characterized with 18 pF parallel resonant crystals. The capacitor values shown in Figure 10 are determined using a 25 MHz 18 pF parallel resonant crystal and are chosen to minimize the ppm error. Note that the optimal values for C1 and C2 depend on the parasitic trace capacitance and are thus layout dependent.

Figure 10. Crystal Input Interface

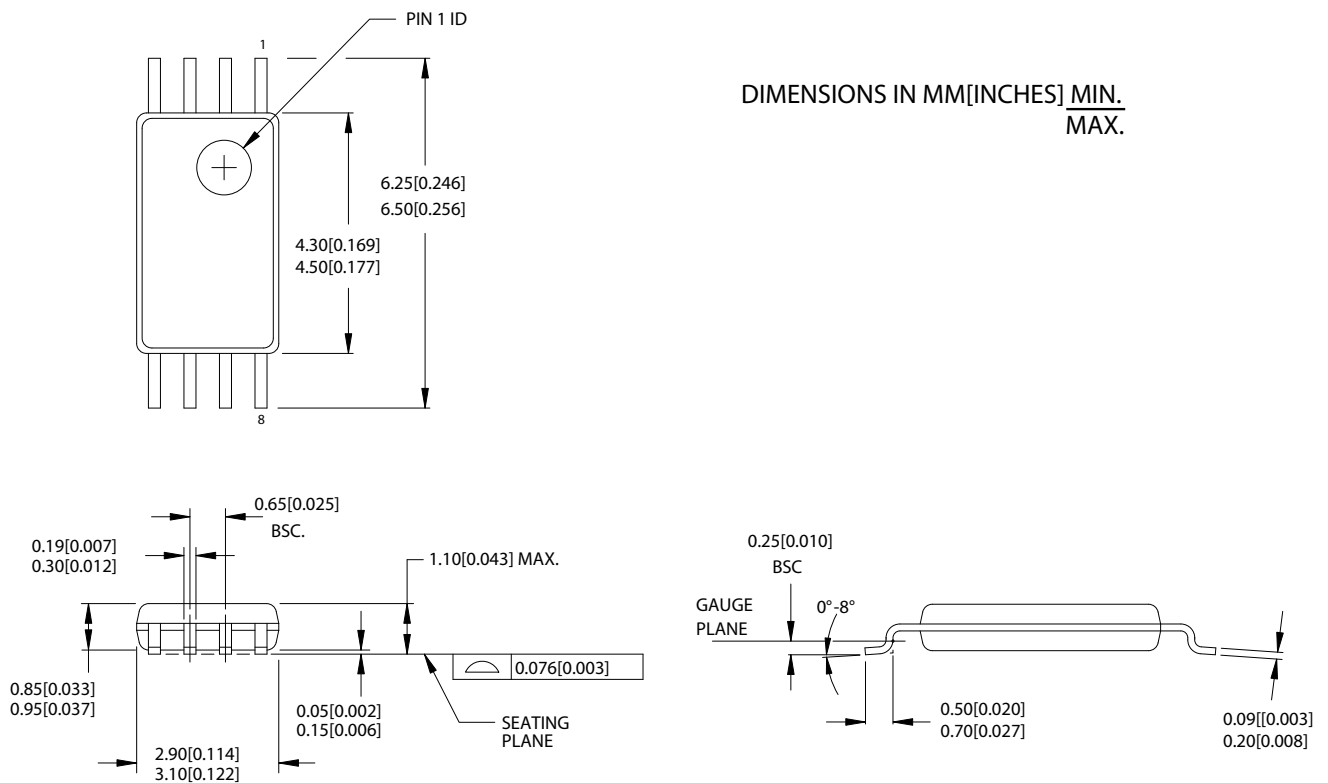


Ordering Information

Part Number	Package Type	Product Flow
CY2XP22ZXC	8-pin TSSOP	Commercial, 0°C to 70°C
CY2XP22ZXCT	8-pin TSSOP - Tape and Reel	Commercial, 0°C to 70°C
CY2XP22ZXI	8-pin TSSOP	Industrial, -40°C to 85°C
CY2XP22ZXIT	8-pin TSSOP - Tape and Reel	Industrial, -40°C to 85°C

Package Drawing and Dimensions

Figure 11. 8-Pin Thin Shrunken Small Outline Package (4.40 MM Body) Z8



51-85093-A

Document History Page

Document Title: CY2XP22 Crystal to LVPECL Clock Generator Document Number: 001-10229				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	506262	See ECN	RGL	New Data Sheet
*A	838060	See ECN	RGL	Changed status from Advance to Preliminary
*B	2700242	04/30/2009	KVM/PYRS	Reformatted Revised phase noise values Replaced VCC with VDD; VEE with VSS; updated pin names Removed pull-up resistor on F_SEL Corrected temperature range, added industrial temperature range Increased IDD from 120 / 100 mA to 150 / 140 mA Added CINX parameter, revised CIN parameter Revised LVPECL output specs Added thermal resistance information Changed VIL, VIH, IIL & IIH specs Revised suggested crystal load capacitor values
*C	2718898	06/15/09	WWZ	Minor ECN to post data sheet to external web

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