ACT5830

Rev 2, 20-Jan-11

Twelve Channel PMU for Mobile Phones

FEATURES

- **Multiple Patents Pending**
- **350mA, PWM Step-Down DC/DC Converter**
- **Eight I²C-Programmable, Low Noise LDOs**
  - **Three Optimized for RF Section Power**
  - **Five Optimized for BB Section Power**
- **Li+ Battery Charger with Integrated MOSFET**
  - **Charger Current Monitor Output (VICHG)**
  - **Charger ON/OFF Control Pin**
- **Two N-channel Open Drain Switches**
- **Minimal External Components**
- **I²C™ Serial Interface**
  - **Configurable Operating Modes**
- **AC-OK and RESET Outputs**
- **5×5mm, Thin-QFN (TQFN55-40) Package**
  - **Only 0.75mm Height**
  - **RoHS Compliant**

APPLICATIONS

- **GSM or CDMA Mobile Phones**

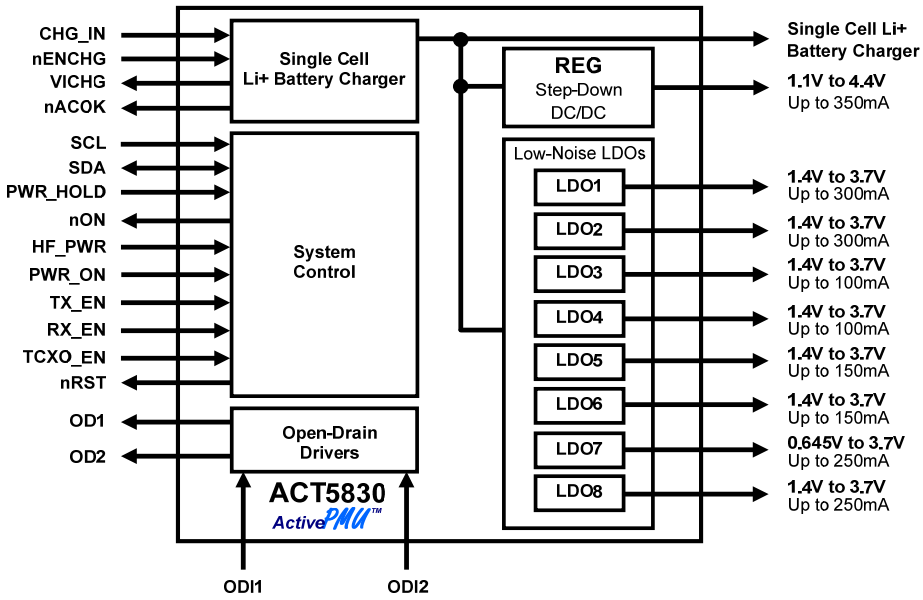
GENERAL DESCRIPTION

The patent-pending ACT5830 is a complete, integrated power management solution that is ideal for mid-high and mobile phones. This device integrates a linear Li+ battery charger with an internal power MOSFET, a high efficiency 350mA DC/DC converter, eight low dropout linear regulators, a reset output, and two N-Channel open drain switches, and an I²C Serial Interface to achieve flexibility for programming LDO outputs and individual on/off control.

The charger is a complete, thermally-regulated, stand-alone single-cell linear Li+ battery charger that incorporates an internal power MOSFET for constant-current/constant-voltage control. The charger includes a variety of value-added features, and it is programmable via the I²C-Interface to control charging current, termination voltage, along with safety features and operation modes.

The ACT5830 is available in a compact 5mm x 5mm 40-pin Thin-QFN package that is just 0.75mm thin.

SYSTEM BLOCK DIAGRAM



Pb-free

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TABLE OF CONTENTS

GENERAL INFORMATION ..... P. 01
Functional Block Diagram ..... p. 03
Ordering Information ..... p. 04
Pin Configuration ..... p. 04
Pin Descriptions ..... p. 05
Absolute Maximum Ratings ..... p. 07

SYSTEM MANAGEMENT ..... P. 08
Electrical Characteristics ..... p. 08
I^2C Interface Electrical Characteristics ..... p. 09
System Management Register Descriptions ..... p. 10
Functional Descriptions ..... p. 11

STEP-DOWN DC/DC CONVERTER ..... P. 13
Electrical Characteristics ..... p. 13
Register Descriptions ..... p. 14
Typical Performance Characteristics ..... p. 16
Functional Description ..... p. 17

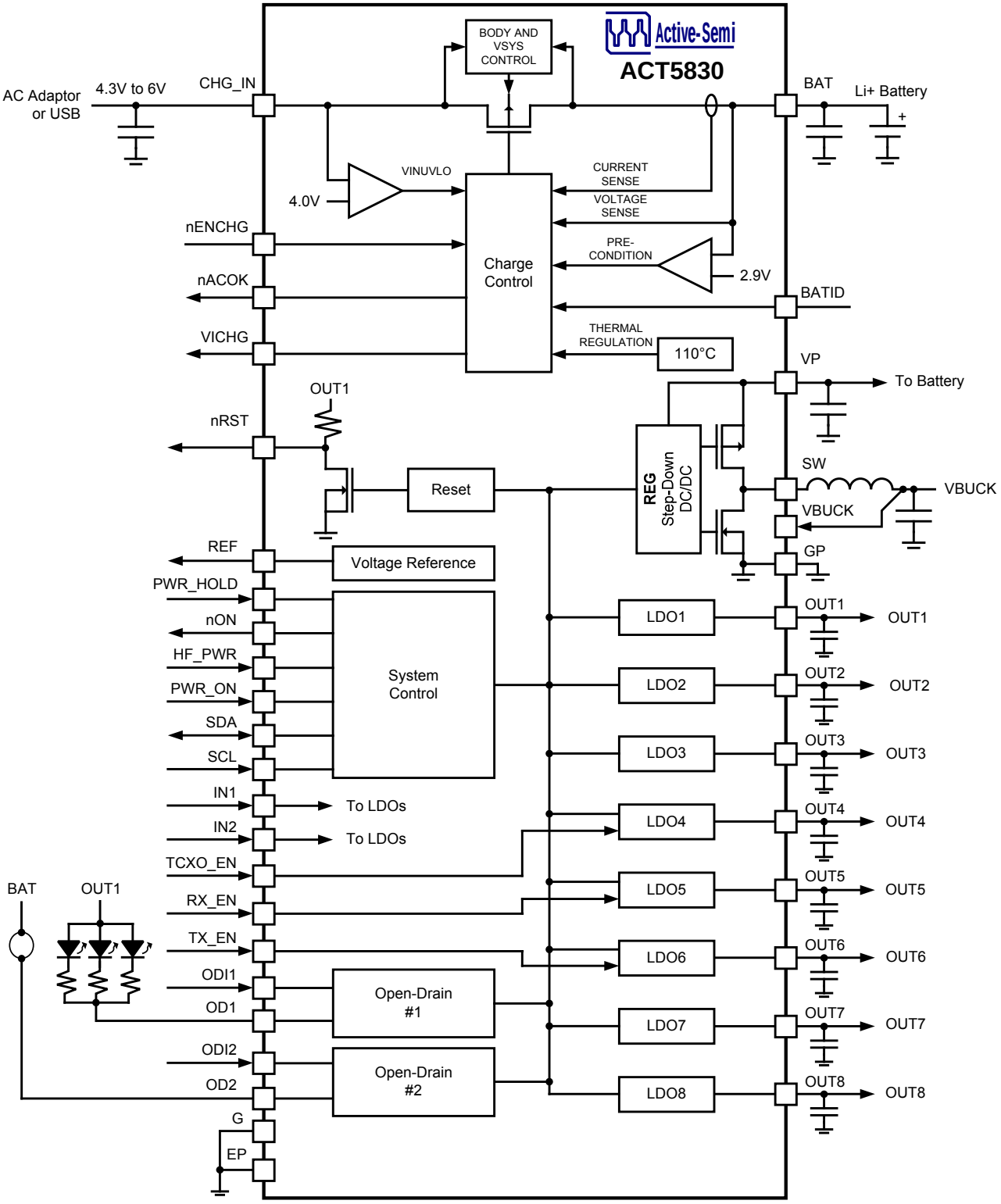
LOW-DROPOUT LINEAR REGULATORS ..... P. 19
Register Descriptions ..... p. 19
Typical Performance Characteristics ..... p. 23
Functional Description ..... p. 24
LDO1 ..... p. 25
LDO2 ..... p. 26
LDO3 ..... p. 27
LDO4 ..... p. 28
LDO5 ..... p. 29
LDO6 ..... p. 30
LDO7 ..... p. 31
LDO8 ..... p. 32

SINGLE-CELL Li+ BATTERY CHARGER (CHGR) ..... P. 33
Electrical Characteristics ..... p. 33
Li+ Battery Charger Register Descriptions ..... p. 35
Typical Performance Characteristics ..... p. 37
Functional Description ..... p. 38

PACKAGE INFORMATION ..... P. 41

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FUNCTIONAL BLOCK DIAGRAM



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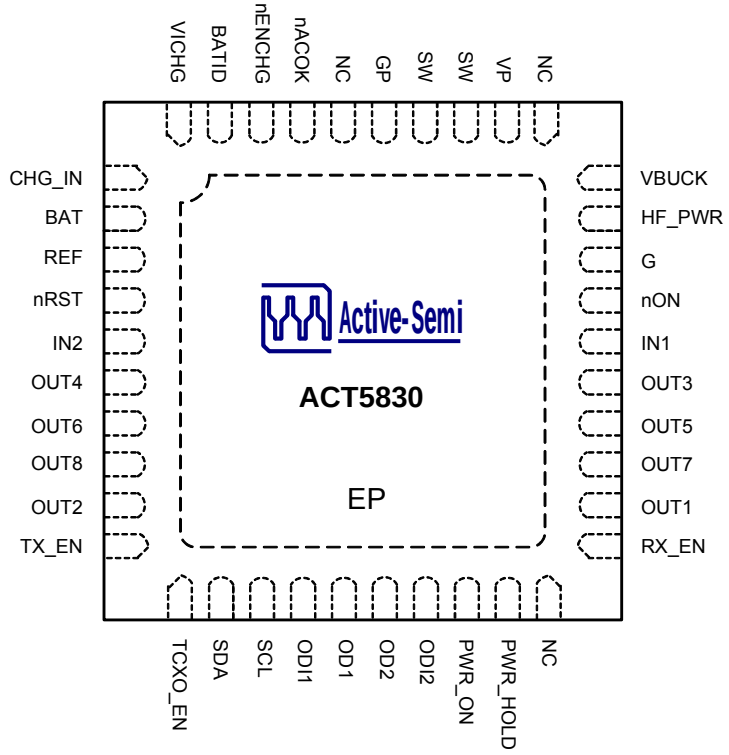
ORDERING INFORMATION①②

PART NUMBER	V_{BUCK}	V_{LDO1}	V_{LDO2}	V_{LDO3}	V_{LDO4}	V_{LDO5}	V_{LDO6}	V_{LDO7}	V_{LDO8}	$I_{CHARGER}$	PACKAGE	PINS	TEMPERATURE RANGE
ACT5830QJ1CF-T	1.2V	3.0V	1.8V	3.0V	3.0V	3.0V	3.0V	1.8V	3.3V	0.45A	TQFN55-40	40	-40°C to +85°C
ACT5830QJ182-T	1.2V	3.0V	1.8V	3.0V	3.0V	2.85V	2.85V	1.8V	1.5V	0.45A	TQFN55-40	40	-40°C to +85°C

①: Output voltage options detailed in this table represent standard voltage options, and are available for samples or production orders. Additional output voltage options, as detailed in the *Output Voltage Codes* table, are available for production subject to minimum order quantities. Contact Active-Semi for more information regarding semi-custom output voltage combinations.

②: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

PIN CONFIGURATION



5×5mm QFN (TQFN55-40)

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PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CHG_IN	Battery Charge Supply Input. Connect a 1µF ceramic capacitor from CHG_IN to G.
2	BAT	Battery Charger Output. Connect this pin directly to the battery anode (+ terminal), and to IN1 and IN2 pins. Bypass with 10µF ceramic capacitor to G.
3	REF	Reference Noise Bypass. Connect a 0.01µF ceramic capacitor from REF to G. This pin is discharged to G in shutdown.
4	nRST	Active Low Reset Output. nRST asserts low for the reset timeout period of 65ms whenever the ACT5830 is first enabled. This output is internally connected to OUT1 via a 15kΩ pull-up resistor.
5	IN2	Input supply to LDO2, LDO4, LDO6, and LDO8. Connect to BAT and IN1.
6	OUT4	LDO4 Output. Capable of delivering up to 100mA of output current. Output is discharged to ground with 1kΩ when disabled.
7	OUT6	LDO6 Output. Capable of delivering up to 150mA of output current. Output is discharged to ground with 1kΩ when disabled.
8	OUT8	LDO8 Output. Capable of delivering up to 250mA of output current. Output is discharged to ground with 1kΩ when disabled.
9	OUT2	LDO2 Output. Capable of delivering up to 300mA of output current. Output is discharged to ground with 1kΩ when disabled.
10	TX_EN	LDO6 Independent On/Off Control. Drive to a logic high for normal operation, and to a logic low to disable.
11	TCXO_EN	LDO4 Independent On/Off Control. Drive to a logic high for normal operation, and to a logic low to disable.
12	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of the clock.
13	SCL	Clock Input for I^2C Serial Interface. Data is read on the rising edge of the clock.
14	ODI1	Digital Control for Open Drain N-channel Switch 1. Drive to a logic high to turn on the switch. Drive to a logic low to turn off the switch.
15	OD1	N-channel Open–Drain Output 1. State of output controlled by ODI1.
16	OD2	N-channel Open–Drain Output 2. State of output controlled by ODI2.
17	ODI2	Digital Control for Open Drain N-channel Switch 2. Drive to a logic high to turn on the switch. Drive to a logic low to turn off the switch.
18	PWR_ON	Push Button On/Off Input. Connect a push-button between this pin and BAT. There is an internal 200kΩ pull down resistor to G. See the *System Startup & Shutdown* section for more information.
19	PWR_HOLD	Power Hold Input. Drive PWR_HOLD to a logic high to complete the startup sequence. Drive the pin to a logic low to disable IC. See the *System Startup & Shutdown* section for more information.
20	NC	No Connect. Not internally connected.
21	RX_EN	LDO5 Independent On/Off Control. Drive to a logic high for normal operation, and to a logic low to disable.
22	OUT1	LDO1 Output. Capable of delivering up to 300mA of output current. Output is discharged to ground with 1kΩ when disabled.
23	OUT7	LDO7 Output. Capable of delivering up to 250mA of output current. Output is discharged to ground with 1kΩ when disabled.

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PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
24	OUT5	LDO5 Output. Capable of delivering up to 150mA of output current. Output is discharged to ground with 1kΩ when disabled.
25	OUT3	LDO3 Output. Capable of delivering up to 100mA of output current. Output is discharged to ground with 1kΩ when disabled.
26	IN1	Input Supply to LDO1, LDO3, LDO5, and LDO7. Connect to BAT and IN2.
27	nON	Push-Button Active Low Open Drain Output. When PWR_ON is low, nON is open drain. When PWR_ON is high or when in shutdown, nON is asserted low. This output is internally connected to OUT1 via a 15kΩ pull-up resistor.
28	G	Ground. Connect G and GP together at a single point place as close to the IC as possible.
29	HF_PWR	Hands Free Input. A high level indicates availability of hands free input. This pin is internally pulled down to G via a 200kΩ resistor. Connect to a 0.1µF capacitor to G to achieve TBDkV (typ) ESD protection.
30	VBUCK	Output Feedback Sense for REG. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
31	NC	No Connect. Not internally connected.
32	VP	Power Input for REG. Connect to BAT, IN1, and IN2. Bypass to GP with a high quality ceramic capacitor placed as close as possible to the IC.
33, 34	SW	Switching Node Output for REG. Connect this pin to the switching end of the inductor.
35	GP	Power Ground for REG. Connect G and GP together at a single point place as close to the IC as possible.
36	NC	No Connect. Not internally connected.
37	nACOK	CHG_IN Active Low Status Output. nACOK is asserted low when V_{CHG_IN} > 4.0V.
38	nENCHG	Charge Enable Active Low Input. Drive low or leave floating to enable the charger. Drive high to disable the charger. This pin has an internal 200kΩ pull-down resistor.
39	BATID	Battery ID pin to detect the presence of the battery. When the battery is present, the voltage at this pin is lower than 2V, otherwise, it is higher than 2V.
40	VICHG	Charge Current Monitor. The voltage at this pin is proportional to the charger current, with a gain of 2.47mV/mA. This output becomes high impedance in shutdown.
EP	EP	Exposed Pad. Must be soldered to ground on the PCB.

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ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
CHG_IN to G t < 1ms and duty cycle <1% Steady State	 -0.3 to +7 -0.3 to +6	 V V
IN1, IN2, BAT, BATID, VICHG, SCL, SDA, PWR_HOLD, nRST, PWR_ON, nON, nACOK, nENCHG, TCXO_EN, RX_EN, TX_EN, ODIx, ODx to G	-0.3 to +6	V
VP, SW, VBUCK to GP	-0.3 to +6	V
REF, HF_PWR to G	-0.3 to V_{BAT} + 0.3	
OUT1, OUT3, OUT5, OUT7 to G	-0.3 to V_{IN1} + 0.3	V
OUT2, OUT4, OUT6, OUT8 to G	-0.3 to V_{IN2} + 0.3	V
GP to G	-0.3 to +0.3	V
Junction to Ambient Thermal Resistance (θ_{JA})	30	°C/W
RMS Power Dissipation (T_A = 70°C)②	2.7	W
Operating Junction Temperature (T_J)	-40 to 150	°C
Operating Temperature Range (T_A)	-40 to 85	°C
Store Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

②: Derate 33mW/°C above T_A = 70°C.

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ELECTRICAL CHARACTERISTICS

(V_{BAT} = V_{IN1} = V_{IN2} = 3.6V, T_A = 25°C, unless otherwise specified.)

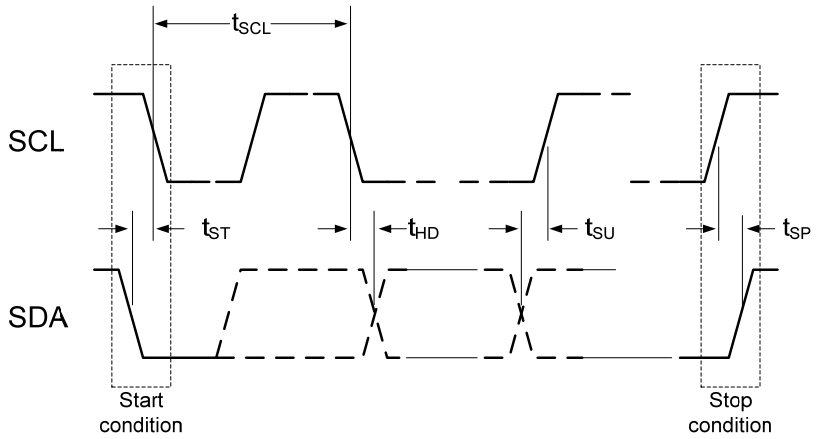
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BAT Operating Voltage Range		2.6		5.5	V
BAT UVLO Threshold	BAT Voltage Rising	2.2	2.35	2.5	V
BAT UVLO Hysteresis	BAT Voltage Falling		80		mV
BAT UVLO Delay	BAT Rising		0.1		ms
	BAT Falling		5		
nRST Delay			65		ms
No Load BAT Supply Current	REG, LDO1, LDO2 and LDO3 Enabled with No Load and CHGR Disabled		0.26	0.5	mA
	REG, All LDOs Enabled and CHGR Disabled.		0.45	0.75	mA
REF Output Voltage		1.24	1.25	1.26	V
Reference PSRR	C_{REF} = 0.01µF, f = 1kHz		75		dB
ODx Output On Resistance	100mA Sink Current		4		Ω
ODx Output Leakage Current	V_{ODx} = V_{BAT}			10	µA
Logic High Input Voltage		1.4			V
Logic Low Input Voltage				0.4	V
Logic Low Output Voltage	nON, nRST, I_{SINK} = 5mA			0.3	V
Logic Leakage Current	V_{nON} = V_{nRST} = V_{CHG_IN} = 4.2V			1	µA
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis	Temperature falling		20		°C

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I²C INTERFACE ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Low Input Voltage				0.4	V
SCL, SDA High Input Voltage		1.4			V
SCL, SDA Leakage Current	V_{CHG_IN} = 4.2V			1	µA
SDA Low Output Voltage	I_{OL} = 5mA			0.3	V
SCL Clock Period, t_{SCL}	f_{SCL} clock freq = 400kHz	2.5			µs
SDA Data In Setup Time to SCL High, t_{SU}		100			ns
SDA Data Out Hold Time after SCL Low, t_{HD}		300			ns
SDA Data Low Setup Time to SCL Low, t_{ST}	Start Condition	100			ns
SDA Data High Hold Time after Clock High, t_{SP}	Stop Condition	100			ns

Figure 1:
I²C Serial Bus Timing



Note: Each session of data transfer is with a start condition, a 7-bits slave address plus a bit to instruct for read or write followed by an acknowledge bit, a register address byte followed by an acknowledge bit, a data byte followed by an acknowledge bit and a stop condition. The device address, the register address and the data are all MSB first transferred. Each bit volume is prepared in during the SCL is low, is latched-in by the rising edge of the SCL. The data byte is accepted and is put effective by the time that the last bit volume is latched-in.

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SYSTEM MANAGEMENT REGISTER DESCRIPTIONS

Table 1:
Global Register Map

OUTPUT	ADDRESS									DATA (DEFAULT VALUES)							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
CHGR	08h	0	0	0	0	1	0	0	0	0	0	0	0	R	V	V	V
CHGR	09h	0	0	0	0	1	0	0	1	0	0	R	R	R	R	R	R
CHGR	0Ah	0	0	0	0	1	0	1	0	R	R	R	R	R	R	R	R
CHGR	0Bh	0	0	0	0	1	0	1	1	R	R	R	R	R	R	R	0
LDO3	0Ch	0	0	0	0	1	1	0	0	1	R	0	V	V	V	V	V
LDO5	0Dh	0	0	0	0	1	1	0	1	1	R	0	V	V	V	V	V
LDO7	07h	0	0	0	0	0	1	1	1	R	V	V	V	V	V	V	V
LDO7	0Eh	0	0	0	0	1	1	1	0	1	R	1	R	R	R	R	R
LDO1	0Fh	0	0	0	0	1	1	1	1	1	R	1	V	V	V	V	V
LDO4	10h	0	0	0	1	0	0	0	0	1	R	0	V	V	V	V	V
LDO6	11h	0	0	0	1	0	0	0	1	1	R	0	V	V	V	V	V
LDO8	12h	0	0	0	1	0	0	1	0	1	R	1	V	V	V	V	V
LDO2	13h	0	0	0	1	0	0	1	1	1	R	0	V	V	V	V	V
REG	14h	0	0	0	1	0	1	0	0	R	V	V	V	V	V	V	V
REG	15h	0	0	0	1	0	1	0	1	R	R	R	R	R	R	R	0
REG	16h	0	0	0	1	0	1	1	0	R	R	R	R	R	R	R	R
REG	17h	0	0	0	1	0	1	1	1	R	R	R	R	R	R	R	1

KEY:

R: Read-Only bit. No Default Assigned.

V: Default Values Depend on Voltage Option. Default Values May Vary.

Note: Addresses other than those specified in Table 1 may be used for factory settings. Do not access any registers other than those specified in Table 1.

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FUNCTIONAL DESCRIPTIONS

The ACT5830 offers a wide array of system management functions that allow it to be configured for optimal performance in a wide range of applications.

I²C Serial Interface

At the core of the ACT5830's flexible architecture is an I^2C interface that permits optional programming capability to enhance overall system performance. Use standard I^2C write-byte commands to program the ACT5830 and read-byte commands to read the IC's status. Figure 1: I^2C Serial Bus Timing provides a standard timing diagram for the I^2C protocol. The ACT5830 always operates as a slave device, with address 1010101.

System Startup & Shutdown

The ACT5830 features a flexible enable architecture that allows it to support a variety of push-button enable/disable schemes. Although other startup routines are possible, a typical startup and shutdown process would proceed as follows (referring to Figure 2):

System startup is initiated whenever one of the following conditions occurs:

1) The user presses the push-button, asserting PWR_ON high,
2) A valid supply (>4V) is connected to the charger input (CHG_IN), or
3) A headset is connected, asserting HF_PWR high.

The ACT5830QJ1CF begins its system startup procedure by enabling REG, LDO7 and LDO8, then LDO1 are enabled when VBUCK reaches 87% of its final value; The ACT5830QJ182 begins its system startup procedure by enabling REG, LDO1, LDO7 and LDO8. nRST is asserted low when VOUT1 reaches 87% of its final value, holding the microprocessor in reset for a user-selectable reset period of 65ms. If VBUCK and VOUT1 are within 13% of their regulation voltages when the reset timer expires, the ACT5830 de-asserts nRST so that the microprocessor can begin its power up sequence. Once the power-up routine is successfully completed, the microprocessor asserts PWR_HOLD high to keep the ACT5830 enabled after the push-button is released by the user.

Once the power-up routine is completed, the remaining LDOs can be enabled/disabled via either the I^2C interface or the TCXO_EN (LDO4), RX_EN (LDO5), TX_EN (LDO6), and PWR_HOLD (REG and LDO1) pins.

This start-up procedure requires that the push-button be held until the microprocessor assumes control of PWR_HOLD, providing protection against inadvertent momentary assertions of the push-button. If desired, longer "push-and-hold" times can be easily implemented by simply adding an additional delay before assuming control of PWR_HOLD. If the microprocessor is unable to complete its power-up routine successfully before the user lets go of the push-button, the ACT5830 will automatically shut itself down.

Once a successful power-up routine is completed, the user can initiate a shutdown process by pressing the push-button a second time. Upon detecting a second assertion of PWR_ON (by depressing the push-button), the ACT5830 asserts nON to interrupt the microprocessor which initiates an interrupt service routine that will reveal that the user pressed the push-button. If HF_PWR and CHG_OK are both low, the microprocessor then initiates a power-down routine, the final step of which will be to de-assert PWR_HOLD, disabling REG and LDO1.

Open Drain Outputs

The ACT5830 includes two n-channel open drain outputs (OD1 and OD2) that can be used for driving external loads such as WLEDs or a vibrator motor, as shown in the functional diagram. Each of the OD outputs is enabled when either it's respective ODIx pin in driven to a logic high.

nACOK Output

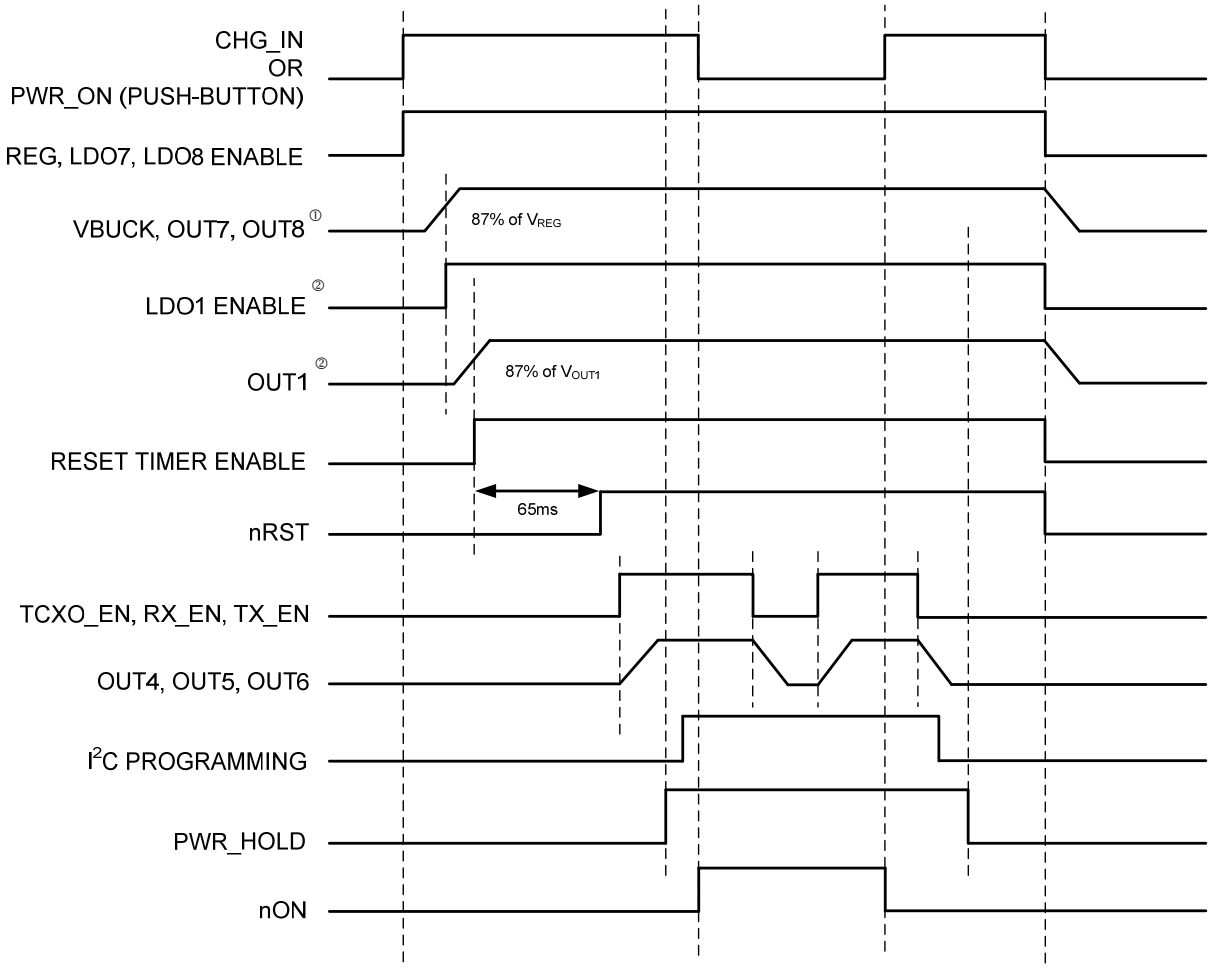
The ACT5830's nACOK output provides a logic-level indication of the status of the voltage at CHG_IN. nACOK is an open-drain output which sinks current whenever V_{CHG_IN} > 4V.

Thermal Overload Protection

The ACT5830 integrates thermal overload protection circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions, for example. This circuitry disables all regulators if the ACT5830 die temperature exceeds 160°C, and prevents the regulators from being enabled until the die temperature drops by 20°C (typ), after which a normal startup routine may commence.

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Figure 2:
Startup and Shutdown Sequence



①: Also the OUT1 for the ACT5830QJ182-T.
②: Apply to the ACT5830QJ1CF only.

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ELECTRICAL CHARACTERISTICS

(V_{VP} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP Operating Voltage Range		3.1		5.5	V
VP UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP UVLO Hysteresis	Input Voltage Falling		80		mV
Standby Supply Current			110	200	µA
Shutdown Supply Current	REG/ON[ ] = [0], V_{VP} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM} < 1.3V, I_{OUT} = 10mA	-2.4%	V_{NOM} ①	+1.8%	V
	V_{NOM} ≥ 1.3V, I_{OUT} = 10mA	-1.2%	V_{NOM}	+1.8%	
Line Regulation	V_{VP} = Max(V_{NOM} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT} = 10mA to 350mA		0.0017		%/mA
Current Limit		0.45	0.6		A
Oscillator Frequency	V_{REG} ≥ 20% of V_{NOM}	1.35	1.6	1.85	MHz
	V_{REG} = 0V		530		kHz
PMOS On-Resistance	I_{SW} = -100mA		0.45	0.75	Ω
NMOS On-Resistance	I_{SW} = 100mA		0.3	0.5	Ω
SW Leakage Current	V_{VP} = 5.5V, V_{SW} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM}
Minimum On-Time			70		ns

①: V_{NOM} refers to the nominal output voltage level for V_{REG} as defined by the *Ordering Information* section.

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REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 2:

Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
14h	R	VRANGE	VSET					
15h	R	R	R	R	R	R	R	MODE
16h	R	R	R	R	R	R	R	R
17h	R	R	R	R	R	R	OK	ON

R: Read-Only bits. Default Values May Vary.

Table 3:

Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
14h	VSET	[5:0]	R/W	REG Output Voltage Selection	See Table 4	
14h	VRANGE	[6]	R/W	REG Voltage Range Selection	0	Min V_{OUT} = 1.1V
					1	Min V_{OUT} = 1.25V
14h		[7]	R		READ ONLY	
15h	MODE	[0]	R/W	Mode Selection	0	PWM/PFM
					1	Forced PWM
15h		[7:1]	R		READ ONLY	
16h		[7:0]	R		READ ONLY	
17h	ON	[0]	R/W	REG Enable	0	REG Disable
					1	REG Enable
17h	OK	[1]	R	REG Power-OK	0	Output is not OK
					1	Output is OK
17h		[2]	R		READ ONLY	
17h		[7:3]	R		READ ONLY	

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REGISTER DESCRIPTIONS CONT'D

Table 4:

REG/VSET[ ] Output Voltage Setting

REG/VSET [3:0]	REG/VSET[5:4]							
	REG/VRANGE[ ] = [0]				REG/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	N/A	N/A	1.455	1.860	1.250	2.050	2.850	3.650
0001	N/A	N/A	1.480	1.890	1.300	2.100	2.900	3.700
0010	N/A	1.100	1.505	1.915	1.350	2.150	2.950	3.750
0011	N/A	1.125	1.530	1.940	1.400	2.200	3.000	3.800
0100	N/A	1.150	1.555	1.965	1.450	2.250	3.050	3.850
0101	N/A	1.175	1.585	1.990	1.500	2.300	3.100	3.900
0110	N/A	1.200	1.610	2.015	1.550	2.350	3.150	3.950
0111	N/A	1.225	1.635	2.040	1.600	2.400	3.200	4.000
1000	N/A	1.255	1.660	2.065	1.650	2.450	3.250	4.050
1001	N/A	1.280	1.685	2.090	1.700	2.500	3.300	4.100
1010	N/A	1.305	1.710	2.115	1.750	2.550	3.350	4.150
1011	N/A	1.330	1.735	2.140	1.800	2.600	3.400	4.200
1100	N/A	1.355	1.760	2.165	1.850	2.650	3.450	4.250
1101	N/A	1.380	1.785	2.190	1.900	2.700	3.500	4.300
1110	N/A	1.405	1.810	2.200	1.950	2.750	3.550	4.350
1111	N/A	1.430	1.835	2.245	2.000	2.800	3.600	4.400

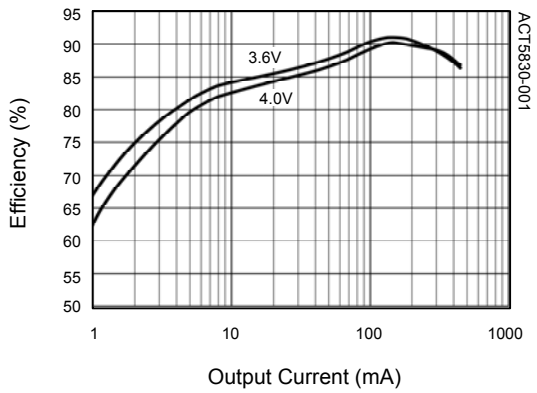
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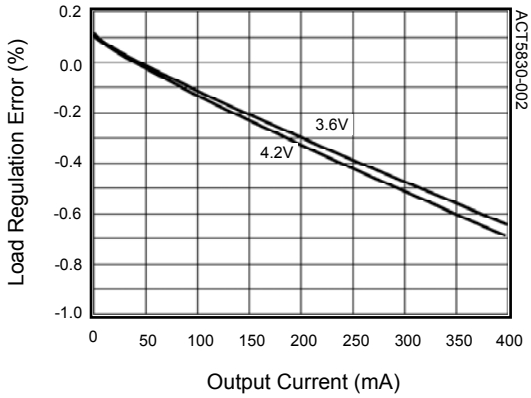
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{INx} = 3.6V, C_{OUTx} = 1µF, T_A = 25°C unless otherwise specified.)

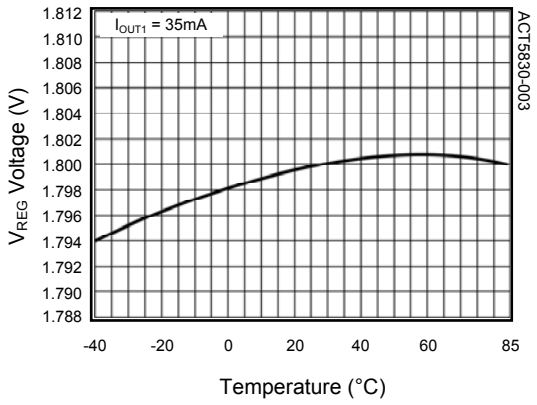
REG Efficiency vs. Load



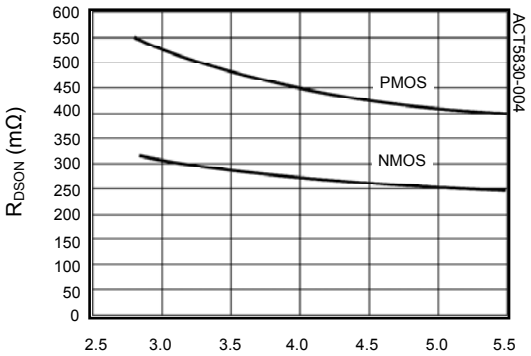
REG Load Regulation



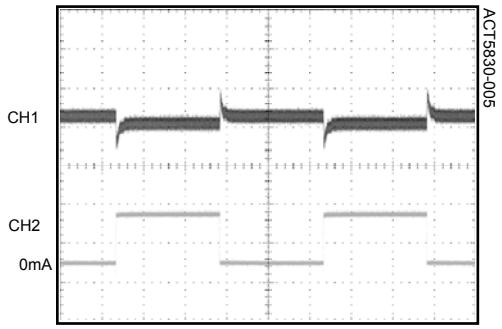
REG Output Voltage vs. Temperature



REG MOSFET Resistance



REG Load Transient Response



CH1: V_{OUT1}, 50mV/div (AC Coupled)
CH2: I_{OUT1}, 200mA/div
TIME: 200µs/div

REG Load Transient Response



CH1: V_{OUT1}, 50mV/div (AC Coupled)
CH2: I_{OUT1}, 200mA/div
TIME: 200µs/div

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FUNCTIONAL DESCRIPTIONS

General Description

REG is a fixed-frequency, current-mode, synchronous PWM step-down converters that achieves a peak efficiency of up to 97%. REG is capable of supplying up to 350mA of output current and operates with a fixed frequency of 1.6MHz, minimizing noise in sensitive applications and allowing the use of small external components. REG is available with a variety of standard and custom output voltages, and may be software-controlled via the I^2C interface by systems that require advanced power management functions.

100% Duty Cycle Operation

REG is capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery-powered applications.

Synchronous Rectification

REG features an integrated n-channel synchronous rectifier, which maximizes efficiency and minimizes the total solution size and cost by eliminating the need for an external rectifier.

Enabling and Disabling REG

Enable/disable functionality is typically implemented as part of a controlled enable/disable scheme utilizing nMSTR and other system control features of the ACT5830. REG is automatically enabled whenever either of the following conditions are met:

1) HF_PWR is asserted high, or
2) PWR_ON is asserted high, or
3) PWR_HOLD is asserted high.

When none of these conditions are true, or if REG/ON[ ] bit is set to [0], REG is disabled, and its quiescent supply current drops to less than 1µA.

Programming the Output Voltage

By default, REG powers up and regulates to its default output voltage. Once the system is enabled, REG's output voltage may be programmed to a different value, typically in order to reduce the power consumption of a microprocessor in standby mode. Program the output voltage via the I^2C serial interface by writing to the REG/VSET[ ] register.

Programmable Operating Mode

By default, REG operates in fixed-frequency PWM mode at medium to heavy loads, then transitions to a proprietary power-saving mode at light loads in order to save power. In applications where low noise is critical, force fixed-frequency PWM operation across the entire load current range, at the expense of light-load efficiency, by setting the REG/MODE[ ] bit to [1].

Power-OK

REG features a power-OK status bit that can be read by the system microprocessor. If the output voltage is lower than the power-OK threshold, typically 6% below the programmed regulation voltage, REG/OK[ ] will clear to 0.

Soft-Start

REG includes internal soft-start circuitry, and enabled its output voltage tracks an internal 80µs soft-start ramp so that it powers up in a monotonic manner that is independent of loading.

Compensation

REG utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. No compensation design is required, simply follow a few simple guidelines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 2.2µF ceramic input capacitor is recommended for most applications.

Output Capacitor Selection

For most applications, a 10µF ceramic output capacitor is recommended. Although REG was designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR, low-ESR tantalum capacitors can provide acceptable results as well.

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FUNCTIONAL DESCRIPTIONS CONT'D

Inductor Selection

REG utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. REG was optimized for operation with a 3.3µH inductor, although inductors in the 2.2µH to 4.7µH range can be used. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current of the application by at least 30%.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Step-down DC/DC exhibits discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of vias if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple vias. The output node should be connected to the VBUCK pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple vias to achieve low electrical and thermal resistance.

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REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 5:

LDO Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
07h	R	VRANGE7	VSET7					
0Fh	DIS1	OK1	ON1	VSET1				
13h	DIS2	OK2	ON2	VSET2				
0Eh	DIS7	OK7	ON7	R	R	R	R	R
12h	DIS8	OK8	ON8	VSET8				
0Ch	DIS3	OK3	ON3	VSET3				
10h	DIS4	OK4	ON4	VSET4				
0Dh	DIS5	OK5	ON5	VSET5				
11h	DIS6	OK6	ON6	VSET6				

Table 6:

LDO Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
07h	VSET7	[5:0]	R/W	LDO7 Output Voltage Selection	See Table 8	
07h	VRANGE7	[6]	R/W	REG Voltage Range Selection	0	Min V_{OUT} = 0.645V
					1	Min V_{OUT} = 1.25V
07h		[7]	R		READ ONLY	
0Fh	VSET1	[4:0]	R/W	LDO1 Output Voltage Selection	See Table 7	
0Fh	ON1	[5]	R/W	LDO1 Enable	0	LDO1 Disable
					1	LDO1 Enable
0Fh	OK1	[6]	R	LDO1 Power-OK	0	Output Out of Regulation
					1	Output In Regulation
0Fh	DIS1	[7]	R/W	LDO1 Output Discharge Enable	0	Output High-Z In Shutdown
					1	Output Discharge Enabled
13h	VSET2	[4:0]	R/W	LDO2 Output Voltage Selection	See Table 7	
13h	ON2	[5]	R/W	LDO2 Enable	0	LDO2 Disable
					1	LDO2 Enable
13h	OK2	[6]	R	LDO2 Power-OK	0	Output Out of Regulation
					1	Output In Regulation
13h	DIS2	[7]	R/W	LDO2 Output Discharge Enable	0	Output High-Z In Shutdown
					1	Output Discharge Enabled
12h	VSET8	[4:0]	R/W	LDO8 Output Voltage Selection	See Table 7	

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REGISTER DESCRIPTIONS CONT'D

Table 6:

LDO Control Register Bit Descriptions (Cont'd)

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
12h	ON8	[5]	R/W	LDO8 Enable	0	LDO8 Disable
					1	LDO8 Enable
12h	OK8	[6]	R	LDO8 Power-OK	0	Output Out of Regulation
					1	Output In Regulation
12h	DIS3	[7]	R/W	LDO8 Output Discharge Enable	0	Output High-Z In Shutdown
					1	Output Discharge Enabled
0Ch	VSET3	[4:0]	R/W	LDO3 Output Voltage Selection	See Table 7	
0Ch	ON3	[5]	R/W	LDO3 Enable	0	LDO3 Disable
					1	LDO3 Enable
0Ch	OK3	[6]	R	LDO3 Power-Ok	0	Output Out of Regulation
					1	Output In Regulation
0Ch	DIS3	[7]	R/W	LDO3 Output Discharge Enable	0	Output High-Z In Shutdown
					1	Output Discharge Enabled
10h	VSET4	[4:0]	R/W	LDO4 Output Voltage Selection	See Table 7	
10h	ON4	[5]	R/W	LDO4 Enable	0	LDO4 Disable
					1	LDO4 Enable
10h	OK4	[6]	R	LDO4 Power-OK	0	Output Out of Regulation
					1	Output In Regulation
10h	DIS4	[7]	R/W	LDO4 Output Discharge Enable	0	Output High-Z In Shutdown
					1	Output Discharge Enabled
0Dh	VSET5	[4:0]	R/W	LDO5 Output Voltage Selection	See Table 7	
0Dh	ON5	[5]	R/W	LDO5 Enable	0	LDO5 Disable
					1	LDO5 Enable
0Dh	OK5	[6]	R	LDO5 Power-OK	0	Output Out of Regulation
					1	Output In Regulation
0Dh	DIS5	[7]	R/W	LDO5 Output Discharge Enable	0	Output High-Z In Shutdown
					1	Output Discharge Enabled
11h	VSET6	[4:0]	R/W	LDO6 Output Voltage Selection	See Table 7	
11h	ON6	[5]	R/W	LDO6 Enable	0	LDO6 Disable
					1	LDO6 Enable

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REGISTER DESCRIPTIONS CONT'D

Table 6:

LDO Control Register Bit Descriptions (Cont'd)

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
11h	OK6	[6]	R	LDO6 Power-OK	0	Output Out of Regulation
					1	Output In Regulation
11h	DIS6	[7]	R/W	LDO6 Output Discharge Enable	0	Output High-Z In Shutdown
					1	Output Discharge Enabled
0Eh		[4:0]	R		READ ONLY	
0Eh	ON7	[5]	R/W	LDO7 Enable	0	LDO7 Disable
					1	LDO7 Enable
0Eh	OK7	[6]	R	LDO7 Power-OK	0	Output Out of Regulation
					1	Output In Regulation
0Eh	DIS7	[7]	R/W	LDO7 Output Discharge Enable	0	Output High-Z In Shutdown
					1	Output Discharge Enabled

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REGISTER DESCRIPTIONS CONT'D

Table 7:
LDO1234568/VSET[ ] Output Voltage Settings

LDOx/VSETx[2:0]	LDOx/VSETx[4:3]			
	00	01	10	11
000	1.4	2.15	2.55	3.0
001	1.5	2.20	2.60	3.1
010	1.6	2.25	2.65	3.2
011	1.7	2.30	2.70	3.3
100	1.8	2.35	2.75	3.4
101	1.9	2.40	2.80	3.5
110	2.0	2.45	2.85	3.6
111	2.1	2.50	2.90	3.7

Table 8:
LDO7/VSET[ ] Output Voltage Settings

LDO7/VSET [3:0]	LDO7/VSET[5:4]							
	LDO7/VRANGE[ ] = [0]				LDO7/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	0.645	1.050	1.455	1.860	1.250	2.050	2.850	3.650
0001	0.670	1.075	1.480	1.890	1.300	2.100	2.900	3.700
0010	0.695	1.100	1.505	1.915	1.350	2.150	2.950	N/A
0011	0.720	1.125	1.530	1.940	1.400	2.200	3.000	N/A
0100	0.745	1.150	1.555	1.965	1.450	2.250	3.050	N/A
0101	0.770	1.175	1.585	1.990	1.500	2.300	3.100	N/A
0110	0.795	1.200	1.610	2.015	1.550	2.350	3.150	N/A
0111	0.820	1.225	1.635	2.040	1.600	2.400	3.200	N/A
1000	0.845	1.255	1.660	2.065	1.650	2.450	3.250	N/A
1001	0.870	1.280	1.685	2.090	1.700	2.500	3.300	N/A
1010	0.895	1.305	1.710	2.115	1.750	2.550	3.350	N/A
1011	0.920	1.330	1.735	2.140	1.800	2.600	3.400	N/A
1100	0.950	1.355	1.760	2.165	1.850	2.650	3.450	N/A
1101	0.975	1.380	1.785	2.190	1.900	2.700	3.500	N/A
1110	1.000	1.405	1.810	2.200	1.950	2.750	3.550	N/A
1111	1.025	1.430	1.835	2.245	2.000	2.800	3.600	N/A

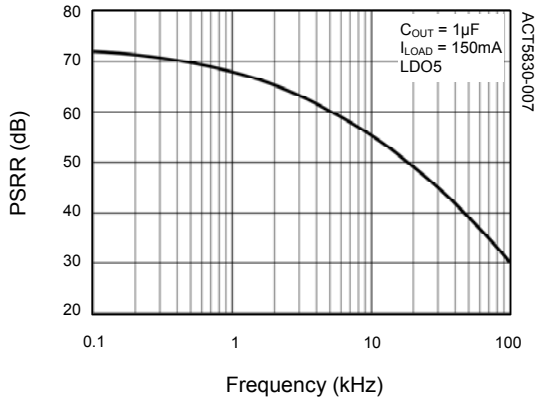
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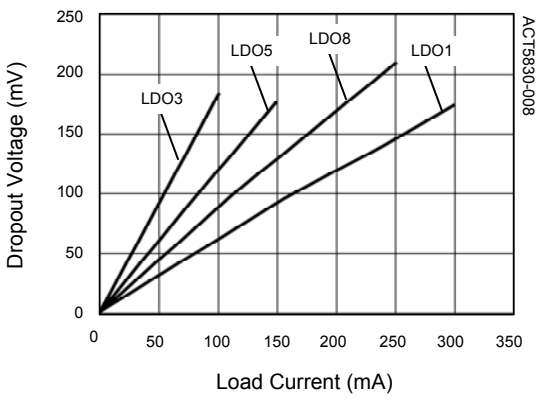
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{INx} = 3.6V, C_{OUTx} = 1µF, T_A = 25°C unless otherwise specified.)

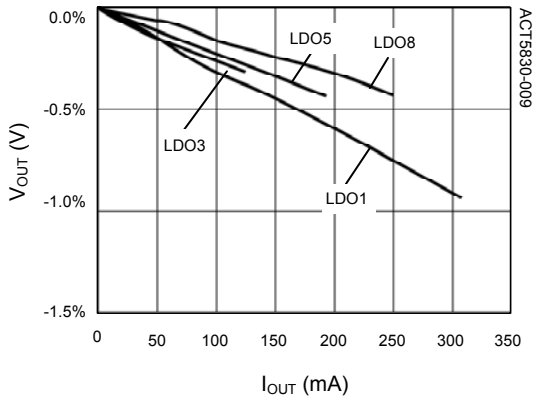
Power Supply Rejection Ratio



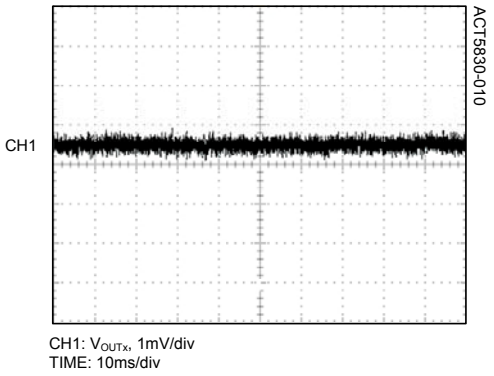
Dropout Voltage vs. Load Current



LDO Load Regulation



LDO Output Voltage Noise



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FUNCTIONAL DESCRIPTIONS

General Description

The ACT5830 features eight high performance, low-dropout, low-noise and low quiescent current LDOs with high PSRR.

Programming Output Voltages (VSET)

All LDOs feature independently-programmable output voltages that are set via the I^2C serial interface, increasing the ACT5830 flexibility while reducing total solution size and cost.

Set the output voltage by writing to the LDOx/VSET[ ] register. See Table 7: LDO1234568/VSET[4:0] and Table 8: LDO7/VSET[ ] Output Voltage Settings for a detailed description of voltage programming options.

Enabling and Disabling LDOs

For information regarding enabling and disabling the LDOs during the startup and shutdown sequence section. Once the startup routine is completed the remaining LDOs can be enabled/disabled via either the I^2C interface or the TCXO_EN (LDO4), RX_EN (LDO5), TX_EN (LDO6), and PWR_HOLD (LDO1, LDO2, LDO3, LDO7, and LDO8).

Reference Bypass Pin

The ACT5830 contains a conference bypass pin which filters noise from the reference, providing a low-noise voltage reference to the LDOs. Bypass REF to G with a 0.01µF ceramic capacitor.

Compensation and Stability

The LDOs need an output capacitor for stability. This capacitor should be connected directly between the output and G pin, as close to the output as possible, and with a short, direct connection to maximize device's performance. To ensure best performance for the device, the output capacitor should have a minimum capacitance of 1µF, and ESR value between 10mΩ and 500mΩ. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

See the *Capacitor Selection* section for more information.

Capacitor Selection

The input capacitor reduces peak currents and noise at the voltage source. Connect a low ESR bulk capacitor (>1µF suggested) to the input. Select this bulk capacitor to meet the input ripple requirements and voltage rating, rather than capacitor size.

PCB Layout Considerations

The ACT5830's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance.

A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW nodes of the DC/DC.

REF is a filtered reference noise, and internally has a direct connection to the linear regulator controller. Any noise injected onto REF will directly affect the outputs of the linear regulators, and therefore special care should be taken to ensure that no noise is injected to the outputs via REF. As with the LDO output capacitors, the REF by pass capacitor should be placed as close to the IC as possible, with short, direct connections to the star-ground. Avoid the use of vias whenever possible. Noisy nodes, such as from the DC/DC, should be routed as far away from REF as possible.

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ELECTRICAL CHARACTERISTICS

(V_{IN1} = 3.6V, C_{OUT1} = 1μF, T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		3.1		5.5	V
Input Under Voltage Lockout	V_{IN1} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{IN1} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	0	2	%
	T_A = -40°C to 85°C	-2.5	0	3	
Line Regulation Error	V_{IN1} = Max (V_{NOM}① + 0.5V, 3.1V) to 5.5V		0		mV/V
Load Regulation Error	I_{OUT1} = 1mA to 300mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT1} = 300mA, C_{OUT1} = 1μF		60		dB
	f = 10kHz, I_{OUT1} = 300mA, C_{OUT1} = 1μF		50		
Supply Current per Output	LDO1 Enabled		20		μA
	LDO1 Disabled		0		
Dropout Voltage②	I_{OUT1} = 150mA		100	200	mV
Output Current				300	mA
Current Limit	V_{OUT1} = 95% of Regulation Voltage	330	580		mA
Current Limit Short Circuit Fold-back	V_{OUT1} = 0V		0.45 x I_{LIM}		
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT1}, Hysteresis = -1%		89		%
Output Noise	C_{OUT1} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT1}		1		20	μF

①: V_{NOM} refers to the nominal output voltage level for LDO1 as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the different voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

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ELECTRICAL CHARACTERISTICS

(V_{IN2} = 3.6V, C_{OUT2} = 1μF, T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		3.1		5.5	V
Input Under Voltage Lockout	V_{IN2} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{IN2} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	0	2	%
	T_A = -40°C to 85°C	-2.5	0	3	
Line Regulation Error	V_{IN2} = Max (V_{NOM}① + 0.5V, 3.1V) to 5.5V		0		mV/V
Load Regulation Error	I_{OUT2} = 1mA to 300mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT2} = 300mA, C_{OUT2} = 1μF		60		dB
	f = 10kHz, I_{OUT2} = 300mA, C_{OUT2} = 1μF		50		
Supply Current per Output	LDO2 Enabled		20		μA
	LDO2 Disabled		0		
Dropout Voltage②	I_{OUT2} = 150mA		100	200	mV
Output Current				300	mA
Current Limit	V_{OUT2} = 95% of Regulation Voltage	330	580		mA
Current Limit Short Circuit Foldback	V_{OUT2} = 0V		0.45 x I_{LIM}		
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT2}, Hysteresis = -1%		89		%
Output Noise	C_{OUT2} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT2}		1		20	μF

①: V_{NOM} refers to the nominal output voltage level for LDO2 as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the different voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

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ELECTRICAL CHARACTERISTICS

(V_{IN1} = 3.6V, C_{OUT3} = 1μF, T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		3.1		5.5	V
Input Under Voltage Lockout	V_{IN1} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{IN1} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	0	2	%
	T_A = -40°C to 85°C	-2.5	0	3	
Line Regulation Error	V_{IN3} = Max (V_{NOM}① + 0.5V, 3.1V) to 5.5V		0		mV/V
Load Regulation Error	I_{OUT3} = 1mA to 100mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT3} = 100mA, C_{OUT3} = 1μF		60		dB
	f = 10kHz, I_{OUT3} = 100mA, C_{OUT3} = 1μF		50		
Supply Current per Output	LDO3 Enabled		40		μA
	LDO3 Disabled		0		
Dropout Voltage②	I_{OUT3} = 50mA		100	200	mV
Output Current				100	mA
Current Limit	V_{OUT3} = 95% of Regulation Voltage	115	180		mA
Current Limit Short Circuit Foldback	V_{OUT3} = 0V		0.45 x I_{LIM}		
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT3}, Hysteresis = -1%		89		%
Output Noise	C_{OUT3} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT3}		1		20	μF

①: V_{NOM} refers to the nominal output voltage level for LDO3 as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the different voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

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ELECTRICAL CHARACTERISTICS

(V_{IN2} = 3.6V, C_{OUT4} = 1μF, T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		3.1		5.5	V
Input Under Voltage Lockout	V_{IN2} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{IN2} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	0	2	%
	T_A = -40°C to 85°C	-2.5	0	3	
Line Regulation Error	V_{IN4} = Max (V_{NOM}① + 0.5V, 3.1V) to 5.5V		0		mV/V
Load Regulation Error	I_{OUT4} = 1mA to 100mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT4} = 100mA, C_{OUT4} = 1μF		70		dB
	f = 10kHz, I_{OUT4} = 100mA, C_{OUT4} = 1μF		60		
Supply Current per Output	LDO4 Enabled		40		μA
	LDO4 Disabled		0		
Dropout Voltage②	I_{OUT4} = 50mA		100	200	mV
Output Current				100	mA
Current Limit	V_{OUT4} = 95% of Regulation Voltage	115	180		mA
Current Limit Short Circuit Foldback	V_{OUT4} = 0V		0.45 x I_{LIM}		
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT4}, Hysteresis = -1%		89		%
Output Noise	C_{OUT4} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT4}		1		20	μF

①: V_{NOM} refers to the nominal output voltage level for LDO4 as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the different voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

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ELECTRICAL CHARACTERISTICS

(V_{IN1} = 3.6V, C_{OUT5} = 1μF, T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		3.1		5.5	V
Input Under Voltage Lockout	V_{IN1} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{IN1} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	0	2	%
	T_A = -40°C to 85°C	-2.5	0	3	
Line Regulation Error	V_{IN5} = Max (V_{NOM}① + 0.5V, 3.1V) to 5.5V		0		mV/V
Load Regulation Error	I_{OUT5} = 1mA to 150mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT5} = 150mA, C_{OUT5} = 1μF		70		dB
	f = 10kHz, I_{OUT5} = 150mA, C_{OUT5} = 1μF		60		
Supply Current per Output	LDO5 Enabled		40		μA
	LDO5 Disabled		0		
Dropout Voltage②	I_{OUT5} = 80mA		100	200	mV
Output Current				150	mA
Current Limit	V_{OUT5} = 95% of Regulation Voltage	165	260		mA
Current Limit Short Circuit Foldback	V_{OUT5} = 0V		0.45 x I_{LIM}		
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT5}, Hysteresis = -1%		89		%
Output Noise	C_{OUT5} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT5}		1		20	μF

①: V_{NOM} refers to the nominal output voltage level for LDO5 as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the different voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

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ELECTRICAL CHARACTERISTICS

(V_{IN2} = 3.6V, C_{OUT6} = 1μF, T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		3.1		5.5	V
Input Under Voltage Lockout	V_{IN2} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{IN2} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	0	2	%
	T_A = -40°C to 85°C	-2.5	0	3	
Line Regulation Error	V_{IN6} = Max (V_{NOM}① + 0.5V, 3.1V) to 5.5V		0		mV/V
Load Regulation Error	I_{OUT6} = 1mA to 150mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT6} = 150mA, C_{OUT6} = 1μF		70		dB
	f = 10kHz, I_{OUT6} = 150mA, C_{OUT6} = 1μF		60		
Supply Current per Output	LDO6 Enabled		40		μA
	LDO6 Disabled		0		
Dropout Voltage②	I_{OUT6} = 80mA		100	200	mV
Output Current				150	mA
Current Limit	V_{OUT6} = 95% of Regulation Voltage	165	260		mA
Current Limit Short Circuit Foldback	V_{OUT6} = 0V		0.45 x I_{LIM}		
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT6}, Hysteresis = -1%		89		%
Output Noise	C_{OUT6} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT6}		1		20	μF

①: V_{NOM} refers to the nominal output voltage level for LDO6 as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the different voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

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ELECTRICAL CHARACTERISTICS

(V_{IN1} = 3.6V, C_{OUT7} = 1μF, T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Supply Range			3.1		5.5	V
Input Under Voltage Lockout	V_{IN1} Input Rising		2.9	3	3.1	V
UVLO Hysteresis	V_{IN1} Input Falling			0.1		V
Output Voltage Accuracy	T_A = 25°C	V_{NOM} < 1.3V, I_{OUT} = 10mA	-2.4	0	2	%
		V_{NOM} ≥ 1.3V, I_{OUT} = 10mA	-1.2	0	2	
	T_A = -40°C to 85°C	V_{NOM} < 1.3V, I_{OUT} = 10mA	-5	0	3	
		V_{NOM} ≥ 1.3V, I_{OUT} = 10mA	-2.5	0	3	
Line Regulation Error	V_{IN7} = Max (V_{NOM}① + 0.5V, 3.1V) to 5.5V			0		mV/V
Load Regulation Error	I_{OUT7} = 1mA to 250mA			-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT7} = 250mA, C_{OUT7} = 1μF			60		dB
	f = 10kHz, I_{OUT7} = 250mA, C_{OUT7} = 1μF			50		
Supply Current per Output	LDO7 Enabled			20		μA
	LDO7 Disabled			0		
Dropout Voltage②	I_{OUT7} = 100mA			100	200	mV
Output Current					250	mA
Current Limit	V_{OUT7} = 95% of Regulation Voltage		275	410		mA
Current Limit Short Circuit Foldback	V_{OUT7} = 0V			0.45 x I_{LIM}		
Internal Soft-Start				100		μs
Power Good Flag High Threshold	V_{OUT7}, Hysteresis = -1%			89		%
Output Noise	C_{OUT7} = 10μF, f = 10Hz to 100kHz			40		$μV_{RMS}$
Stable C_{OUT7}			1		20	μF

①: V_{NOM} refers to the nominal output voltage level for LDO7 as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the different voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

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ELECTRICAL CHARACTERISTICS

(V_{IN2} = 3.6V, C_{OUT8} = 1μF, T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		3.1		5.5	V
Input Under Voltage Lockout	V_{IN2} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{IN2} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	0	2	%
	T_A = -40°C to 85°C	-2.5	0	3	
Line Regulation Error	V_{IN8} = Max (V_{NOM}① + 0.5V, 3.1V) to 5.5V		0		mV/V
Load Regulation Error	I_{OUT8} = 1mA to 250mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT8} = 250mA, C_{OUT8} = 1μF		60		dB
	f = 10kHz, I_{OUT8} = 250mA, C_{OUT8} = 1μF		50		
Supply Current per Output	LDO8 Enabled		20		μA
	LDO8 Disabled		0		
Dropout Voltage②	I_{OUT8} = 100mA		100	200	mV
Output Current				250	mA
Current Limit	V_{OUT8} = 95% of Regulation Voltage	275	410		mA
Current Limit Short Circuit Foldback	V_{OUT8} = 0V		0.45 x I_{LIM}		
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT8}, Hysteresis = -1%		89		%
Output Noise	C_{OUT8} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT8}		1		20	μF

①: V_{NOM} refers to the nominal output voltage level for LDO8 as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the different voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

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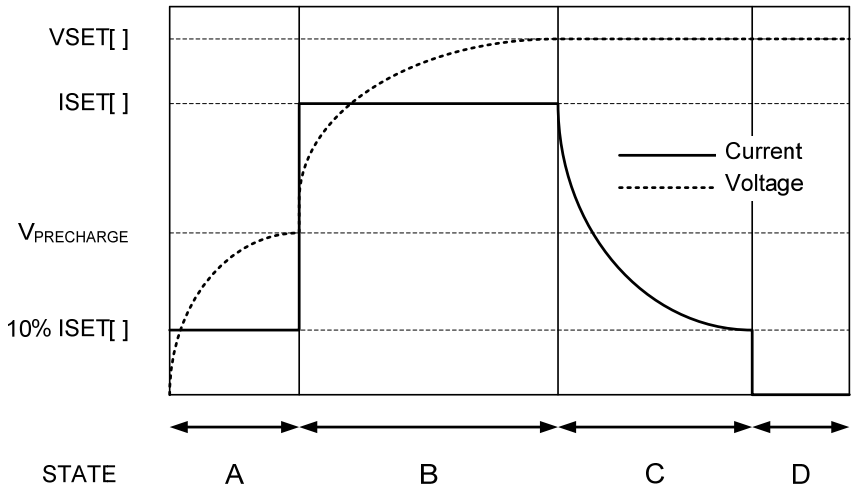
ELECTRICAL CHARACTERISTICS

(V_{CHG_IN} = 5V, V_{BAT} = 3.6V, VSET[ ] = [0101], ISET[ ] = [0101], T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHG_IN Operating Range		4.2		6	V
UVLO Threshold	CHG_IN Voltage Rising	3.75	4	4.25	V
UVLO Hysteresis	CHG_IN Voltage Falling		500		mV
Battery Termination Voltage		4.179	4.200	4.221	V
Line Regulation	V_{CHG_IN} = 4.5V to 5.5V, I_{BAT} = 10mA		0.2		%/V
PMOS On Resistance			0.3	0.5	Ω
Charge Current	V_{BAT} = 3.8V	450	500	550	mA
VICHG Voltage	V_{VICHG} /I_{BAT}		2.3		mV/mA
Precondition Charge Current	V_{BAT} = 2.8V	35	50	65	mA
Precondition Threshold Voltage	V_{BAT} Voltage Rising	2.75	2.9	3.0	V
Precondition Threshold Hysteresis	V_{BAT} Voltage Falling		150		mV
End-of-Charge Current Threshold	V_{BAT} = 4.1V		50		mA
End-of-Charge Qualification Period			32		ms
Charge Restart Threshold	VSET[ ] - V_{BAT}, V_{BAT} Falling		200		mV
BATID High Input Voltage	V_{BATID} Voltage Rising	2.5			V
BATID Low Input Voltage	V_{BATID} Voltage Falling			2	V
BATID Leakage Current	V_{CHG_IN} = 4.5V			1	µA
Thermal Regulation Threshold			105		°C
BAT Reserve Leakage Current	SLEEP, SUSPEND, or TIMER-FAULT state		0.4	5	µA
CHG_IN Supply Current	V_{nENCHG} > 1.4V		65	100	µA
	SLEEP, SUSPEND, or TIMER-FAULT state		200	500	µA
	PRECONDITION, FAST-CHARGE, or TOP-OFF state		0.8	1.2	mA
Precondition Timeout Period	TIMOSET[ ] = [00]		1		hr
	TIMOSET[ ] = [01]		1.43		hr
	TIMOSET[ ] = [10]		2		hr
	TIMOSET[ ] = [11]		INFINITE		
Total Charging Timeout Period	TIMOSET[ ] = [00]		3		hr
	TIMOSET[ ] = [01]		4.3		hr
	TIMOSET[ ] = [10]		6		hr
	TIMOSET[ ] = [11]		INFINITE		

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Figure 3:
Battery Charger Algorithm



A: PRECONDITION State
B: FAST-CHARGE State
C: TOP-OFF State
D: SLEEP State

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Li+ BATTERY CHARGER REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 8:
Battery Charger (CHGR) Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
08h	ISET				R	VSET		
09h	TIMOSET		R	BATFLT	TIMOFLT	R	CHGRSTAT	VINPOK
0Ah	R	R	R	R	R	R	R	R
0Bh	R	R	R	R	R	R	CHGROK	SUSCHG

R: Read-Only bits. Default Values May Vary.

Table 9:
Battery Charger (CHGR) Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
08h	VSET	[2:0]	R/W	Charge Termination Voltage Selection	See Table 11	
08h		[3]	R		READ ONLY	
08h	ISET	[7:4]	R/W	Maximum Charge Current Selection	See Table 10	
09h	VINPOK	[0]	R	Input Supply Power-OK	0	Input Power is not OK
					1	Input Power is OK
09h	CHGRSTAT	[1]	R	Charging Status	0	Not Charging
					1	Charging
09h		[2]	R		READ ONLY	
09h	TIMOFLT	[3]	R	Timeout Fault	0	No Timeout Fault
					1	Timeout Fault
09h	BATFLT	[4]	R	Battery Removed Fault	0	Battery Not Removed
					1	Battery Removed
09h		[5]	R		READ ONLY	
09h	TIMOSET	[7:6]	R/W	Charge Timeout Select	See Table 12	
0Ah		[7:0]	R		READ ONLY	
0Bh	SUSCHG	[0]	R/W	Suspend Charging	0	Charging Enabled
					1	Charging Disabled
0Bh	CHGROK	[1]	R	Charge Status	0	Charging Error Occurred
					1	Charging OK
0Bh		[7:2]	R		READ ONLY	

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Li+ BATTERY CHARGE REGISTER DESCRIPTIONS CONT'D

Table 10:
CHGR Charge Current Settings

CHGR/ISET[3:0]	FAST CHARGE CURRENT SETTINGS (mA)
0000	100
0001	300
0010	350
0011	400
0100	450 (default)
0101	500
0110	550
0111	600
1000	650
1001	700
1010	750
1011	800
1100	850
1101	900
1110	950
1111	1000

Table 11:
Charge Termination Voltage Settings

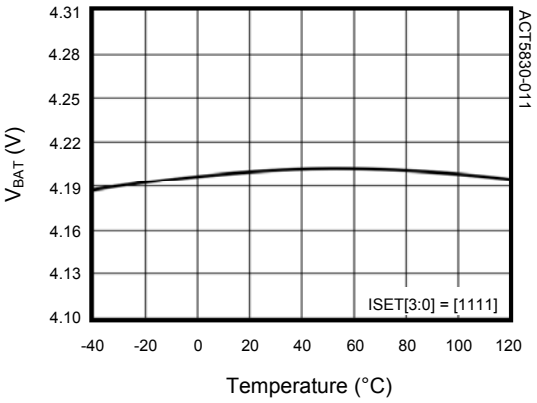
CHGR/VSET[3:0]	CHARGE TERMINATION VOLTAGE (V)
000	4.10
001	4.12
010	4.14
011	4.16
100	4.18
101	4.20 (default)
110	4.22
111	4.24

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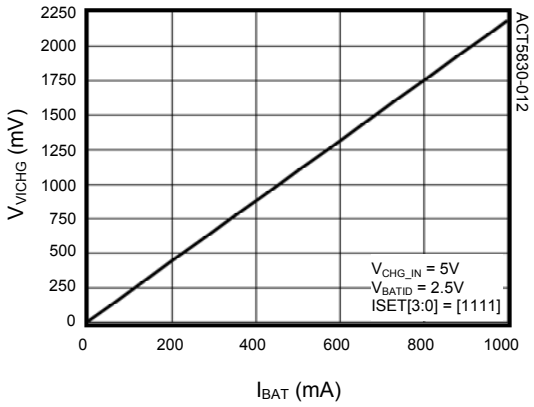
TYPICAL PERFORMANCE CHARACTERISTICS

(C_{OUTx} = 1μF X7R, V_{BAT} = V_{INx} = V_{OUTx} + 0.5V, T_A = 25°C, unless otherwise specified.)

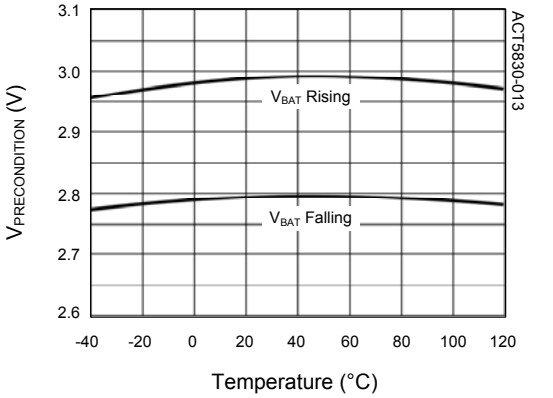
Battery Termination Voltage vs. Temperature



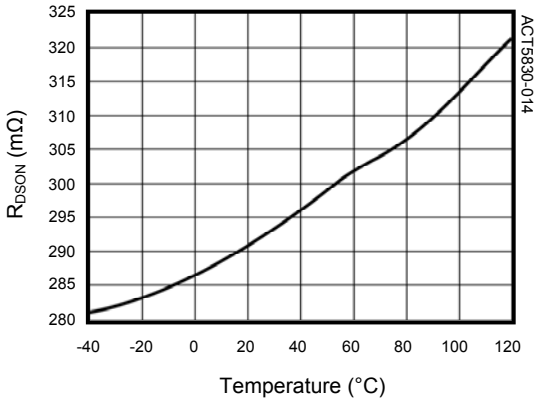
VICHG Voltage vs. I_{BAT}



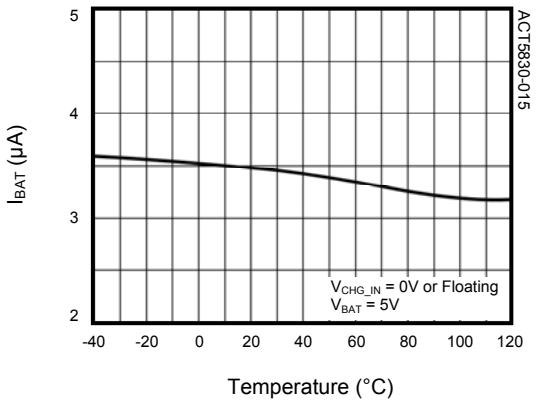
Precondition Threshold Voltage vs. Temperature



MOSFET Resistance vs. Temperature



BAT Reverse Leakage Current vs. Temperature



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FUNCTIONAL DESCRIPTIONS

General Description

The ACT5830's internal battery charger is an intelligent, stand-alone CC/CV (constant-current/constant-voltage), linear-mode single-cell charger for Lithium-based cell-chemistries. This device incorporates current and voltage sense circuitry, an internal power MOSFET, thermal-regulation circuitry, a complete state-machine to implement charge safety features, and circuitry that eliminates the reverse-blocking diode required by conventional charger designs. The ACT5830 battery charger operates independently of the regulators, and is automatically enabled whenever a valid input supply is available.

The ACT5830's battery charger features software-programmable fast-charge current, charge termination voltage, charge safety timeout period.

The ACT5830's battery charger can accept input supplies in the 4.3V to 6V range, making it compatible with lower-voltage inputs such as 5-6V wall-cubes and USB ports. The battery charger, along with LDO1, LDO2, and LDO3, is enabled and initiates a charging cycle whenever an input supply is present.

Enabling/Disabling the Charger

The ACT5830 is enabled when the voltage applied to CHG_IN is greater than the voltage at BAT and is greater than 4.0V, and nENCHG is asserted low. The charger is disabled whenever nENCHG is high, independent of the voltages at battery and CHG_IN. The charger may also be disabled via the I^2C interface.

For more information about enabling and disabling the charger, see the *System Startup & Shutdown* section.

Operation Without a battery

The ACT5830's charger is designed to operate with or without a battery connected. When a battery is connected, a normal charging cycle is performed as described below. If no battery is present, however, the charger will regulate the voltage at BAT to the voltage programmed by CHGR/VSET[ ] to power the system.

CC/CV Regulation Loop

At the core of the ACT5830's battery charger is a CC/CV regulation loop, which regulates either current or voltage as necessary to ensure fast and safe charging of the battery.

In a normal charge cycle, this loop regulates the current to the value set in the CHGR/ISET register. Charging continues at this current until the battery cell voltage reaches the programmed termination voltage, as defined in the CHGR/VSET register. At this point the CV loop takes over, and charge current is allowed to decrease as necessary to maintain charging at the termination voltage.

Programming the Charge Current (ISET[ ])

In order to accommodate both USB and AC-powered inputs with a minimum of external components, the ACT5830 features a I^2C-programmable fast-charge current that requires no external current-setting components. The CHGR/ISET register sets ISET to any value greater than [0000] to program the maximum charge current to values in the 300mA to 1A via software. See for a detailed list of programmable charge currents.

Note that the actual charging current may be lower than the programmed fast-charge current, due to the ACT5830's thermal regulation loop. See the *Thermal Regulation* section for more information.

Measuring the Charge Current

In order to ease monitoring of the charge current, the ACT5830 generates a voltage at VICHG that is proportional to the charge current. The gain is typically 2.47mV/mA, and this voltage can be easily read by a system ADC. VICHG is high-impedance in shutdown.

Thermal Regulation

The ACT5830 features an internal thermal feedback loop that reduces the charging current as necessary to ensure that the die temperature does not rise beyond the thermal regulation threshold of 115°C. This feature protects the ACT5830 against accessing JUNCTION temperature, and allows the ACT5830 to be used in aggressive thermal designs without risk of damage. Note that attention to good thermal design is still required to achieve the fastest possible charge time.

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FUNCTIONAL DESCRIPTIONS CONT'D

Charge Safety Timer

While monitoring the charge cycle, the ACT5830 utilizes a charge safety timer to help identify damaged cells and to ensure that the cell is charged safely. Three timeout options of 1 hour, 1.43 hours, and 2 hours are available, as programmed by the CHGR/TIMOSET register, and a timer-disable option is also available for systems that do not require the ACT5830 to control charge timeouts.

The bit assignments for each timeout period are set as follows:

Table 12:

TIMOSET[ ] Timeout Period Options

TIMOSET [1:0]		PRECONDITION TIMEOUT	TOTAL CHARGING TIMEOUT
0	0	1 hour	3 hours
0	1	1.43 hours	4.3 hours
1	0	2 hours	6 hours
1	1	INFINITE	INFINITE

CHGR State-Machine

PRECONDITION State

A new charging cycle begins with the PRECONDITION state. In this state, the cell is charged at a reduced current of 10% of ISET, the programmed fast charge current. During a normal charge cycle, charging continues at this rate until V_{BAT} reaches the Precondition Threshold Voltage of 2.9V (typ), at which point the charging state machine jumps to its FAST-CHARGE state. If V_{BAT} does not reach the Precondition Threshold Voltage before the Precondition timeout period expires, then a damaged cell is detected and the state machine jumps to the TIMEOUT-FAULT State.

FAST-CHARGE State

In FAST-CHARGE mode, the charger operates in constant-current (CC) mode and charges the cell at the current programmed by CHGR/ISET. During a normal charge cycle fast-charge continues until V_{BAT} reaches the termination voltage programmed by VSET, at which point the state machine jumps to the TOPOFF state. If VBAT does not reach VSET before the total time out period expires then the state-machine will jump to the "SLEEP" state.

TOP-OFF State

In the TOP-OFF state, the cell is charged in constant-voltage (CV) mode. With the charge current limited by the internal chemistry of the cell, decreases as charging continues. During a normal charging cycle charging proceeds until the charge current decreases beyond the End-Of-Charge (EOC) threshold, defined as 10% of ISET. When this happens, the state machine terminates the charge cycle and jumps to the SLEEP state.

SLEEP State

In SLEEP mode the ACT5830 presents a high-impedance to the battery, allowing the cell to "relax" and minimizing battery leakage current. The ACT5830 continues to monitor the cell voltage, however, so that it can re-initiate charging cycles as necessary to ensure that the cell remains fully charged. Under normal operation, the state machine initiates a new charging cycle by jumping to the FAST-CHARGE state when V_{BAT} drops below the Charge Termination Threshold (programmed by VSET) by more than the Charge Restart Threshold of 200mV (typ).

SUSPEND State

The ACT5830 features a user-selectable suspend-charge mode (SUSCHG), which disables the charger but keeps other circuitry functional. Charging continues in the SUSPEND state until CHGR/SUSPEND is cleared, at which point the charge timer is reset and the state machine jumps to the PRECHARGE state.

Suspend charge by setting CHGR/SUSCHG = [1]. Permit charging by clearing CHGR/SUSCHG to [0].

TIMEOUT-FAULT State

In order to prevent continued operation with a damaged cell, there is no direct path to resume charging once a Timeout Fault occurs. In order to resume charging, the state machine must jump to the SUSPEND state as a result of any of the following events:

1) Microprocessor Sets CHGR/SUSCHG to [1],

2) Microprocessor Pulls nENCHG high,

The input supply is removed or the input supply voltage drops below the UVLO threshold (4V), or the battery is removed. Once any of these events occur, the state machine jumps to the SUSPEND

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FUNCTIONAL DESCRIPTIONS CONT'D

state and charging can resume as defined by Figure 4.

NO BAT State

The ACT5830 charger has been designed so that it will provide system power when there is no battery present. If the battery is not present at any time while a valid input voltage (>4V) is applied to CHG_IN, the ACT5830 will enable the charger and regulate the output at the voltage programmed by CHGR/VSET[ ], simulating a battery-present condition. The output current of the charger in this state is default to 1000mA to ensure full operation of the phone. When operating in this state, the charge timers are disabled but the thermal regulation loop is active. It is important for the application designer to consider both the power available from the charger as well as the thermal design in order to ensure proper system operation in this state. The user can prevent this operation by either:

1) Pull nENCHG high, or Setting SUSCHG = [1].

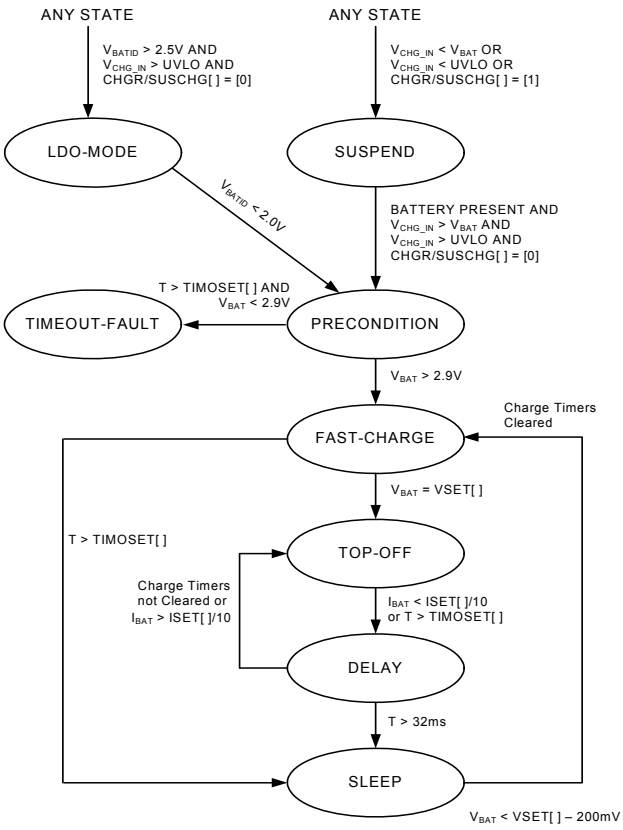
If the battery is reconnected while operating in the NO BAT state, the state machine resets the charge timers and jumps to the PRECONDITION state.

Reverse Battery

The ACT5830 includes internal circuitry that eliminates the need for series blocking diodes, reducing solution size and cost as well as dropout voltage relative to conventional battery chargers. When the input supply is removed, when VIN goes below the ACT5830's under voltage-lockout (UVLO) voltage, or when VIN drops below V_{BAT}, the ACT5830 automatically goes into SUSPEND mode and reconfigures its power switch to minimize current drain from the battery.

Figure 4:

Charger State Diagram

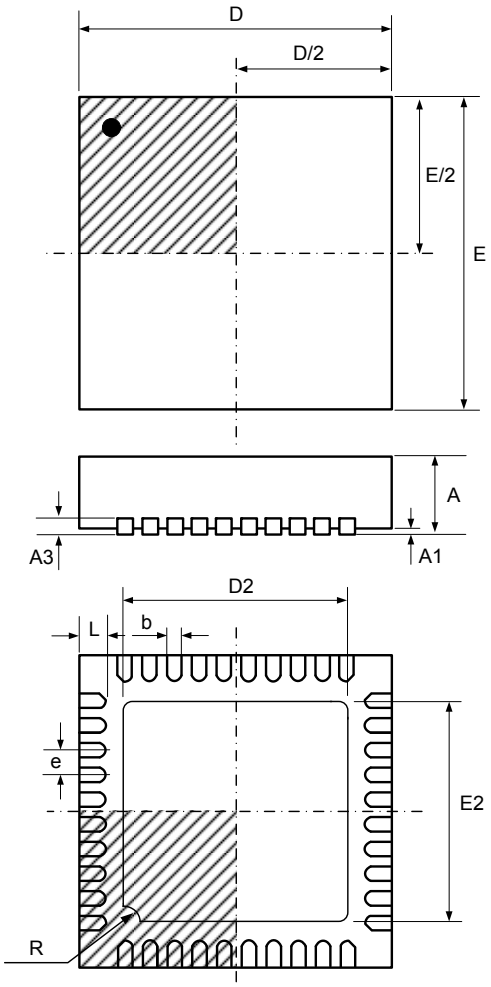


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PACKAGE OUTLINE AND DIMENSIONS

PACKAGE OUTLINE

TQFN55-40 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.200 REF		0.008 REF	
b	0.150	0.250	0.006	0.010
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
D2	3.450	3.750	0.136	0.148
E2	3.450	3.750	0.136	0.148
e	0.400 BSC		0.016 BSC	
L	0.300	0.500	0.012	0.020
R	0.300		0.012	

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