OKI semiconductor

MSM5278

DOT MATRIX LCD 64 DOT COMMON DRIVER

GENERAL DESCRIPTION

The OKI MSM5278GS is a dot matrix LCD's common driver LSI which is fabricated by low power CMOS metal gate technology. This LSI consists of 64-bit bidirectional shift register, 64-bit level shifter and 64-bit 4-level driver.

This LSI has 64 output pins to be connected to the LCD. By connecting more than two MSM5278GSs in series, this LSI is applicable to a wide LCD panel.

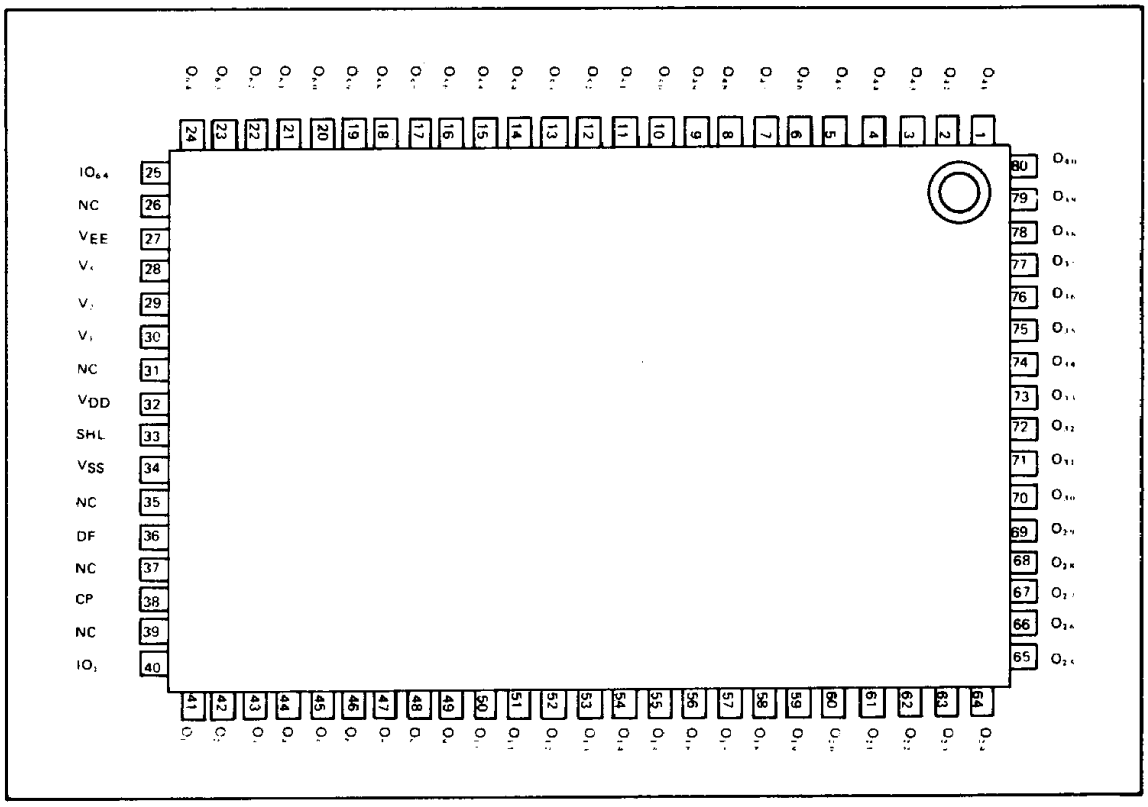
This LSI can drive a variety of LCD because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

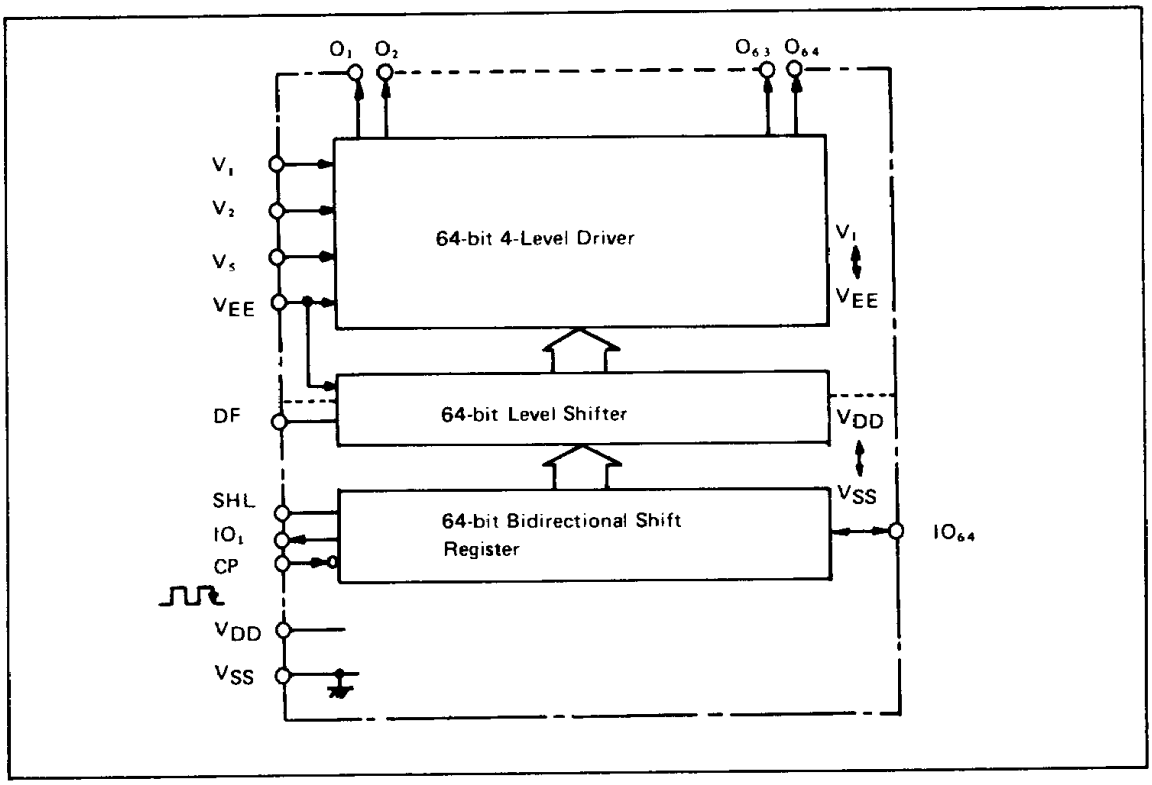
- Supply voltage: 4.5 ~ 5.5V
- LCD driving voltage: 8 ~ 20V
- Applicable LCD duty: 1/64 ~ 1/128
  Two chips of the MSM5278GS are required to drive 1/128 duty LCD.
- Bias voltage can be supplied externally
- 80 pin plastic QFP (QFP80-P-1420-K)

PIN CONFIGURATION

(Top view) 80 pin plastic QFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	T_a = 25°C	−0.3 ~ 6	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	T_a = 25°C	0 ~ 22	V
Input voltage	V_I	T_a = 25°C	−0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ + 150	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leqq V_{DD}$

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	—	4.5 ~ 5.5	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	—	8 ~ 20	V
Operating temperature	T_{op}	—	−20 ~ + 85	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leqq V_{DD}$

D.C. CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = −20 ~ +85°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	V_{IH}*1	—	0.8V_{DD}	–	–	V
"L" Input voltage	V_{IL}*1	—	–	–	0.2V_{DD}	V
"H" Input current	I_{IH}*1	V_{IH} = V_{DD}	–	–	1	μA
"L" Input current	I_{IL}*1	V_{IL} = OV	–	–	−1	μA
"H" Output voltage	V_{OH}*2	I_O = −0.4mA	V_{DD}−0.4	–	–	V
"L" Output voltage	V_{OL}*2	I_O = 0.4mA	–	–	0.4	V
ON Resistance	R_{ON}*4	$V_{DD} - V_{EE}$ = 18V *3 $\|V_N - V_O\|$ = 0.25V	–	1	2	kΩ
Power consumption	I_{DD}	CP = DC $V_{DD}-V_{EE}$ = 18V No load	–	–	100	μA
Input capacitance	C_I	f = 1MHz	–	5	–	pF

*1 Application to CP, IO_1, IO_{64} SHL and DF terminals.

*2 Applicable to IO_1, and IO_{64} terminals.

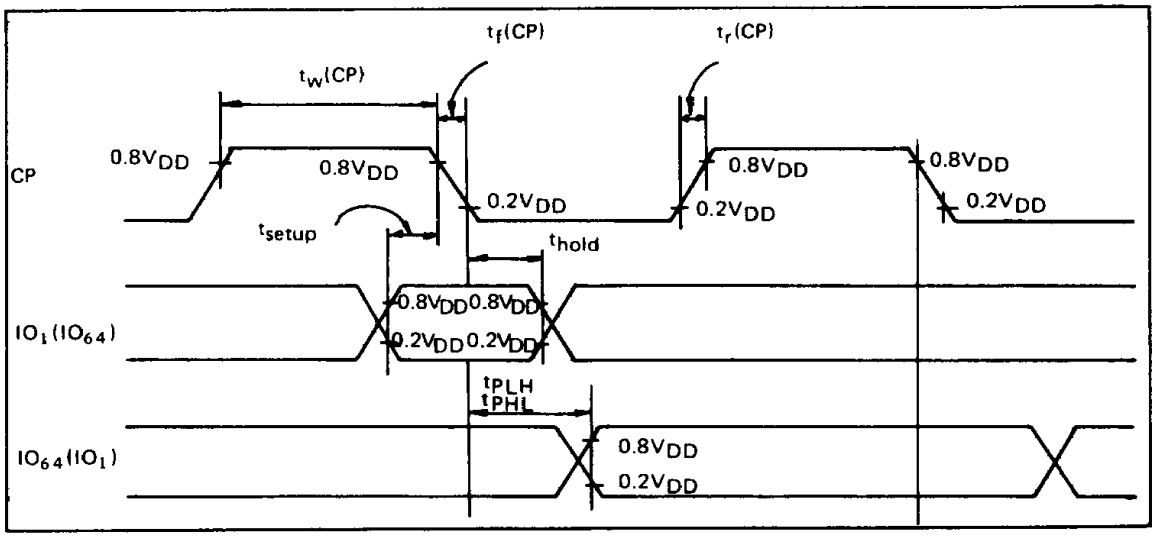
*3 $V_N = V_{DD} \sim V_{EE}$, $V_2 = \frac{10}{11}(V_{DD} - V_{EE})$, $V_5 = \frac{1}{11}(V_{DD} - V_{EE})$, $V_{DD} = V_1$

*4 Applicable to $O_1 \sim O_{64}$ terminals.

SWITCHING CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = −20 ~ +85°C CL = 15pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" "L" propagation delay time	t_{PLH} t_{PHL}	—	–	–	250	ns
Max. clock frequency	f_{CP}	—	1	–	–	MHz
Clock pulse width	$t_{W(CP)}$	—	125	–	–	ns
Data set-up time IO_1 (IO_{64})→CP	t_{setup}	—	100	–	–	ns
Data hold time IO_1 (IO_{64})→CP	t_{hold}	—	100	–	–	ns
Clock pulse Rising/Falling time	$t_{r(CP)}$ $t_{f(CP)}$	—	–	–	50	ns



PIN DESCRIPTION

- **IO_1, IO_{64}, SHL**
  IO_1 and IO_{64} are 64-bit bidirectional shift register input/output pins. The shifting direction is selected by the H/L condition of SHL pin. Refer to the table below.

SEL	Shifting direction	IO_1/IO_{64}	Input/output	Pin description
L	$O_1 \rightarrow O_{64}$	IO_1	Input	The scanning data from the LCD controller LSI is input from IO_1 synchronized with the clock pulse. *1
		IO_{64}	Output	Shift register contents output pin. The data which was input from IO_1 is output from IO_{64} with 64 bits' delay, synchronized with the clock pulse. Refer to the application circuit.
H	$O_{64} \rightarrow O_1$	IO_{64}	Input	The scanning data from the LCD controller LSI is input from IO_{64} synchronized with the clock pulse. *1
		IO_1	Output	Shift register contents output pin. The data which was input from IO_{64} is output from IO_1 with 64 bits' delay, synchronized with the clock pulse. Refer to the application circuit.

*1 The combination of the scanning data, IO_1 or IO_{64}, and the LCD driving output, $O_1 \sim O_{64}$, is shown in the table below.

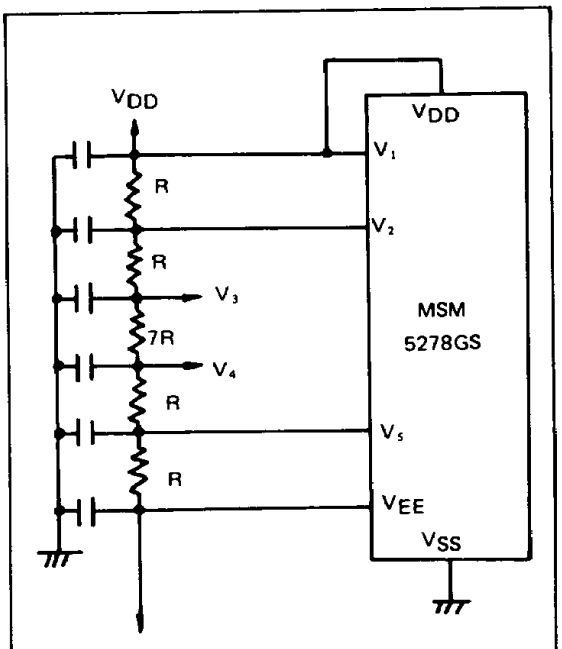
IO_1, IO_{64}	LCD driving output
H	Selected level (V_1, V_{EE})
L	Non-selected level (V_2, V_5)

- **CP**
  Clock pulse input pin for 64-bit bidirectional shift register. The data is shifted to 64-bit level shifter at the falling edge of the clock pulse.

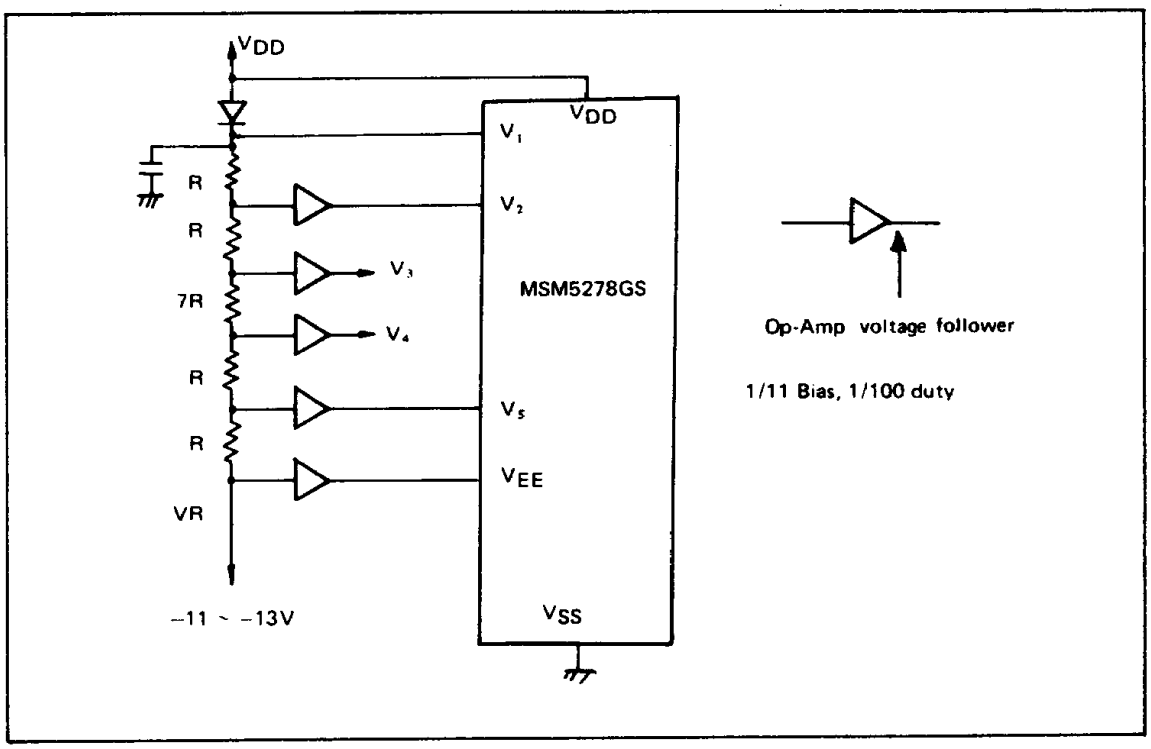
- **DF**
  Alternate signal input pin for LCD driving.
  Normal frame inversion signal is input.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 ~ 5.5V. V_{SS} is a ground pin. (V_{SS} = 0V)

- **V_1, V_2, V_5, V_{EE}**
  Bias supply voltage pins to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source.
  The below figure shows the case when bias voltage is divided by the resistance. V_1 is not necessarily connected to V_{DD}.



The figure below shows the case when bias voltage is supplied by the Op-Amps. By using Op-Amps, the bias voltage becomes low impedance and the power consumption of MSM5278 becomes low.



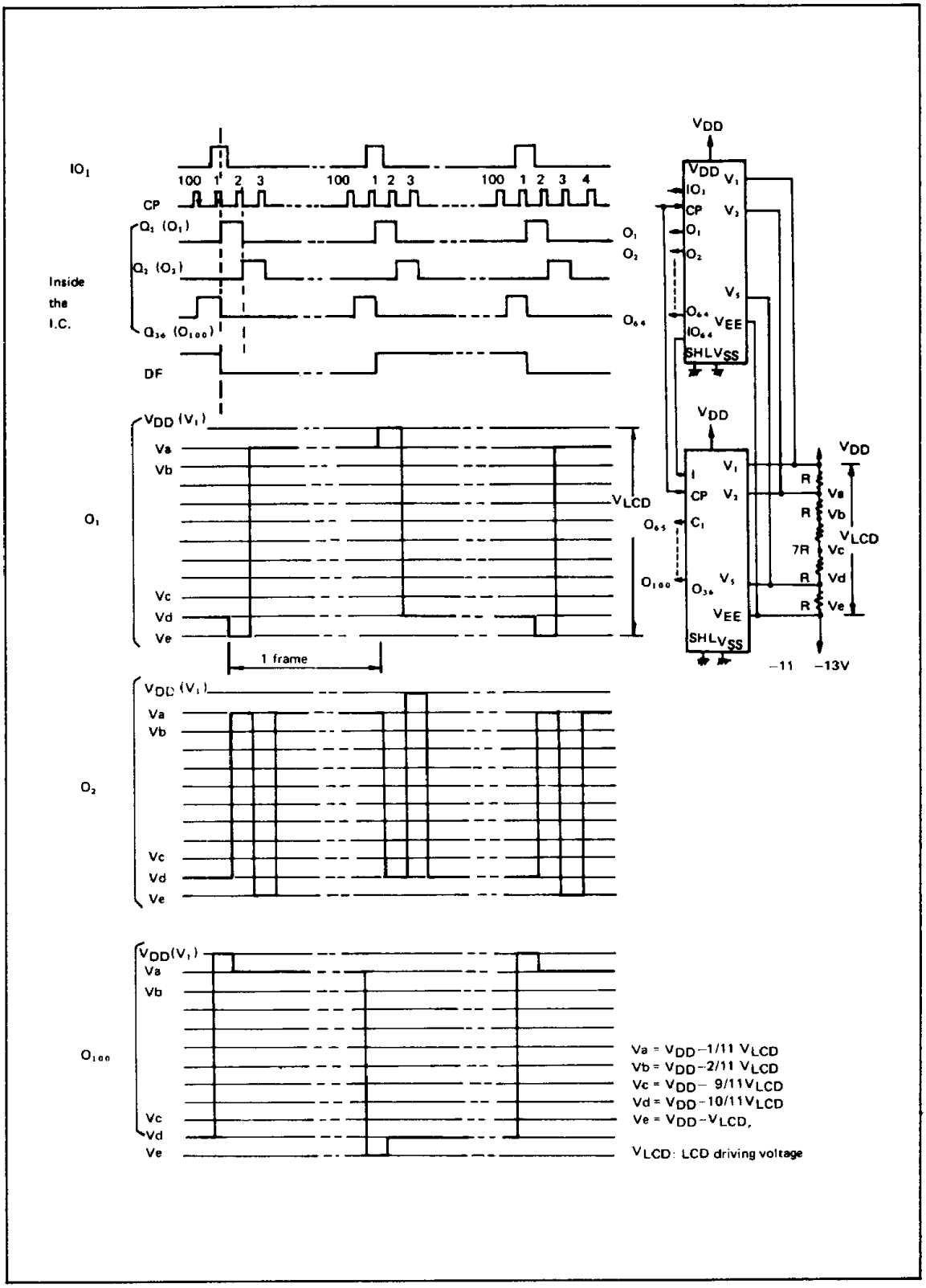
- **$O_1 \sim O_{64}$**
  Display data output pins which correspond to 64-bit shift register contents. One of V_1, V_2, V_5 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and DF signal. (Refer to the truth table below.)

DF	Latched data level	Display data output level ($O_1 \sim O_{64}$)
L	L	V_2
L	H	V_{EE}
H	L	V_5
H	H	V_1

Truth table

TIMING CHART

1/100 duty, 1/11 bias



APPLICATION CIRCUIT