AN2208
APPLICATION NOTE

Designing Industrial Applications with VN808/VN340SP High-side Drivers

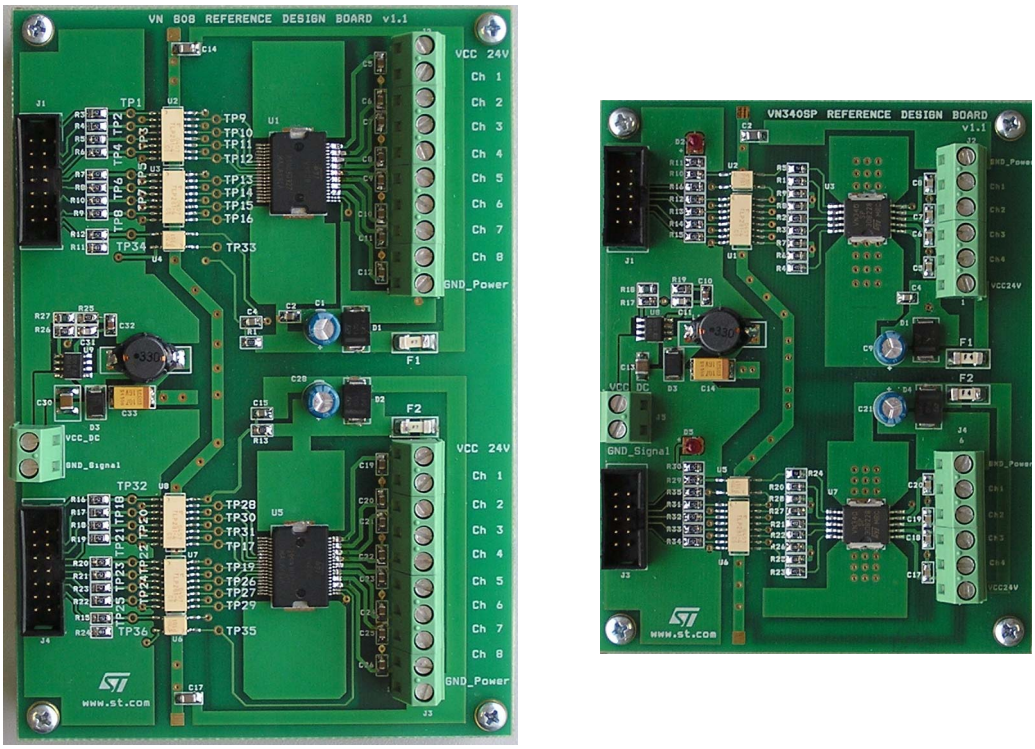
Introduction

This application note describes the functions of VN808/VN340SP high-side drivers in industrial applications. The VN340SP and VN808 are monolithic devices based on VIPower technology. With primary application requirements being safety and reliability, this application note covers the various tests used to ensure compliance with international electromagnetic compatibility (EMC) specifications as well as other requirements.

VN808/VN340SP high-side drivers are tested mounted on their respective reference design board (RDB).

Note: Additional information concerning the L5970D DC/DC converter, based on BCD technology, is included in Section Appendix C: L5970D DC/DC converter on page 46.

Figure 1. VN808 and VN340SP reference design boards



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1 High-side driver description

The VN808 (*Figure 2*) is a high-side driver (HSD) used to drive eight independent loads. Active current limitation combined with thermal shutdown and automatic restart functions protect the device against overload. A thermal case substrate protection is implemented to protect the FRx substrate under short circuit and worst case ambient conditions in terms of reliability. The device automatically turns off when the ground pin is disconnected. The VN340SP and VN808 are especially suitable for use with programmable logic controllers (PLC) in industrial applications.

The VN340SP (*Figure 3*) is used to drive four independent resistive, capacitive and inductive loads in high-side configurations. Active current limitation prevents the system power supply from dropping in the event of a short load. A built-in thermal shutdown circuit protects the chip from high temperatures and short circuits. Each I/O is pulled down when an over-temperature condition of the relative channel is detected and restarts after reaching the lower thermal threshold. The system oscillates depending on the thermal impedance of the application.

Table 1. VN808 and VN340SP main characteristics

VN340SP HSD	VN808 HSD
Output current per channel 0.5A at 24V	
Built-in current limiter	
Short-load and overtemperature (Junction) protection	Short-load and overtemperature (Junction and Case) protection
Under-voltage shutdown	
Open-drain diagnostic output	Status output current 2 to 4 mA
DC supply voltage 36V	DC supply voltage 45V
Very low stand-by current	

Figure 2. VN808 block diagram

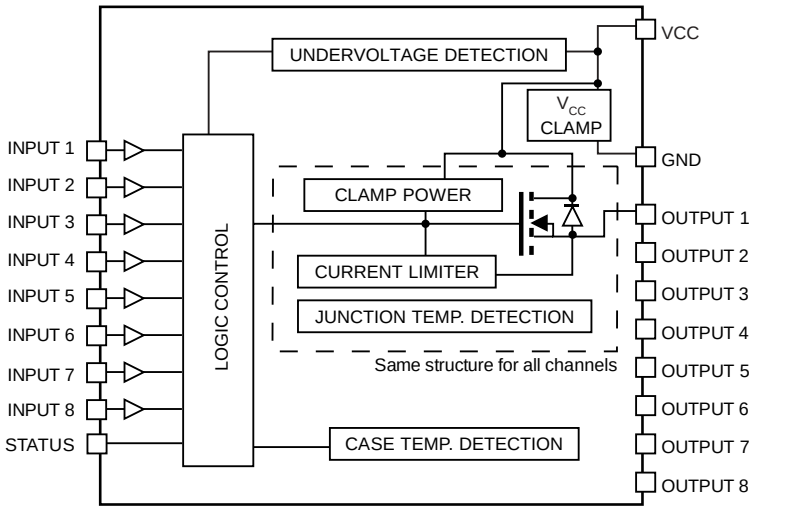
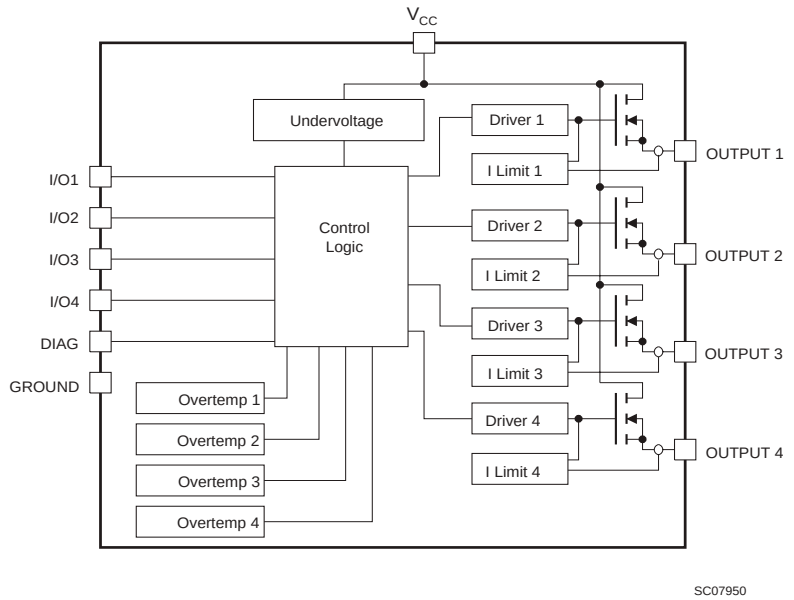


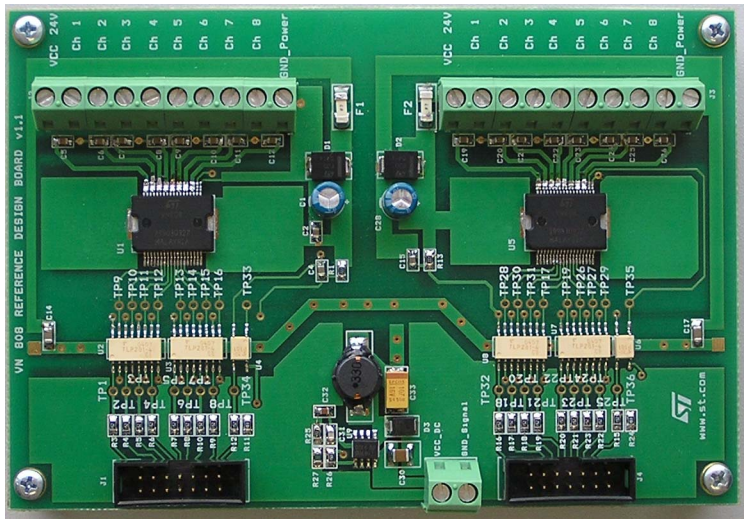
Figure 3. VN340SP block diagram



2 VN808 reference design board

This is a practical example how the VN808 high-side driver (HSD) can be used in applications for an industrial environment.

Figure 4. VN808 reference design board



2.1 Circuit description

In order to protect the high-side driver (HSD) from the harsh industrial conditions of power supply lines, usually optocouplers and Transil diodes are used to separate the application control circuits from the power supply. *Figure 11* shows a complete schematic diagram of the VN808 reference design board.

The VN808 reference design board uses multi-channel TLP281-4 and TLP181 optocouplers. The TLP281-4 and TLP181 are small and thin couplers, suitable for surface-mounted assemblies that consist of a photo transistor optically coupled to a gallium-arsenide infrared emitting diode. The isolation voltage for this type of optocoupler is 2500 V_{RMS}.

The clamping function of Transil diodes protect the HSD against transient overvoltages. The reference design board is assembled with uni-directional SM15TXXA Transil diodes because they protect the HSD against both positive and negative surge pulses. For more information about SM15TXXA Transil diodes from STMicroelectronics, please refer to the SM15T36A Datasheet available at www.st.com.

Refer to *Section A.2: Recommended VN808 PCB Layout on page 43* for more information about designing boards to improve EMC immunity and performance in industrial environments.

2.2 Surge suppression

When designing your application, V_{CC} and ground lines should lay on top of each other, minimizing the closed loop area and increasing the ability of the application to reject

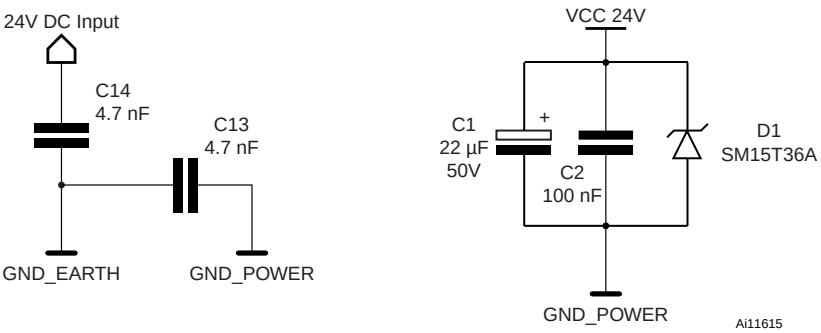
environmental noise. *Figure 5* shows a surge suppression block using a uni-directional SM15T36A Transil diode.

The Transil diode provides overvoltage protection for the HSD. The SM15T36A has a peak pulse power dissipation of 1500 W, stand-off voltage of 36 V and breakdown voltage of 37.8 V. Depending on the application, a Transil diode with a different value (for example, between 28 V and 40 V) may be used.

An electrolytic capacitor (C1) must be placed immediately after the surge suppression block. The size of the electrolytic capacitor is selected based on the slope of the output current, the impedance of the complex power supply cables, as well as the maximum allowed voltage drop across the device. The C1 value is generally 25 µF per chip. For more information about the C1 value, please refer to *Application Note AN1351: VIPower and BCDMultipower: Making life easier with ST's high-side drivers*.

A low ESR SMD capacitor (C2) must be placed as close as possible to the HSD in order to filter the power supply line for electromagnetic compatibility concerns. The suggested C2 value is 100 nF.

Figure 5. Surge Suppression Block



2.3 Isolation recommendations

Industrial environments require good isolation between digital and power supply parts. Optocouplers are widely used and multi-channel optocouplers represent a very attractive solution. *Figure 6* shows a schematic diagram with optocouplers connected to ground.

Although optocouplers are good isolators, they may lower the category of the Electrical Fast Transients (EFT) immunity tests as the primary and secondary sides of the optocouplers may still have parasitic capacitance “bonding” to each other, even though they are isolated. This parasitic capacitance may inject a current through the base emitter junction of the phototransistor when one half of the optocoupler is “tight” due to fast voltage transients with respect to the other side as shown in *Figure 7.*

If an optocoupler is used in an emitter-follower configuration, as in most industrial applications, a high emitter voltage signal may be induced by applying EFTs even after opening the collector termination. An efficient way to prevent this high emitter voltage signal is to provide a conducting plane connected to ground on both the top and bottom layers of the PCB (under the optocouplers) as shown in *Figure 52: VN808 RDB PCB layout (top and bottom)*.

Figure 6. Typical input/status isolation by optocouplers

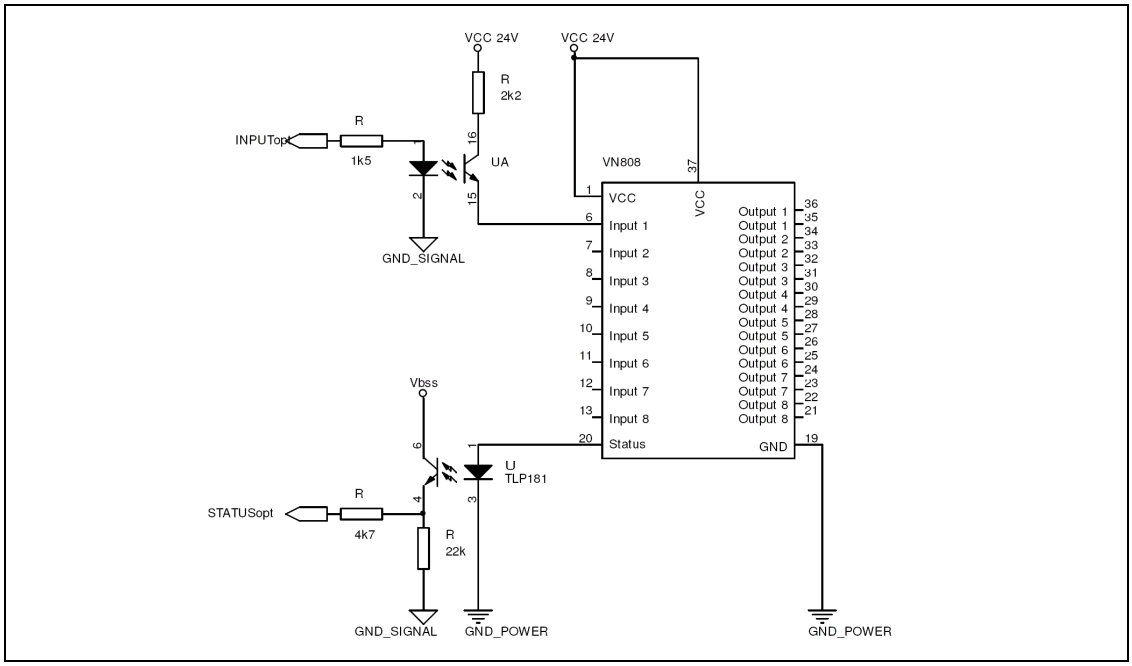
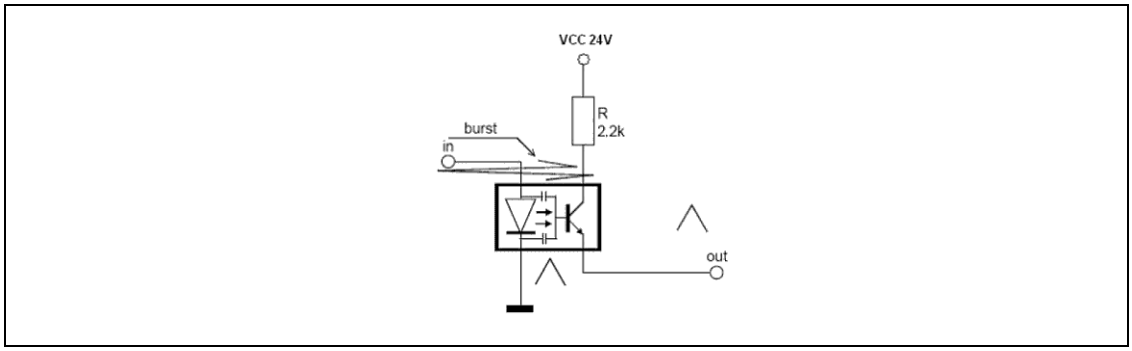


Figure 7. Burst pulse affecting one input

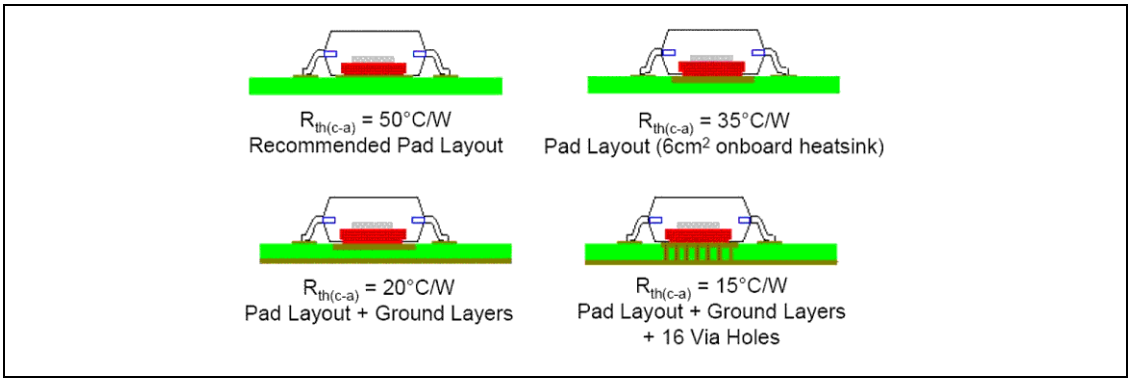


2.4 Heatsink recommendations

Depending on ambient thermal conditions, HSD's with a PowerSO10/SO36 package require external cooling as the copper bottom plate of the PSO-Package, used to maintain the junction temperature during inductive switching, acts as a thermal capacitor.

The VN808 reference board is designed with an onboard heatsink capability (minimum heat sink area is 6 cm²). The recommended layout for Power SO packages is shown in *Figure 8.*

Figure 8. Recommended layout for High Power Dissipation capability



2.5 Schematic diagrams

Figure 9. DC/DC part of the application circuit

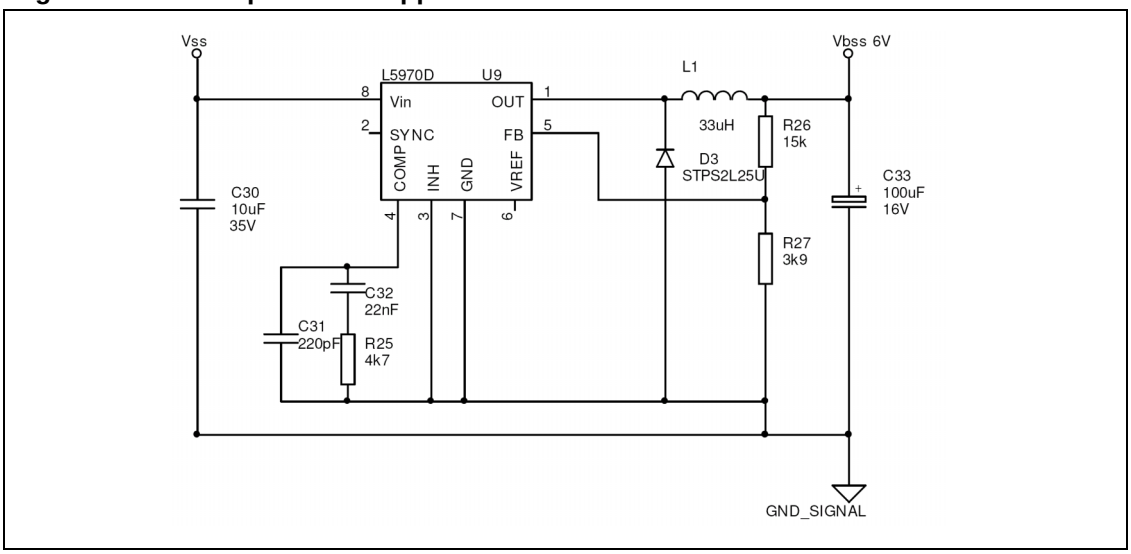


Figure 10. Current and voltage conventions

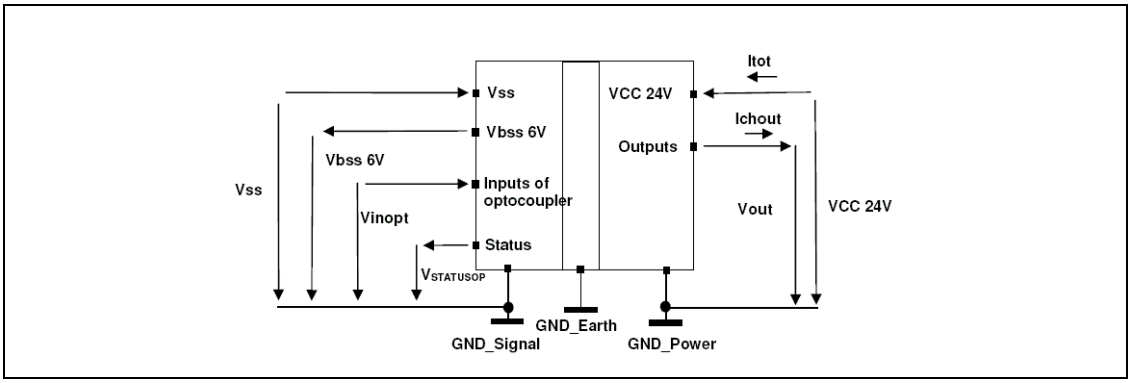


Figure 11. Complete application circuit with VN808 and L5970D devices

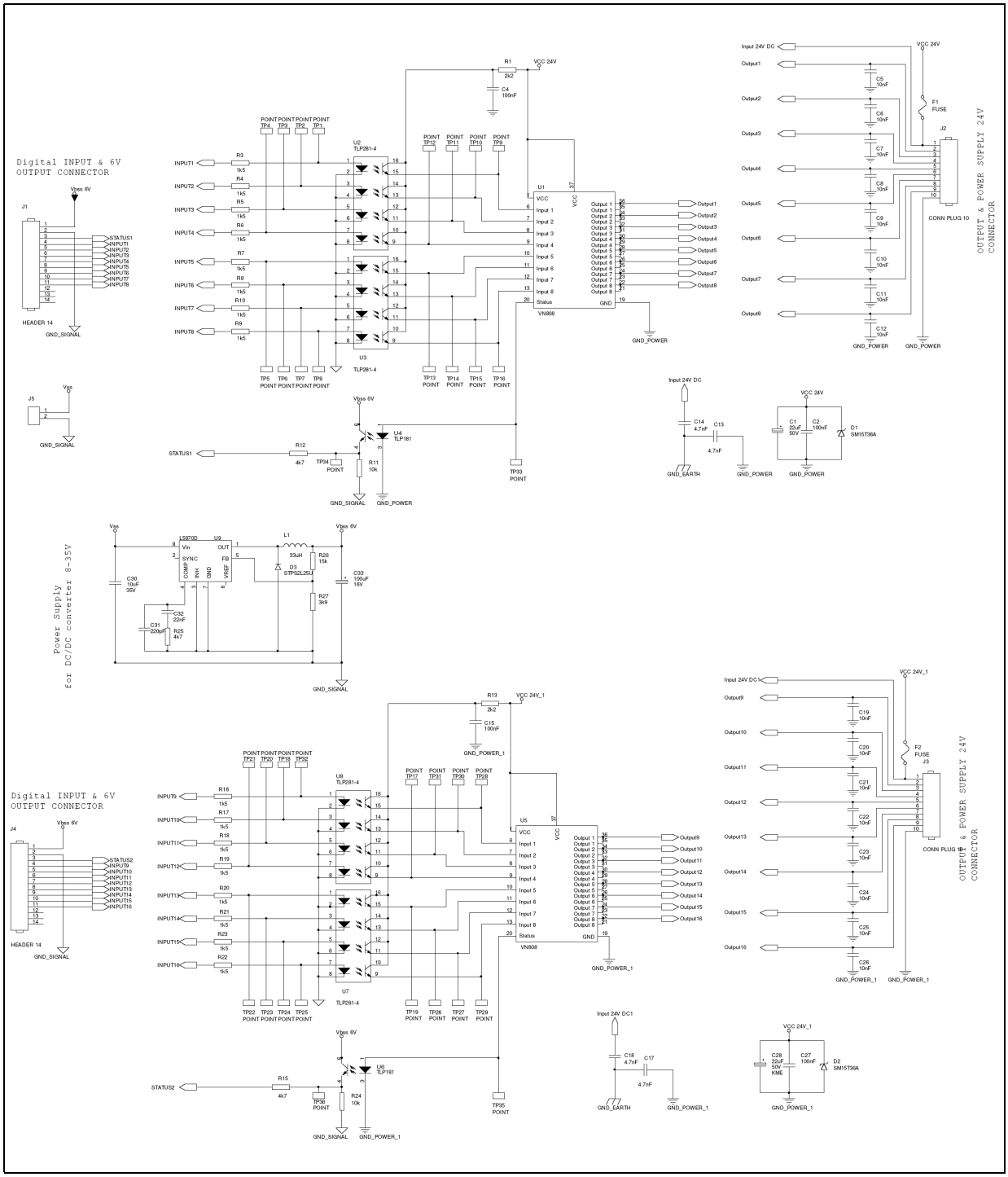
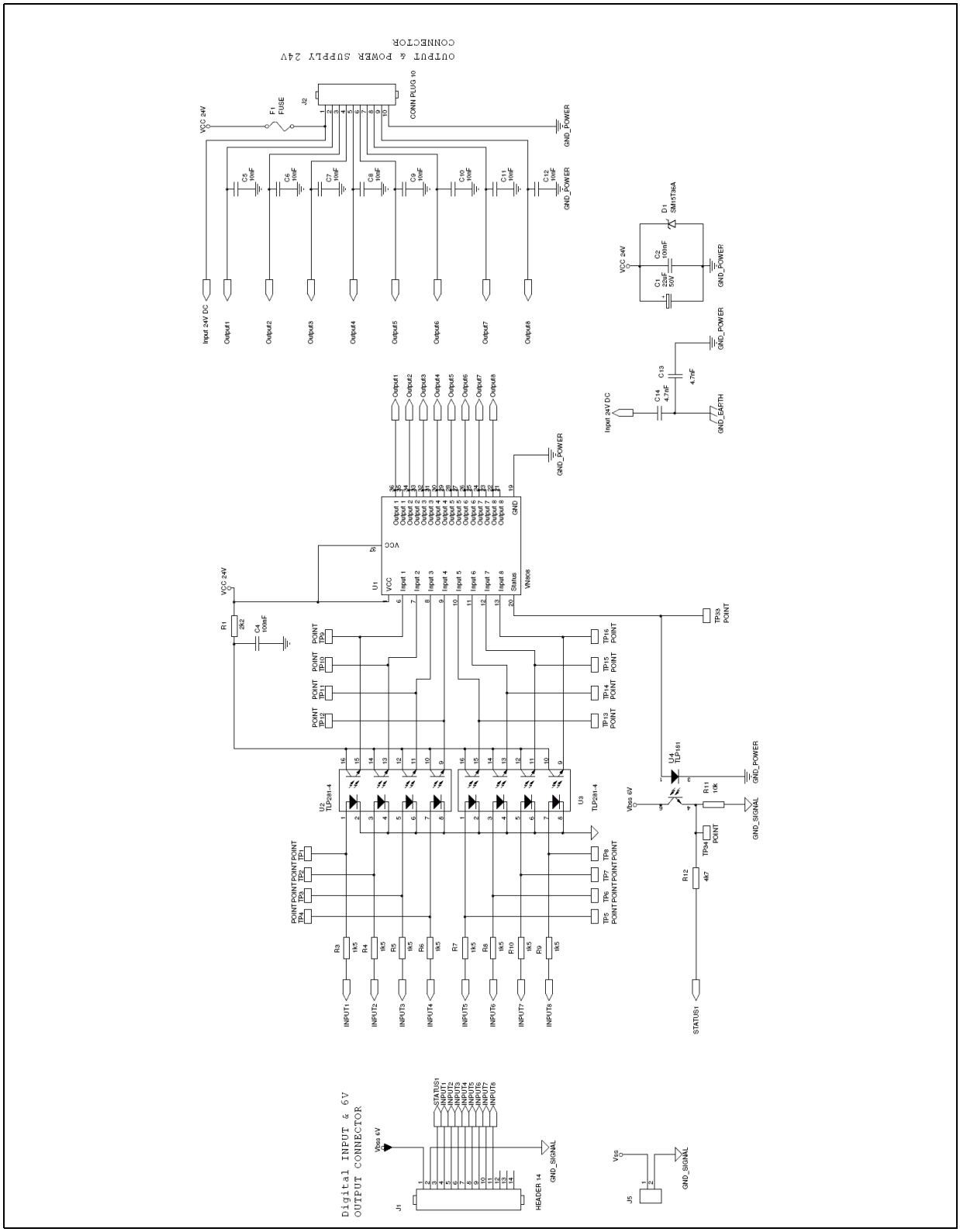


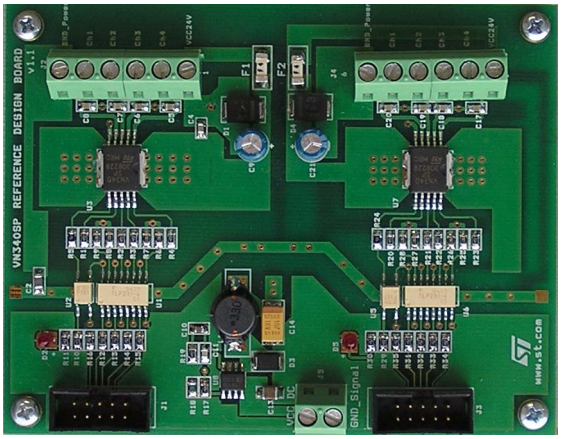
Figure 12. Switching part of the application circuit



3 VN340SP reference design board

This is a practical example how the VN340SP high-side driver (HSD) can be used in applications for an industrial environment.

Figure 13. VN340SP reference design board



3.1 Circuit description

The application described below is very similar to that of the VN808 reference design board; only the type of HSD and the optocoupler inter-connection is different. *Figure 15* shows a complete schematic diagram of the VN340SP reference design board. The optocouplers and Transil diodes are the same as those used in the VN808 reference design board.

3.2 Schematic diagrams

Figure 14. Switching part of the application circuit

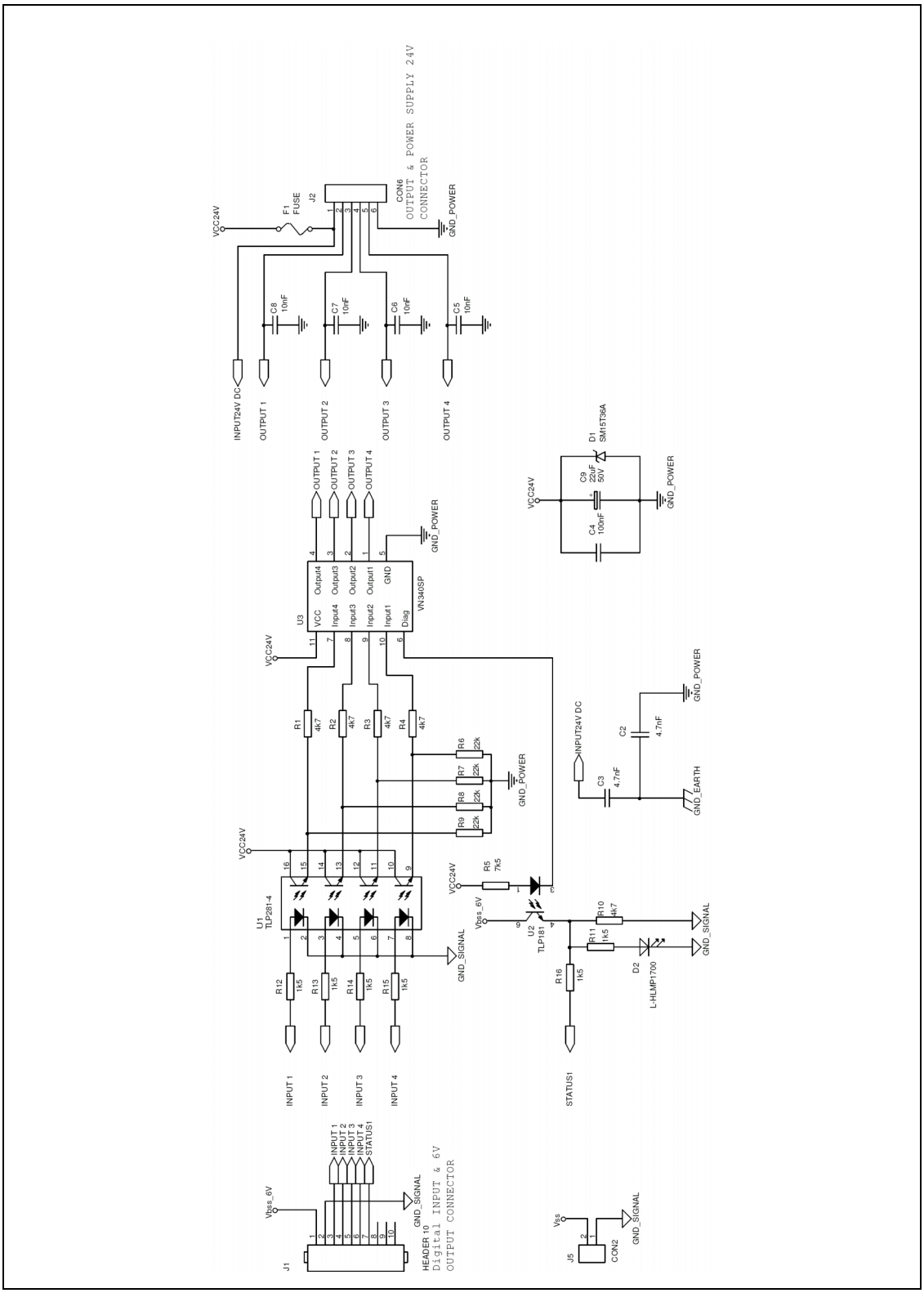
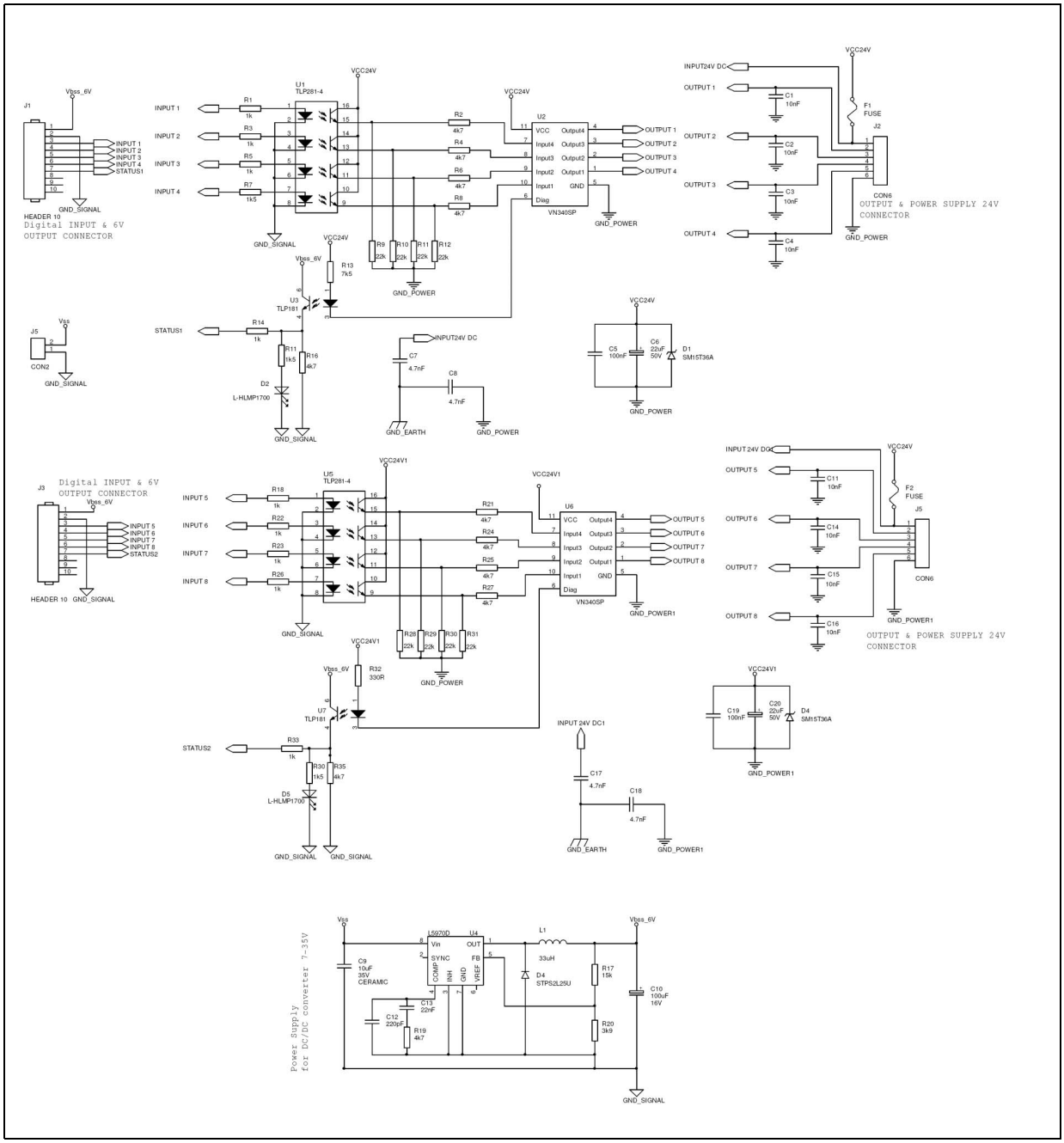


Figure 15. Complete application circuit with VN340SP and L5970D devices



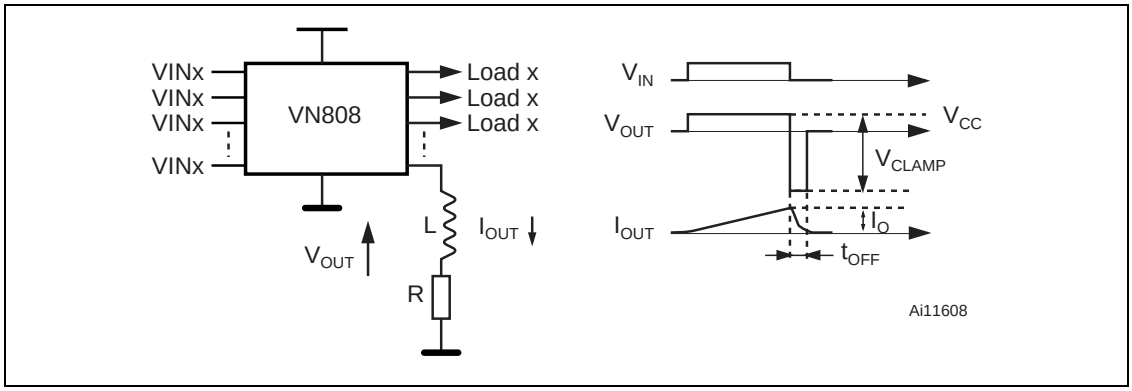
4 Load switching tests

Many different types of loads can be found in an industrial environment. Typical loads have inductive or resistive characteristics. Applications compliant with UL 508 (48Ω and 1.15H) specifications are generally considered as the worst case.

A basic description of typical switching inductor loads is given in *Figure 16*. The supply voltage is nominally 24V but can rise up to 30.5V. In this application, 24V filament lamps are used with 130mH/48Ω inductors as the loads. The V_{CC} supply condition is between 18.5V and 28.5V DC.

The V_{CLAMP} voltage value decides the t_{OFF} demagnetization duration: the faster you want to switch off the circuit, the bigger | V_{CLAMP}| compared with | V_{CC}| has to be.

Figure 16. Description of the switching inductor loads



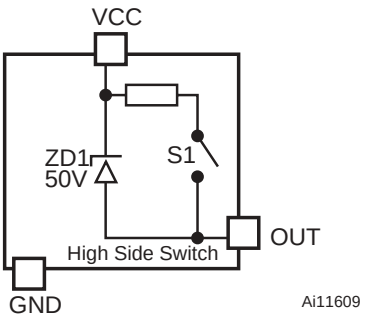
Note: Typical V_{CLAMP} value for VN808 is 52V.

STMicroelectronics' Intelligent Power Switches (IPSs) provide a "fast demagnetization" output structure, an integrated solution for fast switch-off of inductive loads.

IPSs are basically a Zener diode with a 52V breakdown (approx.) and high power dissipation capability connected between an output and V_{CC} as shown in *Figure 17.* In most applications, the output voltage is then clamped at $V_{OUT} = V_{CC} - 52$, and is therefore dependent on the supply voltage.

The integrated clamping structure saves on components and space. Internal demagnetization can be used only if thermal behavior and load conditions are well known to designers. Therefore a detailed analysis of thermal behavior related to inductive load switching is mandatory to prevent improper utilization of the IPSs.

Figure 17. IPS simplified structure



The parameters are given by the following formulas:

$$t_{OFF} = \frac{L}{R_{LOAD}} \bullet \ln\left(1 + \frac{V_{CC}}{V_{CLAMP} - V_{CC}}\right)$$

$$E_{OFF} = \frac{V_{CLAMP}}{R_{LOAD}} \bullet \left(\frac{L \bullet V_{CC}}{R_{LOAD}} - ((V_{CLAMP} - V_{CC}) \bullet t_{OFF})\right)$$

$$P_{t_{OFF}} = \frac{E_{OFF}}{t_{OFF}}$$

For example for VN808:

Where, I_{OUT} = 0.5 A, L = 130 mH, f = 0.5 Hz, V_{CC} = 24 V and V_{CLAMP} = 52 V

V_{CLAMP} - V_{CC} = 28 V and R_{LOAD} = 48 Ω

t_{OFF} = 1.6 ms

E_{OFF} = 21 mJ per channel

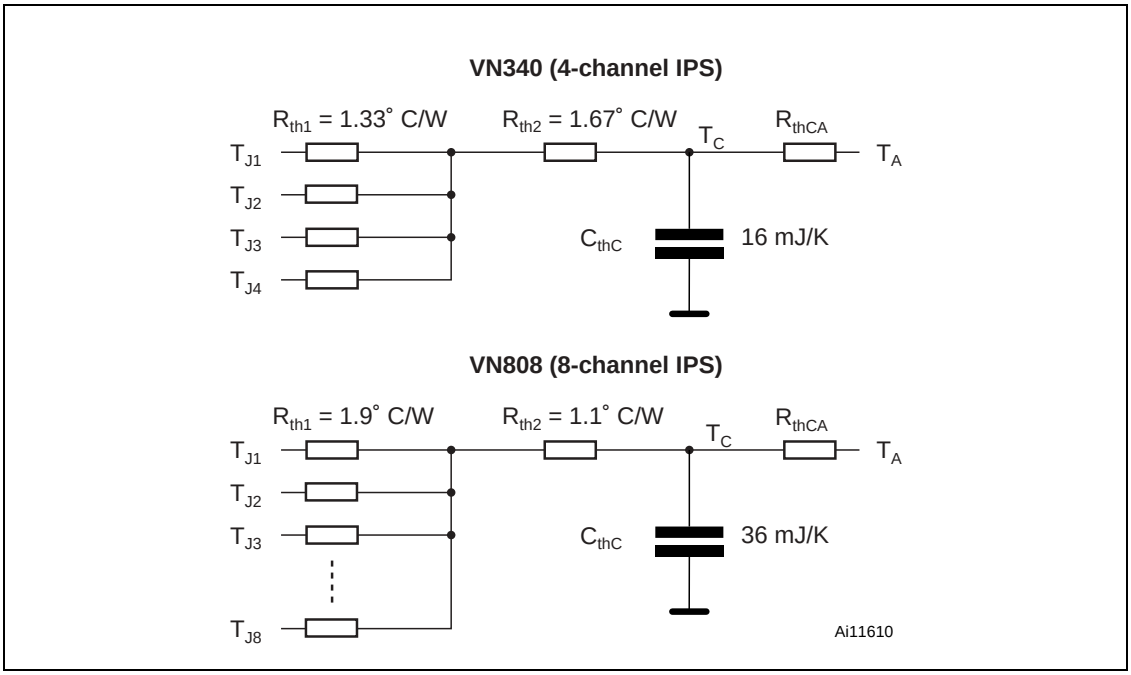
$$P_{t_{OFF}} = 4 \bullet \frac{21mJ}{1.6ms} = 52.5W$$

Note: For more information about switching inductor loads, see Application Note AN1351.

5 Thermal stress tests

The thermal model of a generic Intelligent Power Switch (IPS) can be exemplified as shown in *Figure 18.* R_{thJC} and R_{thCA} represent the junction-to-case and the case-to-ambient thermal resistance, whereas C_{thC} is the predominant thermal capacitance and is basically related to the package itself.

Figure 18. Simplified thermal models



Note: Case thermal time constant of 48 ms without external cooling.

$R_{thJC} = R_{th2}+R_{th1}$/Nb of channels
If Nb = 8, R_{thJC} = 1.34°C/W
If Nb = 4, R_{thJC} = 2°C/W

The aim of the designer will be to provide the lowest possible junction–ambient thermal impedance, in order to minimize the chip temperature jump-up.

Example VN808:
I = 0.5 A, L = 130 mH, f = 0.5 Hz, T_A = 60°C, Duty cycle = 0.5, V_{CC} = 24 V,
8 channels active, 4 channels working at the same time.

Conduction losses:
Losses due to I_{SON} (supply current): 24V* 12mA(max.) = 288 mW
PowerMOS losses at ON State: 280 mΩ(max.)*(0.5)^2*0.5*8 = 280 mW

Switching losses:
Switching losses are due to inductance discharge:
P_{DOFF} = 8* E_{OFF}*F = 8* 21mJ * 0.5 = 84 mW

Total losses and Junction temperature:
Total power losses = 652 mW (0.652 W)

If the PSO36 is on FR4, R_{thCA} = 50°C/W
t_{OFF} = 1.6 ms << 48 ms (constant time of the PSO36)

$T_C = T_A + Pmean^* R_{thCA}$

T_C = 60°C +34 °C = 94°C
T_{JMax} during t_{OFF} = 94 + (1.1 + (1.9/4))*52 = 175°C

6 Electromagnetic compatibility (EMC) tests

The VN808 and VN340SP reference design boards pass the following industrial tests. (Refer to specific product datasheet for electrostatic discharge (ESD) characteristics).

Table 2. EMC industrial compliance

IEC Specification	Description
61000-4-4	Electric Fast Transients (EFT)
61000-4-5	Surge protection
61000-4-6	Immunity to conducted disturbances

6.1 Terminology

Table 3. Abbreviations

Abbreviations	Description
CC	Current Clamp
CCC	Capacitive Coupling Clamp
CDN	Coupling/Decoupling Network
DN	Decoupling Network
EFT	Electric Fast Transients
EFT Generator	Generator with CDN according IEC 61000-4-4
ESD	Electrostatic Discharge
EUT	Equipment Under Test
HSD	High-side Driver
IPS	Intelligent Power Switch
PE	Protected Earth (metal plane)
Signal Generator	Wave generator with power amplifier according IEC 61000-4-6
Surge Generator	Generator with CDN according IEC 61000-4-5

6.2 List of EMC test equipment

Table 4. Equipment list for EMC tests

Equipment	Description
Surge Generator	EM Test Surge generator VCS 500 with CDN
EFT Generator	EM Test EFT 800 EFT/burst generator with CDN
CC	EMC Partner CN-EFT 1000 Capacitive coupling clamp
Power Supply	PCE A1200 40 30 DC power supply 40V/30A Toellner TOE 8733
Decoupling network	Trennstelltrafo LTS 606 for separation from the mains
Loads	Osram 8x lamps 24V/15W 8x Inductor 130mH/48Ω
Signal Generator	Agilent 33220A PMM 3000 according IEC 61000-4-6
CDN	EMC Partner CDN-1000 KIT for surge test EMC Partner CN-EFT-1000 FCC-M3-16A for IEC 61000-4-6 FCC F-120-9A Current Injection Probe for IEC 61000-4-6
Attenuator	EM TEST ATT6/75
Multimeter	FLUKE 189
Oscilloscope	LECROY LT 374M
Current Probe	LECROY AP015
Wood table	1-meter high
Metal plane	Size in proportion to wood table and test setup
Wood isolation	0.1-meter thick

6.3 Requested test levels

6.3.1 IEC 61000-4-4

- Polarity: positive/negative
- Test voltage: Level 4 (4 kV)
- Burst duration: 15 ms±20% at 5 kHz
- Burst period: 300 ms±20%
- Duration time: 60 seconds (min.)
- Applied to: Input/Output ports and Supply lines

6.3.2 IEC 61000-4-5

- Polarity: positive/negative
- Test voltage: Level 3 (2 kV)
- Number of Discharges: 5
- Repetition Rate: 1 per min.
- Applied to: Output ports and Supply lines (all combinations)

6.3.3 IEC 61000-4-6

- Test voltage: Level 3 (10 V)
- Frequency range: 150 kHz to 80MHz
- Modulation: 80% depth by AM 1 kHz
- Frequency step: 1%
- Dwell Time 100 ms
- Applied to: Input/Output ports and Supply lines

6.4 IEC 61000-4-4 EFT test setup

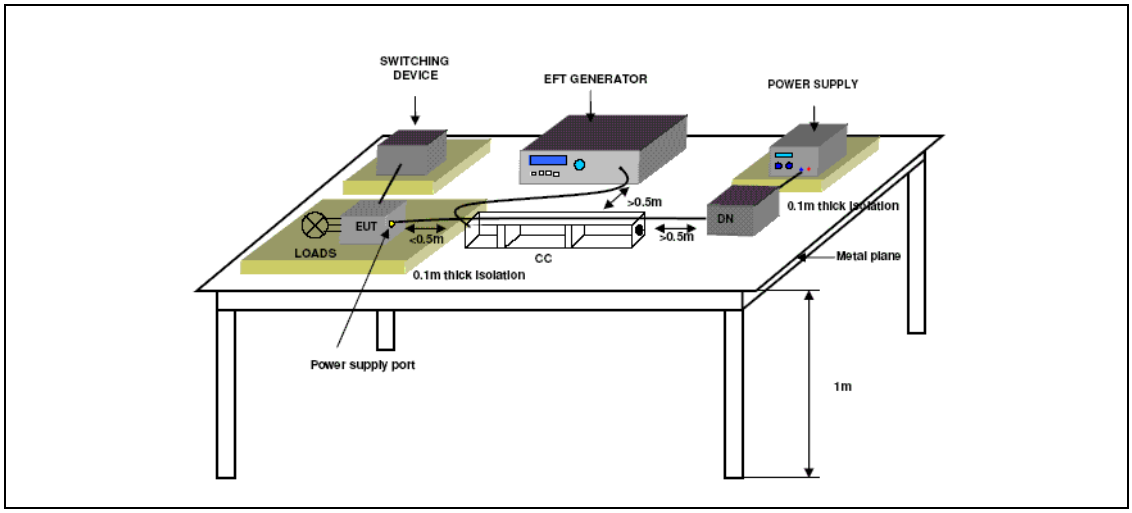
The reference design boards are tested on input/output ports and power supply lines. The test voltage is applied from the EFT generator to the EUT via a capacitive coupling clamp. The test setup and test voltage waveform comply with IEC 61000-4-4 specifications. The capacitive coupling clamp is connected by a high-voltage coaxial cable to the generator as close as possible to the EUT.

6.4.1 Power supply tests

Figure 19 illustrates the power supply test setup. A capacitive coupling clamp applies the test voltage (max. 4 kV) to the power supply lines. A decoupling network (DN) protects the power supply against the test voltage.

EUT test conditions:
Input port ON/OFF and f_{OPER} = 1 Hz
Input port wave form: Square 0/5V; f = 1 Hz

Figure 19. Power supply tests (IEC 61000-4-4)



6.4.2 Input port tests

Figure 21 illustrates the input port test setup. The RDB input ports are tested by first switching them to ground and then to the 5V supply using the battery-powered switch shown in *Figure 20* to increase protection.

Maximum test voltage must not exceed 4 kV.

Figure 20. Switch diagram

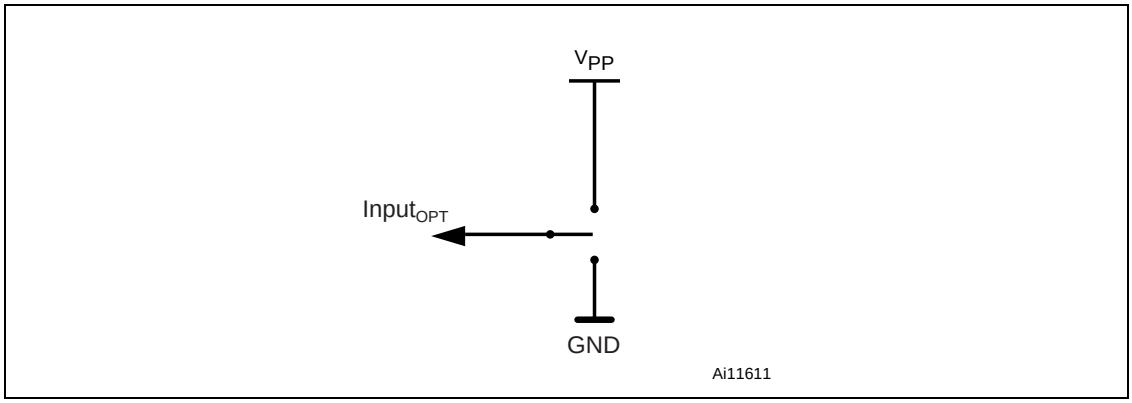
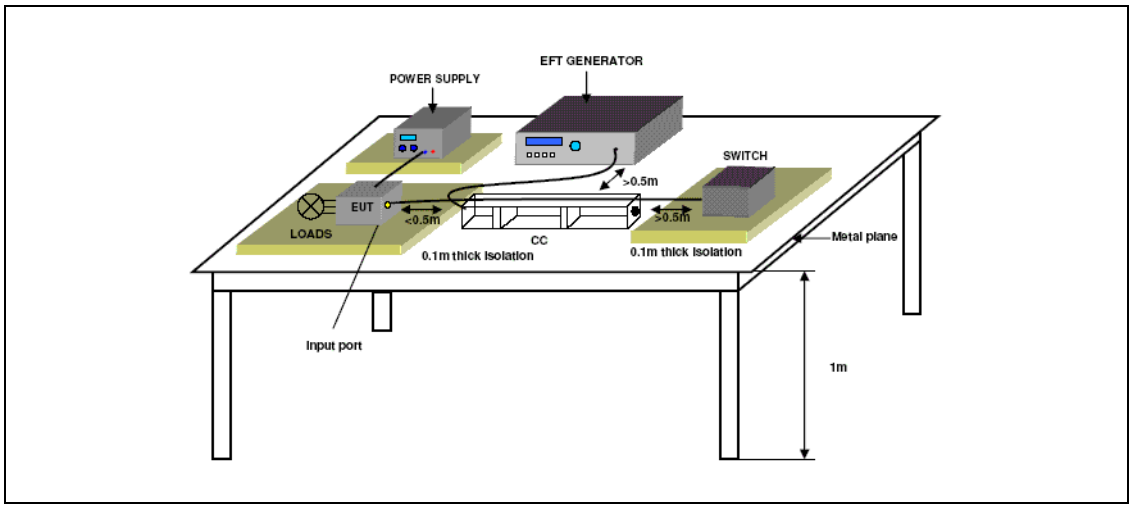


Figure 21. Test on input ports (IEC 61000-4-4)

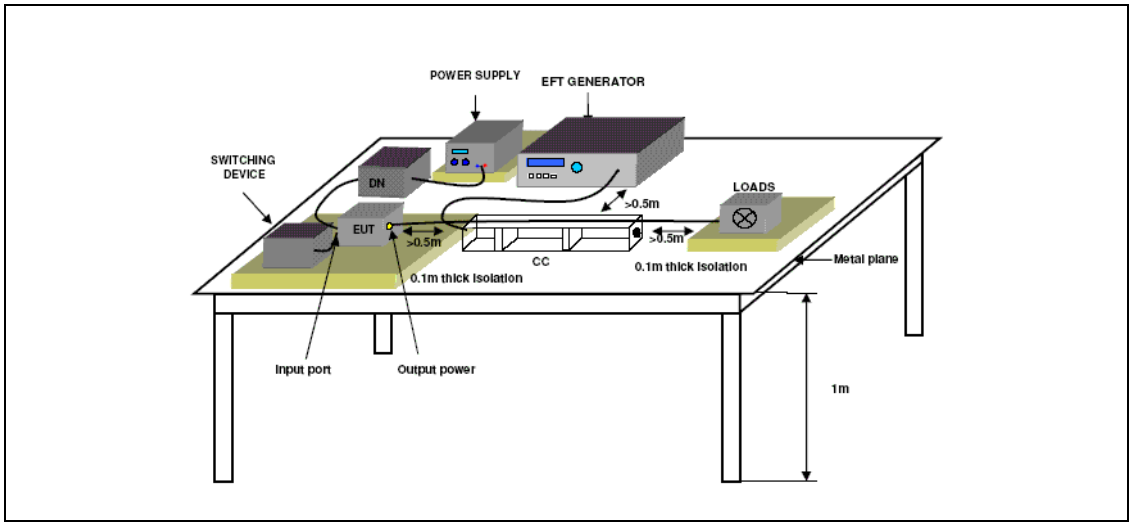


6.4.3 Output port tests

Figure 22 illustrates the output port test setup. The capacitive coupling clamp is the recommended method for coupling the generator source voltage into the output ports. All auxiliary devices are placed on the wood isolation board (0.1-meter thick). The test is performed while the HSD output port is switched On/Off at 1 Hz.

Maximum test voltage must not exceed 4 kV.

Figure 22. Output port tests (IEC 61000-4-4)



6.5 IEC 61000-4-5 surge test setup

Section 5 of the IEC 61000-4 specification concerns the immunity requirements, test methods, and range of recommended test levels for equipment to unidirectional surges caused by overvoltages from switching and lightning transients. The reference design boards are tested on the power supply lines and output port.

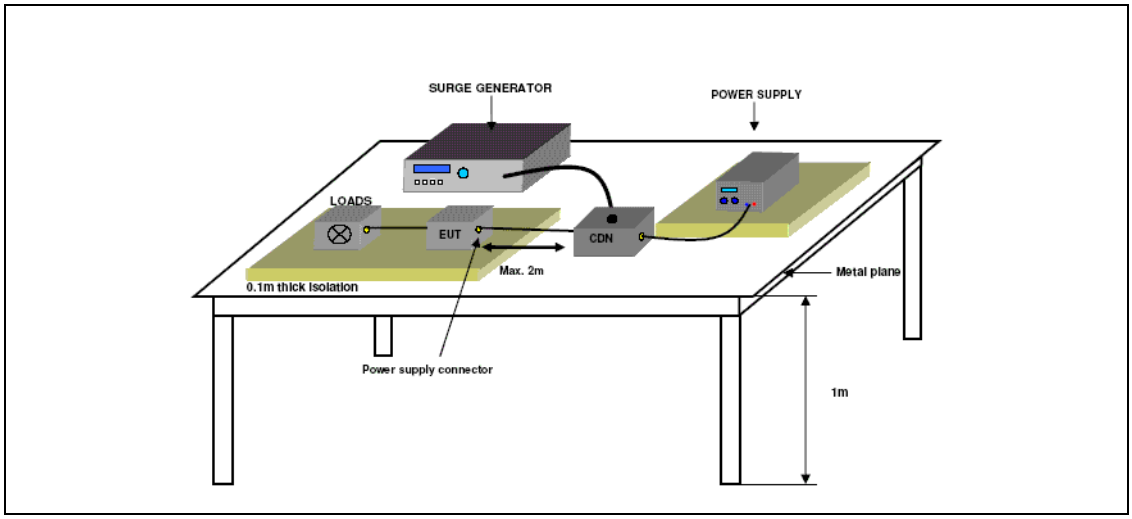
6.5.1 Power supply tests

Figure 23 illustrates the power supply test setup. The reference design boards are tested with different coupling modes:

- Line-to-line coupling mode with source impedance 42Ω (meaning V_{CC} 24V and GND_Power on the board, both polarities)
- Line-to-PE coupling mode with source impedance 42Ω (meaning V_{CC} 24V/GND_Power to GND_earth on the board, both polarities)
- Output to GND_Power with source impedance 42Ω
- Output to V_{CC} 24V with source impedance 42Ω
- Output to Protect Earth with source impedance 42Ω

The maximum surge voltage may not exceed 2kV for line-to-line coupling mode and 2kV for line-to-PE coupling mode. The test is performed while the HSD output port is switched On/Off at 1Hz. The maximum length of the cables between the EUT and CDN is 2 meters.

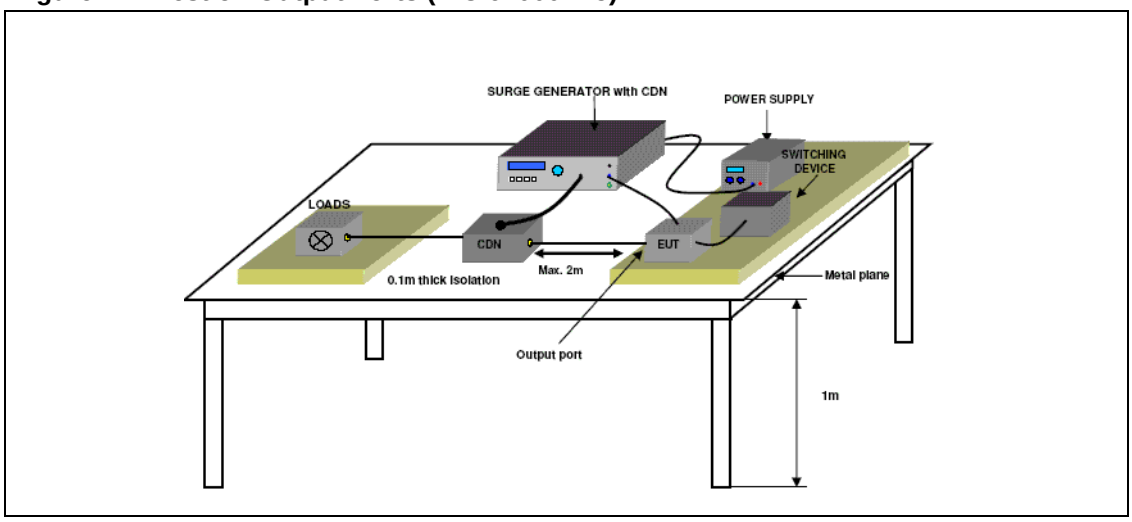
Figure 23. Power supply tests (IEC 61000-4-5)



6.5.2 Output port tests

Figure 24 illustrates the output port test setup. The maximum surge voltage and coupling mode is same as with the power supply tests. The test is performed while the HSD output port is switched On/Off with both polarities. The output lines are tested between V_{CC}/GND and PE.

Figure 24. Test on Output Ports (IEC 61000-4-5)



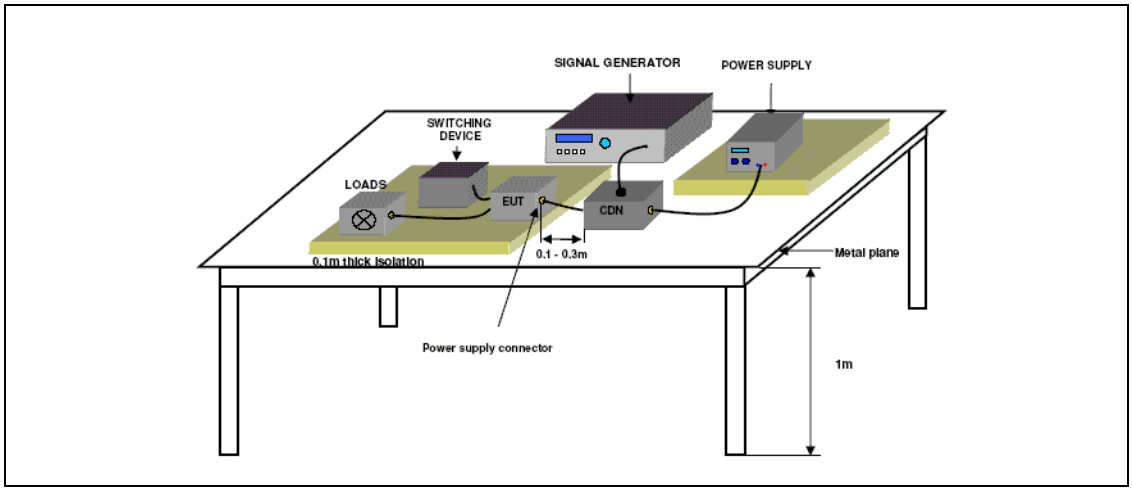
6.6 IEC 61000-4-6 conducted immunity

The reference design boards are tested on the Input/Output ports and Power supply lines with a maximum voltage of 10 V_{RMS}. The test signal is basically a sinusoidal waveform, whose frequency sweeps from 150 kHz up to 80 MHz with a 80% amplitude modulation at 1 kHz of the same signal. The EUT clearance from all metallic objects must be at least 0.5 meters.

6.6.1 Power supply tests

Figure 25 illustrates the power supply test setup. The test voltage is applied by coupling decoupling networks CDN. The maximum voltage is 10 V_{RMS}. The maximum distance between EUT and CDN is 0.3 meters. All Auxiliary Units (AU) such as power supplies switching devices must be placed on the wood isolation.

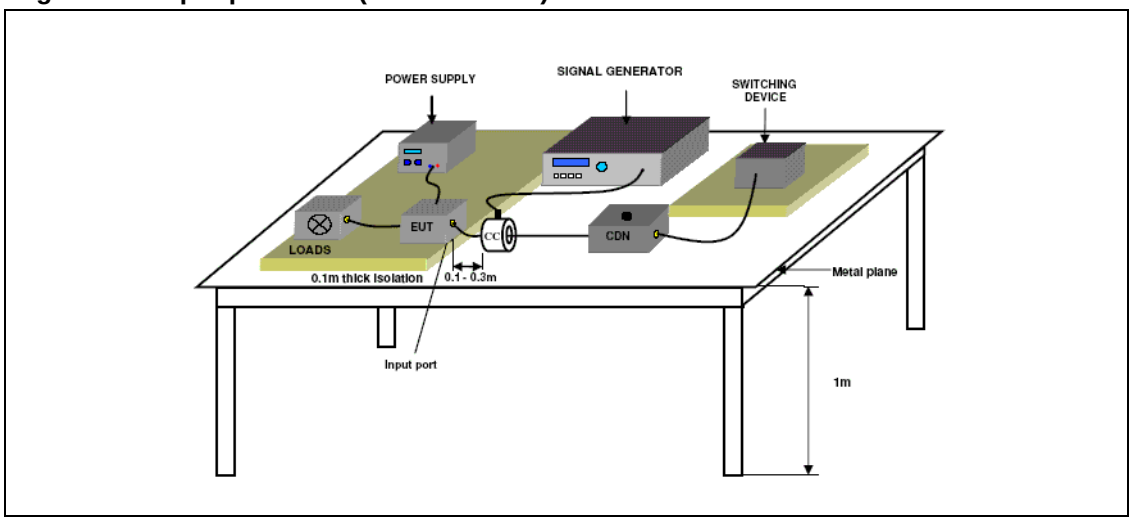
Figure 25. Power supply tests (IEC 61000-4-6)



6.6.2 Input port tests

Figure 26 illustrates the input port test setup. The test voltage from the signal generator to the EUT is applied by the current clamp. This device establishes inductive coupling to the cable connected to the EUT. The maximum distance between the EUT and the CC is 0.3 meters. The test is performed while the HSD input port is switched On/Off at 1Hz.

Figure 26. Input port tests (IEC 61000-4-6)

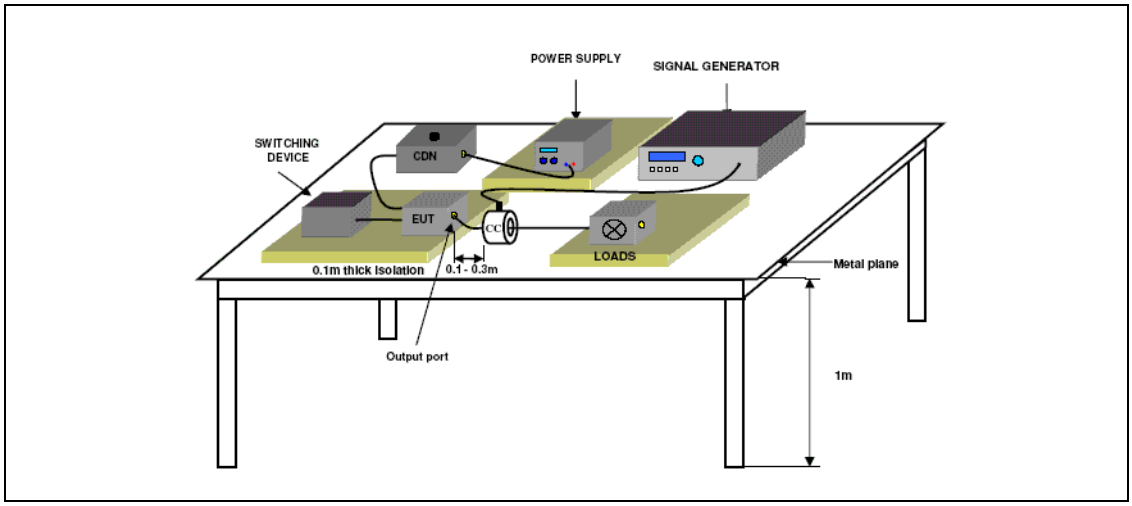


6.6.3 Output port tests

Figure 27 illustrates the output port test setup. The power supply must be protected to disturbance signal by a decoupling network. The current clamp is used as the coupling device

for the signal generator. The test is performed while the HSD output port is switched On/Off at 1Hz.

Figure 27. Output port tests (IEC 61000-4-6)



7 Test results

The following abbreviations are used in this section.

Table 5. Abbreviations

Symbol	Parameter
V_{IN}	Input Voltage
V_{OUT}	Output Voltage
V_{STAT}	Voltage on STATUS pin
T_A	Ambient temperature
T_{JSD}	Junction shut-down temperature
T_R	Junction Reset temperature
T_{CSD}	Case shut-down temperature
T_C	Case operating temperature
T_{CR}	Case reset temperature
T_j	Junction operating temperature

7.1 VN808 HSD test results

The typical behavior of the VN808 HSD according the datasheet is shown in *Figure 28* and *Figure 29*.

Figure 28. VN808 Waveforms (Part 1)

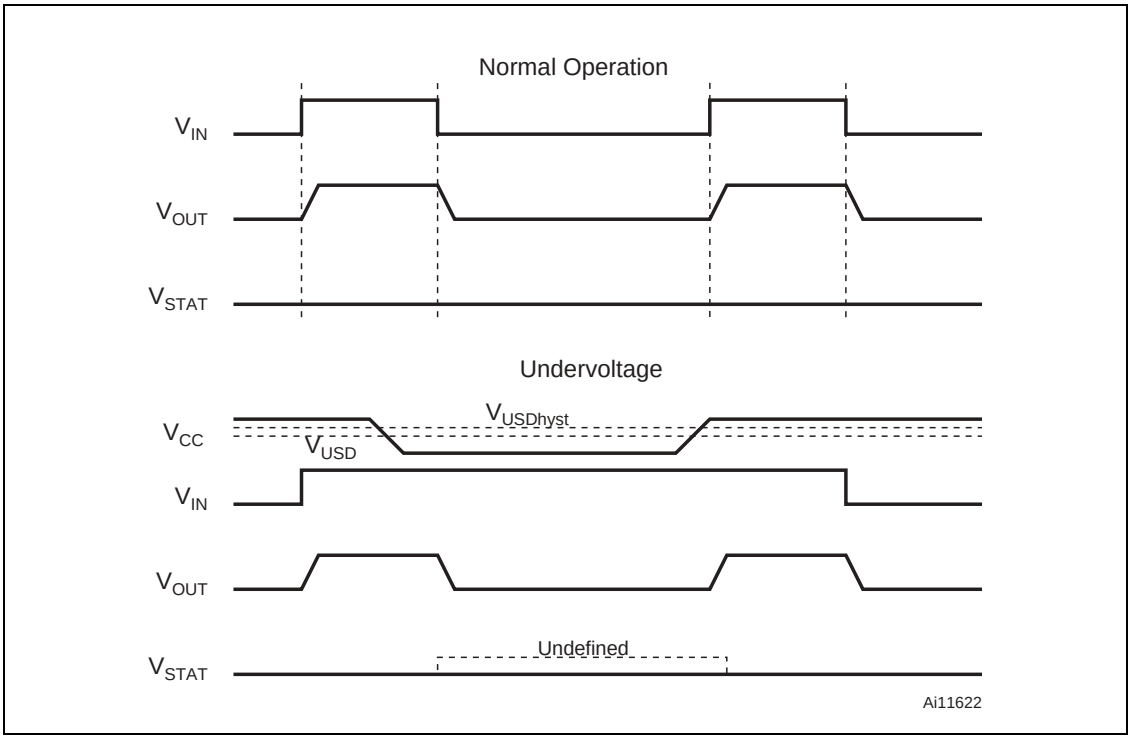
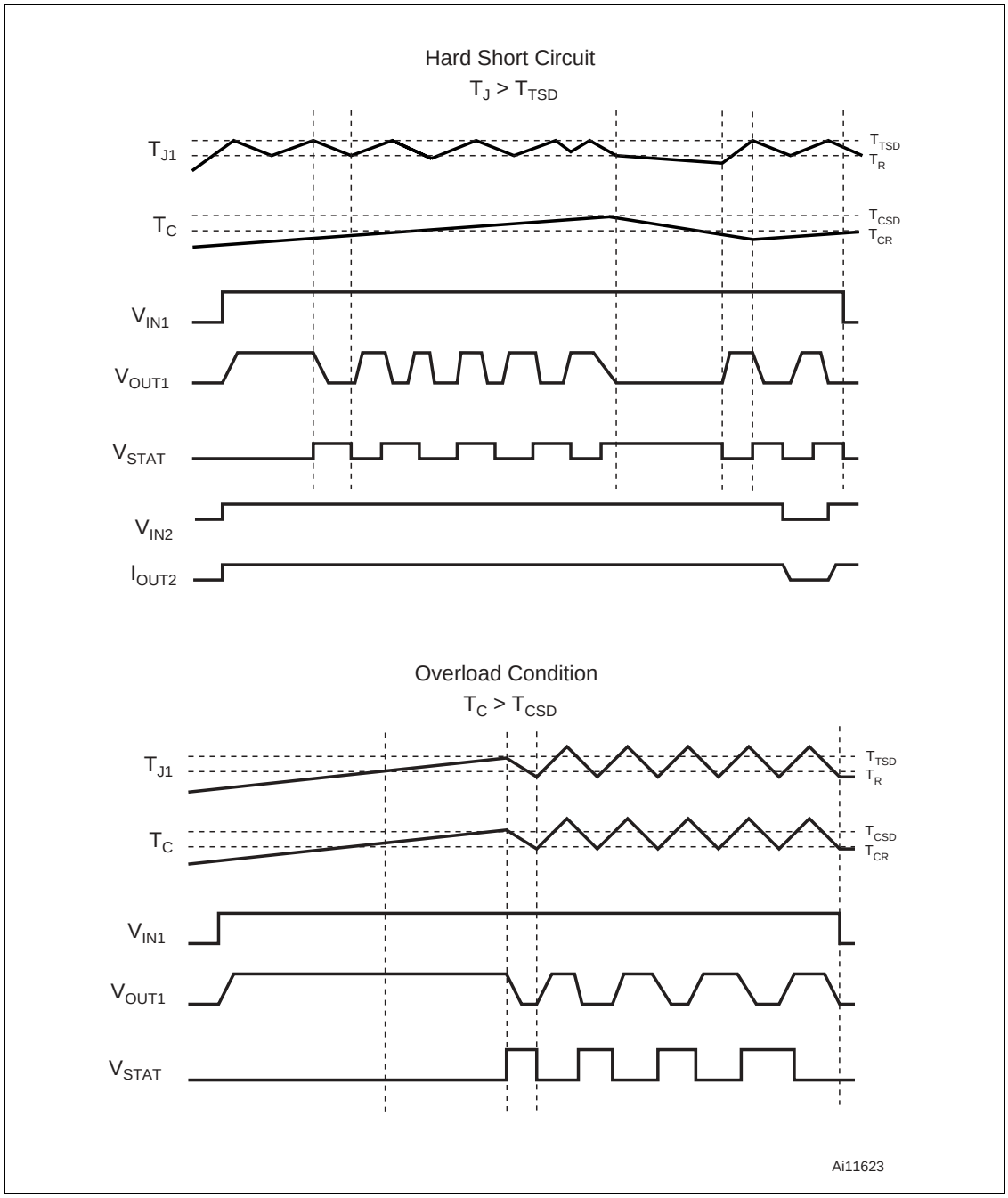


Figure 29. VN808 Waveforms (Part 2)



7.1.1 Load switching test results

Test conditions: T_{AMB} = 25° C, V_{CC} = 24 V, f = 0.5 Hz

Switching loads: Lamp 24V, 15W; Inductor L = 130 mH, R_{LOAD} = 48Ω

In the event of GND_Power disconnection, the device turns off immediately. The test was performed with different V_{CC} values.

Test Results: The VN808 HSD worked properly during the test.

The waveform after GND_Power disconnection is shown in *Figure 30* with the following conditions: Power supply = 24V, Load = 24V /15W lamp, and HSD input = ON.

If the HSD input is OFF, then the output will still switch OFF after GND_Power disconnection.

Figure 30. GND_Power disconnection

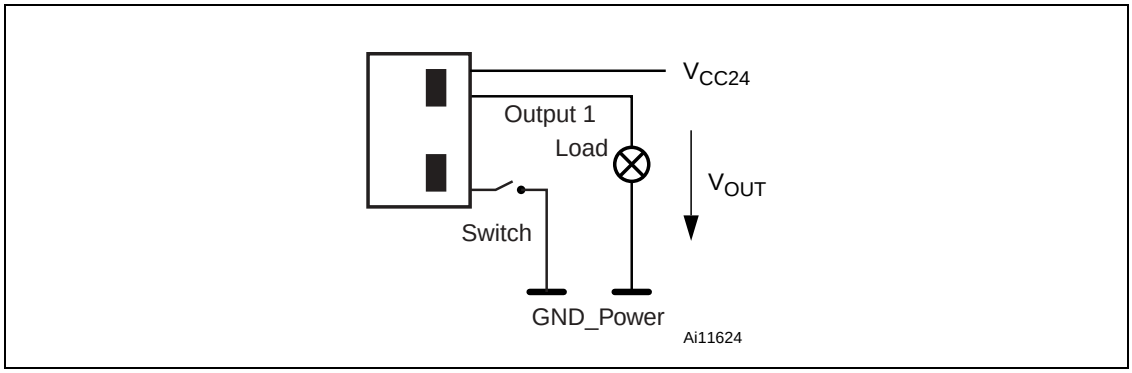


Figure 31. Switching lamps: V_{CC} = 24V, f = 0.5 Hz, Wave1 = V_{INOPT}, Wave2 = V_{OUT}, Wave4 = I_{CH1OUT}

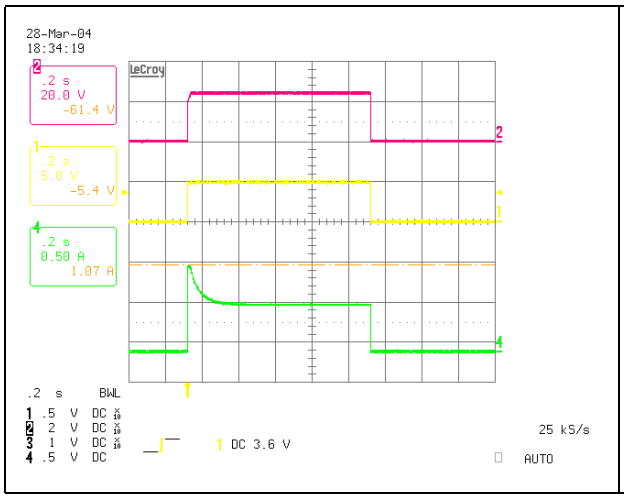


Figure 32. Waveform t_{OFF} inductor load: V_{CC} = 24V, L = 130mH, R_{LOAD} = 63Ω, t_{OFF} = 1.2101 ms, Wave2 = V_{OUT}, Wave1 = V_{INOPT}, Wave4 = I_{CH1OUT}

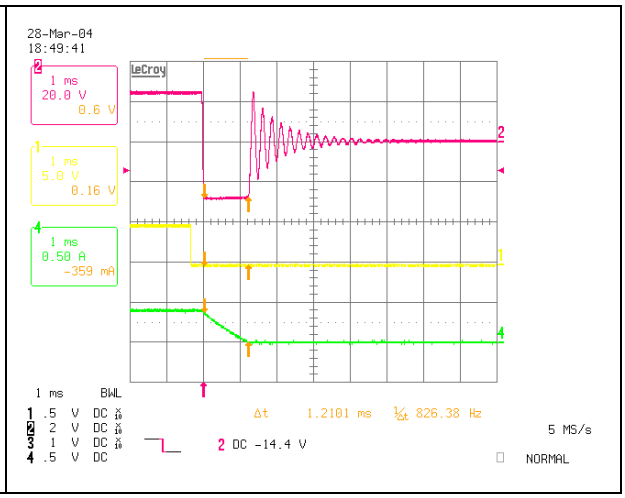


Figure 33. Waveform switching inductive load: V_{CC} = 24V, L = 130mH, R_{LOAD} = 48Ω, f = 0.5Hz, Wave2 = V_{OUT}, Wave1 = V_{INOPT}, Wave4 = I_{CH1OUT}

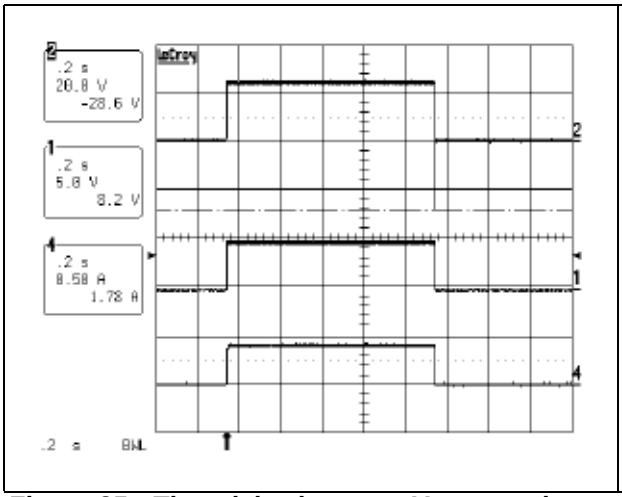


Figure 34. Switching with short circuit: V_{CC} = 24V, f = 0.5Hz, Wave2 = $V_{STATUSOPT}$, Wave1 = V_{INOPT}, Wave4 = I_{CH1OUT}

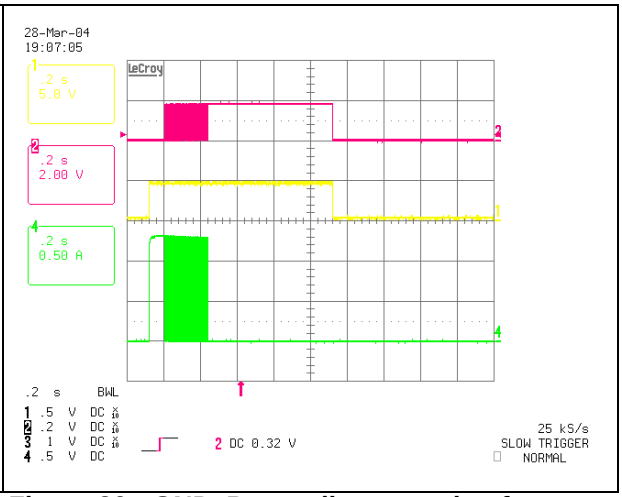


Figure 35. Time delay between V_{INOPT} and V_{OUT}: V_{CC} = 24V, Load = Lamp, Wave2 = V_{OUT}, Wave3 = V_{INOPT}, Δt = 58.462 µs

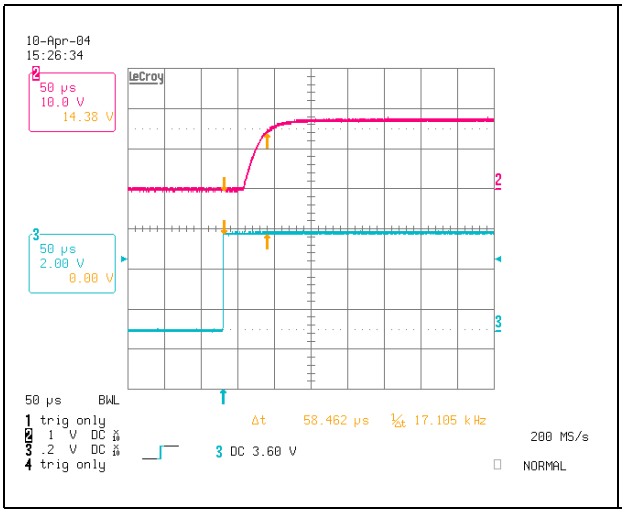
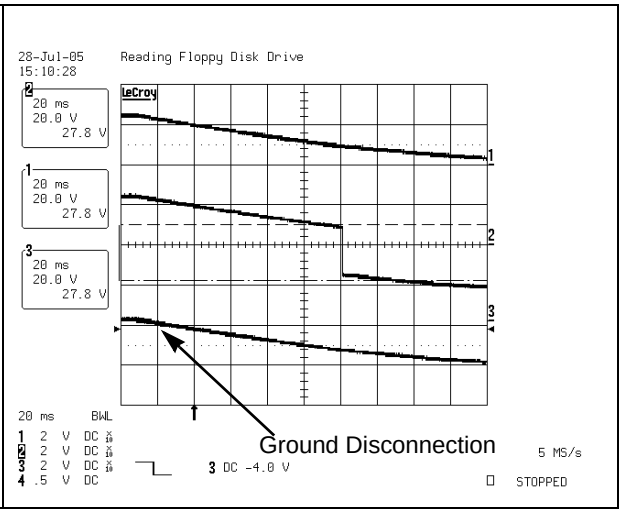


Figure 36. GND_Power disconnection for VN808: V_{CC} = 25V, Load = Lamp, Wave1 = V_{CC}, Wave2 = V_{OUT}, Wave3 = GND of power supply



7.1.2 Thermal stress test results

1. All channels shorted: f_{SWITCH} = 0.5 Hz, V_{CC} = 28V, duration 72 hours, T_A = 25°C.
2. All channels shorted: f_{SWITCH} = 0.5 Hz, V_{CC} = 28V, duration 8 hours, T_A = 85°C.
3. All channels shorted: f_{SWITCH} = 0.5 Hz, V_{CC} = 28V, duration 8 hours, T_A = –25°C.

Test Results: The case temperature with 8 channels shorted oscillates between 116 and 119°C with an ambient temperature of 25°C. The case temperature increases to between 116 and 121°C with an ambient temperature of 85°C.

Figure 37 and *Figure 38* illustrate thermal behavior by showing the waveform of I_{TOT} current to HSD during the short circuit with different ambient temperature. The input is switched at 1 Hz. The thermal shutdown is active and the output channel is switched off because it is shorted. The maximum case temperature with maximum current I_{TOT} is 42°C during normal operation (without short circuit) as shown in *Figure 39*.

Figure 37. Waveform I_{TOT} and V_{INOPT} during the test with short circuit V_{CC} = 28V, T_A = 85°C, Wave4 = I_{TOT}, Wave1 = V_{INOPT}

Figure 38. Waveform on I_{TOT} and V_{INOPT} during the test with short circuit V_{CC} = 28V, T_A = –25°C, Wave4 = I_{TOT}, Wave1 = V_{INOPT}

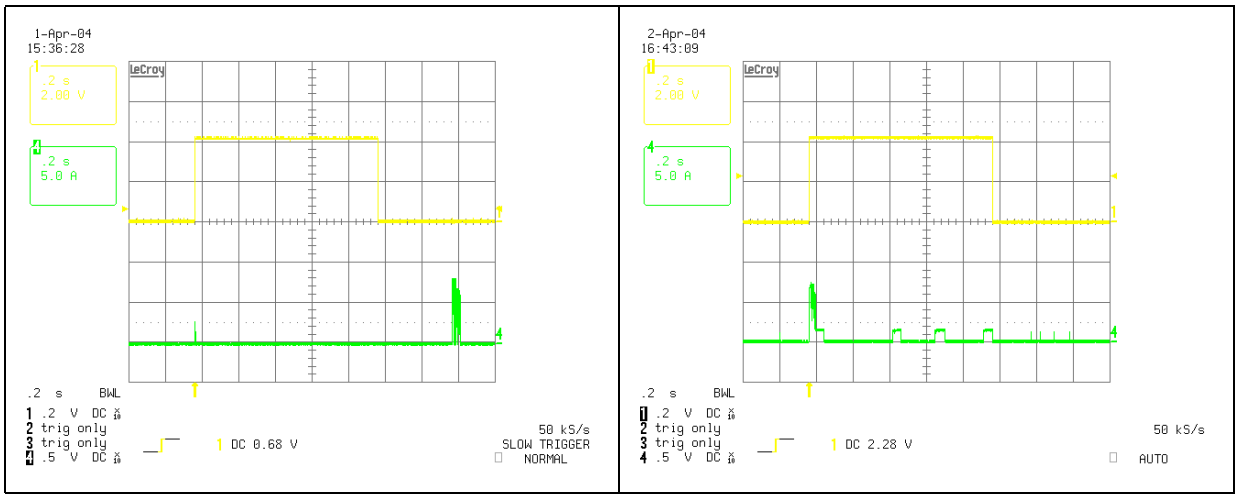
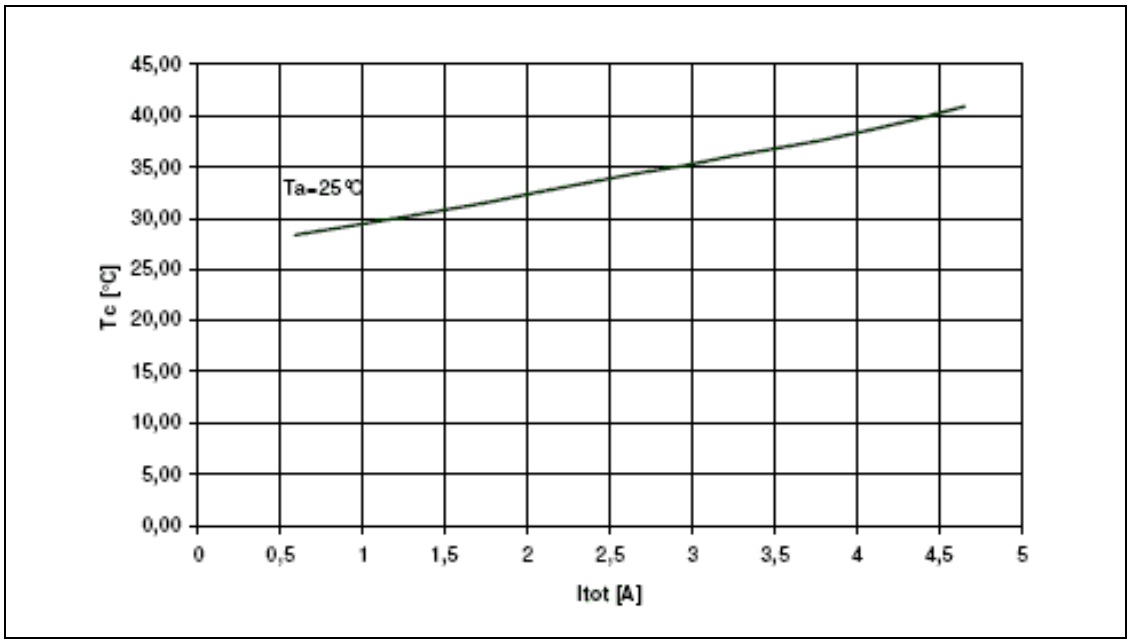


Figure 39. Case temperature dependency vs. current I_{TOT} (T_A = 25°C and V_{CC} = 24 V)



Note: The temperature measured in thermal chamber using the FLUKE 189 multimeter and thermo-coupler. No airflow present during the test.

7.1.3 EMC test results

IEC 61000-4-4 EFT test

The VN808 reference design board is tested according IEC 61000-4-4 for ±4kV level. *Table 6* lists test results. Waveforms of bursts injected during the tests are shown in *Figure 40* and *Figure 41*.

The test lasted approximately 1 minute with ±4 kV and a repetition rate of 5 kHz. During the tests, all channels were switched.

Test result: The VN808 HSD worked properly during the test.

Table 6. EMC test IEC 61000-4-4 EFT test results (VN808 RDB)

IEC 61000-4-4 Burst test	Test Condition	VN808 RDB 1/2	VN808 RDB 2/2
Power supply	Input ON	±4kV OK	±4kV OK
	Input OFF	±4kV OK	±4kV OK
	Switch @ 1Hz	±4kV OK	±4kV OK
Output	Input ON	±4kV OK	±4kV OK
	Input OFF	±4kV OK	±4kV OK
	Switch @ 1Hz	±4kV OK	±4kV OK
Input	Input ON	±4kV OK	±4kV OK
	Input OFF	±4kV OK	±4kV OK

Figure 40. Burst applied on the power supply

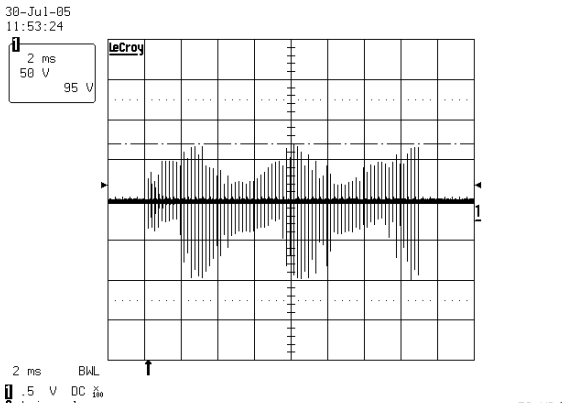
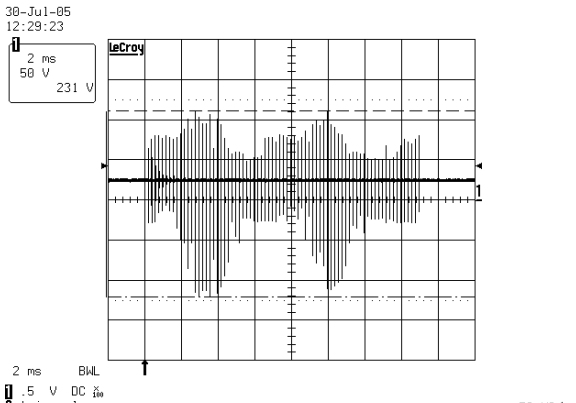


Figure 41. Burst applied on the output channel



IEC 61000-4-5 surge test

A coupling decoupling network with a 42Ω impedance was used when performing the test. The test was executed with ±2kV.

When testing power supply lines, all channels were switched. When testing the output channel, only the tested channel was switched.

A 4.7nF 500V capacitor was placed between the power supply and the earth protection.

Figure 42 and *Figure 43* illustrate active Transil protection. The pulse from generator was applied on the power supply and the Transil diode limited the voltage from 2kV to approximately 50V. The test contained five positive and five negative discharges with each polarity. Repetition rate was 1 discharge per minute.

Test result: The VN808 HSD worked properly during the test.

Table 7. EMC test IEC61000-4-5 surge test results (VN808 RDB)

IEC 61000-4-5 Surge Test	Test Condition	VN808 RDB 1/2	VN808 RDB 2/2
Power supply V_{CC} to GND_Power	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK
V_{CC} to Earth	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK
GND to Earth	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK
Output of the RDB to V_{CC}	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK
Output of the RDB to GND_Power	Input ON	± 2kV OK	± 2kV OK
	Input OFF	± 2kV OK	± 2kV OK
Output of the RDB to Earth	Input ON	± 2kV OK	± 2kV OK
	Input OFF	± 2kV OK	± 2kV OK

Figure 42. Positive surge applied on power supply

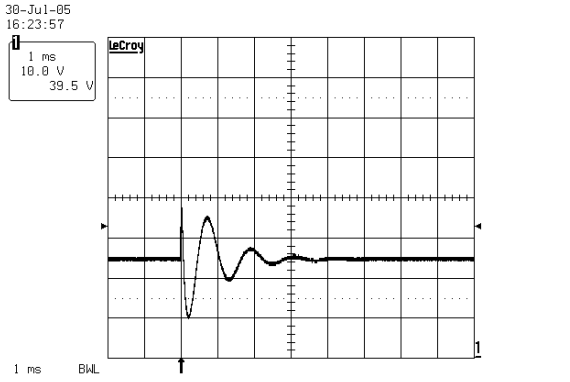
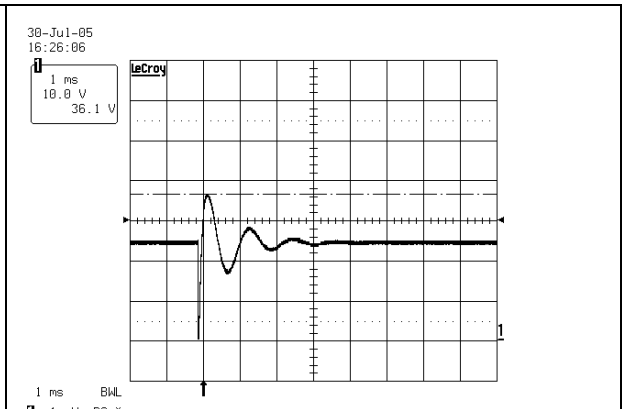


Figure 43. Negative surge applied on power supply



IEC61000-4-6 conducted immunity

This is the most difficult test and requires the use of a coupling decoupling network for power supply lines and special current clamp for output and data lines. The test was executed with Level 3 (10V) compliance. *Table 8* lists test results.

If input lines are grounded, the optocoupler will switch on during the test because the inducted voltage is too high. This is a normal reaction and when the test finishes, the optocoupler works normally.

Test result: The VN808 HSD worked properly during the test.

Table 8. EMC test IEC 61000-4-6 conducted immunity test results (VN808 RDB)

IEC 61000-4-6	Test Condition	VN808 RDB 1/2	VN808 RDB 2/2
Power supply	Input ON	10V OK	10V OK
	Input OFF	10V OK	10V OK
	Switch @ 1Hz	10V OK	10V OK
Output	Input ON	10V OK	10V OK
	Input OFF	10V OK	10V OK
	Switch @ 1Hz	10V OK	10V OK
Input	Input ON	10V OK	10V OK
	Input OFF	10V OK **B**	10V OK **B**
	Switch @ 1Hz	10V OK	10V OK

*Note: **B** means a temporary degradation or loss of function or performance, with an automatic return to normal operation.*

7.2 VN340SP HSD test results

7.2.1 Load switching test results

Test conditions: T_{AMB} = 25° C, V_{CC} = 24 V, f = 0.5 Hz

Switching loads: Lamp = 24V, 15W; Inductor L = 130 mH, R_{LOAD} = 48Ω

Test result: The VN340SP HSD worked properly during the test.

Figure 44 to *Figure 49* show the waveforms during the load switching tests.

If input is ON, the output will switch off immediately if GND_Power is disconnected. If the input is OFF, the output remains OFF.

7.2.2 Thermal stress test results

1. All channels shorted: f_{SWITCH} = 0.5 Hz, V_{CC} = 28V, duration 72 hours, T_A = 25°C.
2. All channels shorted: f_{SWITCH} = 0.5 Hz, V_{CC} = 28V, duration 8 hours, T_A = 85°C.
3. All channels shorted: f_{SWITCH} = 0.5 Hz, V_{CC} = 28V, duration 8 hours, T_A = –25°C.

Test result: The VN340SP HSD worked properly during the test.

The maximum temperature with 4 channels shorted is 156°C with an ambient temperature of 25°C and 159°C with an ambient temperature of 85°C. *Figure 50* and *Figure 51* show behavior during the thermal stress tests.

The input was switched at 1 Hz. The thermal shutdown is shown in the figures below.

Figure 44. Switching lamps: V_{CC} = 24V, f = 0.5Hz, Wave3 = V_{INOPT}, Wave2 = V_{OUT}, Wave4 = I_{CH1OUT}

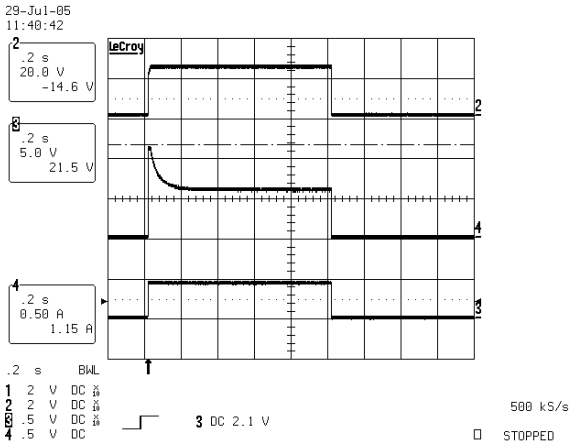


Figure 45. Waveform t_{OFF} inductor load: V_{CC} = 24V, L = 130mH, R_{LOAD} = 60Ω, t_{OFF} = 1.2276ms, Wave2 = V_{OUT}, Wave3 = V_{INOPT}, Wave4 = I_{CH1OUT}

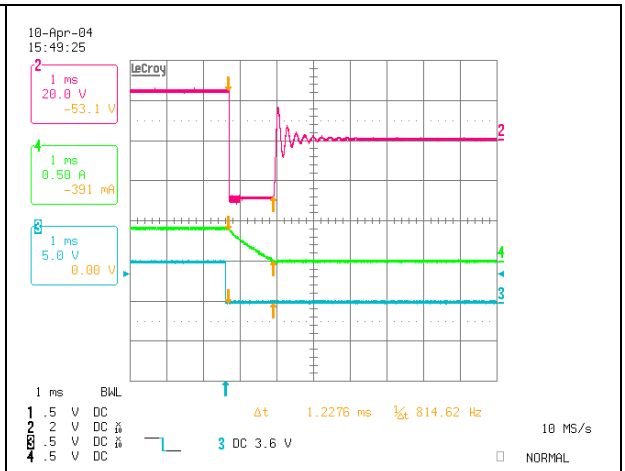


Figure 46. Time delay between V_{INOPT} and V_{OUT}: V_{CC} = 24V, Load = Lamp, Wave2 = V_{OUT}, Wave3 = V_{INOPT}, Δt = 139µs

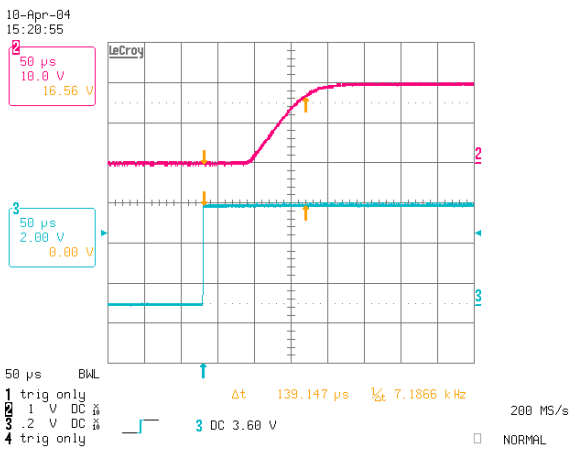


Figure 47. Switching with short circuit: V_{CC} = 24V, f = 0.5Hz, Wave2 = $V_{STATUSOPT}$, Wave3 = V_{INOPT}, Wave4 = I_{CH1OUT}

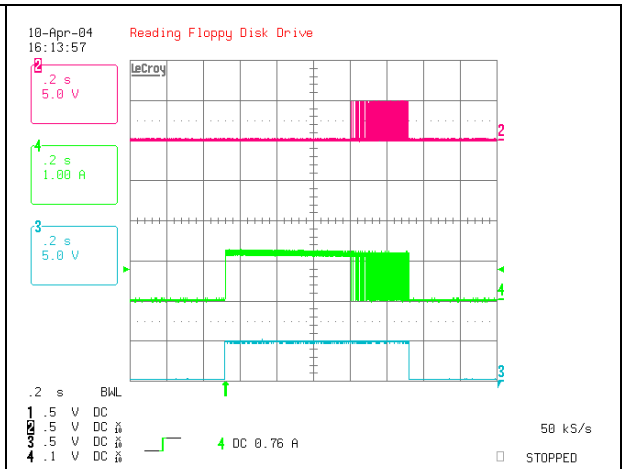


Figure 48. Waveform switching inductive load: V_{CC} = 24V, L = 130mH, R_{LOAD} = 48Ω, f = 0.5Hz, Wave2 = V_{OUT}, Wave3 = V_{INOPT}, Wave4 = I_{CH1OUT}

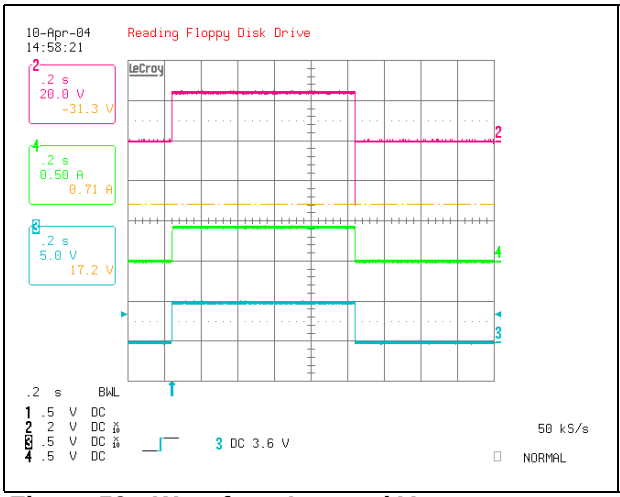


Figure 49. Switching with short circuit: V_{CC} = 24V, f = 0.5Hz, Wave2 = $V_{STATUSOPT}$, Wave3 = V_{INOPT}, Wave4 = I_{CH1OUT}

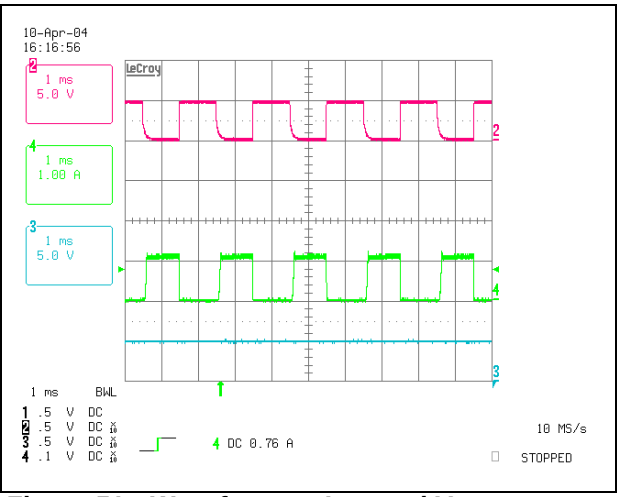


Figure 50. Waveform I_{TOT} and $V_{STATUSOPT}$ during the test with short circuit: V_{CC} = 28V, T_A = 85°C, Wave4 = I_{TOT}, Wave1 = $V_{STATUSOPT}$

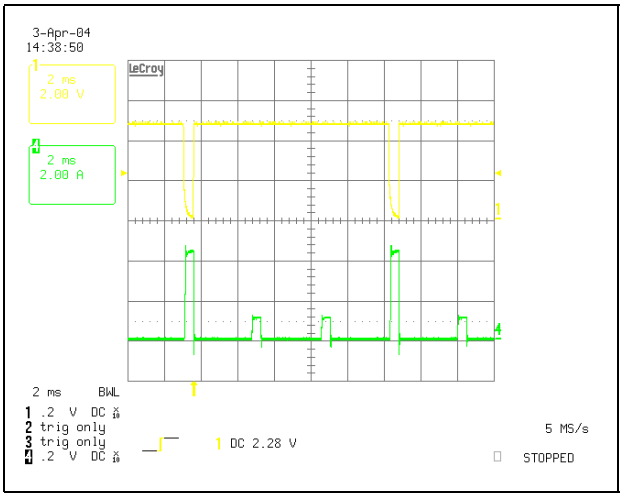
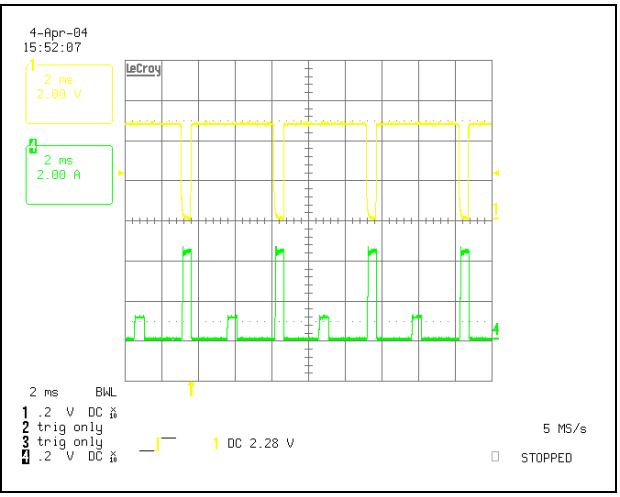


Figure 51. Waveform on I_{TOT} and $V_{STATUSOPT}$ during the test with short circuit: V_{CC} = 28V, T_A = –25°C, Wave4 = I_{TOT}, Wave1 = $V_{STATUSOPT}$



Note: The temperature measured in thermal chamber using a FLUKE 189 multimeter and thermo-coupler.

7.2.3 EMC test results

IEC 61000-4-4 EFT test results

The VN340SP HSD is tested according IEC 61000-4-4 Level 4 (4kV). Power supply and input/output ports are tested while all other channels are active. *Table 9* lists test results.

Test result: The VN340SP HSD worked properly during the test.

Table 9. EMC test IEC 61000-4-4 EFT test results (VN340SP RDB)

IEC 61000-4-4 Burst Test	Test Condition	RDB VN340SP 1/2	RDB VN340SP 2/2
Power supply	Input ON	±4kV OK	±4kV OK
	Input OFF	±4kV OK	±4kV OK
	Switch @ 1Hz	±4kV OK	±4kV OK
Output	Input ON	±4kV OK	±4kV OK
	Input OFF	±4kV OK	±4kV OK
	Switch @ 1Hz	±4kV OK	±4kV OK
Input	Input ON	±4kV OK	±4kV OK
	Input OFF	±4kV OK	±4kV OK

IEC 61000-4-5 surge test results

The board was tested with 42Ω coupling/decoupling network. All channels were active during the test. Different combinations of channel activity were also tested. *Table 10* lists test results.

A 4.7nF 500V capacitor was placed between the power supply and earth protection.

Test result: The VN340SP HSD worked properly during the test.

Table 10. EMC test IEC61000-4-5 surge test results (VN340SP RDB)

IEC 61000-4-5 Surge Test	Test Condition	VN340SP RDB 1/2	VN340SP RDB 2/2
Power supply V_{CC} to GND:_Power	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK
V_{CC} to Earth	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK
GND to Earth	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK
Output of the RDB to V_{CC}	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK
Output of the RDB to GND_Power	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK
Output of the RDB to Earth	Input ON	±2kV OK	±2kV OK
	Input OFF	±2kV OK	±2kV OK

IEC61000-4-6 conducted immunity test results

The test was executed according the standard with required levels. *Table 11* lists test results.

Test results: Loss of function was observed during the test on output lines when HSD input was OFF. Lamps shone little bit. (Normal behavior: Lamps switched OFF.)

Loss of function was observed during the test on input lines, but is considered as normal behavior because the conducted voltage was too high and optocoupler input channels were switched.

Table 11. EMC test IEC 61000-4-6 conducted immunity test results (VN340SP RDB)

IEC 61000-4-6	Test Condition	VN340SP RDB 1/2	VN340SP RDB 2/2
Power supply	Input ON	10V OK	10V OK
	Input OFF	10V OK	10V OK
	Switch @ 1Hz	10V OK	10V OK
Output of the RDB	Input ON	10V OK	10V OK
	Input OFF	10V OK **B**	10V OK **B**
	Switch @ 1Hz	10V OK	10V OK
Input of the RDB	Input ON	10V OK	10V OK
	Input OFF	10V OK **B**	10V OK **B**
	Switch @ 1Hz	10V OK	10V OK

*Note: **B** means a temporary degradation or loss of function or performance, with an automatic return to normal operation.*

Appendix A VN808 reference design board (RDB)

A.1 VN808 RDB bill of materials

The list of parts for the VN808 Reference Design Board is provided in *Table 12*.

Table 12. VN808 RDB bill of materials

Item	Quantity	Reference	Value	Note
1	16	C5, C6, C7, C8, C9, C10, C11, C12	10nF	
		C19, C20, C21, C22, C23, C24, C25, C26		
2	4	C14, C13, C18, C17	4.7nF 500V SMD 1206	
3	4	C2, C4, C15, C27	100nF 50V SMD 0805	
4	2	C1, C28	22uF/50V	
5	1	C30	10µF/35V ceramic	
6	1	C33	100µF/16V tantalum	
7	1	C31	220pF	
8	1	C32	22nF	
9	2	D1, D2	SM15T36A	
10	1	D3	STPS2L25U	
11	2	J1, J4	Headers 2line 14pin	
12	2	J2, J3	Terminal block 5,08mm	
13	1	L1	33µH/2A	
14	2	R1, R13	2k2	
15	16	R3, R4, R5, R6, R7, R8, R9, R10	1k5	
		R16, R17, R18, R19, R20, R21, R22,		
		R23		
16	1	R26	15K	
17	3	R12, R15, R25	4k7	
18	1	R27	3k9	
19	1	R11, R24	10k	
20	1	J5	Terminal block 5.08mm	
21	4	U2, U3, U7, U8	TLP281-4	
22	2	U1, U5	VN808	
23	2	U4, U6	TLP181	
24	1	U9	L5970	
25	2	F1, F2	7A	

A.2 Recommended VN808 PCB Layout

The PCB layout is very important in order to operate the devices in the worst condition and under EMC immunity.

Figure 52. VN808 RDB PCB layout (top and bottom)

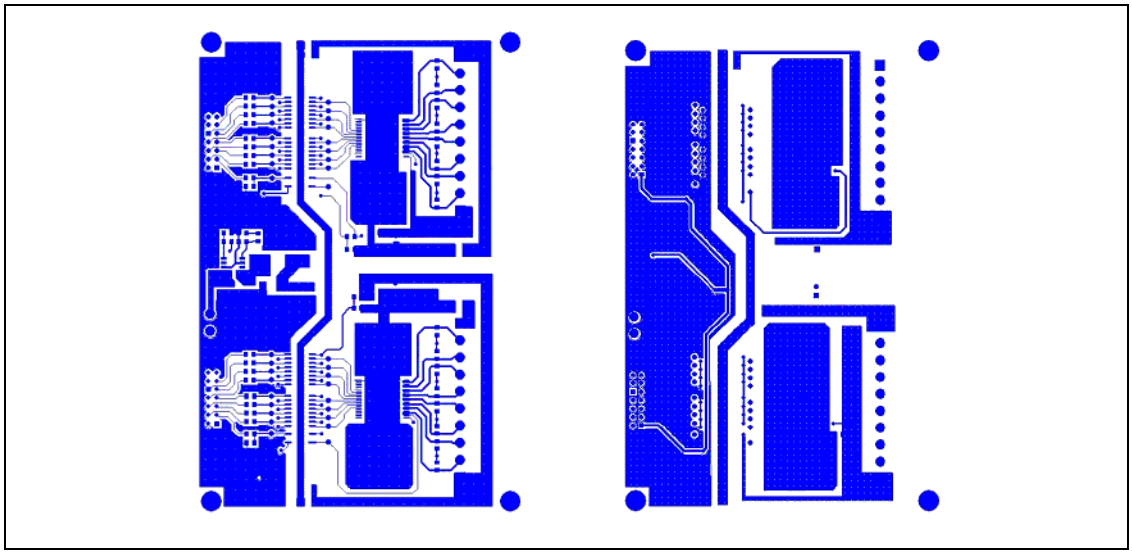
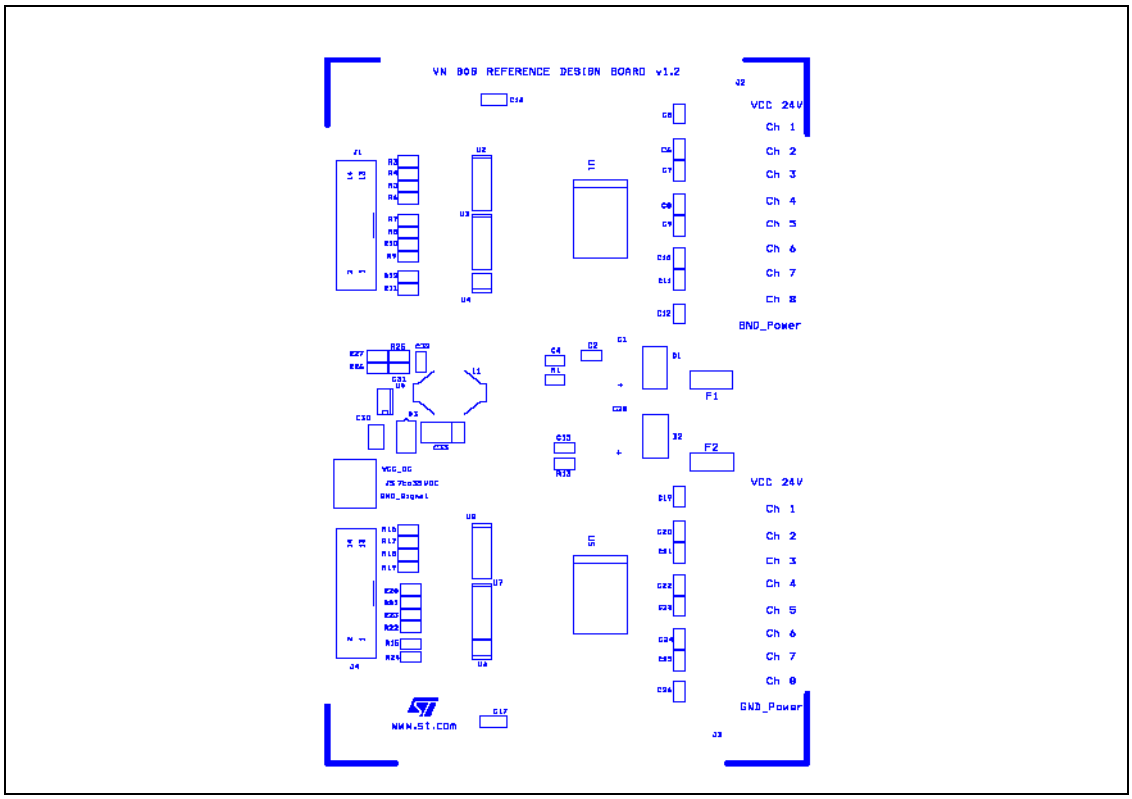


Figure 53. VN808 RDB PCB layout (component side)



Appendix B VN340SP reference design board (RDB)

B.1 VN340SP RDB bill of materials

The list of parts for the VN340SP Reference Design Board is provided in *Table 13*.

Table 13. VN340SP RDB bill of materials

Item	Quantity	Reference	Part	Note
1	4	C2, C3, C12, C15	10nF	
2	2	C4, C16	100nF 50V 0805	
3	8	C5, C6, C7, C8, C17, C18, C19, C20	4n7 500V 1206	
4	2	C9, C21	22µF	
5	1	C10	22nF	
6	1	C11	220pF	
7	1	C13	10uF/35V	Ceramic
8	1	C14	100uF/16V	Tantalum
9	2	D1, D4	SM15T36A	
10	1	D3	STPS2L25U	
11	2	D2, D5	L-HLMP1700	
12	1	J5	Terminal Block 5.08mm	
13	2	J1, J3	HEADER 2 line 10 pin	
14	2	J2, J4	Terminal Block 5.08mm	
15	1	L1	33uH/2A	
16	13	R1, R2, R3, R4, R19, R10, R20, R21, R22, R23, R29,	4k7	
17	2	R5, R24	7k5	
18	8	R6, R7, R8, R9, R25, R26, R27, R28,	22k	
19	10	R11, R12, R13, R14, R15, R30, R31, R32, R33, R34, R16, R35	1k5	
20	1	R17	15k	
21	1	R18	3k9	
22	2	F1, F2	Fuse 4A	
23	2	U1, U6	TLP281-4	
24	2	U2, U5	TLP181	
25	2	U3, U7	VN340SP	
26	1	U8	L5970D	

B.2 Recommended VN340SP RDB PCB layout

Figure 54. VN340SP RDB PCB layout (Top side) and (Bottom side)

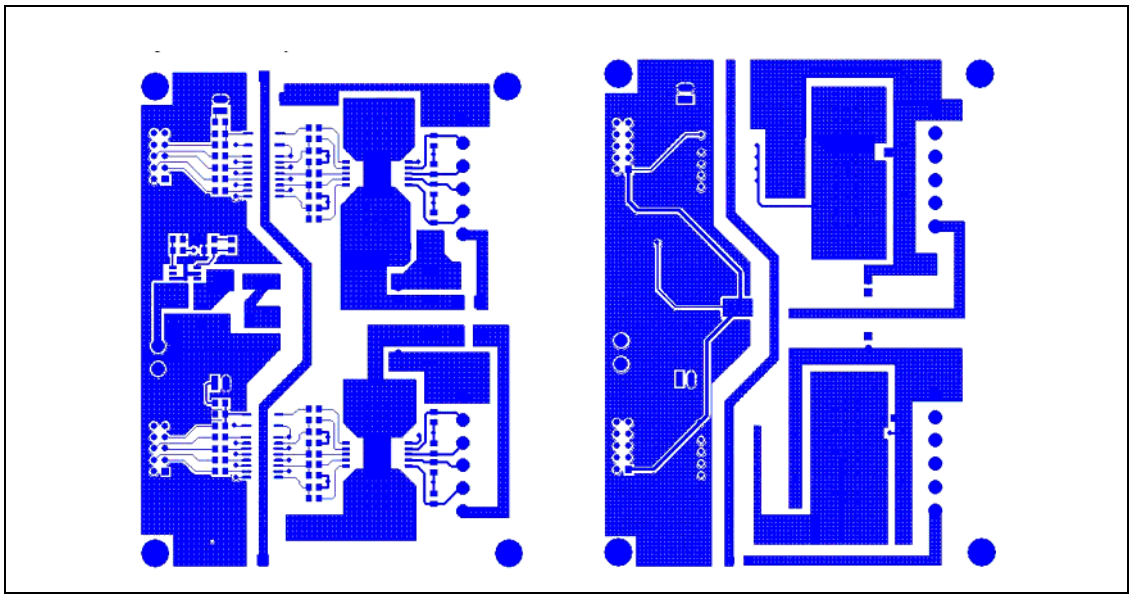
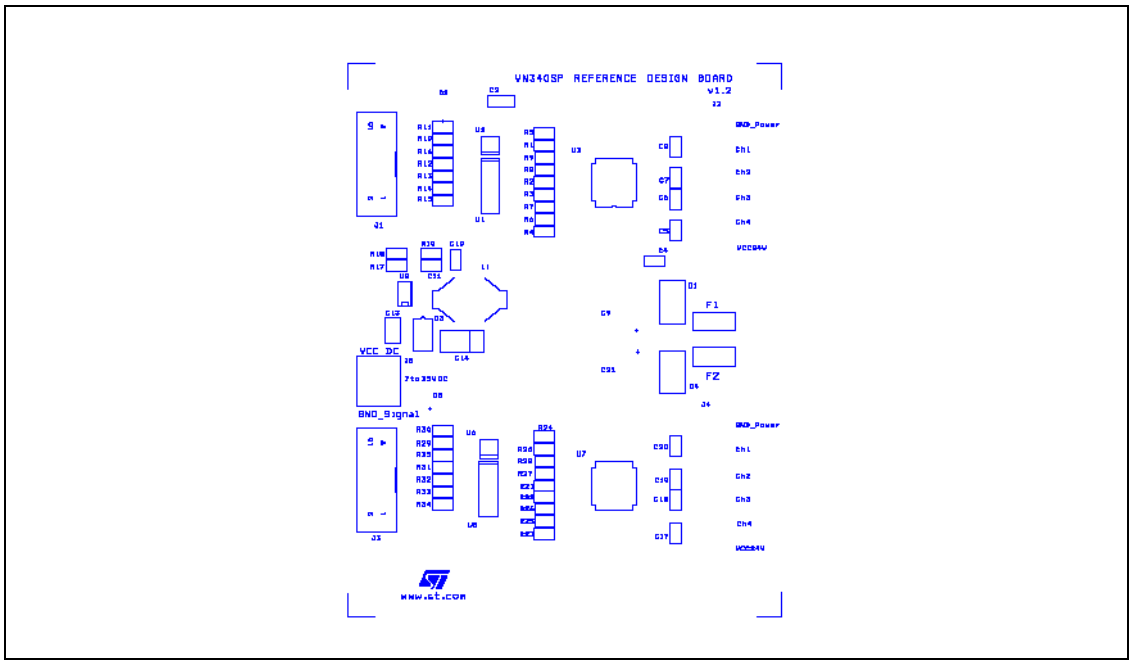


Figure 55. VN340SP RDB PCB layout (component side)

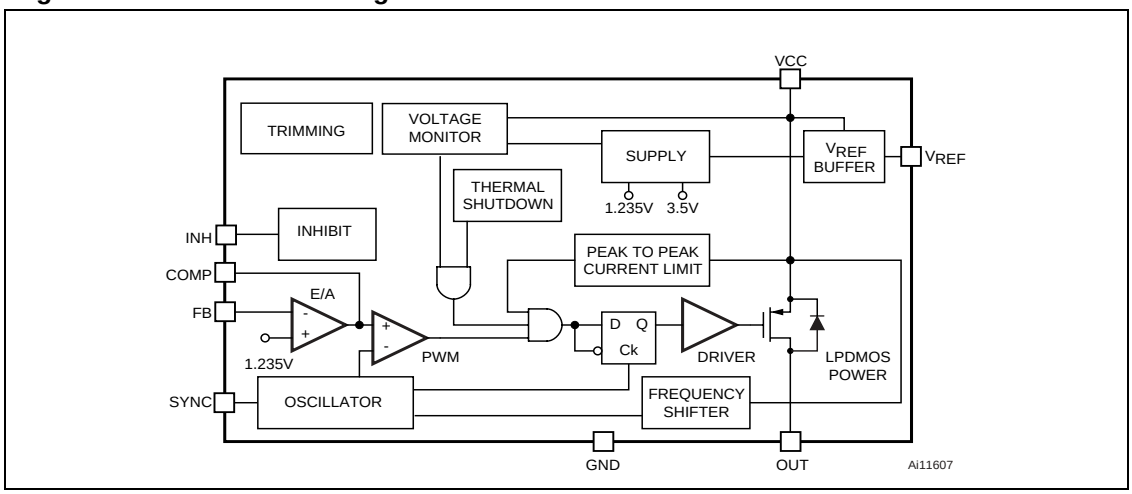


Appendix C L5970D DC/DC converter

C.1 Functional description

The L5970D (*Figure 56*) is a step-down power regulator capable of delivering output voltages from 1.235 to 35V (up to 1A). The operating input voltage ranges from 4.4 to 36V. It is designed in BCD5 technology and the power switching element is a P-Channel D-MOS power transistor. An internal oscillator sets the switching frequency at 250 kHz, minimizing the LC output filter. The L5970D is used for supplying optocouplers and other applications.

Figure 56. L5970D block diagram



The VN808 and VN340SP reference design boards use the L5970D DC/DC Converter for the power supplies for the data parts. With an output voltage of 6V and output current up to 1A, the L5970D is an attractive and simple solution.

The main internal blocks are shown in *Figure 56* where is reported the device block diagram. They are:

- A voltage regulator that supplies the internal circuitry. From this regulator a 3.3V reference voltage is externally available.
- A voltage monitor circuit that checks the input and internal voltages.
- A fully integrated sawtooth oscillator whose frequency is 250 kHz ±5%, including also the voltage feed forward function and an input/output synchronization pin.
- Two embedded current limitations circuitries which control the current that flows through the power switch. The Pulse by Pulse Current Limit forces the power switch OFF cycle by cycle if the current reaches an internal threshold, while the Frequency Shifter reduces the switching frequency in order to strongly reduce the duty cycle.
- A transconductance error amplifier.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- A high-side driver for the internal P-MOS switch.
- An inhibitor block for stand-by operation.
- A circuit to provide the thermal protection function.

The output voltage can be adjustable by voltage divider. In *Figure 9* can be seen voltage divider by resistors R26 and R27. The value of resistor R26 is equal to:

$$R26 = R27\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right)$$

Note: V_{FB} *= 1.235 V*
For more information and technical data about L5970D, refer to the L5970D datasheet.

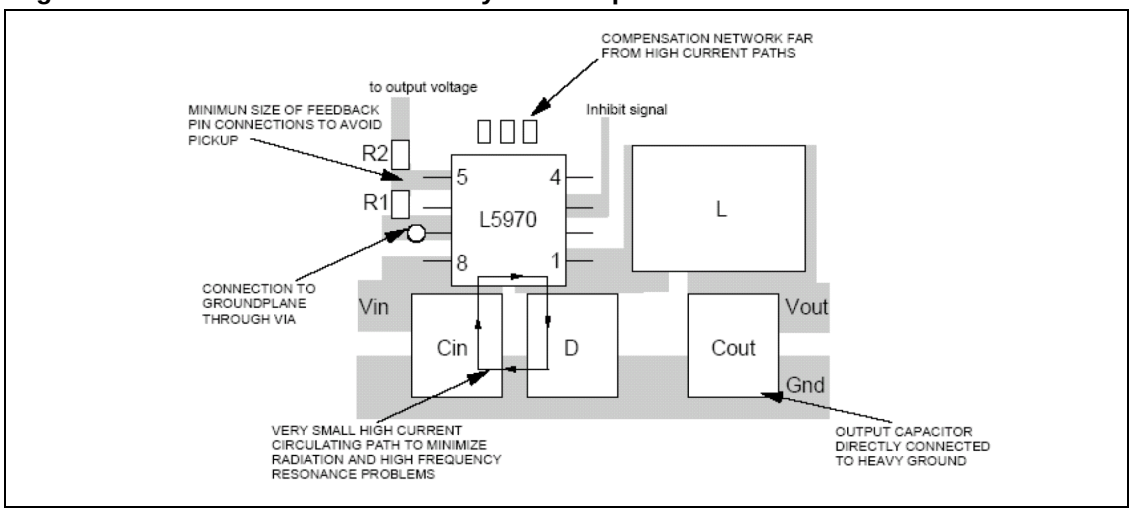
C.2 L5970D layout recommendations

A optimized layout is on of the key factors to operate the DC/DC converter. It reduce noise and interference. Power-generating portions of the layout are the main cause of noise, therefore, the high switching current loop areas, should be kept as small as possible as well as lead lengths has to be kept short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference and so they should be as far as possible from the high current paths.

Below there is a layout example on *Figure 57.* The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device to avoid pick up noise. Moreover the GND pin of the device is connected to the ground plane directly with VIA on the bottom side of the PCB.

Figure 57. L5970 DC/DC converter layout example



C.3 L5970D DC/DC converter load test results

Table 14. L5970D electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{SS}	Operating input voltage	6.6		35	V
I_{QOP}	Total operating quiescent current		2.4	5	mA
I_{OUTDC}	Maximum limiting current		1.0	1.4	A
f_S	Switching frequency		243	250	kHz
d	Duty cycle	0		100	%
T_A	Operating Temperature Range	–25 to 85°C			°C
P_{TOTDC}	Power dissipation at Tamb = 60°C	0.75			W

The DC/DC converter was tested with a constant output current with resistive load.

The Waveform on coil L1 has to be clear without overshot (see *Figure 61.*, *Figure 63.*).

Input/output voltage ripple depends on ESR capacitor values.

Only low ESR capacitors have been used on V_{SS} and V_{OUT}.

Test conditions

- Resistive load = 12Ω
- Input voltages V_{SS} = 8, 12, and 24V.
- Output voltage V_{BSS} = 5V
- Output current I_{OUTDC} = 0.4A
- Ambient Temperature (T_A) = 25°C

Test results: If output current is increase up to 1.4 A, then the current limiter will be active. Output voltage ripple can be seen in *Figure 62.* The maximum value of ripple is 93 mV. The efficiency measurement results are shown in *Figure 58.*

Figure 58. Efficiency vs. output current

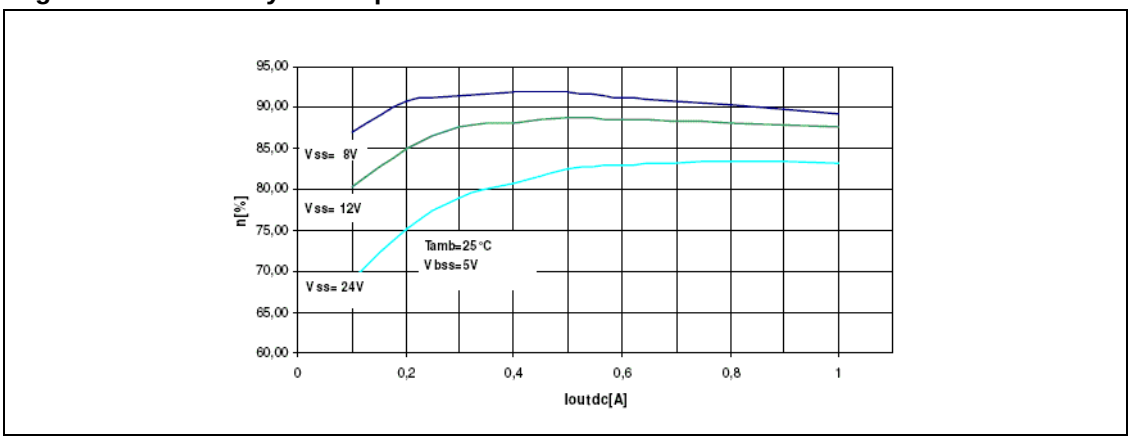


Figure 59. Output voltage stability of L5970D, V_{SS} = 24 V

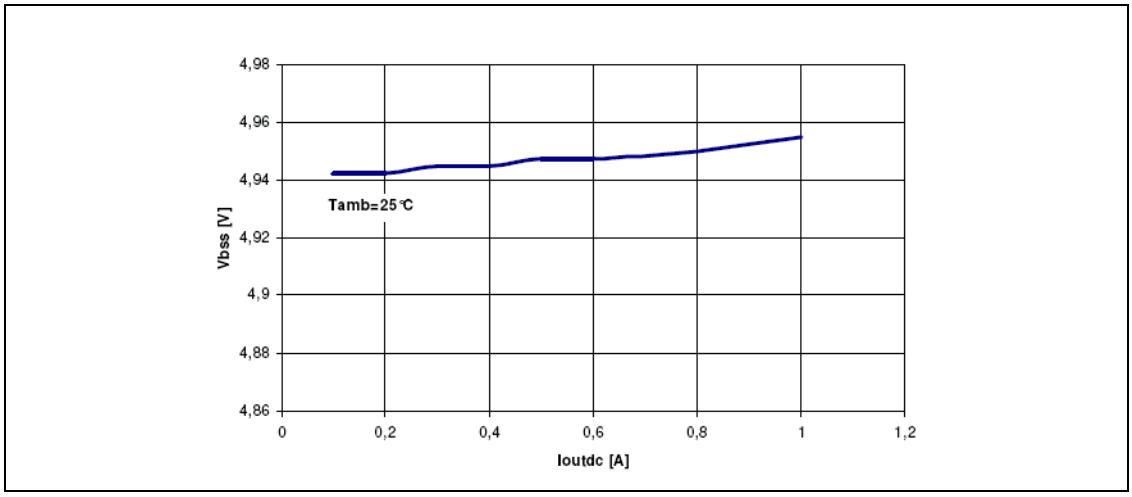


Figure 60. Voltage ripple on capacitor C30, I_{OUTDC} = 0.4A, V_{SS} = 24V

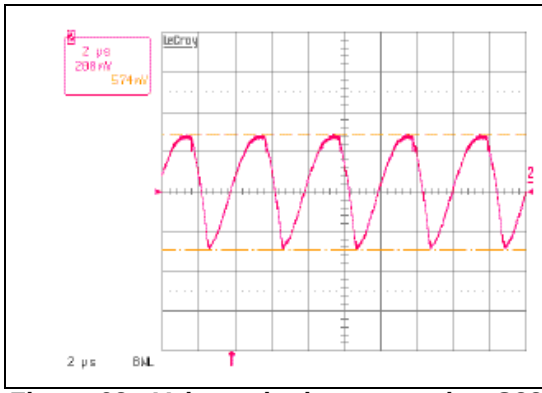


Figure 61. Waveform on coil L1, I_{OUTDC} = 0.4A, V_{SS} = 24V

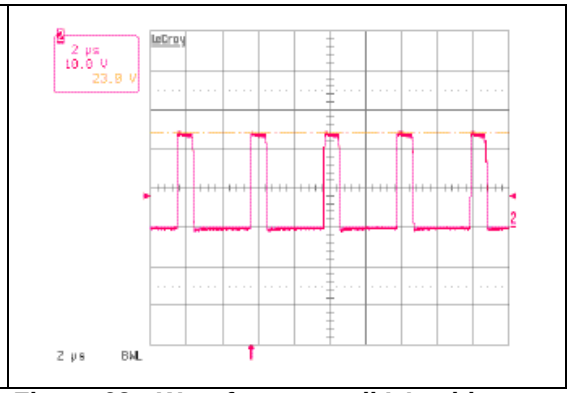


Figure 62. Voltage ripple on capacitor C33, V_{SS} = 24V, I_{OUTDC} = 0.4 A

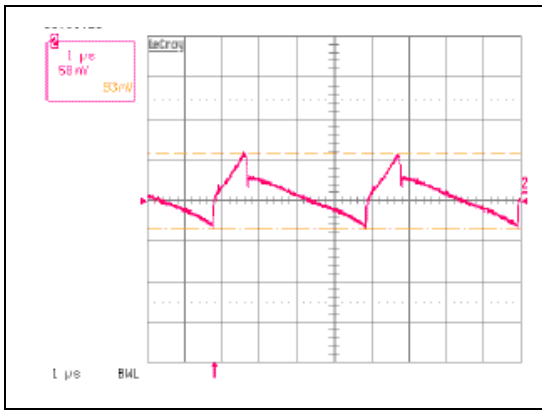
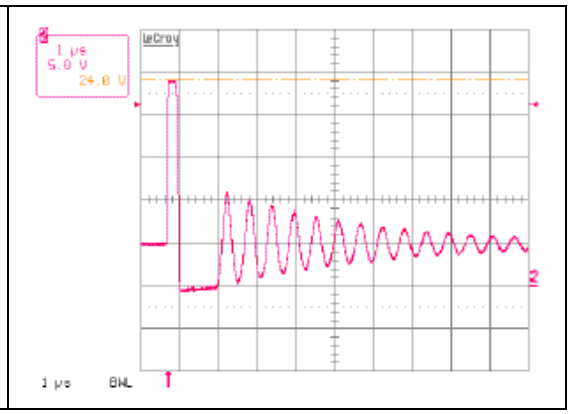


Figure 63. Waveform on coil L1, without load, V_{SS} = 24V



8 Revision history

Date	Revision	Changes
16-Sept-2005	1.0	Initial release.

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